# Hex buffer with open-drain outputs Rev. 1 — 19 December 2016

**Product data sheet** 

#### **General description** 1.

The 74AHCT07A is a hex buffer with open-drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Designed to operate over a V<sub>CC</sub> range from 4.5 V to 5.5 V, the inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

#### 2. Features and benefits

- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t<sub>P7I</sub> of 3.4 ns at 5 V
- Typical  $V_{OL(p)}$  < 0.8 V at  $V_{CC}$  = 5 V,  $T_{amb}$  = 25 °C
- Supports mixed-mode voltage operation on all ports
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
  - MM JESD22-A115-A exceeds 150 V
  - CDM JESD22-C101E exceeds 2 kV
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

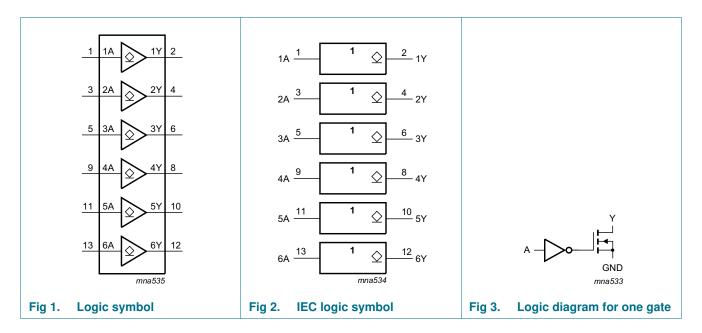


# 3. Ordering information

Table 1. Ordering information

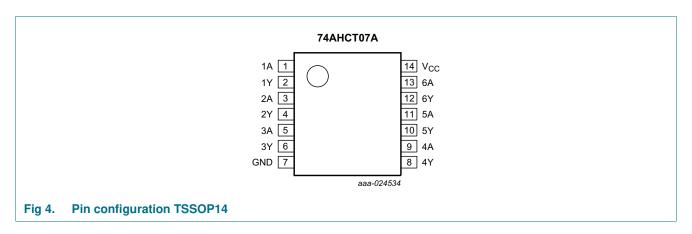
Type number Package									
	Temperature range	Name	Description	Version					
74AHCT07APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					

## 4. Functional diagram



# 5. Pinning information

### 5.1 Pinning



74AHCT07A

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
Vcc	14	supply voltage

# 6. Functional description

Table 3. Function selection [1]

Input	Output
nA	nY
L	L
Н	Z

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
VI	input voltage		[1]	-0.5	+7.0	V
V <sub>O</sub>	output voltage	output LOW state, power-down or 3-state mode	[2]	-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V		-20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V		-20	-	mA
Io	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±25	mA
I <sub>CC</sub>	supply current			-	75	mA
I <sub>GND</sub>	ground current			<b>−75</b>	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[3]	-	500	mW

<sup>[1]</sup> The minimum input voltage ratings may be exceeded if the input current ratings are observed.

<sup>[2]</sup> The output voltage ratings may be exceeded if the output current ratings are observed.

<sup>[3]</sup> For TSSOP14 packages: above 75  $^{\circ}$ C the value of P<sub>tot</sub> derates linearly at 7 mW/K.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	٧
VI	input voltage		0	-	5.5	٧
V <sub>O</sub>	output voltage	output LOW state, power-down or 3-state mode	0	-	5.5	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	ns/V

## 9. Static characteristics

#### Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	$V_{CC}$ = 4.5 V to 5.5 V	2	-	-	2	-	2	-	V
V <sub>IL</sub>	LOW-level input voltage	$V_{CC}$ = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	$V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$ ; $V_O$ = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	μА
I <sub>OFF</sub>	power-off leakage current	$V_I$ or $V_O$ = GND to 5.5 V; $V_{CC}$ = 0 V	-	-	0.5	-	5	-	5	μА
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0$ V to 5.5 V	-	-	±0.1	-	±1	-	±1	μА
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2	-	20	-	20	μА
Δl <sub>CC</sub>	additional supply current	per input pin; $V_I = 3.4 \text{ V}$ ; $I_O = 0 \text{ A}$ ; other pins at $V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA

# 10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit see Figure 6.

Symbol	Parameter	Conditions			25 °C		-40 °C 1	to +85 °C	-40 °C t	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>PZL</sub>	OFF-state to	nA to nY; see Figure 5									
	LOW propagation	V <sub>CC</sub> = 4.5 V to 5.5 V									
	delay	C <sub>L</sub> = 15 pF		-	3.4	5.3	1	6.5	1	7.6	ns
		C <sub>L</sub> = 50 pF		-	5	7.8	1	9.7	1	11.4	ns
t <sub>PLZ</sub>	LOW to	nA to nY; see Figure 5									
	OFF-state	V <sub>CC</sub> = 4.5 V to 5.5 V									
	propagation delay	C <sub>L</sub> = 15 pF		-	2.9	4	1	4.6	1	5.2	ns
		C <sub>L</sub> = 50 pF		-	5.2	6.7	1	7.6	1	8.5	ns
Cı	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 5 V$		-	2	6	-	6	-	6	pF
Co	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 5 \text{ V}$		-	5	-	-	-	-	-	pF
C <sub>PD</sub>	power dissipation capacitance		[2]	-	2	-	-	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 5 V.

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum{(C_L \times V_{CC}{}^2 \times f_o)}$  where:

 $f_i$  = input frequency in MHz;

 $f_o$  = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in Volts.

<sup>[2]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu W$ ).

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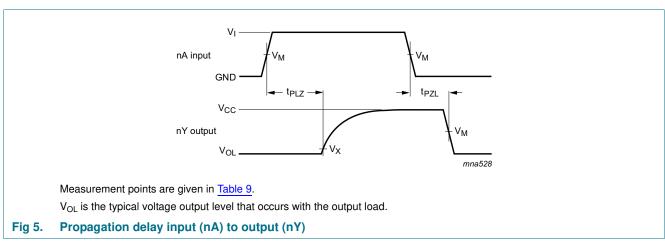
### Hex buffer with open-drain outputs

 Table 8.
 Noise characteristics

GND = 0 V. For test circuit see Figure 6.

Symbol	Parameter	Conditions	Т	T <sub>amb</sub> = 25 °C				
		Min Typ N						
V <sub>CC</sub> = 5 V	; C <sub>L</sub> = 50 pF		,			·		
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.4	8.0	V		
$V_{OL(v)}$	LOW-level output voltage (valley)		-0.8	-0.2	-	V		
V <sub>IH(AC)</sub>	AC HIGH-level input voltage (dynamic)		2	-	-	V		
V <sub>IL(AC)</sub>	AC LOW-level input voltage (dynamic)		-	-	8.0	٧		

### 11. Waveforms

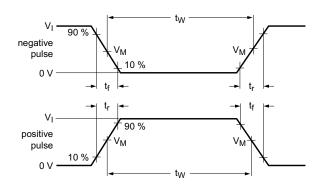


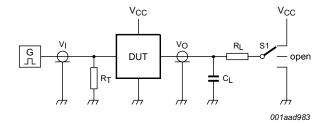
**Measurement points** 

Input	Output						
$V_{M}$	V <sub>M</sub>	$V_X$					
1.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 V$					

Table 9.

### Hex buffer with open-drain outputs





Test data is given in Table 10.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator

C<sub>L</sub> = Load capacitance including jig and probe capacitance

S1 = Test selection switch

Fig 6. Test circuit for measuring switching times

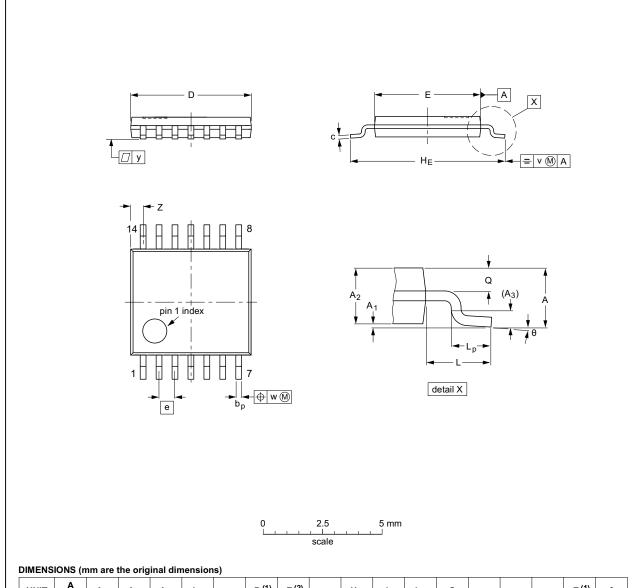
Table 10. Test data

Input		Load	S1 position		
$V_{I}$	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>		
GND to 3.0 V	3.0 ns	15 pF, 50 pF	V <sub>CC</sub>		

# 12. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



	(					Ψ,												
UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D (1)	E (2)	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

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Fig 7. Package outline SOT402-1 (TSSOP14)

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## 13. Abbreviations

#### Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

### Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCT07A v.1	20161219	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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### Hex buffer with open-drain outputs

## 17. Contents

1	General description
2	Features and benefits 1
3	Ordering information
4	Functional diagram 2
5	Pinning information 2
5.1	Pinning
5.2	Pin description
6	Functional description 3
7	Limiting values
8	Recommended operating conditions 4
9	Static characteristics 4
10	Dynamic characteristics 5
11	Waveforms 6
12	Package outline 8
13	Abbreviations9
14	Revision history 9
15	Legal information
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks
16	Contact information
17	Contents