

## INTEGRATED LDO WITH SWITCHOVER CIRCUIT FOR NOTEBOOK COMPUTERS

### FEATURES

- Wide Input Voltage Range: 4.5 V to 28 V
- 5-V/3.3-V, 100-mA, LDO Output
- Glitch Free Switch Over Circuit
- *Always-On* 3.3-V, 5-mA LDO Output for RTC
- 250 kHz Clock Output for Charge Pump
- Thermal Shutdown (Non-latch)
- 10Ld QFN (DRC) Package

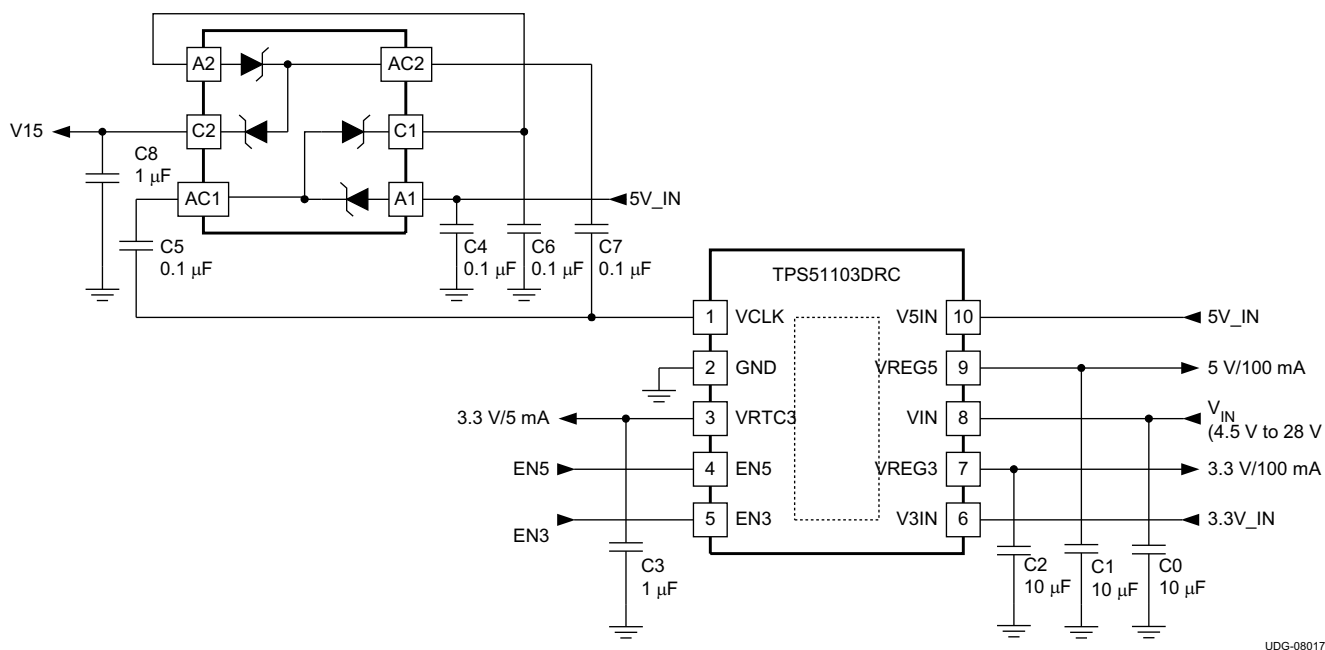
### APPLICATIONS

- Notebook Computers
- Mobile Digital Consumer Products

### DESCRIPTION

The TPS51103 integrates three LDOs. The 5-V and 3.3-V LDOs are both rated at 100 mA and also include a glitch-free switch-over feature allowing for optimized battery life. An additional 3.3-V LDO is designed to provide an *always on* power output for the real time clock (RTC). The TPS51103 integrates a clock output to use with an external charge pump. The TPS51103 offers an innovative solution for optimizing the complex and multiple power rails typically found in a Notebook Computer. The TPS51103 is available in the 10-pin QFN package and is specified from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### TYPICAL APPLICATION CIRCUIT



UDG-08017



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION

$T_A$	PACKAGE	PART NUMBER	TAPE & REEL QUANTITY	ECO-PLAN
–40°C to 85°C	Plastic DRC <sup>(1)</sup>	TPS51103DRCT	250	Green (RoHS and No Sb/Br)
		TPS51103DRCR	3000	

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	VALUE	UNIT
Input voltage range <sup>(2)</sup>	V <sub>IN</sub>	–0.3 to 30
	EN3, EN5, V3IN	–0.3 to 6
	V5IN	–0.3 to 6
	V5IN, (V <sub>VIN</sub> < 5.7 V)	–0.3 to V <sub>VIN</sub> + 0.3
Output voltage range <sup>(2)</sup>	V <sub>RTC3</sub> , V <sub>CLK</sub> , V <sub>REG3</sub> , V <sub>REG5</sub>	–0.3 to 6
Junction temperature, T <sub>J</sub>	150	°C
Storage temperature, T <sub>st</sub>	–55 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### DISSIPATION RATINGS<sup>(1)</sup>

PACKAGE	POWER RATING BELOW AND AT $T_A = 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
10-pin DRC	1.256 W	12.6 mW/°C	0.502 W

(1)  $\theta_{JA}$  (junction to air) for high-K board in still air environment is 80°C/W.

### RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Input voltage range	V <sub>IN</sub>	4.5	28	V
	EN5, EN3, V3IN	–0.1	5.5	
	V5IN	–0.1	5.5	
	V5IN, (V <sub>VIN</sub> < 5.5 V)	–0.1	V <sub>VIN</sub>	
Output voltage range	V <sub>CLK</sub> , V <sub>RTC3</sub> , V <sub>REG3</sub> , V <sub>REG5</sub>	–0.1	5.5	
Operating free-air temperature, T <sub>A</sub>	–40		85	°C

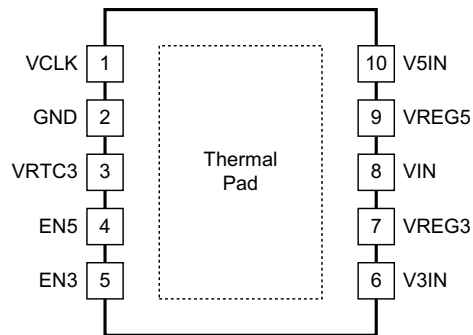
**ELECTRICAL CHARACTERISTICS**

 over recommended free-air temperature range,  $V_{VIN}=12\text{ V}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{VIN}$	VIN supply current	$I_{VIN}$ current, $T_A = 25^\circ\text{C}$ , No Load, $V_{EN3}=V_{EN5}=5\text{ V}$ , $V_{V5IN} = V_{V3IN} = 0\text{ V}$		35	50	$\mu\text{A}$
$I_{VINSTBY}$	VIN standby current	$I_{VIN}$ current, $T_A = 25^\circ\text{C}$ , No Load, $V_{EN3}=V_{EN5}= 0\text{ V}$ , $V_{V5IN} = V_{V3IN} = 0\text{ V}$		7	20	$\mu\text{A}$
<b>VRTC3 OUTPUT</b>						
$V_{VRTC3}$	VRTC3 output voltage	$I_{VRTC3} = 1\text{ mA}$ , $T_A = 25^\circ\text{C}$	3.27	3.32	3.37	V
		$0\text{ A} < I_{VRTC3} < 5\text{ mA}$ , $5.5\text{ V} < V_{VIN} < 28\text{ V}$	3.17		3.43	
		$0\text{ A} < I_{VRTC3} < 5\text{ mA}$ , $4.5\text{ V} < V_{VIN} \leq 5.5\text{ V}$	3.15		3.43	
$I_{VRTC3}$	VRTC3 output current	$V_{VRTC3} = 2\text{ V}$	5	10	15	mA
<b>VREG5 OUTPUT</b>						
$V_{VREG5}$	VREG5 output voltage	$V_{V5IN} = 0\text{ V}$ , $I_{VREG5} = 1\text{ mA}$ , $T_A = 25^\circ\text{C}$	4.95	5.05	5.15	V
		$V_{V5IN} = 0\text{ V}$ , $10\text{ }\mu\text{A} < I_{VREG5} < 100\text{ mA}$ , $6.5\text{ V} < V_{VIN} < 28\text{ V}$	4.80		5.20	
		$V_{V5IN} = 0\text{ V}$ , $0\text{ A} \leq I_{VREG5} < 50\text{ mA}$ , $5.5\text{ V} < V_{VIN} < 28\text{ V}$	4.75		5.25	
$V_{VREG5DO}$	VREG5 drop out voltage	$V_{V5IN} = 0\text{ V}$ , $I_{VREG5} = 50\text{ mA}$ , $V_{VREG5} = 4.5\text{ V}$		400	750	mV
$I_{VREG5}$	VREG5 output current	$V_{V5IN} = 0\text{ V}$ , $V_{VREG5} = 4.5\text{ V}$	100	160	250	mA
$V_{TH5VSW}$	Switch overthreshold	Turns on	4.45	4.65	4.80	V
		Hysteresis	25	50	75	mV
$R_{5VSW}$	5V SW $R_{DS(on)}$	$V_{V5IN} = 5\text{ V}$ , $I_{VREG5} = 100\text{ mA}$		1		$\Omega$
$Td_5$	Delay for 5V SW	Turns on		1		ms
<b>VREG3 OUTPUT</b>						
$V_{VREG3}$	VREG3 output voltage	$V_{V3IN} = 0\text{ V}$ , $I_{VREG3} = 1\text{ mA}$ , $T_A = 25^\circ\text{C}$	3.23	3.33	3.37	V
		$V_{V3IN} = 0\text{ V}$ , $10\text{ }\mu\text{A} < I_{VREG3} < 100\text{ mA}$ , $6.5\text{ V} < V_{VIN} < 28\text{ V}$	3.17		3.43	
		$V_{V3IN} = 0\text{ V}$ , $0\text{ A} < I_{VREG3} < 50\text{ mA}$ , $5.5\text{ V} < V_{VIN} < 28\text{ V}$	3.14		3.47	
		$V_{V3IN} = 0\text{ V}$ , $0\text{ A} < I_{VREG3} < 50\text{ mA}$ , $4.5\text{ V} < V_{VIN} \leq 5.5\text{ V}$	3.00		3.47	
$I_{VREG3}$	VREG3 output current	$V_{V3IN} = 0\text{ V}$ , $V_{VREG3} = 3\text{ V}$	100	150	250	mA
$V_{TH3VSW}$	Switchover threshold	Turns on	2.95	3.07	3.17	V
		Hysteresis	20	35	50	mV
$R_{3VSW}$	3V SW $R_{DS(on)}$	$V_{V3IN} = 3.3\text{ V}$ , $I_{VREG5} = 100\text{ mA}$		1.5		$\Omega$
$Td_3$	Delay for 3V SW	Turns on		1		ms
<b>LOGIC THRESHOLD</b>						
$V_{THEN}$	EN3, EN5 threshold	Enable		1.05	2.0	V
		Shutdown	0.3	0.7		
$I_{EN3,5}$	EN3, EN5 pulldown current	$V_{EN3} = 3\text{ V}$ , $V_{EN5} = 3\text{ V}$	0.5	1.5	3.0	$\mu\text{A}$
<b>VCLK OUTPUT</b>						
$f_{VCLK}$	Clock frequency	$T_A = 25^\circ\text{C}$	200	250	320	kHz
$R_{VCLK}$	Driver impedance	V5IN to VCLK, $I_{VCLK} = 10\text{ mA}$		6	15	$\Omega$
		VCLK to GND, $I_{VCLK} = 10\text{ mA}$		4	15	
$V_{THV5IN}$	V5IN threshold	VCLK on	1.5	2.0	2.5	V
		Hysteresis		0.3		
<b>THERMAL SHUTDOWN</b>						
TSDN	Thermal SDN threshold	Shutdown temperature <sup>(1)</sup>		150		$^\circ\text{C}$
		Hysteresis <sup>(1)</sup>		20		

(1) Ensured by design. Not production tested.

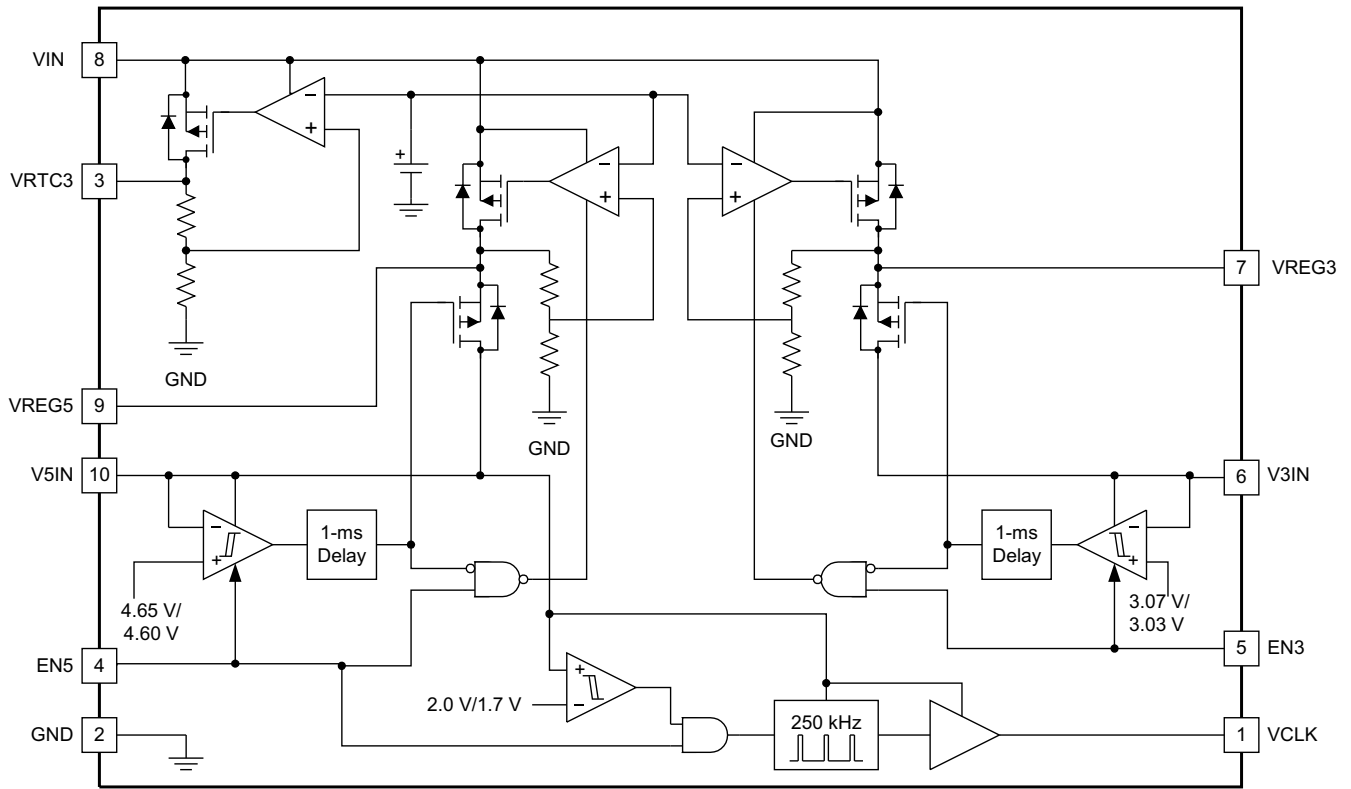
### DRC PACKAGE (Top View)



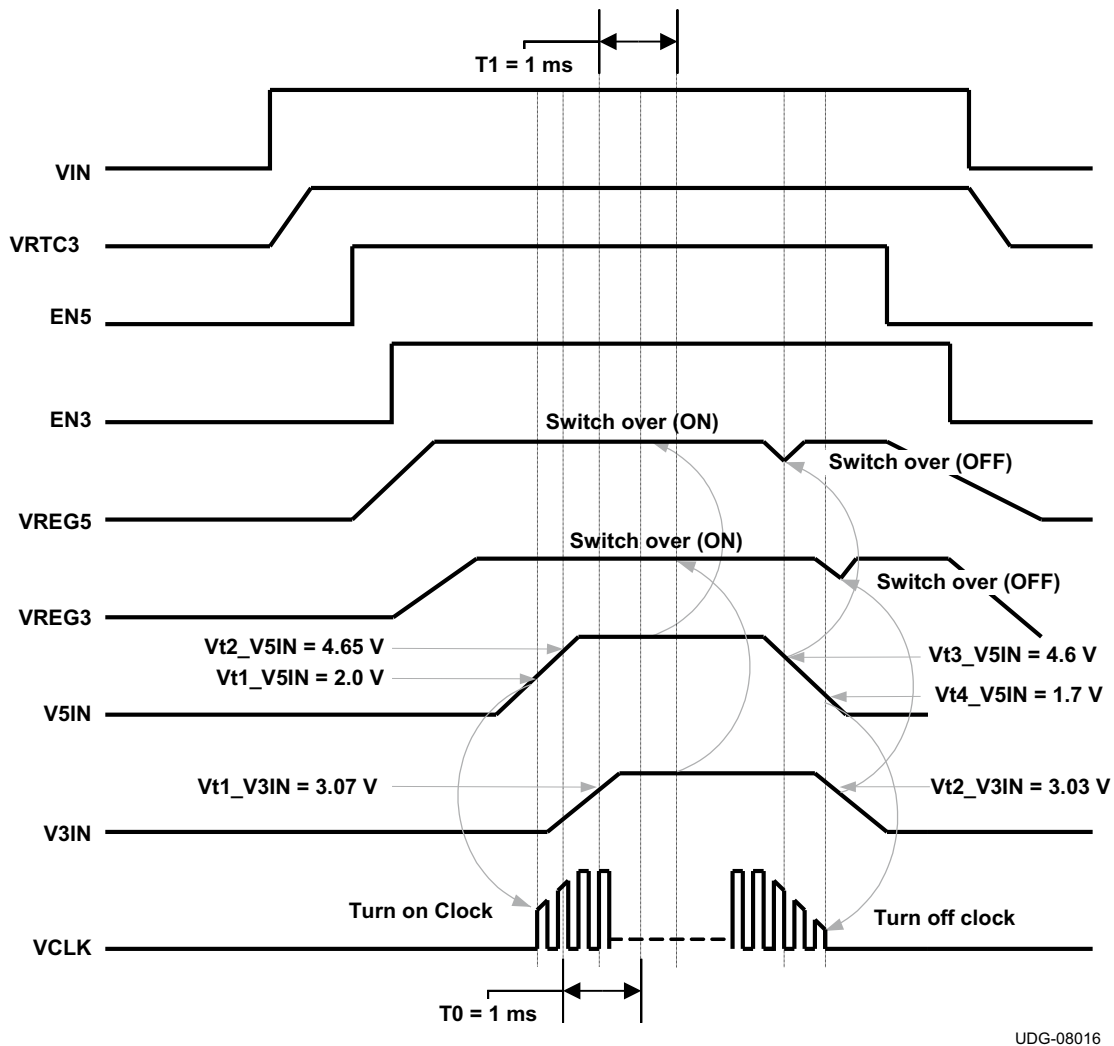
### TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN3	5	I	3.3-V LDO enable input.
EN5	4	I	5-V LDO enable input.
GND	2	–	Ground.
V3IN	6	I	3.3-V switchover power supply input. Switchover occurs 1 ms after this input voltage reaches the threshold voltage.
V5IN	10	I	5-V switchover power supply input. Switchover occurs 1 ms after this input voltage reaches to threshold voltage.
VCLK	1	O	50% duty 250-kHz clock output for charge pump power supply.
VIN	8	I	Power supply input for LDOs.
VREG3	7	O	3.3-V 100 mA LDO output.
VREG5	9	O	5-V 100 mA LDO output.
VRTC3	3	O	3.3-V 5 mA always on LDO output for RTC.

FUNCTIONAL BLOCK DIAGRAM



UDG-08026



UDG-08016

Figure 1. Power Sequencing

## DETAILED DESCRIPTION

### GENERAL DESCRIPTION

The TPS51103 integrates three LDOs. The VREG5 and VREG3 can each deliver 100 mA of current. The device includes glitch free switch-over circuits which turn off VREG5 and VREG3 LDOs and switch VREG5 and VREG3 to V5IN and V3IN external power inputs respectively when the external high efficiency 5V and 3.3V power rails are available. It improves overall system efficiency and therefore extends battery life. An additional 5-mA VRTC3 LDO is designed to provide an *always on* feature for the real time clock (RTC). A 5-V clock with 50% duty cycle runs at 250 kHz. It can be used as a simple external charge pump driver to generate a 10-V or 15-V low-current voltage rail (see Figure 2). In the notebook application, the 10 V or 15 V created by this circuit could be used to drive an N-channel MOSFET instead of the traditional P-channel MOSFET load switch. The TPS51103 boosts performance and reduce the cost of load switch.

## VREG5

When EN5 is asserted high, VREG5 supplies 5 V through an LDO from  $V_{IN}$ . Its maximum sourcing current is 100 mA. If EN5 is high and the V5IN voltage becomes higher than 4.65 V, then the VREG5 output is switched over to the V5IN input after a 1-ms delay. In the switched over condition, the LDO is turned off and VREG5 is connected to V5IN through the 1.0- $\Omega$   $R_{DS(on)}$  MOSFET switch. When the V5IN voltage becomes lower than 4.6 V, this MOSFET turns off and 5-V LDO is turned back on immediately. A bypass ceramic capacitor is required to stabilize LDO. The recommended value is between 10  $\mu$ F and 22  $\mu$ F. Place the bypass capacitor close to the VREG5 pin. When EN5 is asserted low, both the 5-V LDO and switchover circuit are turned off.

## VREG3

When EN3 is asserted high, VREG3 supplies 3.3 V through an LDO from  $V_{IN}$ . Its maximum sourcing current is 100 mA. If EN3 is high and the V3IN voltage becomes higher than 3.07 V, then the VREG3 output is switched over to the V3IN input after a 1-ms delay. In the switched over condition, LDO is turned off and VREG3 is connected to V3IN through the 1.5- $\Omega$   $R_{DS(on)}$  MOSFET switch. When the V3IN voltage becomes lower than 3.03 V, this MOSFET turns off and the 3.3-V LDO is turned back on immediately. A bypass ceramic capacitor is needed to stabilize LDO, recommended value is between 10  $\mu$ F and 22  $\mu$ F. Place the bypass capacitor close to the VREG3 pin. When EN3 is asserted low, both the 3.3-V LDO and the switchover circuit are turned off.

## VRTC3

This 3.3-V low-current auxiliary power source is typically used for the system's RTC bias voltage. It is powered on after  $V_{IN}$  is applied. A ceramic capacitor with a value between 1  $\mu$ F and 2.2  $\mu$ F placed close to the VRTC3 pin is needed to stabilize the LDO.

## VCLK OUTPUT

When the V5IN voltage becomes higher than 2.0 V, the internal 250-kHz clock turns on and the VCLK pin outputs a 50% duty-cycle clock signal. The voltage swing of VCLK is equal to the GND to V5IN voltage

## THERMAL SHUTDOWN

When the device temperature exceeds the internal threshold value (typically 150C) the TPS51103 shuts off the VREG3, VREG5 and VCLK outputs. This is a non-latch protection.

## THERMAL DESIGN

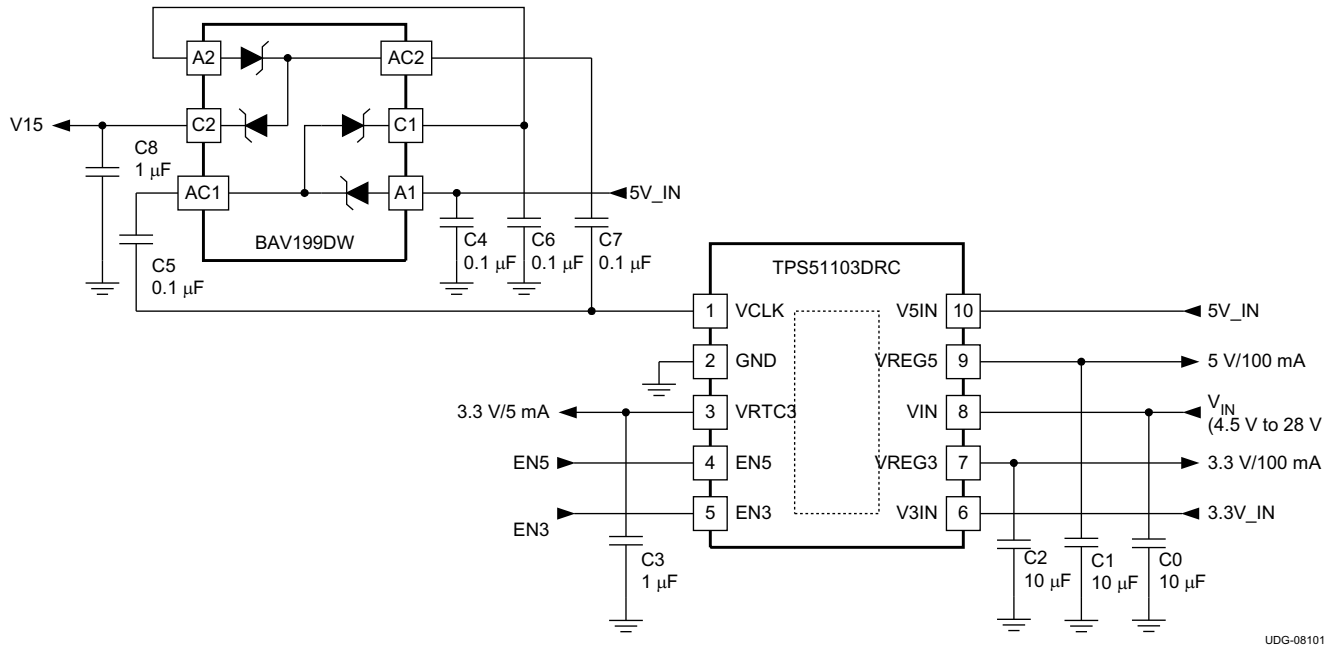
The thermal performance greatly depends on the printed circuit board (PCB) layout. The TPS51103 is housed in a thermally-enhanced PowerPAD™ package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to ground via thermal land on the PCB. This ground trace acts as a heatsink and a heat spreader. For further information regarding the PowerPAD™ package and the recommended board layout, refer to the PowerPAD™ package application note ([SLMA002](#)). This document is available at [www.ti.com](http://www.ti.com).

## LAYOUT GUIDELINES

Consider the following points before starting the TPS51103 layout design.

- The input bypass capacitor for  $V_{IN}$  should be placed as close as possible to the pin with short and wide connection.
- The output capacitors for VREG5, VREG3 and VRTC3 should be placed close to the pins with short and wide connections.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. Wide copper traces connected to the thermal land help to dissipate heat. Numerous 0.33 mm diameter vias are connected from the thermal land to the internal and/or solder-side system ground plane(s) can also be used to help dissipation.
- The GND pin, output capacitors for VREG5, VREG3 and VRTC3 should be connected to the internal and/or solder-side system ground plane(s) with multiple vias. Use as many vias as possible to reduce the impedance between them and the system ground plane.

APPLICATION INFORMATION



UDG-08101

Figure 2. Typical Application



TYPICAL CHARACTERISTICS

INPUT CURRENT  
vs  
INPUT VOLTAGE

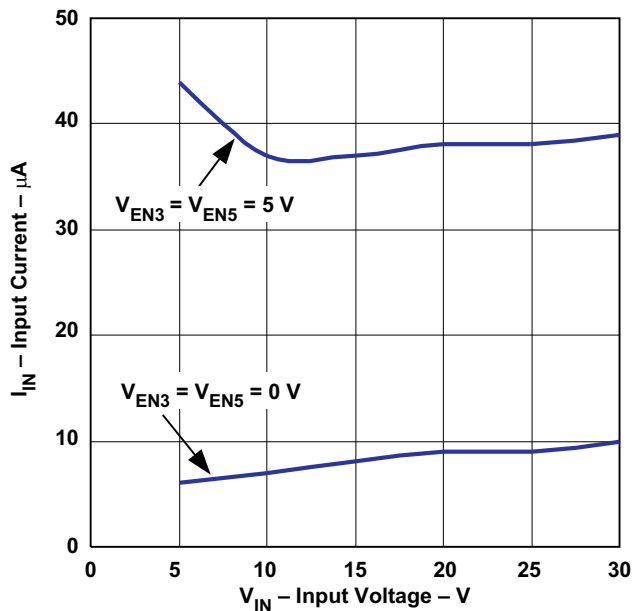


Figure 3.

VREG3 LDO OUTPUT VOLTAGE  
vs  
LDO OUTPUT CURRENT

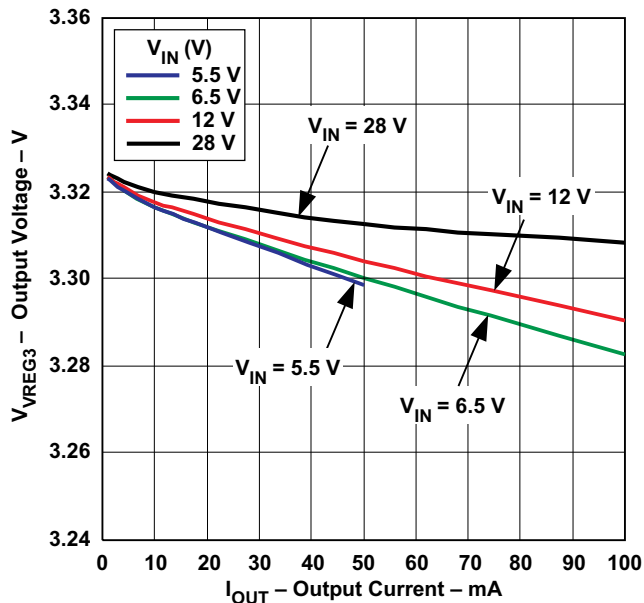


Figure 4.

VREG5 LDO OUTPUT VOLTAGE  
vs  
LDO OUTPUT CURRENT

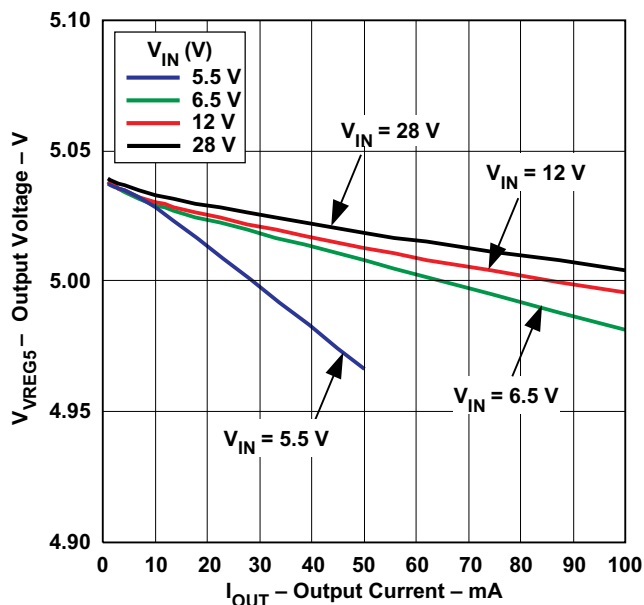


Figure 5.

CHARGE PUMP OUTPUT VOLTAGE  
vs  
CHARGE PUMP OUTPUT CURRENT

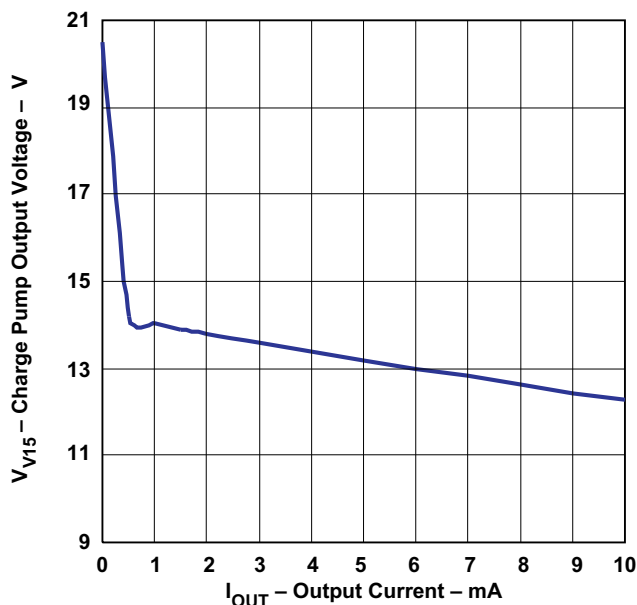


Figure 6.

TYPICAL CHARACTERISTICS (continued)

ALWAYS ON OUTPUT VOLTAGE  
vs  
ALWAYS ON OUTPUT CURRENT

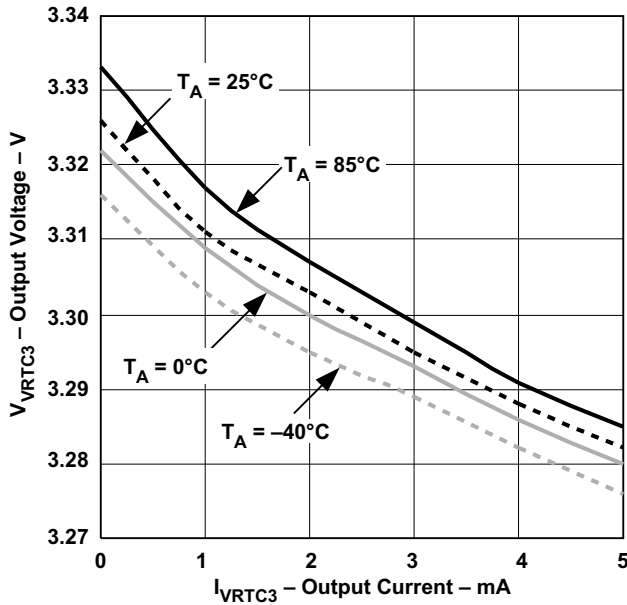


Figure 7.

VREG5 SWITCHOVER OUTPUT VOLTAGE  
vs  
VREG5 SWITCHOVER OUTPUT CURRENT

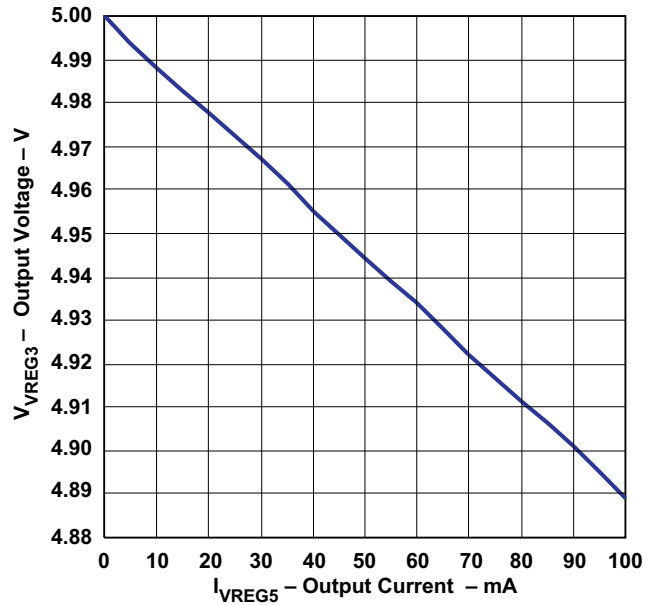


Figure 8.

VREG3 SWITCHOVER OUTPUT VOLTAGE  
vs  
VREG3 SWITCHOVER OUTPUT CURRENT

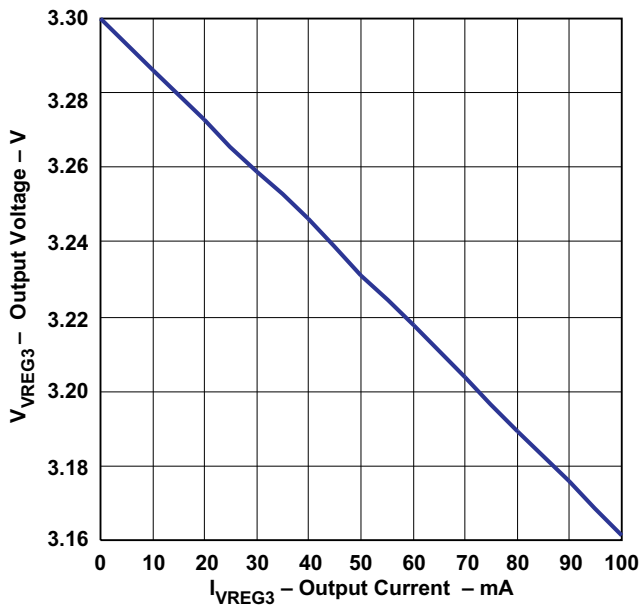


Figure 9.

INPUT CURRENT  
vs  
JUNCTION TEMPERATURE

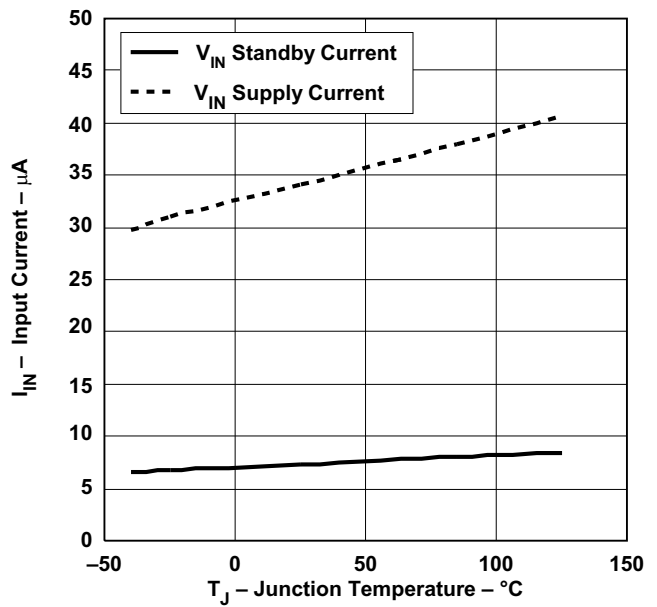


Figure 10.

TYPICAL CHARACTERISTICS (continued)

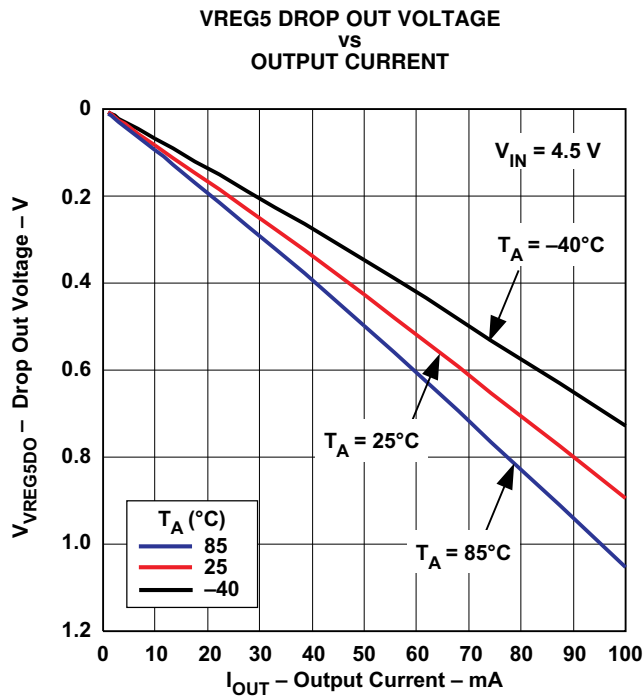


Figure 11.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51103DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51103DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

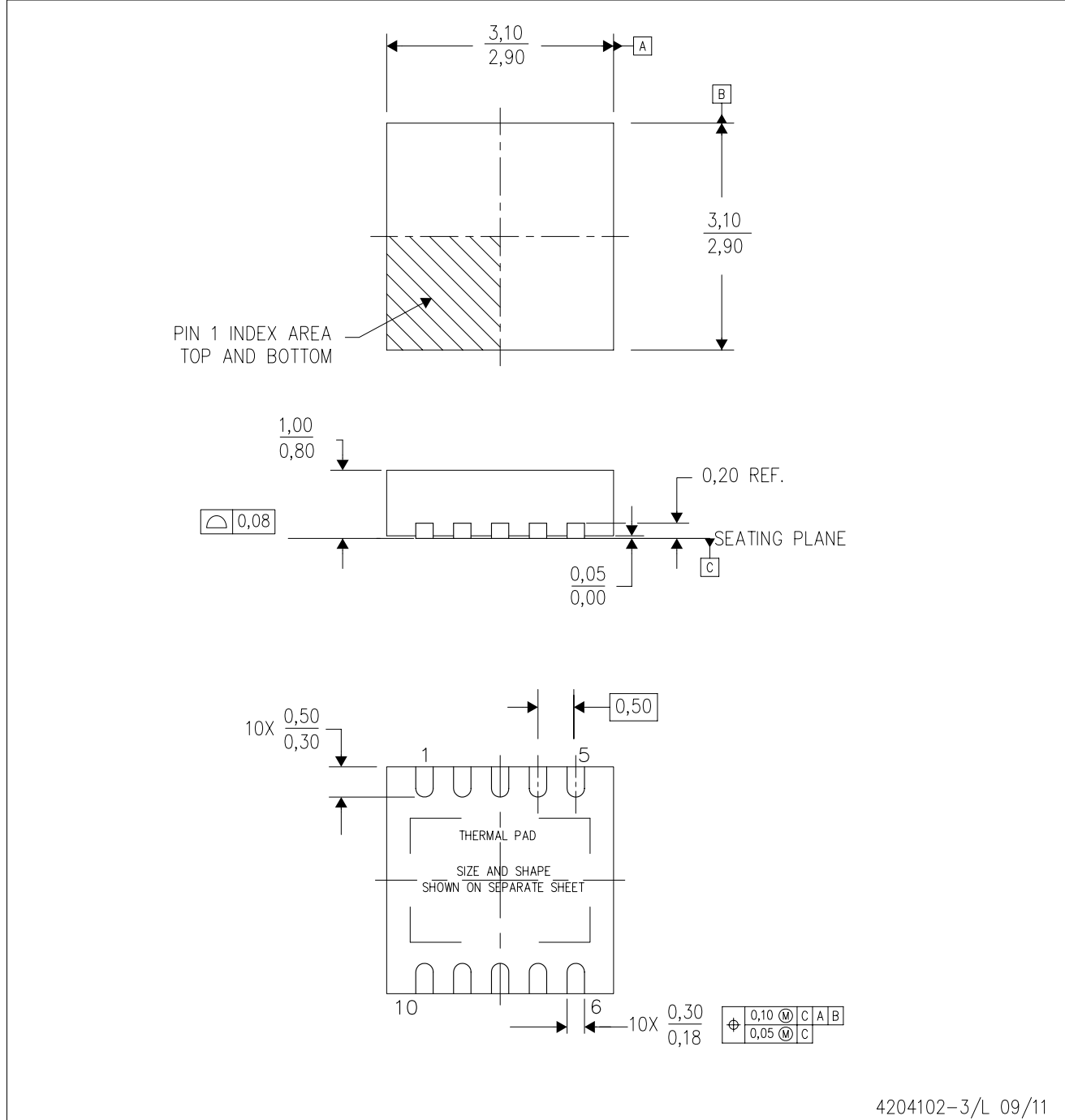
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51103DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS51103DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

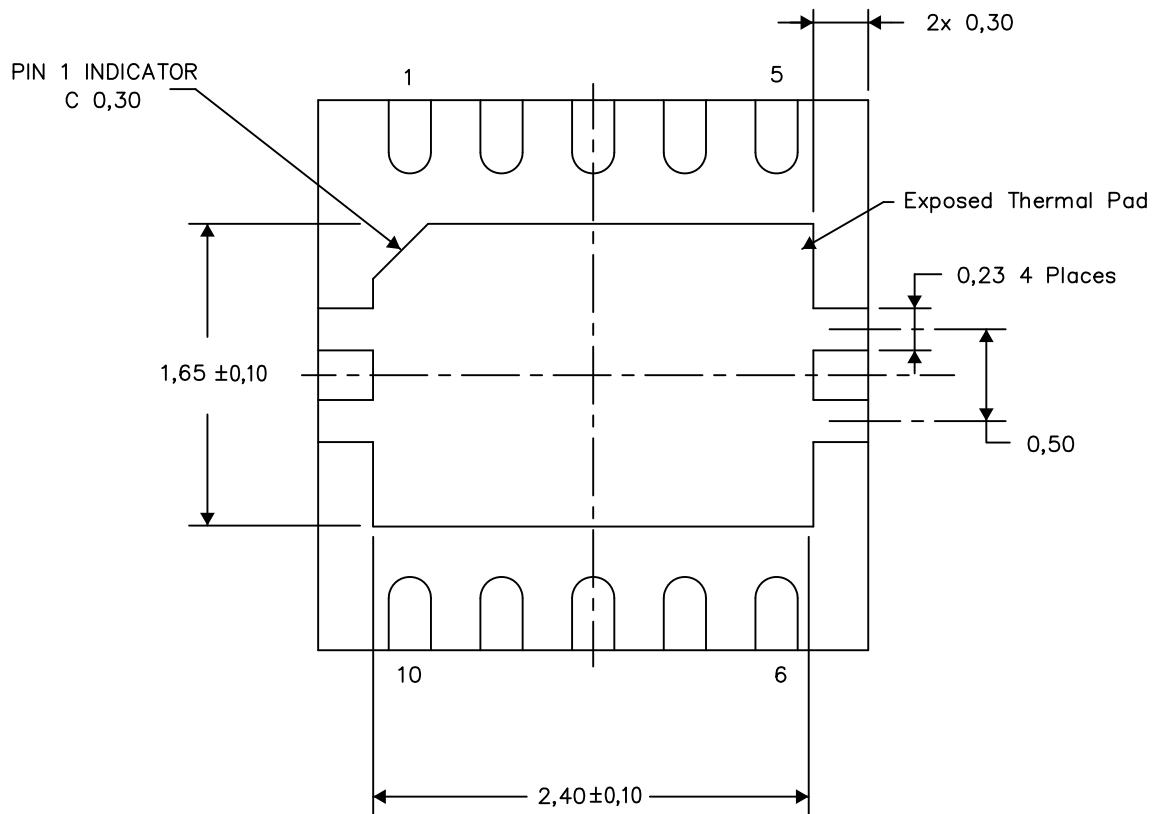
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

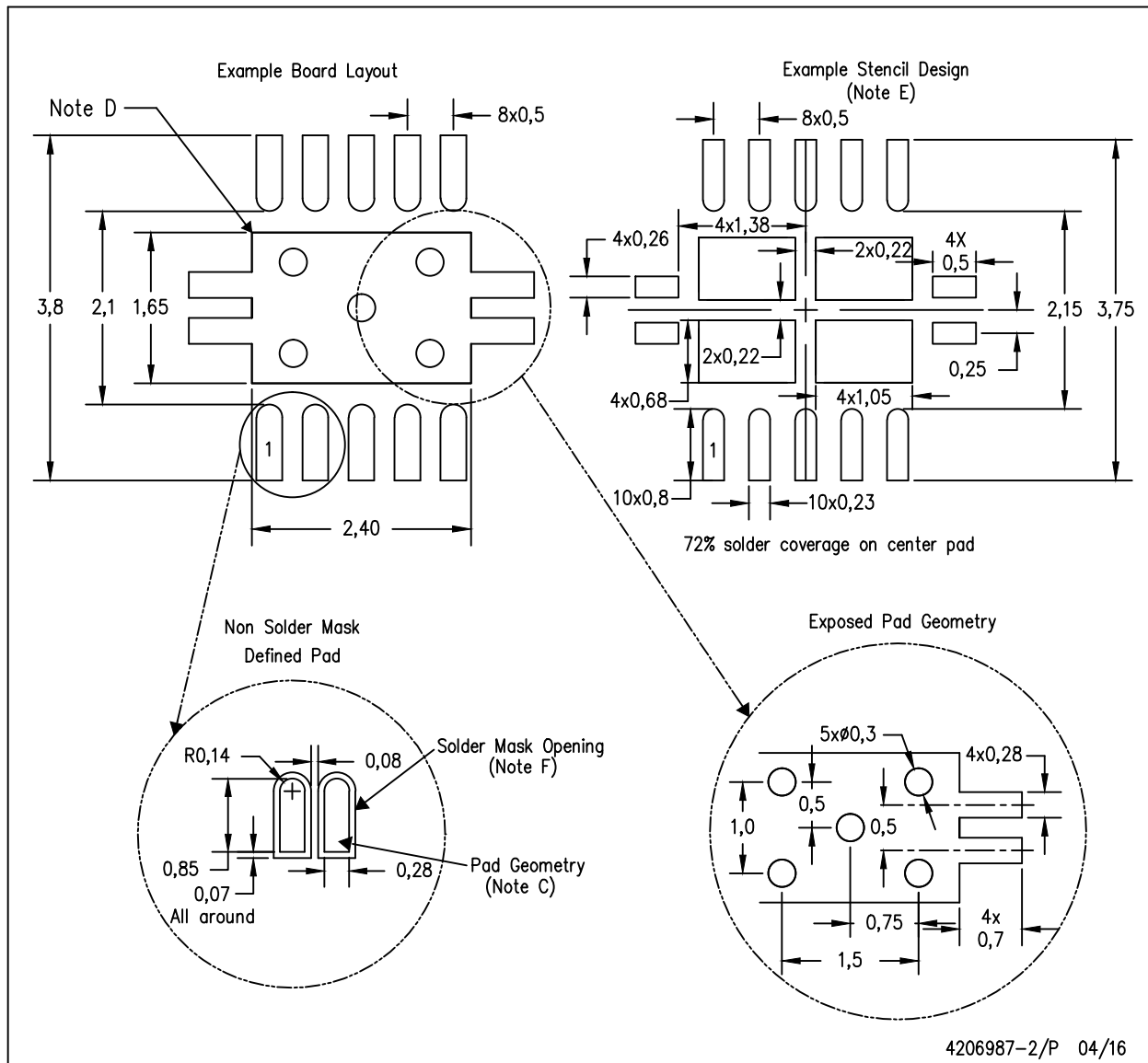
4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

# LAND PATTERN DATA

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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