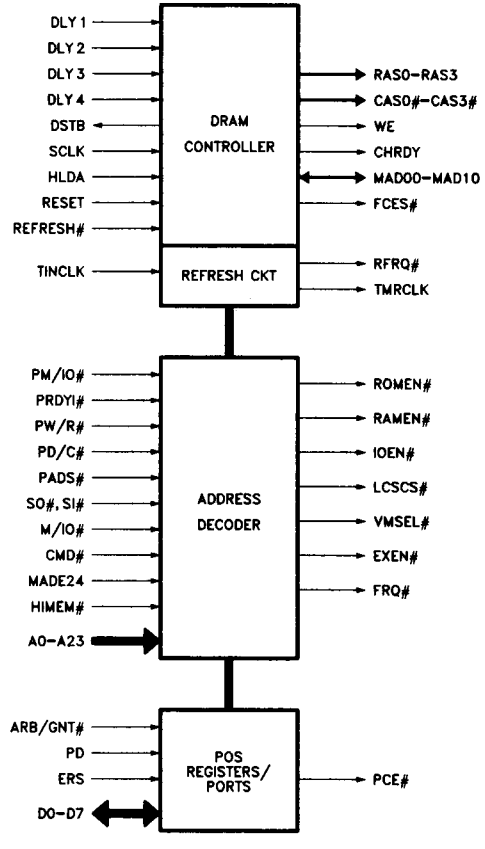
82309
ADDRESS BUS CONTROLLER

- **Address Decoder**
- **DRAM Controller . . . Up to Four Banks of Page Interleaved Memory (Max 16M)**
- **Refresh Timer**
- **Integrated I/O Ports and Registers**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Packaging**
  (See Packaging Specifications, Order # 240800-001, Package Type KU)

The 82309 Address Bus Controller provides Address decoding for devices on the motherboard, including the shadowed DRAM address of the ROM BIOS. The Address Bus Controller also has integrated DRAM controller, Refresh Timer and miscellaneous registers for memory control and error recovery, specifically ports E0, E1, E3, E4, E5, E7 and 103.

The 82309 Address Bus Controller provides the designer several price/performance choices for the configuration of up to 16 MBytes of Page Interleave DRAM memory on the motherboard. Up to four banks of 256K, 1M and 4M DRAMs are supported.

The 82309 Address Bus Controller generates periodic refresh requests to the 82307 DMA controller to run refresh cycles. The 82309 does not use the Refresh Address generated by the DMA controller but provides its own refresh address to the 256K, 1M and 4M DRAMs.



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PORTS AND REGISTERS

Configuration bits SS1 and SS2 control the function of the Ports and Register Block. The Ports and Register Block, in turn, control the function of the Refresh Timer and the address mapping of the motherboard DRAMs and the BIOS EPROMs.

SS1 and SS2 essentially select one of four definitions of the memory encoding registers (E0, E1), error trace registers (E3, E4, E5, E7), and motherboard POS setup port (103). These defintions are depicted in Table 0, and go by the names System A, System B, System C and System D.

System A presents a Model 50/60 compatible definition of these ports. Specifically, Port 103 is defined as it is in the IBM PS/2 Model 50/60 Technical Reference and ports E0–E7 are non-existent. System B presents a Model 80 compatible definition of these ports, as detailed in the IBM PS/2 Model 80 Technical Reference.

System B has a limitation in that due to the definition of the card enable bits in ports E0 and E1 (described later), it is limited to 4 Mbytes of system board memory. System C overcomes this by making the card enable bits "free form"; i.e., accessible as read/write bits, but otherwise meaningless in terms of their effect on the system. System C allows a Model 80 type system to provide up to 16 Mbytes of system board memory.

System D provides a Model 50/60 compatible definition of port 103 and a Model 80 compatible definition of ports E0–E7. This system is targeted for designs that wish to present a Model 50/60 port definition, but wish to make use of features provided in the Model 80 register set, specifically the ability to copy ROM into RAM for increased performance. This system requires external logic (approx. ½ of a 16L8 PAL) that essentially makes E0–E7 disappear from a software point of view once the ROM has been copied into RAM. (Details are provided in the *82311 Micro Channel Compatible Peripheral Chip Set Designer's Guide.*)

In systems A and D, bit 0 (the Memory Enable Bit) is the only accessible bit in Port 103. This bit can be accessed via channel I/O Read and/or Write operations. When Port 103 is read only bit 0 is driven, all other data bus bits remain tristated. This bit is set to a 1 by RESET. When the Memory Enable Bit = 0 all of the motherboard DRAM is disabled (but still refreshed). In both systems A and D, the refresh timer produces a 400 ns pulse every 15.12 μs. In system D, mapping is controlled by ports E0 and E1, as described in a moment. In system A, the other functions of the ports and register block are as follows:

— The Split in the first megabyte is located at 640 Kbytes.

— If the motherboard DRAM space equals 16 Mbytes then the remaining DRAM is disabled, otherwise the remaining 384 Kbytes are remapped to the first 384 Kbytes past the end of

Table 0. Configuration Bits SS1, SS2 Definition

Config Bits		System	Description
SS1	SS2		
0	0	A	Model 50/60 Compatible Port 103(1) Registers E0–E7 Non-Accessible
1	0	B	Model 80 Compatible Port 103 Error Trace Registers E3, E4, E5 and E7 Accessible Memory Encoding Registers E0 and E1 Accessible Compatible Card Enable Bits in E0 and E1
1	1	C	Model 80 Compatible Port 103 Error Trace Registers E3, E4, E5 and E7 Accessible Memory Encoding Registers E0 and E1 Accessible Free Form Card Enable Bits In E0 and E1
0	1	D	Model 50/60 Compatible Port 103 Error Trace Registers E3, E4, E5 and E7 Accessible (But Not Typically Used) Memory Encoding Registers E0 and E1 Accessible Free Form Card Enable Bits In E0 and E1

NOTES:
1. Port 103 is a motherboard POS port; i.e., accessible only when the motherboard is in Setup Mode.

the motherboard DRAM address space. (i.e., if there are 4 Mbytes of DRAM then the split is remapped to address 00400000 → 0045FFFF.)

— The BIOS EPROMs are mapped to both 000E0000 → 000FFFFF and FFFE0000 → FFFFFFFF.

In systems B and C, port 103 is defined as follows:

— Port 103 bit 0 (the Memory Enable Bit) is not accessible.

— Port 103 bit 1 (the Refresh Rate Bit) is accessible for write operations only. If this bit is a 1 then the Refresh Timer produces an approximately 400 ns long pulse once every 15.12 μs. If this bit is a 0 then the Refresh Timer produces a continuous stream of 400 ns pulses with a period of approximately 800 ns. This bit is set to a 1 by RESET.

In systems B, C and D, ports E0, E1, E3, E4, E5 and E7 are defined as follows:

— Four of the Read only Micro Channel Error Trace Registers (Ports 00E3, 00E4, 00E5 and 00E7) are accessible. (Typically, a system D design will not utilize these registers and will thus not require any external logic to implement any error register support.) These registers sample SA<02:23>, M/IO#, D/C# and ARB/GNT# on every rising edge of the ERS input pin. The bit assignments for these registers are as follows:

Bit	00E3	00E4	00E5	00E7
7	SA23	SA15	SA07	—
6	SA22	SA14	SA06	—
5	SA21	SA13	SA05	—
4	SA20	SA12	SA04	—
3	SA19	SA11	SA03	—
2	SA18	SA10	SA02	—
1	SA17	SA09	M/IO#	—
0	SA16	SA08	ARB/GNT#	D/C#

These four registers are all set to 00 by RESET. When Register E7 is read, only data bus bit 0 is driven by the ABC, data bus bit 1–7 remain tristated.

— Registers E0 and E1 are accessible via the channel for both I/O read and I/O write operations. These two registers control the address mapping of both the motherboard DRAMs and the BIOS EPROMs. (The reset state of E0 and E1 is FF.) The two most significant bits of both of these registers are free form register bits and have no effect on the functioning of the ABC. The functioning of the two next most significant bits (bits 5 & 4, the card enable bits) of both of these registers are controlled by configuration bits SS2 and SS1 as discussed in a moment.

— The four least significant bits (bits 3, 2, 1 & 0) of register E1 are defined as follows:

Bit 3	2	1	0	
0	.	.	.	- Memory beyond split Enabled
1	.	.	.	- Memory beyond split Disabled
.	0	.	.	- Split is at 640K (000A0000)
.	1	.	.	- Split is at 512K (00080000)
.	.	0	.	- BIOS ROMs deactivated in 000E0000 to 000FFFFF BIOS ROMs active in FFFE0000 to FFFFFFFF Shadow RAM Write Protected
.	.	1	.	- BIOS ROMs active in 000E0000 to 000FFFFF BIOS ROMs active in FFFE0000 to FFFFFFFF Shadow RAM Writeable.
.	.	.	0	- Parity Checking enabled
.	.	.	1	- Parity Checking disabled

If the memory beyond the Split is enabled by bit 3 then the four least significant bits (bits 3, 2, 1 & 0) of register 00E0 define the address range in memory where the portion of the first megabyte of system RAM beyond the split will be remapped. Bits 3, 2, 1 & 0 of this register correspond to address bits 23, 22, 21 & 20 of the remap location for this memory.

Bit 2 of register E1 defines the partitioning of the first megabyte of the motherboard DRAM. Figure 0 details the effect of this bit. The S in the remap addresses represents the value of the four least significant bits of register E0.

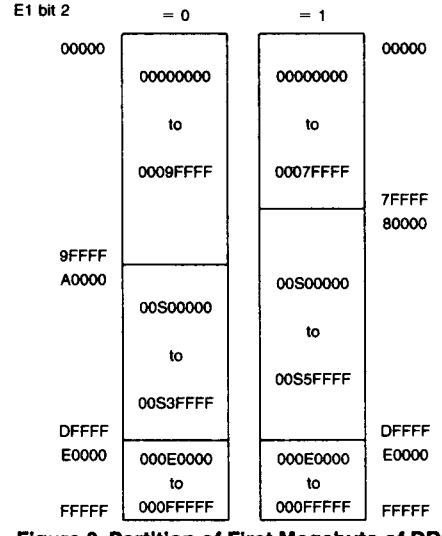


Figure 0. Partition of First Megabyte of DRAM

There is DRAM mapped in the address range 000E0000 to 000FFFFF. The function of this DRAM is controlled by bit 1 of register E1. If bit 1 = 1 then this RAM is writeable but not readable (thus the BIOS EPROMs can be Shadowed by Reading and Writing to the same address). If bit 1 = 0 then the BIOS EPROMs are disabed and this area of RAM is read enabled but write protected.

When bit 1 of register E1 is a 1 both the ROMEN# and the RAMEN# signals will respond to accesses in the range 000E0000 to 000FFFFF. In this way, the 82308 Bus Controller knows to direct reads to ROM and writes to RAM to allow shadowing. (In system D, if memory is disabled via bit 0 of port 103, then ROM is enabled in 000E0000 to 000FFFFF, regardless of the status of bit 1 in E1.)

Bit 0 of register E1 is output to the Bus Controller on the PCE# pin for use as an (active low) Parity Check Enable control bit.

— In system B, the amount of the physical motherboard DRAM that is accessable is controlled by the card enable bits (bits 5 and 4 of registers E0 and E1). These four bits act as enables (active low) for each of the first four megabytes of the physical motherboard DRAM space. Any additional DRAM controlled by the ABC will be refreshed but is otherwise disabled.

Register				Function
E0		E1		
Bit 5	Bit 4	Bit 5	Bit 4	
0	X	X	X	Megabyte #3 Enabled
1	X	X	X	Megabyte #3 Disabled
X	0	X	X	Megabyte #2 Enabled
X	1	X	X	Megabyte #2 Disabled
X	X	0	X	Megabyte #1 Enabled
X	X	1	X	Megabyte #1 Disabled
X	X	X	0	Megabyte #0 Enabled
X	X	X	1	Megabyte #0 Disabled

All megabytes that are enabled by these bits are mapped into one continuous block (with the exception of the Split from the first active megabyte) starting at address 00000000. (Thus if megabyte #0 is disabled, then the rest of the megabytes are remapped down to the range 00000000 to 002FFFFF, etc.)

In systems C and D, bits 5 and 4 of both registers E0 and E1 are free form register bits and have no effect on the functioning of the ABC.

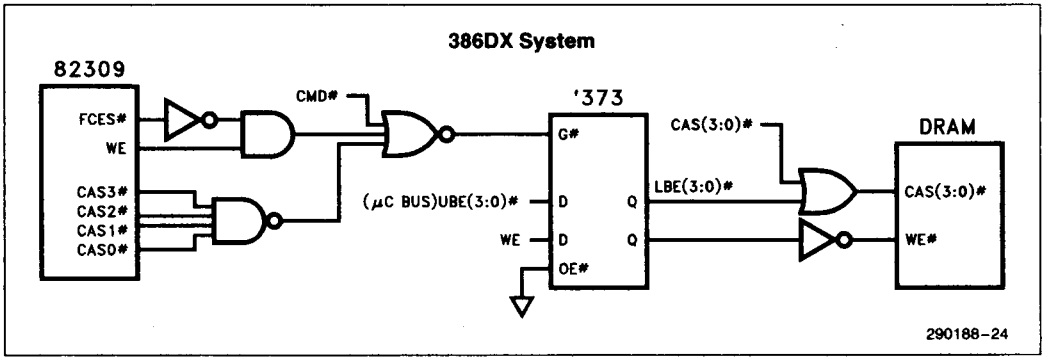
NOTE:
During pipelined mode, an accidental write to Port E0h with E1h data can occur when the latched addresses (A2:A0) are allowed to change to the next address (pipelined) before the write strobe (UCCMD#) goes inactive. For example, this can occur when (A2:A0) change from "000" to "001" while UCCMD# is active. This condition is not seen on designs which use the Intel Cache Controller (82385), since it does not allow pipelining for I/O write cycles. In systems without an 82385, UCMMD# must be synchronized prior to being input to the 82309 CMD# pin. The workaround that follows provides a comprehensive solution independent of software sequence. UCMMD# must be "ORed" with the result of the inverted 82308 IOW signal "NORed" with DMARDY#. DMARDY# is synchronized from the 82308 PRDYO# signal. The latch that generates DMARDY# is shown on Sheet 4 in the 82311 Micro Channel Peripheral Chip Set Designer's Guide schematics.

DRAM CONTROLLER

The DRAM controller supports page interleaved memory designs in the configurations shown in Table 1. This table also details which channel address bits map to which DRAM address bits. Note that even though options D and G are two-bank options, the ABC thinks of these banks as 0 and 2, not banks 0 and 1, i.e., use RAS0, RAS2, CAS0# and CAS2#.

Table 1 describes the basic memory configurations A through N. However, a wide variety of additional options can be easily realized by building on A through N with minimal external address decode logic. These additional options include the ability to mix DRAM types (for example 256K and 1M DRAMs in the same system), and allow for a great deal of flexibility in memory upgrade paths. Examples of how to do this are included in the *82311 Micro Channel Compatible Peripheral Chip Set Designer's Guide*.

Figure 1 shows the BHE#, BE#, and A0 latch for the 82309 to DRAM interface.



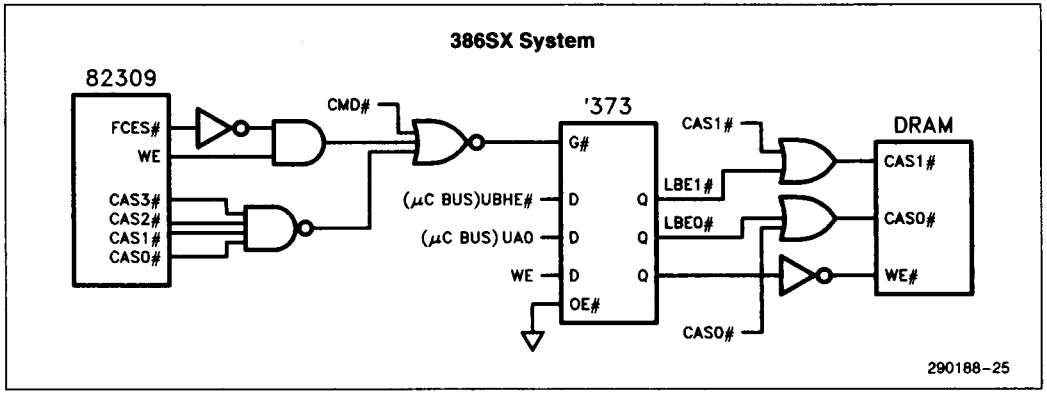


Figure 1. BHE#, BE#, A0 Latch Control

Table 1. Memory Configuration Options and Channel Address-To-DRAM Address Mapping

Opt	Size	Memory Configuration Options	Page Size
A	1M	1 Bank of 256K DRAMs (x 32) Page Mode	512
B	1M	2 Banks of 256K DRAMs (x 16) Page Mode	512
C	2M	1 Bank of 1M DRAMs (x 16) Page Mode	1024
D	2M	2 Banks of 256K DRAMs (x 32) Page Mode	512
E	2M	4 Banks of 256K DRAMs (x 16) Page Mode	512
F	4M	1 Bank of 1M DRAMs (x 32) Page Mode	1024
G	4M	2 Banks of 1M DRAMs (x 16) Page Mode	1024
H	4M	4 Banks of 256K DRAMs (x 32) Page Mode	512
I	8M	1 Bank of 4M DRAMs (x 16) Page Mode	2048
J	8M	2 Banks of 1M DRAMs (x 32) Page Mode	1024
K	8M	4 Banks of 1M DRAMs (x 16) Page Mode	1024
L	16M	1 Bank of 4M DRAMs (x 32) Page Mode	2048
M	16M	2 Banks of 4M DRAMs (x 16) Page Mode	2048
N	16M	4 Banks of 1M DRAMs (x 32) Page Mode	1024

Opt	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A					Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
B					Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
C				Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
D				Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
E				Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
F			Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
G			Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
H			Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
I		Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
J		Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
K		Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
L	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		
M	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	
N	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Ps	Bs	Bs	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws	Ws		

Ps ≥ Page Select Ws ≥ Word Select Bs ≥ Bank Select

NOTE:
Options A, C, F, I & L use Bank 0
Options D & G use Bank 0 & 2
Options B, J & M use Bank 0 & 1
Options E, H, K & N use all Banks

Opt	Ps											Ws										Bs	
	10	09	08	07	06	05	04	03	02	01	00	10	09	08	07	06	05	04	03	02	01	00	01	00
A	><	><	11	12	13	19	18	17	16	15	14	><	><	02	10	03	09	08	07	06	05	04	><	><
B	><	><	11	12	13	19	18	17	16	15	14	><	><	02	01	03	09	08	07	06	05	04	><	10
C	><	11	20	12	13	19	18	17	16	15	14	><	01	02	10	03	09	08	07	06	05	04	><	><
D	><	><	20	12	13	19	18	17	16	15	14	><	><	02	10	03	09	08	07	06	05	04	11	><
E	><	><	20	12	13	19	18	17	16	15	14	><	><	02	01	03	09	08	07	06	05	04	11	10
F	><	21	20	12	13	19	18	17	16	15	14	><	11	02	10	03	09	08	07	06	05	04	><	><
G	><	21	20	12	13	19	18	17	16	15	14	><	01	02	10	03	09	08	07	06	05	04	11	><
H	><	><	20	21	13	19	18	17	16	15	14	><	><	02	10	03	09	08	07	06	05	04	11	12
I	22	21	20	12	13	19	18	17	16	15	14	01	11	02	10	03	09	08	07	06	05	04	><	><
J	><	21	20	22	13	19	18	17	16	15	14	><	11	02	10	03	09	08	07	06	05	04	><	12
K	><	21	20	22	13	19	18	17	16	15	14	><	01	02	10	03	09	08	07	06	05	04	11	12
L	23	21	20	22	13	19	18	17	16	15	14	12	11	02	10	03	09	08	07	06	05	04	><	><
M	23	21	20	22	13	19	18	17	16	15	14	01	11	02	10	03	09	08	07	06	05	04	><	12
N	><	21	20	22	23	19	18	17	16	15	14	><	11	02	10	03	09	08	07	06	05	04	13	12

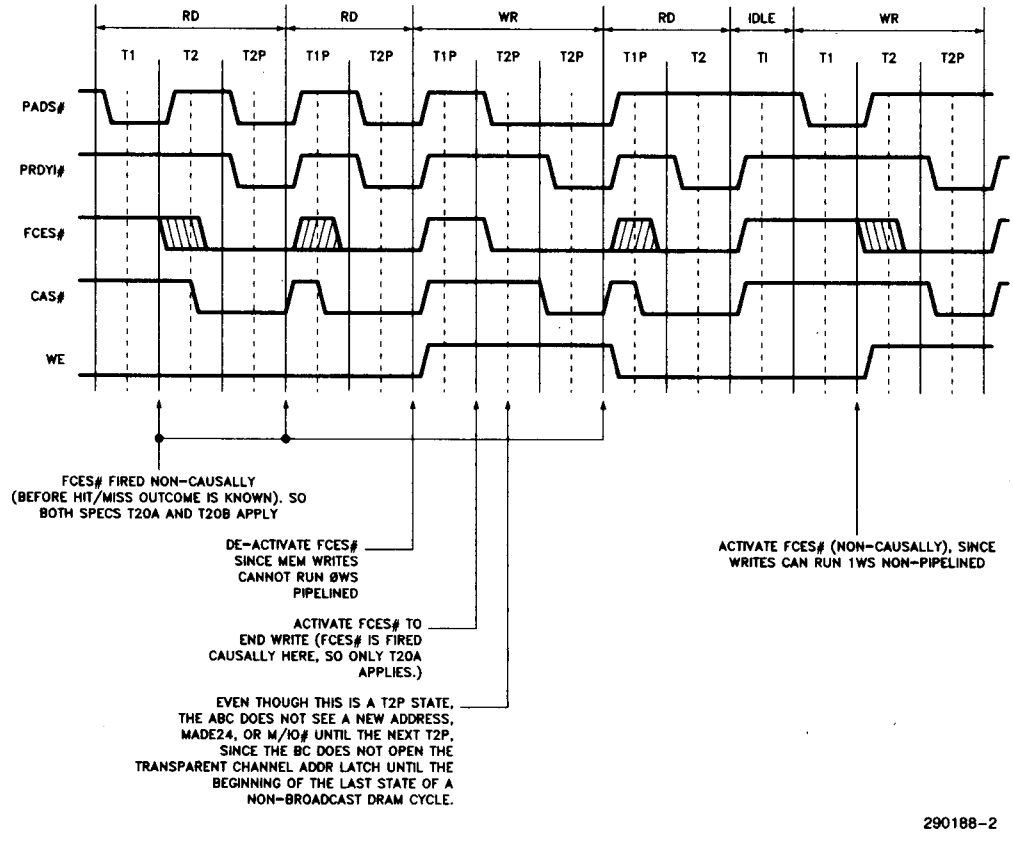
Typically, zero wait state pipelined page hit performance can be achieved at 16 MHz using 100 ns or 120 ns DRAMs, resulting in an aggregate of 0.5 to 0.8 wait states on average. The same DRAMs at 20 MHz will yield 1 wait state page hits.

At power-up, the 82309 Address Bus Controller samples its memory address bus to determine the desired system configuration. (This operation is described in detail later in the data sheet under "MAD BUS RESET CONFIGURATION".) The three configuration switches, C0, C1 and C2 are used to select a specific performance level as measured in page hit/page miss wait states. DRAM selection involves not only selecting a DRAM, but also choosing delay line taps to control the sequence of DRAM control signals, and then choosing the performance level that can be reliably supported using a particular DRAM and set of delay line taps. The next several pages describe all the available configuration options, and following this is a DRAM/Delay Tap selection guide along with some sample calculations.

Table 2. 82309 ABC Configuration and CPU Performance(3)

	Config Inputs			Pipelined Read		Pipelined Write		Non-Pipelined Read		Non-Pipelined Write		Reference Figures
	C0	C1	C2	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss	
(1)	0	0	0	0	2	1(2)	2	1	3	1(2)	3	1, 4
(1)	0	0	1	0	3	1(2)	3	1	4	1(2)	4	1, 4
(1)	0	1	0	0	4	1(2)	4	1	5	1(2)	5	1, 4
	0	1	1	1	4	1	4	2	5	2	5	2, 5
	1	0	0	1	5	1	5	2	6	2	6	2, 5
	1	0	1	1	6	1	6	2	7	2	7	2, 5
	1	1	0	1	7	1	7	2	8	2	8	2, 5
	1	1	1	2	7	2	7	3	8	3	8	3, 5

NOTES:
1. These three configuration options feature 0WS pipelined page read hits. Strapping for one of these directs the ABC to determine whether a cycle is a page hit or miss, and to generate CAS# one SCLK phase earlier then the other options. Hence, these options are only supported at 16 MHz except the SX part can run 0WS at 20 MHz because of AC Specification changes.
2. Note that both pipelined and non-pipelined write page hits run 1WS in these three configuration options.
3. The ABC completely controls the wait state counts in memory cycles according to this table via its FCES# output. The BC can however, (via its WS# strap) insert an additional wait state beyond those stated above in memory reads. (The WS# strap is intended for cache systems, which typically require additional data setup.)



NOTE:
Once the ABC fires FCES# to terminate a DRAM cycle, it remains active until the ABC detects the actual CPU end of cycle via the PRDYI# input. This allows the BC or any other external device to extend DRAM cycles if desired.

Figure 2. 0/2, 0/3, 0/4 Page Hits
(Cycles Named According to Pipelined Read Performance)

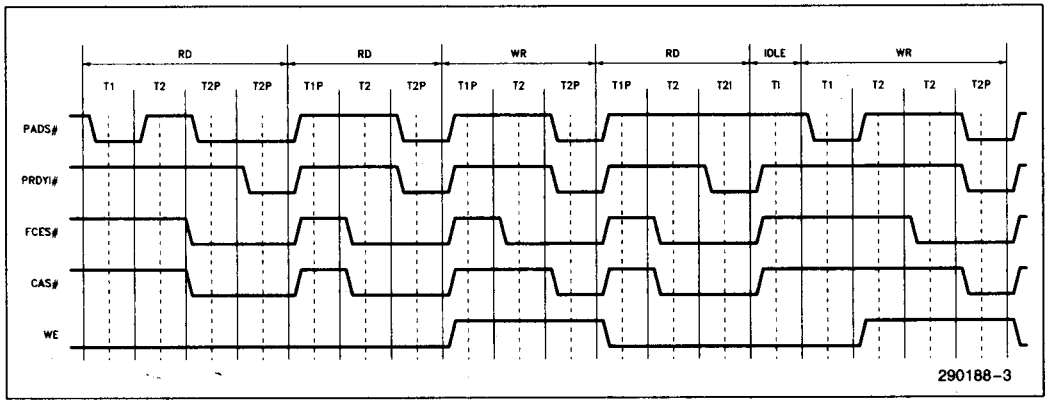


Figure 3. 1/4, 1/5, 1/6, 1/7 Page Hits (Cycles Named According to Pipelined Read Performance)

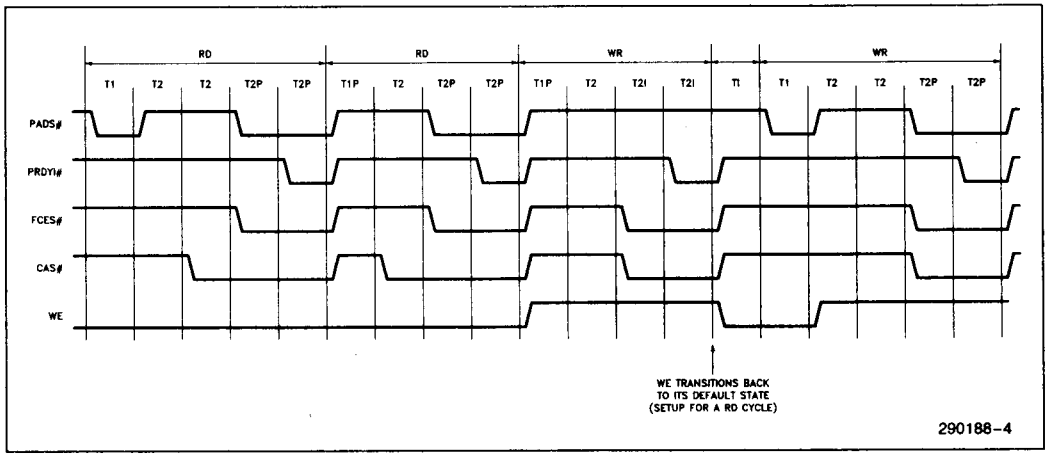


Figure 4. 2/7 Page Hit

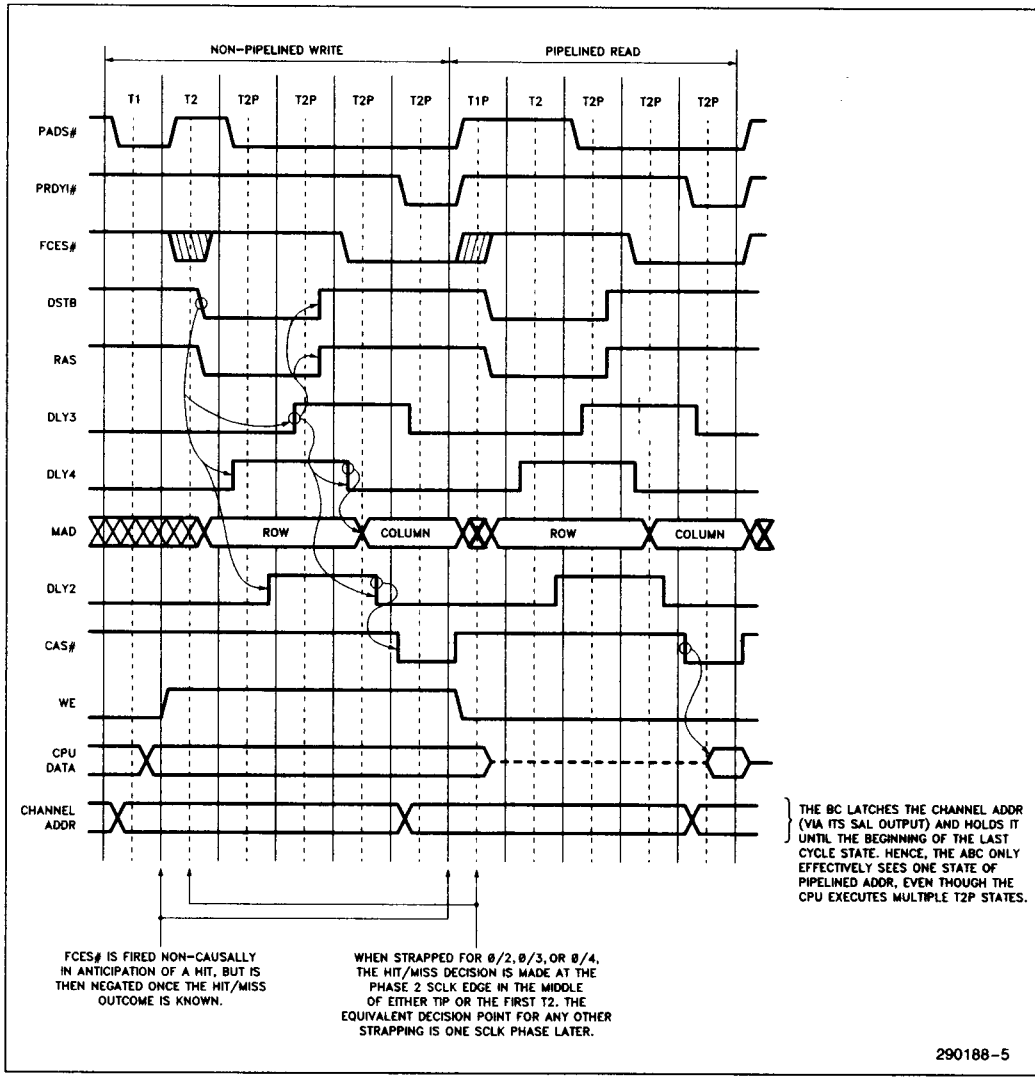


Figure 5. 0/2, 0/3, 0/4 Page Misses (Diagram Depicts 0/3 Operation. In 0/2, FCES# Fired One State Earlier. In 0/4, FCES# Fired One State Later.)

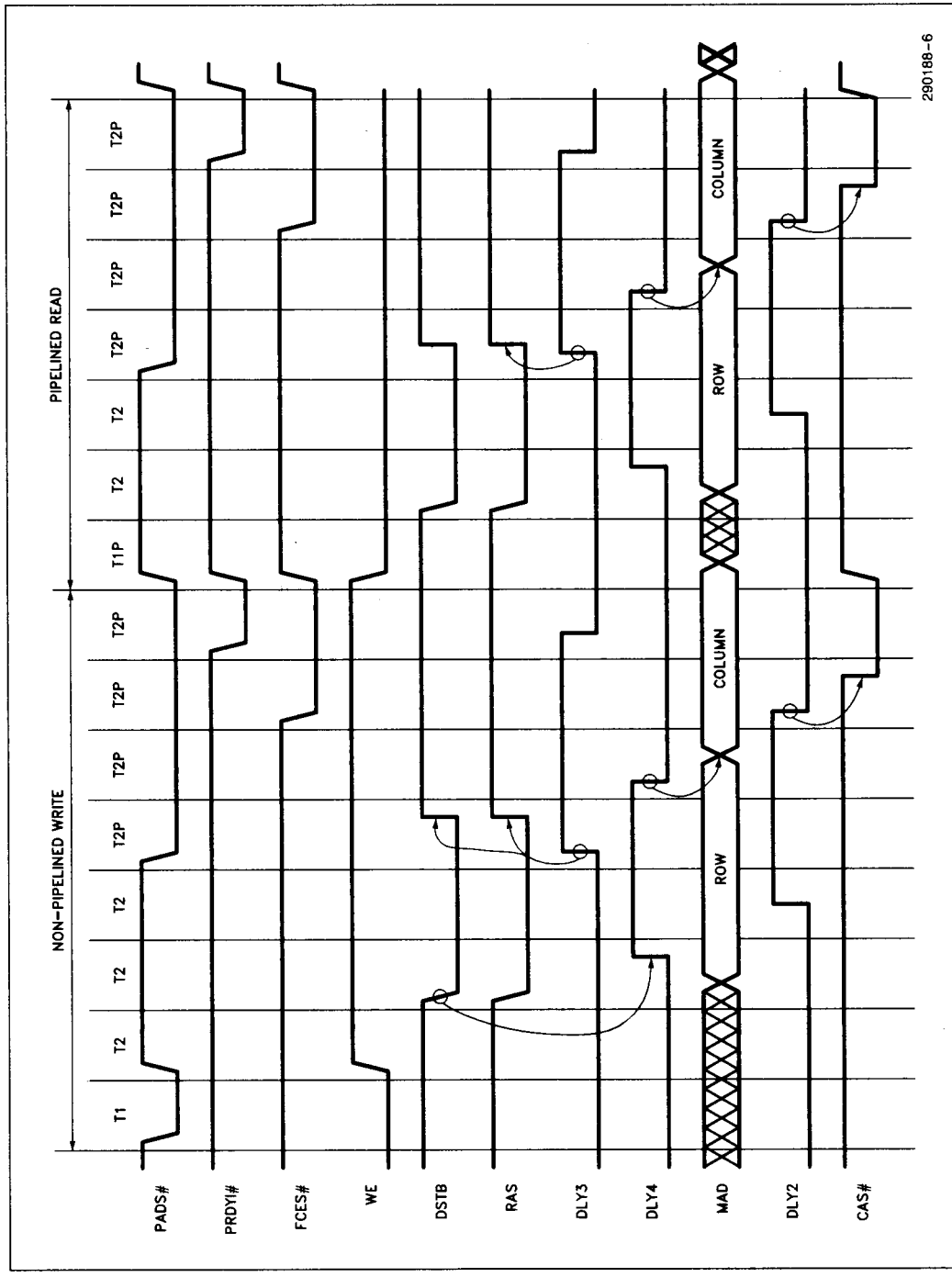
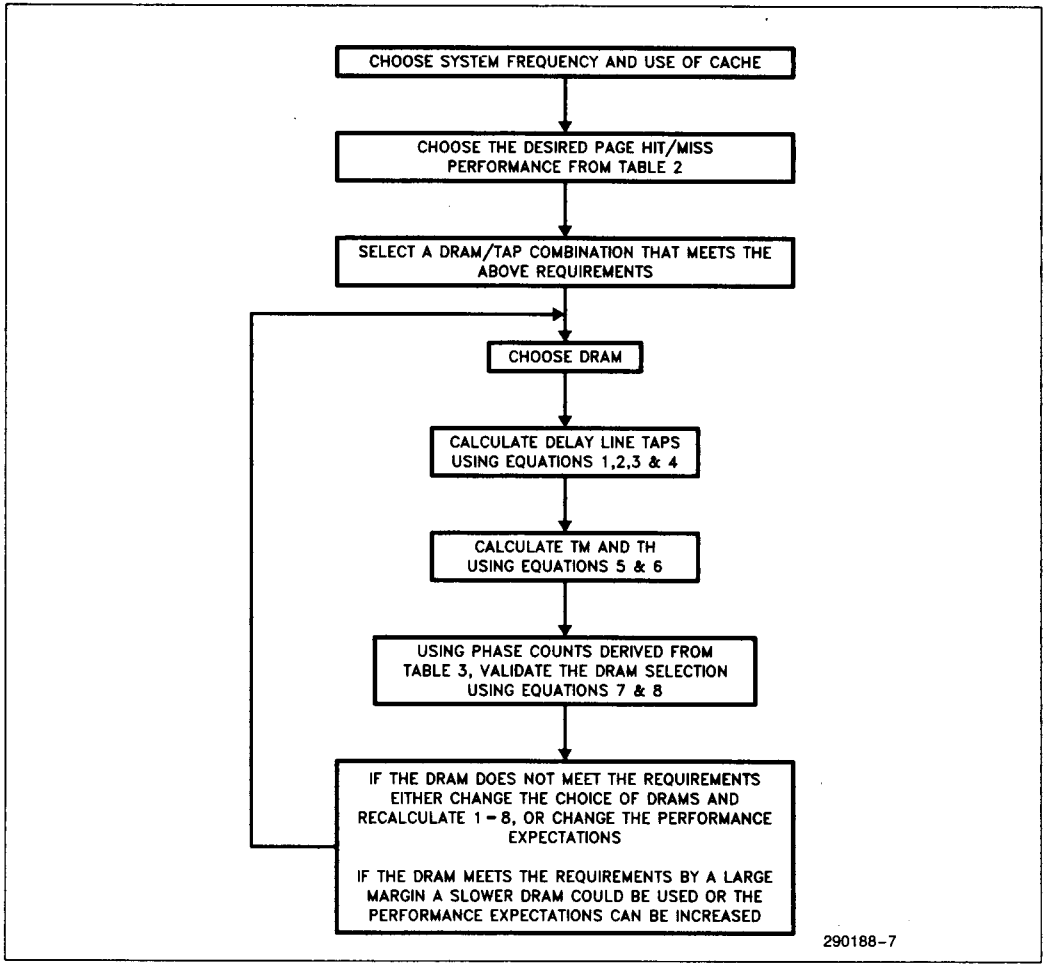


Figure 6. 1/4, 1/5, 1/6, 1/7, 2/7 Page Misses (Diagram Depicts 1/5 Operation. FCES# is Fired One State Earlier in 1/4 Operation, One State Later in 1/6 Operation, and Two States Later in Either 1/7 or 2/7 Operation.)

DRAM AND DELAY LINE TAP SELECTION

This chapter illustrates the methods that should be used to determine the delay line taps for a given DRAM, and the number of wait states a given DRAM will require.

The Flow Chart below should be used to select a DRAM/Delay line tap combination that meets the performance requirements of a system.



DELAY LINE TAP SELECTION

Function of the 4 Delay Line Taps

DLY1— Guarantees max. DRAM data from CHRDY on Micro Channel

DLY2— Guarantees the minimum RAS to CAS delay and DRAM address setup to CAS

DLY3— Guarantees min. RAS# precharge time

DLY4— Guarantees min. address hold to RAS#

Simplified DRAM Tap Selection Equations

DLY1 is the maximum of the following:

80386 System—

$$\text{Trac (Max)} - 10 \quad (1a)$$

$$\text{Trcd (Min)} + \text{Tcac (Max)} \quad (1b)$$

$$\text{Tasc (Min)} + \text{Trah (Min)} + \text{Tcac (Max)} + 20 \quad (1c)$$

80386SX System—

$$\text{Trac (Max)} - 25 \quad (1a)$$

$$\text{Trcd (Min)} + \text{Tcac (Max)} - 15 \quad (1b)$$

$$\text{Tasc (Min)} + \text{Trah (Min)} + \text{Tcac (Max)} + 5 \quad (1c)$$

DLY2 is the maximum of the following:

$$\text{Trcd (Min)} + 10 \quad (2a)$$

$$\text{Tasc (Min)} + \text{Trah (Min)} + 30 \quad (2b)$$

$$\text{DLY3} = \text{Trp (Min)} \quad (3)$$

$$\text{DLY4} = \text{Trah (Min)} + 10 \quad (4)$$

DRAM Access Time Calculations

Two access time parameters have been derived, one for hits (Th) and one for misses (Tm). These are the time from the decision to start a DRAM access to the time that data is available to the motherboard CPU.

$$\text{Th} = \text{Tcac (Max)} + \text{K1} \quad (5)$$

Tm is the maximum of the following:

$$\text{DLY3} + \text{Trac (Max)} + \text{K2} \quad \text{(RAS Path Limited)} \quad (6a)$$

$$\text{DLY3} + \text{DLY2} + \text{Tcac (Max)} + \text{K3} \quad \text{(CAS Path Limited)} \quad (6b)$$

The constants K1, K2 and K3 in equations 5 and 6 are simply a sum of all the propagation delay elements in the appropriate data access path including capacitive load derating:

$$\text{K1} = \underset{\text{(T41A)}}{\text{ABC CAS\# DLY}} + \underset{\text{(INCLUDE DERATE)}}{\text{CAS\# BUFFER DLY}} + \underset{\text{('F657)}}{\text{DATA BUFFER DLY}} = 44.5$$

$$\text{K2} = \underset{\text{(T32E)}}{\text{ABC DSTB DLY}} + \underset{\text{('AS02)}}{\text{NOR GATE DLY}} + \underset{\text{(T32G)}}{\text{ABC RAS DLY}} + \underset{\text{(INCLUDE DERATE)}}{\text{RAS BUFFER DLY}} + \underset{\text{('F657)}}{\text{DATA BUFFER DLY}} = 79$$

$$\text{K3} = \underset{\text{(T32E)}}{\text{ABC DSTB DLY}} + \underset{\text{('AS02)}}{\text{2X NOR GATE DLY}} + \underset{\text{(T34)}}{\text{ABC CAS\# DLY}} + \underset{\text{(INCLUDE DERATE)}}{\text{CAS\# BUFFER DLY}} + \underset{\text{('F657)}}{\text{DATA BUFFER DLY}} = 81.5$$

(See Figure 6 for a diagram of the timing model used.)

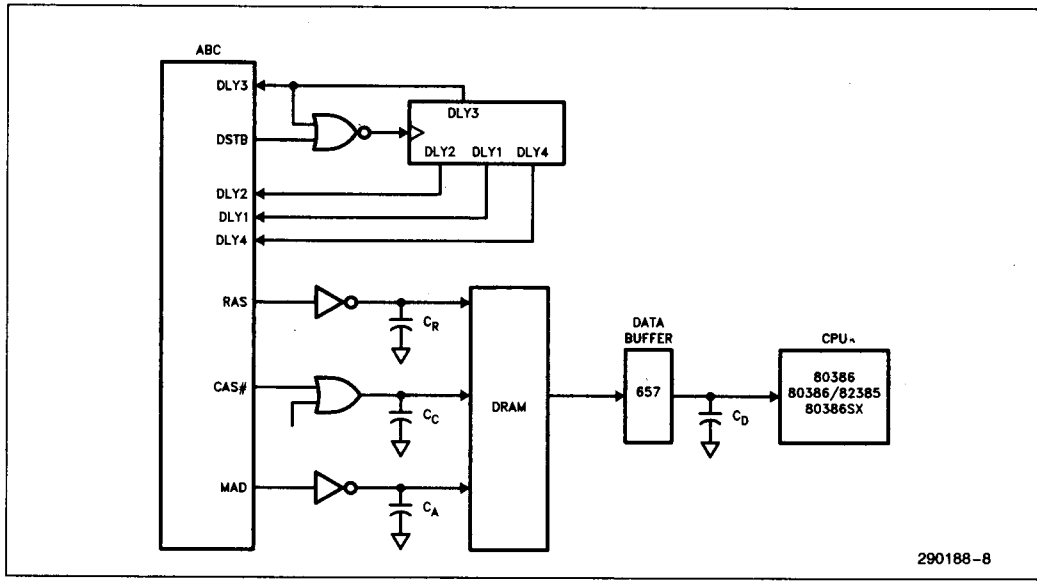


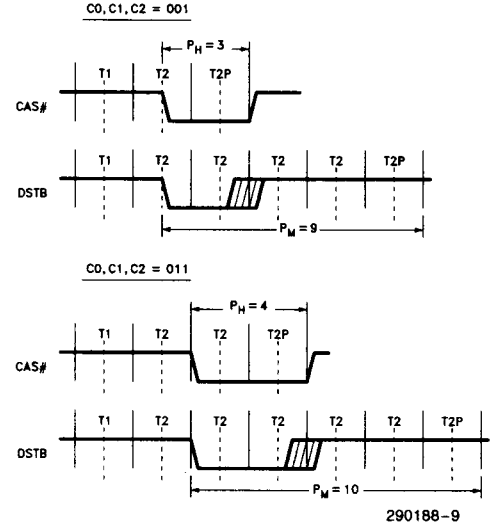
Figure 7. DRAM Timing Analysis Model

Tables 2 and 3 define the number of DRAM wait states that the motherboard CPU will see for all combinations of the configuration bits C0, C1 and C2.

Table 3. Configuration and DRAM Calculation Clock Phase Counts

Config Inputs			SCLK Phases	
C0	C1	C2	PH	PM
0	0	0	3	7
0	0	1	3	9
0	1	0	3	11
0	1	1	4	10
1	0	0	4	12
1	0	1	4	14
1	1	0	4	16
1	1	1	6	16

PH, PM Definition Examples



NOTES:
1. The phase counts are from the clock edge that either fires CAS# (Hit) or fires DSTB (Miss) to the end of cycle, as shown above.
2. Cache systems typically require additional read data setup. The BC WS# (Wait State) strap inserts an additional wait state into system board memory reads, and can be used to accommodate this increased setup if required. If WS# is tied low, then the phase counts above all increase by two.

Validation of DRAM Selection

After Th and Tm have been calculated the performance expectations of the DRAM can be checked.

First the number of clock phases both hit and miss DRAM cycles are allowed are calculated. For Configurations 0, 1 & 2 this is 2 × the number of non-pipelined waitstates + 1. For other Configurations this is just 2 × the number of non-pipelined waitstates. The phases for hits are called Ph, Pm for misses.

The following equations must then be satisfied:

$$Ph/(2*Clk\ Freq.) - Th - CPU\ Data\ setup \geq 0 \quad (7)$$

$$Pm/(2*Clk\ Freq.) - Tm - CPU\ Data\ setup \geq 0 \quad (8)$$

Two examples of Delay Line Tap Selection and DRAM Performance Verification are given below, one for an 80386 system and one for an 80386SX system.

Sample Calculation—80386 20 MHz 100 ns DRAMs 1/5 Performance

Target Dram

Key Specs (ns)

Trac	100
Trp	80
Trah	15
Trcd	25
Tasc	0
Tcac	35

Delay Line Calculations

DLY3 = Trp = 80 ns

DLY4 = Trah + 10 = 15 + 10 = 25 ns

DLY2 = Trcd + 10 = 25 + 10 = 35 ns
or
= Tasc + Trah + 30 = 0 + 15 + 30 = 45 ns

DLY1 = Trac − 10 = 100 − 10 = 90 ns
or
= Trcd + Tcac = 25 + 35 = 60 ns
or
= Tasc + Trah + Tcac + 20
= 0 + 15 + 35 + 20 = 70 ns

Delay Line Summary

DLY1	90
DLY2	45
DLY3	80
DLY4	25

Page Hit Access Time & Performance

Th = Tcac + 44.5
= 35 + 44.5 = 79.5 ns

80386 Data Setup Time = 10 ns

1 Waitstate Margin (Pipelined)

Ph/(2*CLK Freq.) − Th − 386 Data Setup = 100 − 79.5 − 10
= 10.5 ns

Page Miss Access Time & Performance

Tm is the maximum of EQN 6a and 6b.

Tm = DLY3 + Trac + 79
= 80 + 100 + 79 = 259

or

Tm = DLY3 + DLY2 + Tcac + 81.5
= 80 + 45 + 35 + 81.5 = 241.5

5 Waitstate (Pipelined) Margin

Pm/(2* CLK Freq.) − Tm − 80386 Data Setup = 300 − 259 − 10
= 31 ns

Sample Calculation—80386SX 16 MHz 100 ns DRAMs

0/3 Performance

Only DLY1 changes

DLY1 = Trac − 25 = 100 − 25 = 75 ns

Delay Line Summary

DLY1	75
DLY2	45
DLY3	80
DLY4	25

Page Hit Access Time & Performance

Th = Tcac + 44.5
= 35 + 44.5 = 79.5

80386SX Data Setup = 5 ns

0 Waitstate Margin (Pipelined)

Ph/(2* CLK Freq.) − Th − 80386SX Data Setup > = 0
93.75 − 79.5 − 5 = 9.25 ns

Page Miss Access Time & Performance

Tm = 259

(Same as for 20 MHz 386 Case)

3 Waitstate Margin (Pipelined)

Pm/(2* CLK Freq.) − Tm − 80386SX Data Setup > = 0
281.25 − 259 − 5 = 17.5 ns

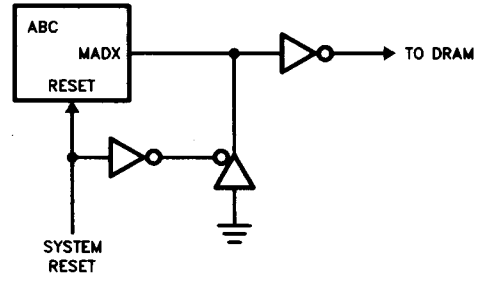
MAD BUS RESET CONFIGURATION

The ABC samples the MAD bus at the falling edge of RESET to determine system configuration as shown:

Table 4

MAD Bus Bits										Options
10	9	8	7	6	5	4	3	2	1	0	
0	0										256K DRAMs
0	1										1M DRAMs
1	1										4M DRAMs
										0	32 Bit Memory
										1	16 Bit Memory
									0		SS1 = 0
									1		SS1 = 1
							0	0			Invalid
							0	1			Single Bank
							1	0			Two Banks
							1	1			Four Banks
						0					Reserved
						1					Normal Mode
					0						C2 = 0
					1						C2 = 1
				0							C1 = 0
				1							C1 = 1
			0								C0 = 0
			1								C0 = 1
		0									SS2 = 0
		1									SS2 = 1

NOTES:
1. When either MAD09 or MAD10 is sensed as a zero, it's output driver is tri-stated, thus allowing these two pins to be tied directly to ground. For example, if 1M DRAMs are used, MAD10 should be tied to ground, since 1M DRAMs only require use of bits 0–9. MD09 should be lightly pulled up (~ 10K).
2. For MAD bits 0–8, any bit that is to be sensed as a one should be lightly pulled up. Any bit that is to be sensed as a zero must be driven low by a tri-state driver that is active while the ABC RESET input is active, and then tri-stated from the falling edge of RESET, as depicted in the figure:



290188-10

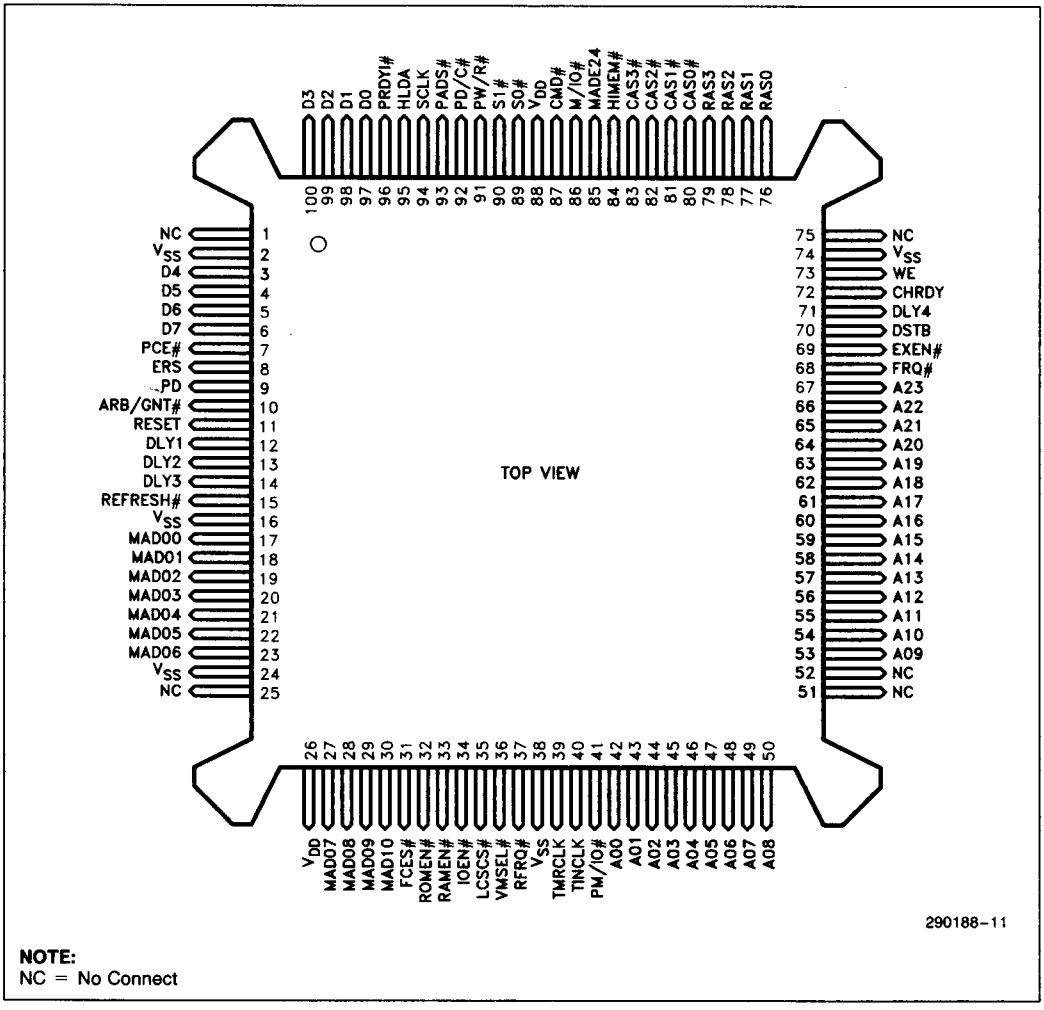
3. MAD4 sensed as a 0 is a reserved state. This bit should be lightly pulled up.
4. MAD0 is typically configured low for an 80386 system, and high for an 80386SX system.
5. MAD1 and MAD8 are respectively the system select bits SS1 and SS2. These bits determine the definition of ABC ports E0, E1 and 103, as described in the section on ABC ports and registers.
6. MAD5, MAD6 and MAD7 are respectively the DRAM performance select bits C2, C1 and C0. The effect of these bits is described in the DRAM control section.

82309 Address Bus Controller Pin Definitions

Signal Name	Pin Number	I/O	Description
A<00:23>	42–50, 53–67	I	Micro Channel Address 0 to 23
HIMEM#	84	I	Micro Channel Address 24 to 31 = FF (Active Low). Used in decoding the top-of-memory mapping of the BIOS EPROMs.
MADE24	85	I	Micro Channel Address 24 to 31 = 00 (Active High)
ROMEN#	32	O	EPROM Decode. In systems that support shadow RAM, if ROM is enabled (bit 1 in port E1), accesses to ROM space actually generate both ROMEN# and RAMEN#. In this mode, reads are from ROM, and writes are to RAM.
RAMEN#	33	O	DRAM Decode
IOEN#	34	O	Motherboard I/O devices decode (Active Low). Decode also includes memory decode of video RAM.
LCSCS#	35	O	Chip Select for the LCS (82306) Chip (Active Low). Decodes address range 0–3FFH when CPU master, or 100–3FFFH when CPU is not master.
VMSEL#	36	O	VGA Memory Space Selected (Active Low) (000A0000–000BFFFF)
S0#	89	I	Micro Channel S0# Signal
S1#	90	I	Micro Channel S1# Signal
PM/IO#	41	I	Microprocessor M/IO# Signal
PW/R#	91	I	Microprocessor W/R# Signal
PD/C#	92	I	Microprocessor D/C# Signal
PADS#	93	I	Microprocessor ADS# Signal
SCLK	94	I	Microprocessor CLK2
HLDA	95	I	HLDA Signal from the Processor
PRDYI#	96	I	READY# Signal from the Processor
M/IO#	86	I	Micro Channel M/IO# Signal
CMD#	87	I	Micro Channel CMD Signal

82309 Address Bus Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
WE	73	O	DRAM Write Enable Signal (Active High)
RAS<0:3>	76–79	O	DRAM RAS Strobes (Active High)
CAS# <0:3>	80–83	O	DRAM CAS Strobe Enables (Active Low)
MAD<00:10>	17–23, 27–30	B	DRAM Muxed Address bus. These signals are sampled at reset to determine ABC configuration.
DSTB	70	O	Output to Delay Line. A pulse put into the delay line controls page miss timing.
DLY<1:4>	12–14, 71	I	Inputs from the Delay Line. DLY1 controls CHRDY timing in non-CPU cycles. DLY2 controls RAS active to CAS active timing. DLY3 controls RAS precharge, and DLY4 controls row-to-column address multiplex.
CHRDY	72	O	DRAM Ready Signal (Active High)
REFRESH#	15	I	Refresh Operation in Progress (Active Low)
FCES#	31	O	Request to BC to terminate CPU accesses to system board memory.
TINCLK	40	I	14.3 MHz Clock for Refresh Timer
RFRQ#	37	O	Refresh Request (Active Low)
TMRCLK	39	O	14.3 MHz Clock divided by 12 to get 1.19 MHz.
FRQ#	68	O	Asynchronous Cache Flush Request. Activated in I/O writes to ports E0, E1, or 100–107 (POS Address Space).
EXEN#	69	O	Read/Write Strobe for Ports 00E0–00E7 (Active Low)
ERS	8	I	Sampling Strobe for Ports 00E2–00E7
PD	9	I	Select Signal for POS Register 10X
ARB/GNT#	10	I	Micro Channel ARB/GNT# Signal
D<0:7>	97–100, 3–6	I/O	Data Bus
PCE#	7	O	Enable Parity Checking (MER<0>)
RESET	11	I	Synchronous reset input. RESET falling edge used to synchronize ABC internal clock to CPU phase.
NC	1, 25, 51, 52, 75		No Connect
V_{DD}	26, 88		Power
V_{SS}	2, 16, 24, 38, 74		Ground



NOTE:
NC = No Connect

Figure 8. 82309 Address Bus Controller (ABC) Pin Diagram

82309 PARAMETRICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground ..... −0.3V to (V_{CC} + 0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1

D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	SCLK
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	SCLK
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

82309 ADDRESS BUS CONTROLLER A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		CL(PF)	Notes
		Min	Max	Min	Max	Min	Max		
T1	SCLK PERIOD	31.25		25		20			
T2A	SCLK HIGH/LOW TIME (50%)	12		10		8			
T2B	SCLK HIGH/LOW TIME (90%)	8		6.5		6			
T3	RESET SETUP	10		10		10			
T4	RESET HOLD	4		4		4			
T5A	STATUS SETUP TO SCLK	11		11		8			1
T5B	CMD# SETUP TO SCLK	11		11		8			1
T6	PADS#,PW/R#,PD/C#,PM/IO# SETUP	25		22		13			
T7	PADS#,PW/R#,PD/C#,PM/IO# HOLD	4		4		4			
T8	ADDRESS,M/IO#,MADE24,REFRESH# SETUP	10		10		10			
T9	ADDRESS,M/IO#,MADE24,REFRESH# HOLD	12		12		12			
T10	ADDRESS, M/IO# SETUP	40		50		36			3
T11	ADDRESS, M/10# HOLD	8		8		8			3
T12	MADE24 SETUP	32		40		28			3
T13	MADE24 HOLD	8		8		8			3
T14	M/IO#,ARB/GNT# SETUP TO ERS	20		20		20			
T15	M/IO#,ARB/GNT# HOLD FROM ERS	10		10		10			
T16	PRDYI# SETUP	18		18		15			
T17	PRDYI# HOLD	3		3		3			
T18A	ROMEN#,RAMEN#,IOEN#,VMSEL# DLY FRM MADE24 HIMEM#	2	30	2	30	2	30	75	
T18B	ROMEN#,RAMEN#,IOEN#,VMSEL# DLY FRM ADDR	2	38	2	38	2	38	75	14
T18C	ROMEN#,RAMEN#,IOEN#,VMSEL# DLY FRM A20	2	35	2	35	2	35	75	14
T19	LCSCS# DELAY	2	45	2	45	2	45	75	
T20A	FCES# DELAY FROM SCLK	3	45	3	35	3	26	25	5
T20B	FCES# DLY FRM ADDR, M/IO#, MADE24		50					25	2, 5
T21	PD SETUP TO CMD# ↑	100		100		100			
T22	WRITE DATA SETUP	30		30		30			
T23	WRITE DATA HOLD	5		5		5			
T24	READ DATA VALID DELAY		200		200		200	75	
T24A	CMD# ↓ TO READ DATA LOW-Z	25		25		25		75	
T25	READ DATA FLOAT DELAY	2	35	2	35	2	35	75	
T26	EXEN# DELAY (INACTIVE)	2	50	2	50	2	50	50	
T26A	EXEN# DELAY (ACTIVE)	25	150	25	150	25	150	50	
T27A	CHRDY DELAY (FROM ADDR)	2	50	2	50	2	50	50	4, 5, 7
T27B	CHRDY DLY FROM STATUS OR CMD#	0	33	0	33	0	33	50	4, 5, 7
T29	TMRCLK HIGH/LOW TIME	300		300		300		50	
T30	RFRQ# PULSE WIDTH	300		300		300		50	
T31	TINCLK HIGH/LOW TIME	21		21		21			
T32B	CMD# ↑ -RAS ↓ (REFRESH CYCLE ONLY)	0	55	0	55	0	55	75	10
T32C	CMD# ↑ -CAS# ↑	0	38	0	38	0	38	75	
T32E	SCLK-DSTB ↓	4	27	4	27	4	27	50	8
T32F	DLY3 ↑ -DSTB ↑	0	50	0	50	0	50	50	
T32G	DLY3 ↑ -RAS ↑	4	26	4	26	4	26	75	
T32I	SCLK-RAS ↓	8	40	8	40	8	40	75	8
T33	DLY1 ↓ TO CHRDY ↑	5	30	5	30	5	30	50	
T34	DLY2 ↓ TO CAS# ↓	3	27	3	27	3	27	75	

82309 ADDRESS BUS CONTROLLER A.C. SPECS (Continued)

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		CL(PF)	Notes
		Min	Max	Min	Max	Min	Max		
T35	CMD# ↓ TO CAS# ↓ (WRITE CYCLES ONLY)	25	115	25	115	25	115	75	6
T39A	WE DLY FROM STATUS	2	30	2	30	2	30	75	13
T39B	WE DLY FROM CMD# ↑	2	30	2	30	2	30	75	13
T41A	CAS# ↓ DELAY FROM SCLK (READS)	2	30	2	30	2	30	75	
T41B	CAS# ↑ DELAY FROM SCLK	5	34	5	34	5	34	75	9
T41C	CAS# ↓ DELAY FROM SCLK (WRITES)	2	38	2	38	2	38	75	
T43A	ADDR TO MAD DELAY (COLUMN ADDR)		45		45		40	75	12
T43B	SCLK TO MAD DELAY (COLUMN ADDR)		36		36		31	75	12
T43C	CMD# TO MAD DELAY (COLUMN ADDR)		38		38		38	75	12
T43D	SCLK TO MAD DELAY (ROW ADDR)		50		50		50	75	12
T44	WE DELAY FROM SCLK	2	42	2	42	2	42	75	
T45	DLY4 ↓ TO MAD	6	32	6	32	6	32	75	
T46	MAX PAGE MODE RAS ACTIVE	15 μs		15 μs		15 μs			10, 11

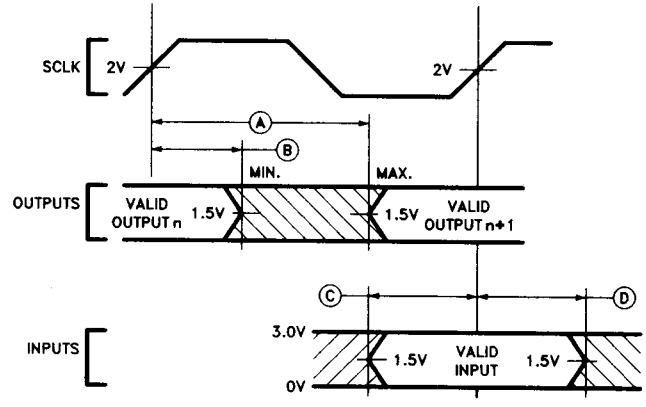
NOTES:
1. Status and CMD# are asychronous inputs. T5 simply guarantees that they are recognized at a particular clock edge.
2. FCES# is speced from address only in 0WS pipelined/1WS non-pipelined memory cycles, which are only supported at 16 MHz.
3. Address, M/IO# and MADE24 setup times are speced relative to the Phase 2 SCLK edge only in 0WS pipelined/1WS non-pipelined memory cycles, which are only supported at 16 MHz. (This Phase 2 edge is in the middle of the first T2 state, or the middle of the T1P state.)
4. The 82309 de-activates CHRDY for motherboard I/O and VGA Memory cycles (as decoded by IOEN#), and then re-activates it when CMD# is activated. The 82309 also de-activates CHRDY for non-CPU (DMA or channel master) accesses to motherboard DRAM that are decoded as page misses. CHRDY is then re-activated according to the appropriate external DRAM control delay line tap (DLY1), or else when CMD# is activated, whichever comes later.
5. FCES# is used to terminate CPU accesses to motherboard DRAM, as these cycles are not broadcast on the Micro Channel. CHRDY is used to terminate DMA and channel master accesses to motherboard DRAM, which are broadcast.
6. The large value for T35 (Min) guarantees that data being written into motherboard DRAM by a channel master or DMA controller has adequate time to propogate through the data buffers between the channel or DMA and memory. T35 (Min) is guaranteed on any non-CPU write, both page hit and page miss. (The Micro Channel specs 0NS of data setup to CMD# active.) T35 (Max) applies only when CMD# ↓-to-CAS# ↓ is indeed the limiting spec; specifically, when neither T34 (Max) nor T41A (Max) limits CAS# activation.
7. The 82309 guarantees that any time it de-asserts CHRDY, it will not re-assert it until after CMD# is activated.
8. These specs are referenced with respect to the causal SCLK edge, which differs in different frequency systems. At 16 MHz, the appropriate edge is one clock phase after the edge that recognizes status in non-CPU cycles, or one phase after the edge that samples PADS# active in CPU cycles. At 20 MHz, the appropriate edge is two clock phases after these events. The 82309 distinguishes 16 MHz from 20 MHz via the memory performance configuration inputs C0, C1 and C2. 16 MHz is assumed anytime these inputs indicate a zero wait state pipelined read page hit. (C0, C1, C2 = 000,001,010).
9. This spec insures a minimum CAS# high time of 25 ns at 16 MHz. (16 MHz is the worst case since the CAS# inactive and CAS# active SCLK edges are only one phase apart. At 20 MHz, these edges are always at least two phases apart.)
10. Refresh cycles are RAS only, and are forced to be page misses. Thus, the refresh interval (typically 15 μs) defines the required page mode RAS active time. RAS is de-activated at the end of a refresh cycle since typical page mode DRAMs spec a maximum RAS active time less than 15 μs for refresh cycles. (Note that the first access to any bank following a refresh cycle is also a forced page miss.)
11. Functional spec only . . . Not tested. Max page mode RAS active is governed by refresh interval.
12. T43A, T43B, and T43C all refer to column address, as the 82309 assumes a page hit as the default case until proven otherwise. In case of a page miss, the row address is muxed onto the MAD lines from the same clock edge that de-activates RAS and fires a pulse (DSTB) into the delay line. The column address is then muxed onto the MAD lines by delay tap DLY4.
13. In Non-CPU cycles, WE (active high from the 82309) is simply an inverted version of channel S0#, which indicates a write cycle when low. This signal is internally latched (transparent latch) by the leading edge of CMD#, and then released by the trailing edge of CMD#, hence the need for T39B.
14. A20 typically has more logic in its path than the other address bits, hence the tighter spec. T18B applies to all bits except A20.

82309SX Micro Channel Address Bus Controller

A.C. SPECIFICATIONS

The following specifications are the only exceptions to the A.C. specifications listed on the previous pages.

Symbol	Parameter	16 MHz and 20 MHz
T10	ADDRESS, M/IO# SETUP	30 ns
T12	MADE24 SETUP	NA
T20B	FCES# DLY FROM ADDR, M/IO#, MADE24	39 ns
T32E	SCLK TO DSTB FALLING EDGE	24 ns
T32G	DLY3 RISING TO RAS# RISING	23 ns
T34	DLY2 FALLING TO CAS# FALLING	25 ns
T41a	CAS# DELAY FROM SCLK (READS)	24 ns
T43A	ADDR TO MAD DELAY (COLUMN ADDR)	38 ns
T43B	SCLK TO MAD DELAY (COLUMN ADDR)	33 ns
T45	DELAY4 FALLING EDGE TO MAD	30 ns



LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.

Figure 9. Drive Levels and Measurement Points for A.C. Specifications

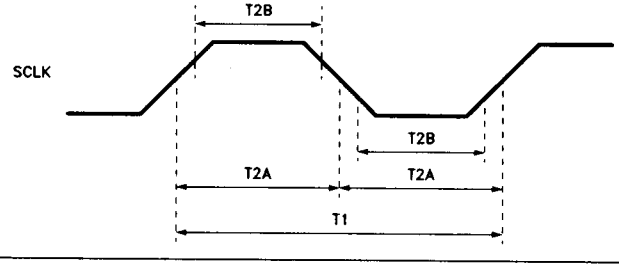


Figure 10. SCLK Waveform

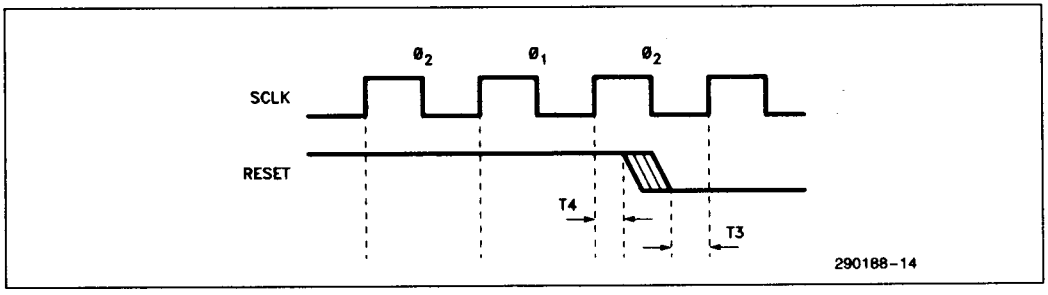


Figure 11. RESET Setup and Hold Diagram

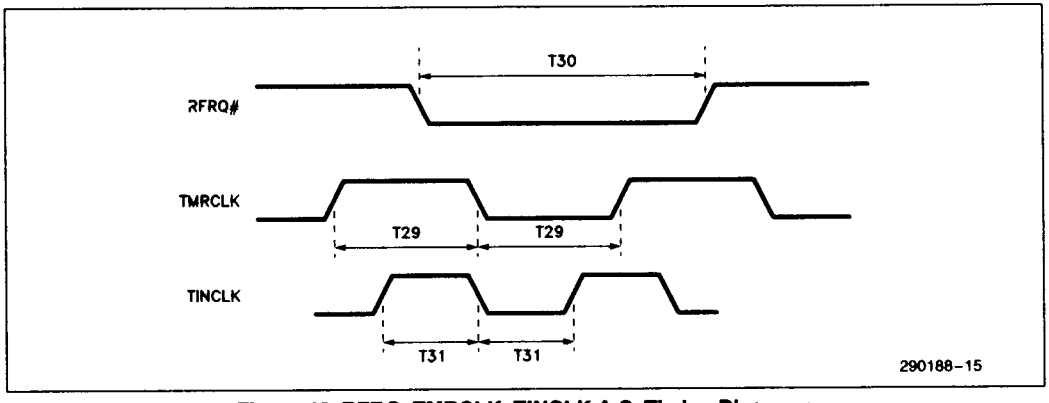


Figure 12. RFRQ, TMRCLK, TINCLK A.C. Timing Diagrams

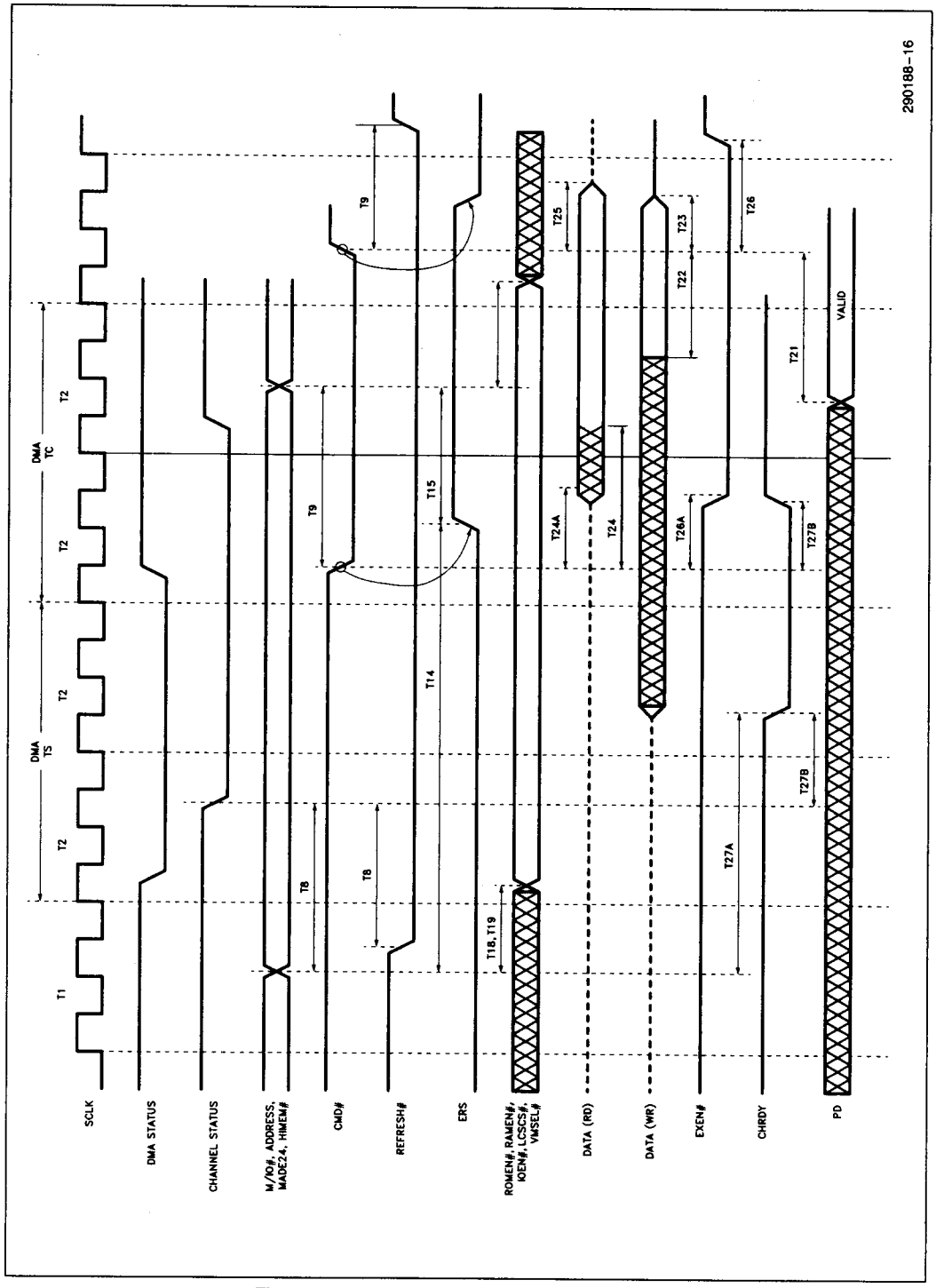
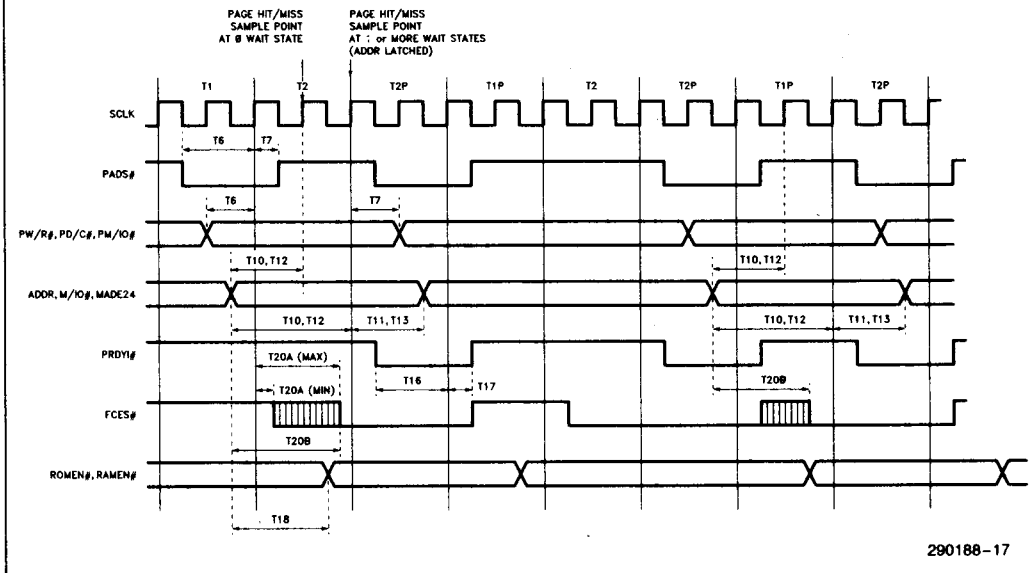


Figure 13. A.C. Diagram for DMA Master Cycles



NOTE:
Once the ABC fires FCES#, it remains active until the ABC detects and end of cycle via its PRDYI# input. This allows the BC or other external devices to extend DRAM cycles if desired.

Figure 14. 82309/80386 Interface Timings

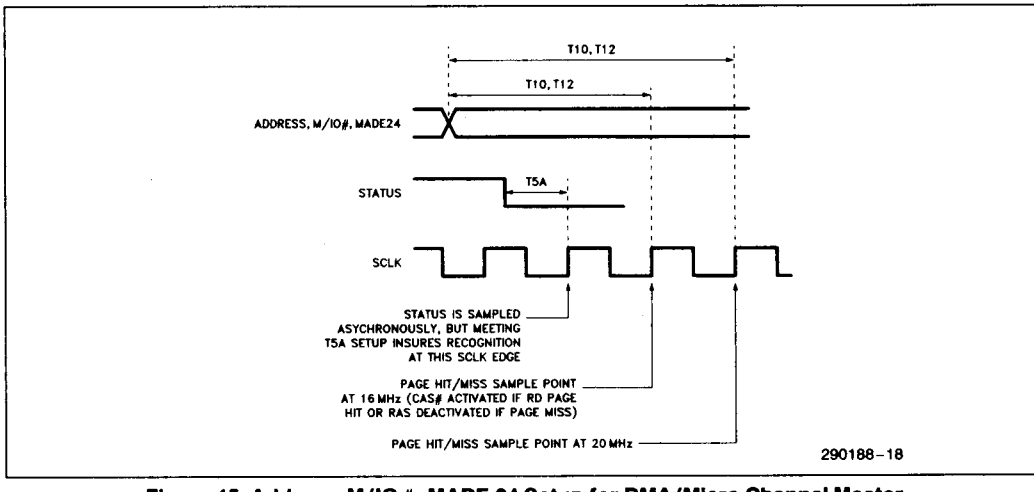


Figure 15. Address, M/IO#, MADE 24 Setup for DMA/Micro Channel Master

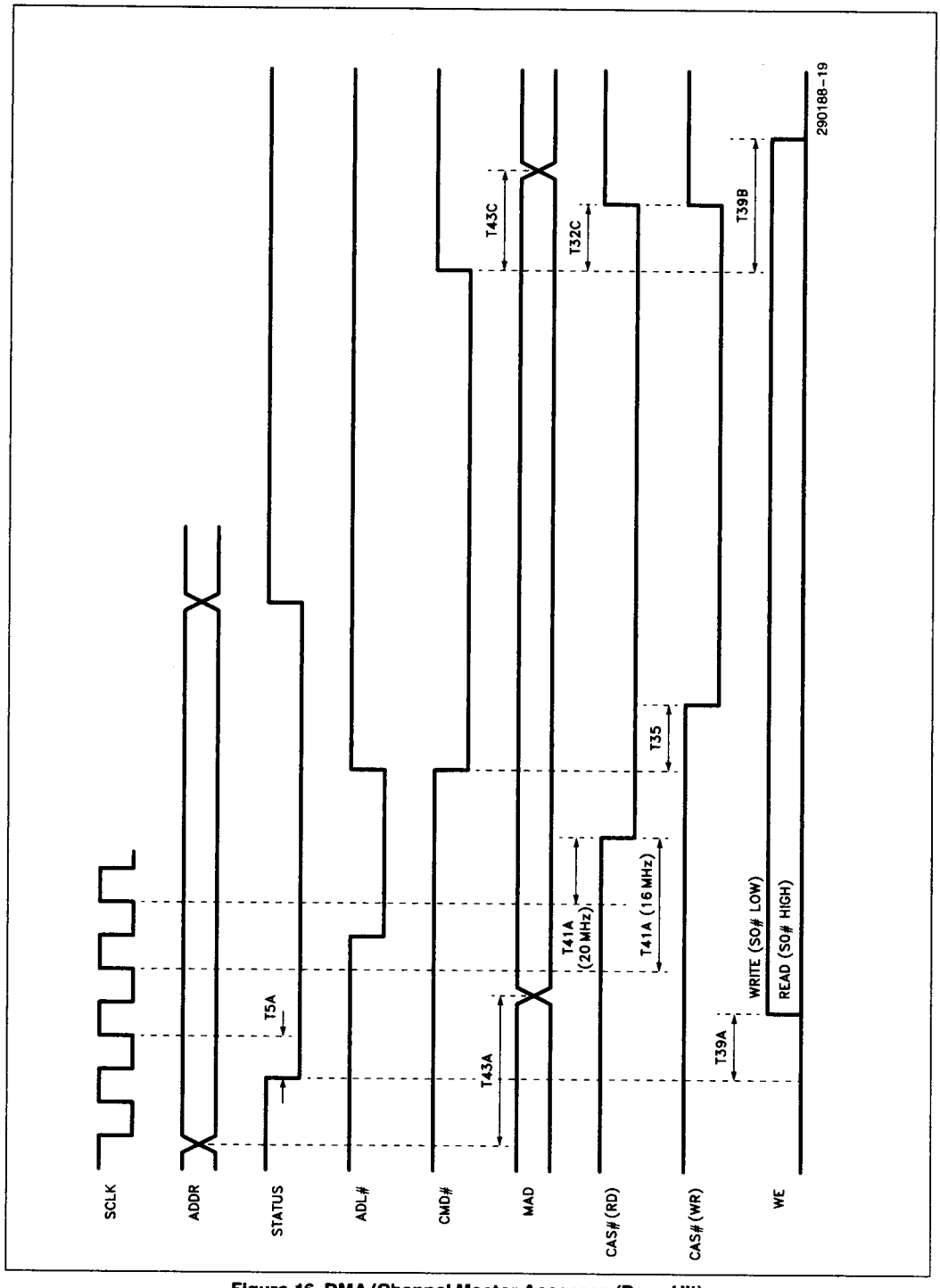


Figure 16. DMA/Channel Master Accesses (Page Hit)

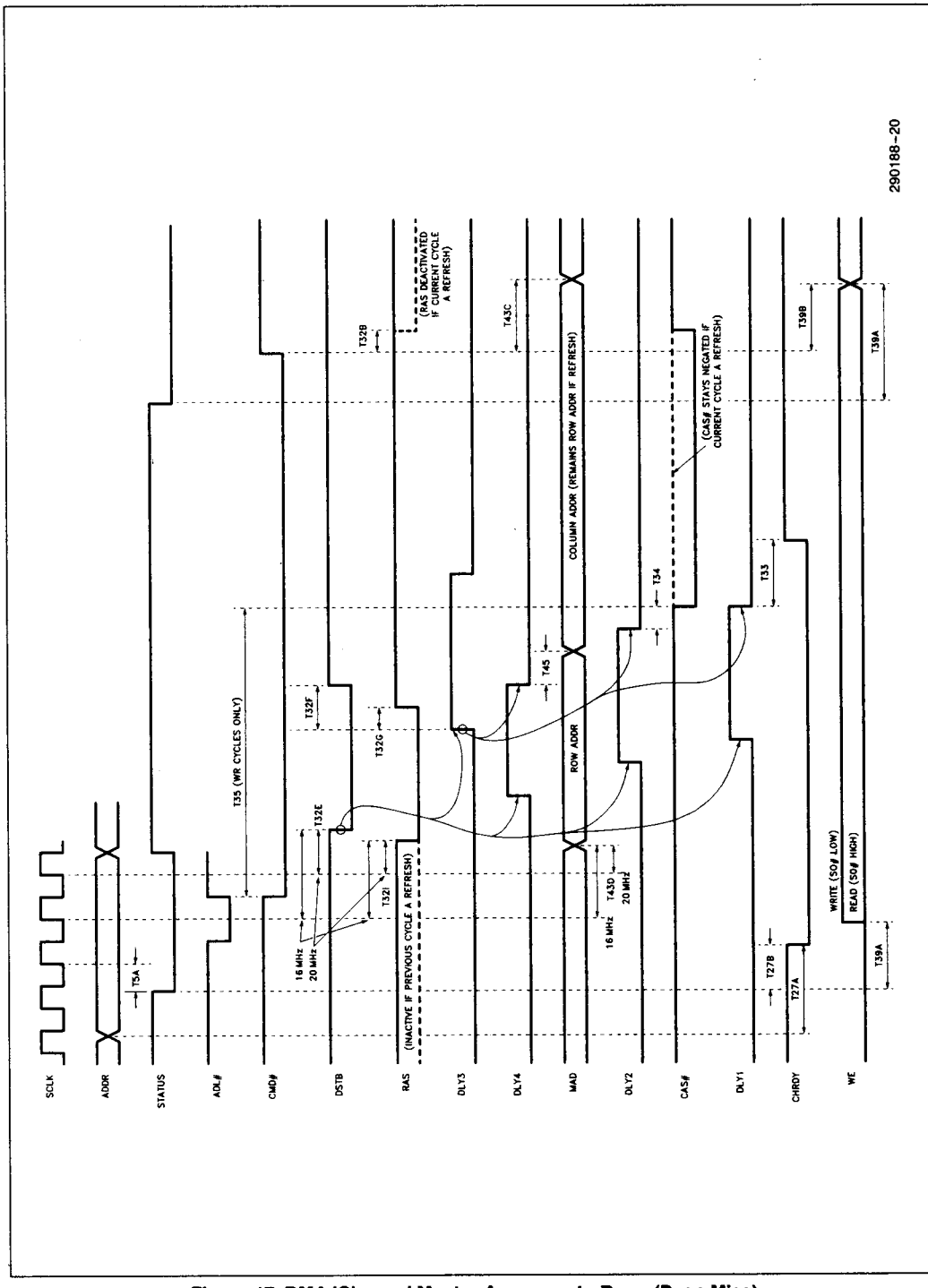
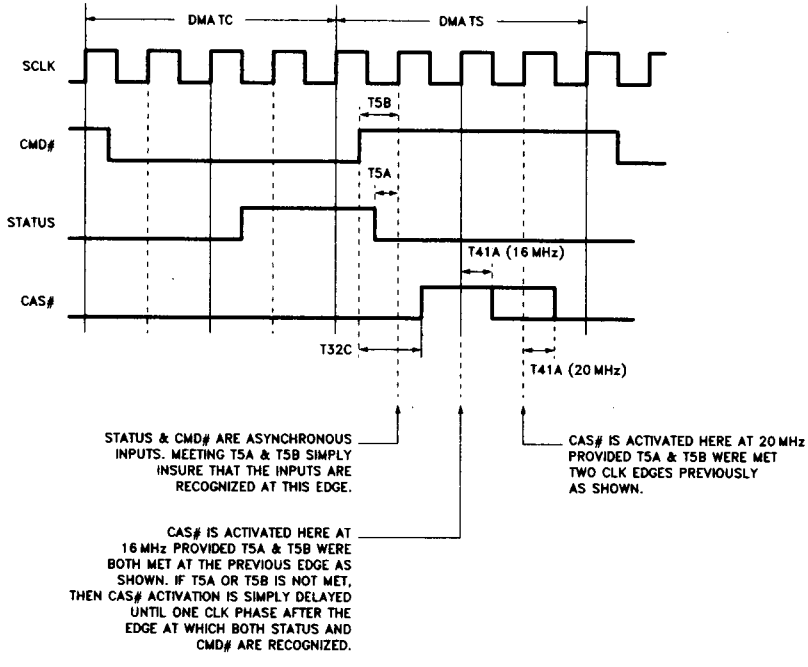


Figure 17. DMA/Channel Master Accesses to Dram (Page Miss)



The requirement that T5B be met before CAS# is allowed (one or two phases later) insures adequate CAS# high time in back-to-back cycles. (One SCLK phase at 16 MHz; Two SCLK phases at 20 MHz.)

Figure 18. DMA Master . . . Back-to-back RD Page Hits

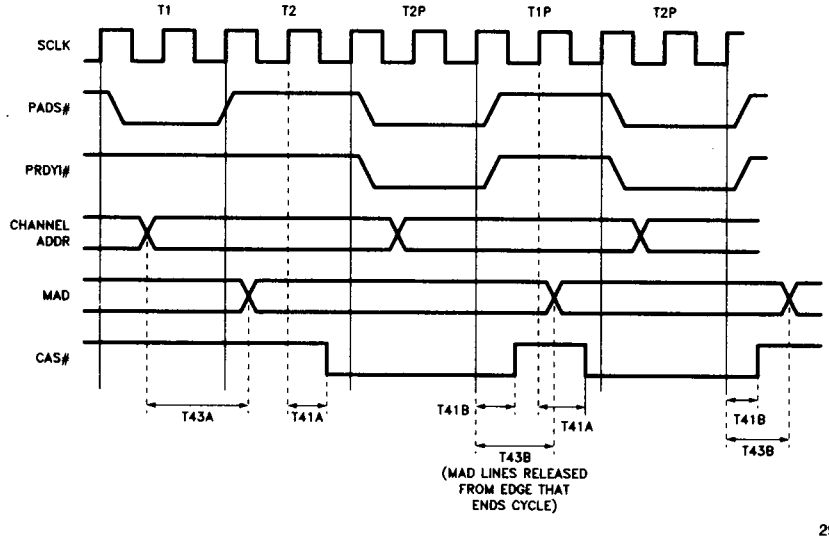


Figure 19. 0 WAIT STATE (Pipelined) Read Page Hits

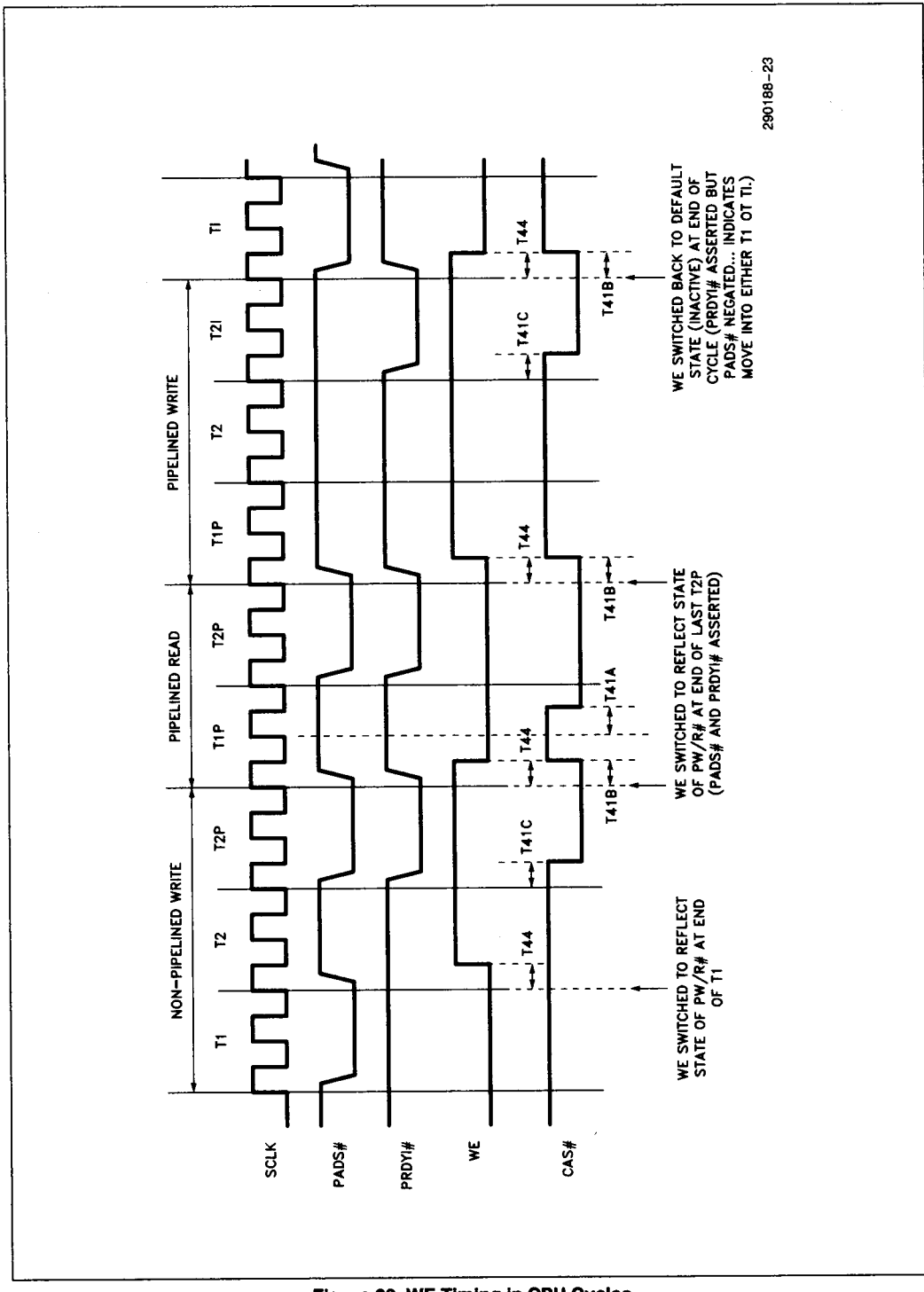


Figure 20. WE Timing in CPU Cycles

Revision Summary

82309 Address Bus Controller

DRAM Controller Section:

Added "except the SX part can run 0WS at 20 MHz because of A.C. Specifications".