Freescale Semiconductor
Technical Data

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RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MD7IC2012NR1
MD7IC2012GNR1

1805–2170 MHz, 1.3 W AVG., 28 V
SINGLE W–CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MD7IC2012N wideband integrated circuit is designed with on–chip matching that makes it usable from 1805 to 2170 MHz. This multi–stage structure is rated for 24 to 32 volt operation and covers all typical cellular base station modulation formats.

Driver Application — 2100 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQ1A} = I_{DQ1B} = 20 mA, I_{DQ2A} = I_{DQ2B} = 70 mA, P_{out} = 1.3 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

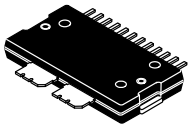
Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2110 MHz	31.0	14.7	–51.3
2140 MHz	31.3	14.8	–51.2
2170 MHz	31.5	14.9	–50.6

- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2140 MHz, 14 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 1 dB Compression Point ≃ 12 Watts CW

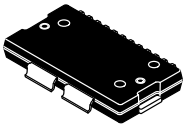
Driver Application — 1800 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQ1A} = I_{DQ1B} = 20 mA, I_{DQ2A} = I_{DQ2B} = 70 mA, P_{out} = 1.3 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1805 MHz	32.8	13.4	–51.0
1840 MHz	32.2	13.6	–51.2
1880 MHz	31.6	13.8	–51.8



TO–270 WB–14
PLASTIC
MD7IC2012NR1



TO–270 WB–14 GULL
PLASTIC
MD7IC2012GNR1

Features

- Characterized with Series Equivalent Large–Signal Impedance Parameters and Common Source S–Parameters
- On–Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- 225°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13–inch Reel.

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.

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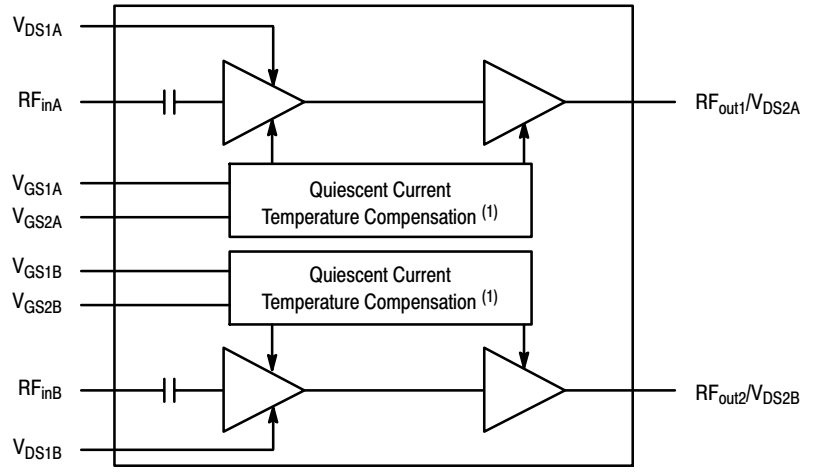
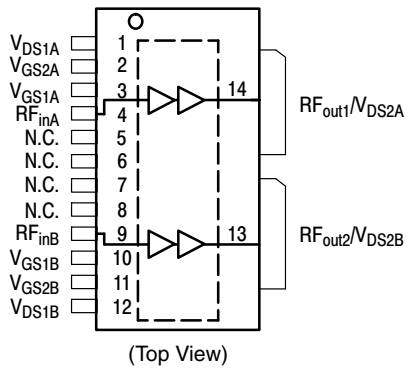


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (2,3)	T_J	225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 77°C, 1.3 W, 2170 MHz			
Stage 1, 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA, 2170 MHz		7.8	
Stage 2, 28 Vdc, I_{DQ2A} = I_{DQ2B} = 70 mA, 2170 MHz		3.1	
Case Temperature 79°C, 12 W CW, 2170 MHz			
Stage 1, 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA, 2170 MHz		7.3	
Stage 2, 28 Vdc, I_{DQ2A} = I_{DQ2B} = 70 mA, 2170 MHz		2.4	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	1A
Machine Model (per EIA/JESD22–A115)	A
Charge Device Model (per JESD22–C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 5 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA, Measured in Functional Test)	$V_{GG(Q)}$	4.2	5.0	5.7	Vdc
Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 24 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = I_{DQ2B} = 70 mA)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = I_{DQ2B} = 70 mA, Measured in Functional Test)	$V_{GG(Q)}$	3.2	4.0	4.7	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 200 mAdc)	$V_{DS(on)}$	0.1	0.24	1.5	Vdc

Functional Tests (2,3) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA, I_{DQ2A} = I_{DQ2B} = 70 mA, P_{out} = 1.3 W Avg., f = 2170 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Power Gain	G_{ps}	30.7	31.5	34.7	dB
Power Added Efficiency	PAE	13.2	14.9	—	%
Output Peak–to–Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	–50.6	–48.3	dBc

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurement made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA, I_{DQ2A} = I_{DQ2B} = 70 mA, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	12	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	13	—	W
IMD Symmetry @ 10 W PEP, P_{out} where IMD Third Order Intermodulation ≧ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	60	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	85	—	MHz
Quiescent Current Accuracy over Temperature **(1,2)** with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	— —	2.5 2.5	— —	%
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 1.3 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.03	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.012	—	dB/°C

1. Each side of device measured separately.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.

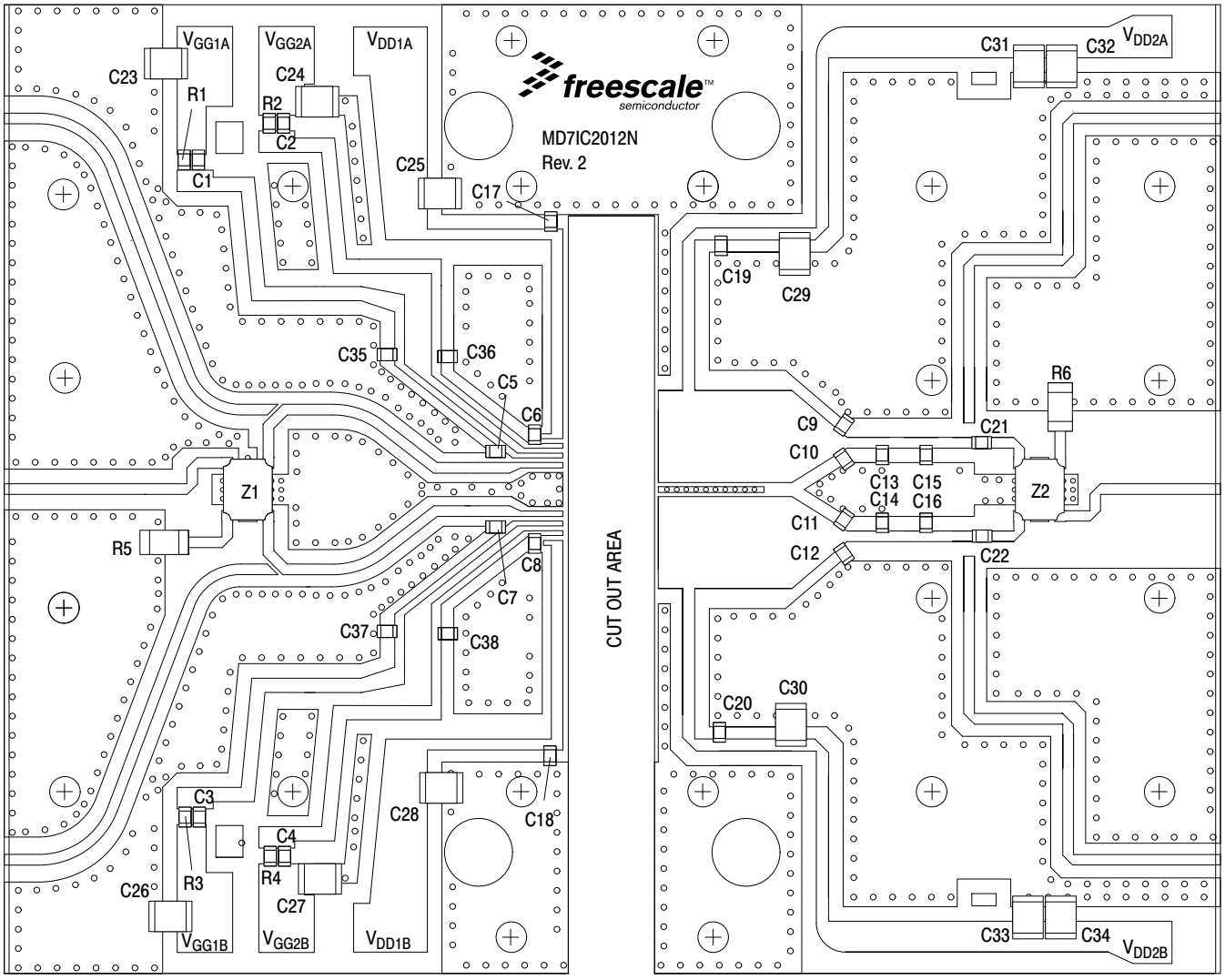


Figure 3. MD7IC2012NR1 Test Circuit Component Layout — 1805–2170 MHz

Table 6. MD7IC2012NR1 Test Circuit Component Designations and Values — 1805–2170 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	3.9 pF Chip Capacitors	ATC600F3R9BT250XT	ATC
C5, C6, C7, C8	1.0 pF Chip Capacitors	ATC600F1R0BT250XT	ATC
C9, C10, C11, C12	0.6 pF Chip Capacitors	ATC600F0R6BT250XT	ATC
C13, C14	0.8 pF Chip Capacitors	ATC600F0R8BT250XT	ATC
C15, C16	1.2 pF Chip Capacitors	ATC600F1R2BT250XT	ATC
C17, C18, C19, C20	10 pF Chip Capacitors	ATC600F10RBT250XT	ATC
C21, C22	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34	10 μF, Chip Capacitors	C5750X7S2A106M230KB	TDK
C35, C36, C37, C38	22 nF Chip Capacitors	GRM31BR72E223KW01L	Murata
R1, R2, R3, R4	2 kΩ, 1/8 W Chip Resistors	CRCW12062K00FKEA	Vishay
R5, R6	50 Ω, 20 W SM Chip Power Resistors	C20N50Z4	Anaren
Z1, Z2	1800–2300 MHz Band, 90°, 3 dB Hybrid Coupler	X3C21P1–03S	Anaren
PCB	0.020″, ε_r = 3.50	RO4350B	Rogers

TYPICAL CHARACTERISTICS — 1805–2170 MHz

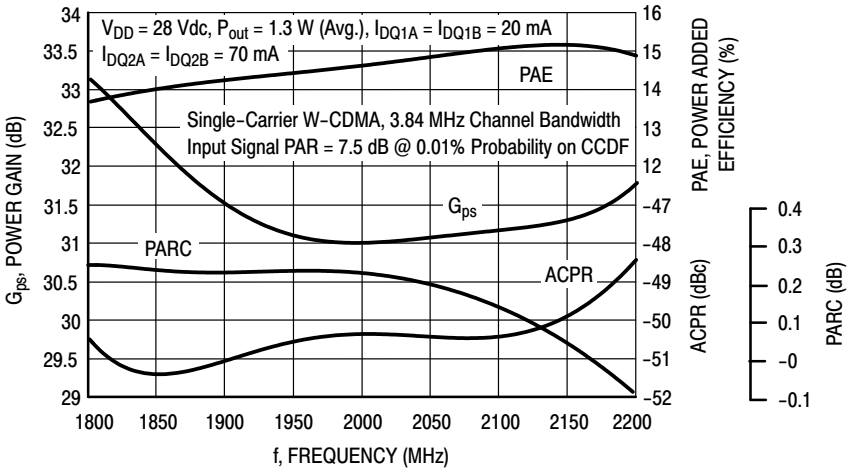


Figure 4. Output Peak–to–Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 1.3 Watts Avg.

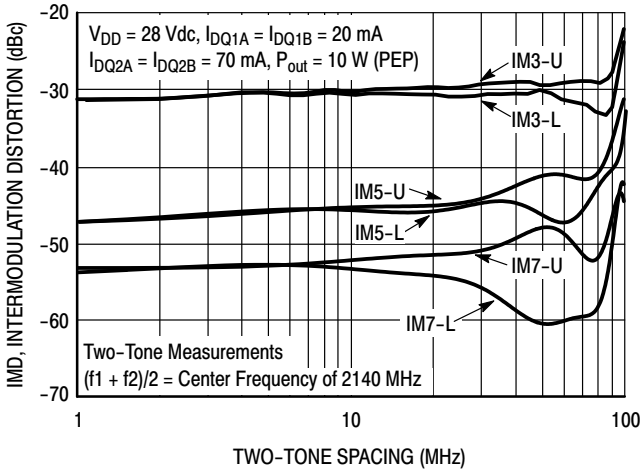


Figure 5. Intermodulation Distortion Products versus Two–Tone Spacing

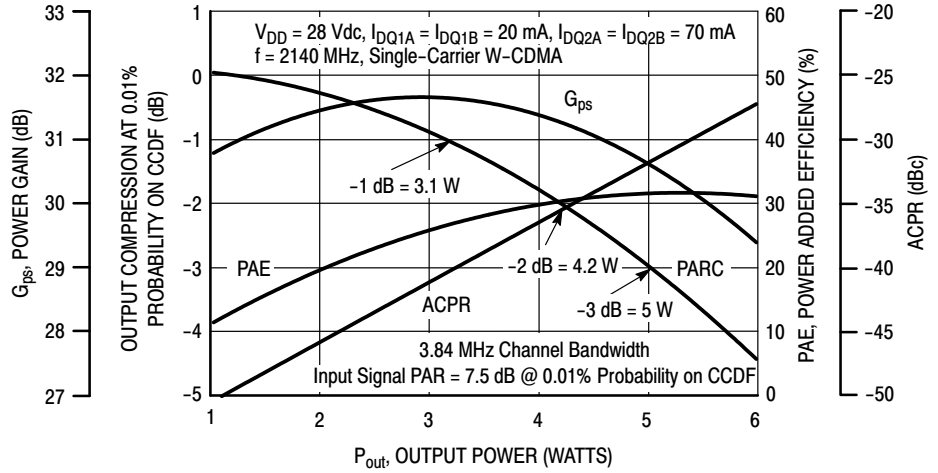


Figure 6. Output Peak–to–Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–2170 MHz

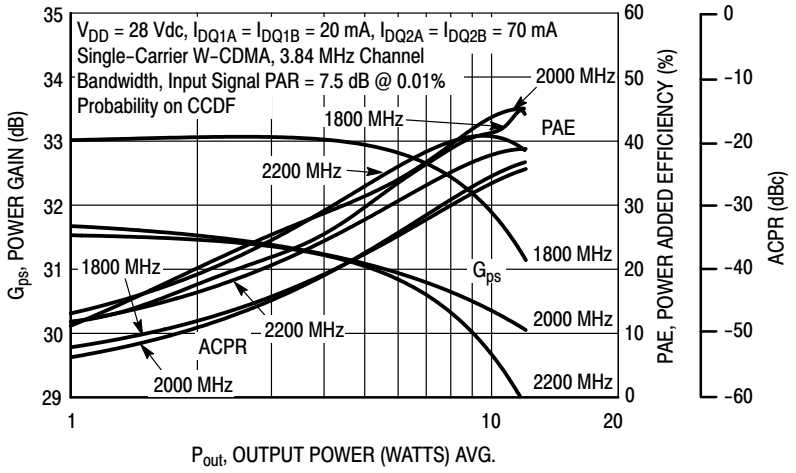


Figure 7. Single−Carrier W−CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

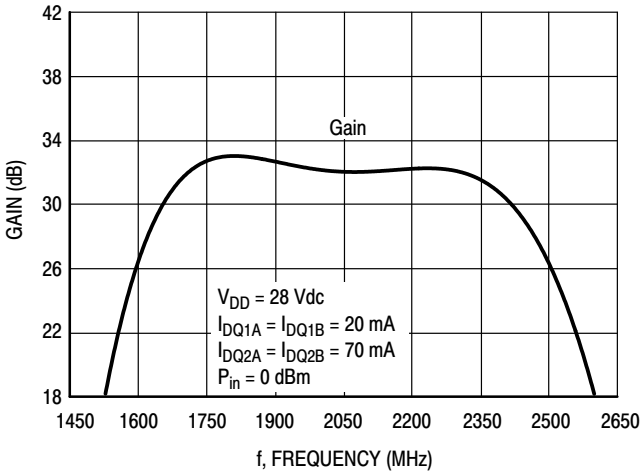


Figure 8. Broadband Frequency Response

W–CDMA TEST SIGNAL

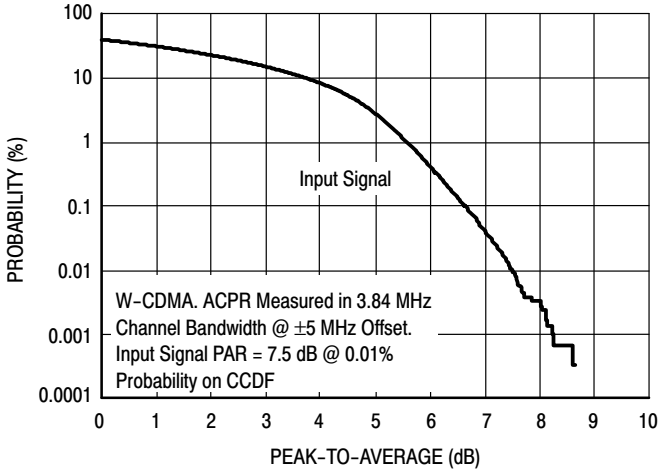


Figure 9. CCDF W–CDMA IQ Magnitude Clipping, Single–Carrier Test Signal

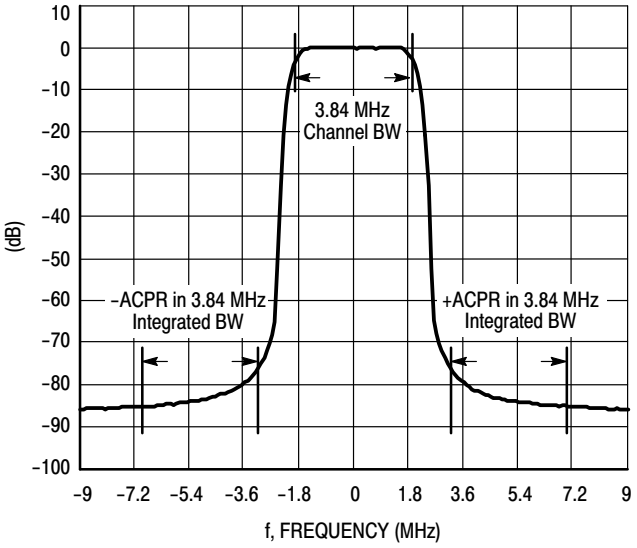


Figure 10. Single–Carrier W–CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 20 mA, I_{DQ2A} = I_{DQ2B} = 70 mA, P_{out} = 1.3 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
1800	73.3 + j2.21	7.94 – j1.22
1850	82.5 – j7.53	8.26 – j0.97
1900	80.1 – j27.0	8.40 – j1.13
1950	73.8 – j29.4	8.55 – j2.03
2000	64.6 – j33.8	8.67 – j2.62
2050	55.8 – j28.6	8.85 – j2.62
2100	50.5 – j27.2	8.64 – j2.79
2150	50.5 – j27.2	8.43 – j2.89
2200	45.7 – j19.8	8.05 – j2.95

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

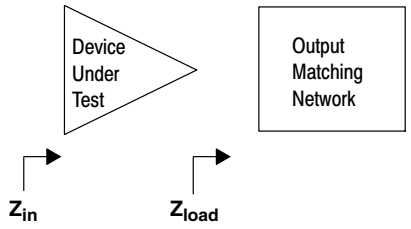


Figure 11. Series Equivalent Input and Load Impedance — 1805–2170 MHz

V_{DD} = 28 Vdc, I_{DQ1A} = 12 mA, I_{DQ2A} = 80 mA, CW

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	48.7 + j29.5	46.6 – j28.5	8.66 – j3.87	28.2	40.0	10.0	50.8	–5.3
2140	46.8 + j28.4	43.5 – j25.5	7.73 – j3.91	28.8	40.0	10.0	52.7	–7.2
2170	44.5 + j20.1	42.5 – j22.4	7.57 – j4.37	29.0	40.0	10.0	52.7	–6.9

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	48.7 + j29.5	46.3 + j26.5	8.66 – j3.87	26.2	40.7	11.8	51.6	–7.9
2140	46.8 + j28.4	43.9 – j22.5	9.01 – j4.25	26.4	40.7	11.8	50.8	–9.4
2170	44.5 + j20.1	42.9 – j19.4	8.73 – j4.51	26.6	40.7	11.8	51.2	–9.2

(1) Load impedance for optimum P1dB power. (2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 12. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 12 mA, I_{DQ2A} = 80 mA, CW

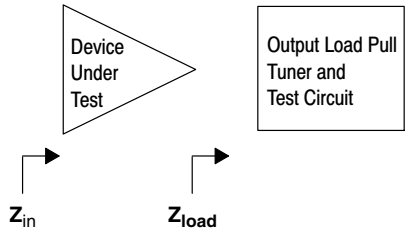
			Max Power Added Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	48.7 + j29.5	43.2 – j34.5	4.39 – j1.83	30.0	38.8	7.5	57.7	–12
2140	46.8 + j28.4	40.9 – j30.0	4.39 – j2.52	30.4	38.9	7.7	57.2	–13
2170	44.5 + j20.1	39.6 – j25.9	4.69 – j2.49	30.5	38.9	7.8	56.9	–12

			Max Power Added Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	48.7 + j29.5	44.3 – j30.6	5.17 – j2.00	27.7	39.7	9.4	56.5	–12
2140	46.8 + j28.4	41.8 – j25.9	5.53 – j2.22	27.9	39.8	9.6	56.1	–13
2170	44.5 + j20.1	40.2 – j23.7	4.69 – j2.49	28.4	39.4	8.7	55.7	–14

(1) Load impedance for optimum P1dB efficiency (2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 13. Load Pull Performance — Maximum Power Added Efficiency Tuning



V_{DD} = 28 Vdc, I_{DQ1A} = 12 mA, I_{DQ2A} = 80 mA, CW

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	61.8 – j5.85	61.6 + j7.80	8.04 – j0.206	29.6	40.0	10.0	54.7	–11
1840	73.7 – j4.41	70.3 + j1.44	8.01 – j0.273	29.8	40.0	10.0	55.9	–7.6
1880	73.3 + 8.94	74.5 – j7.06	8.65 – j1.23	29.2	40.0	10.0	53.8	–6.9

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	61.8 – j5.85	61.7 + j5.98	8.65 – j0.359	27.4	40.7	11.7	55.4	–18
1840	73.7 – j4.41	67.7 – j0.606	9.34 – j0.874	27.3	40.7	11.7	54.7	–13
1880	73.3 + j8.94	72.8 – j7.46	8.65 – j1.23	27.2	40.8	12.0	55.5	–10

(1) Load impedance for optimum P1dB power. (2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 14. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 12 mA, I_{DQ2A} = 80 mA, CW

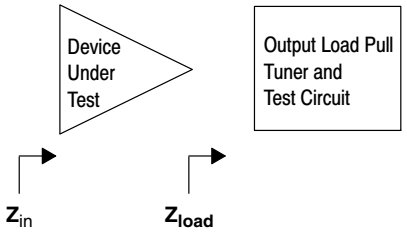
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Power Added Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	61.8 – j5.85	69.9 + j14.4	5.10 + j2.07	31.4	38.9	7.8	60.8	–13
1840	73.7 – j4.41	81.0 + j0.271	5.52 + j2.11	31.6	38.8	7.6	60.3	–9.1
1880	73.3 + j8.94	87.3 – j10.7	4.69 + j0.912	31.0	38.9	7.8	61.1	–10

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Power Added Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	61.8 - j5.85	68.1 + j8.57	5.05 - j0.32	29.3	39.6	9.3	61.4	-15
1840	73.7 - j4.41	76.4 - j1.31	5.52 + j2.11	29.6	39.5	9.3	61.3	-11
1880	73.3 + j8.94	79.4 - j10.8	5.43 + j1.07	28.8	39.8	9.3	61.4	-12

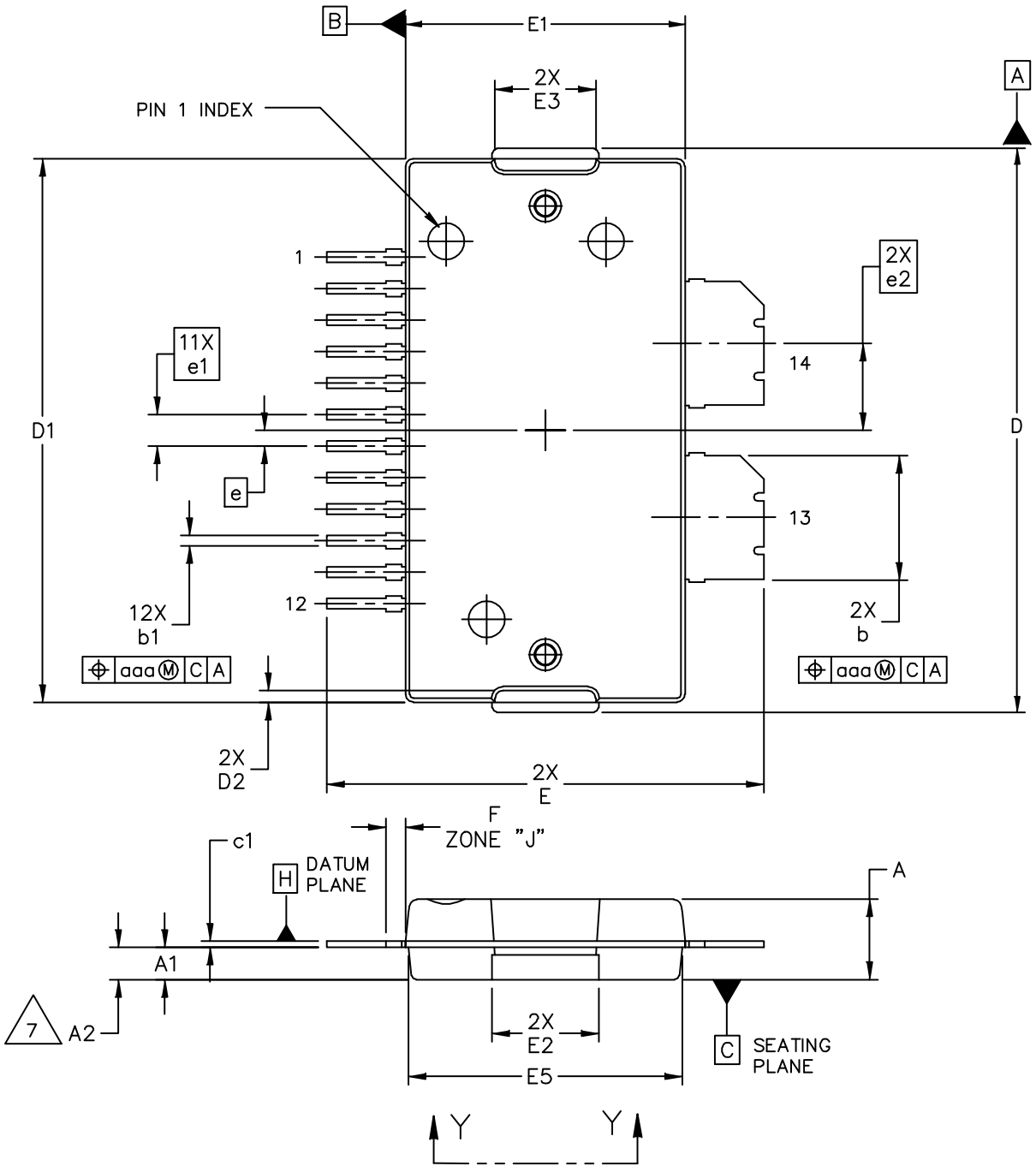
(1) Load impedance for optimum P1dB efficiency (2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 15. Load Pull Performance — Maximum Power Added Efficiency Tuning



PACKAGE DIMENSIONS



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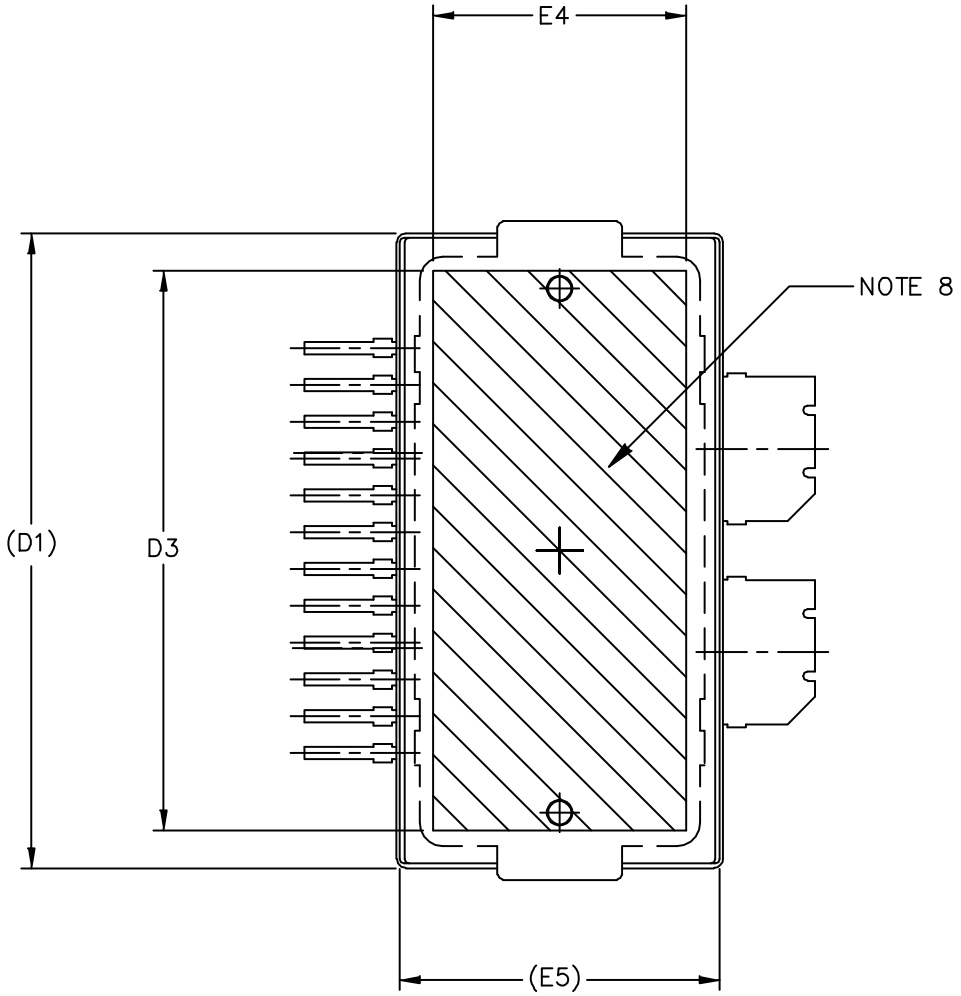

VIEW Y–Y

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	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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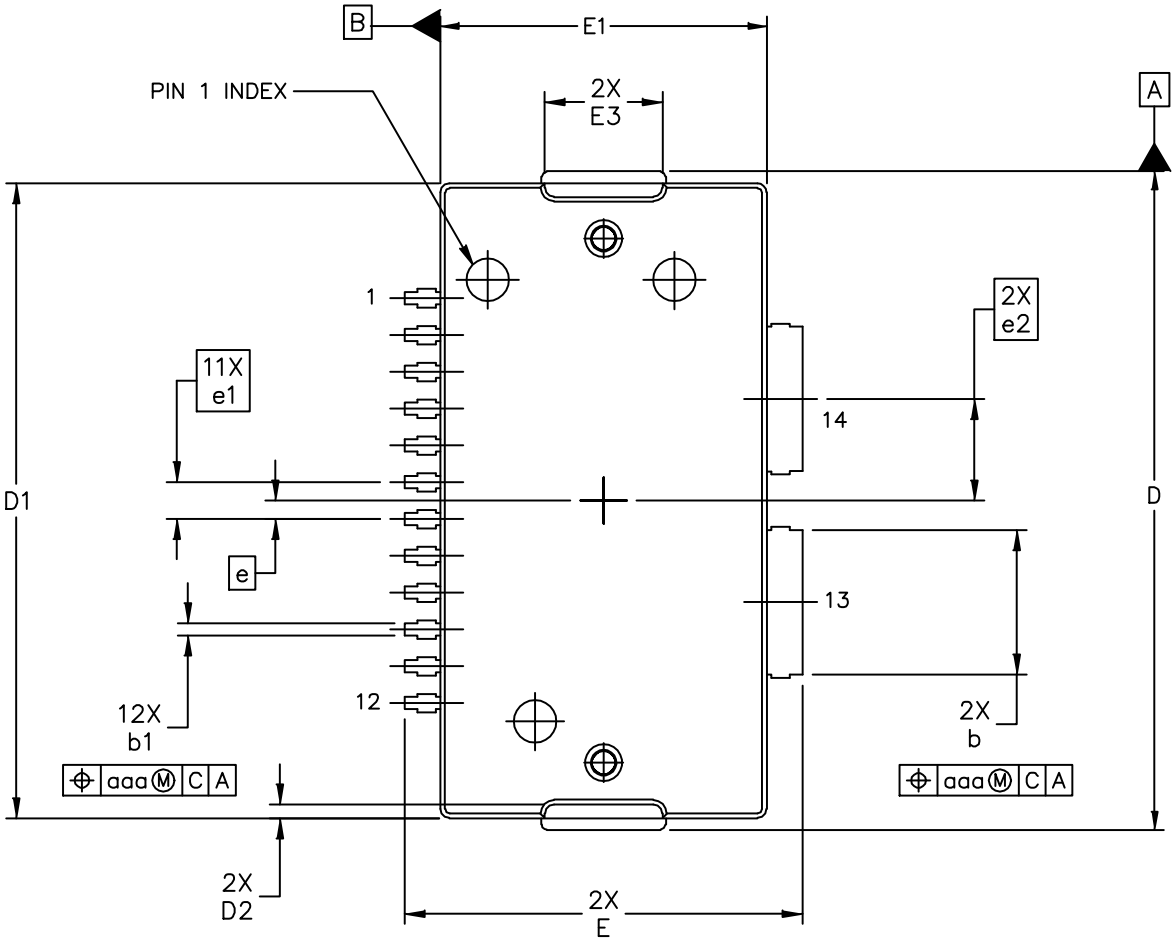

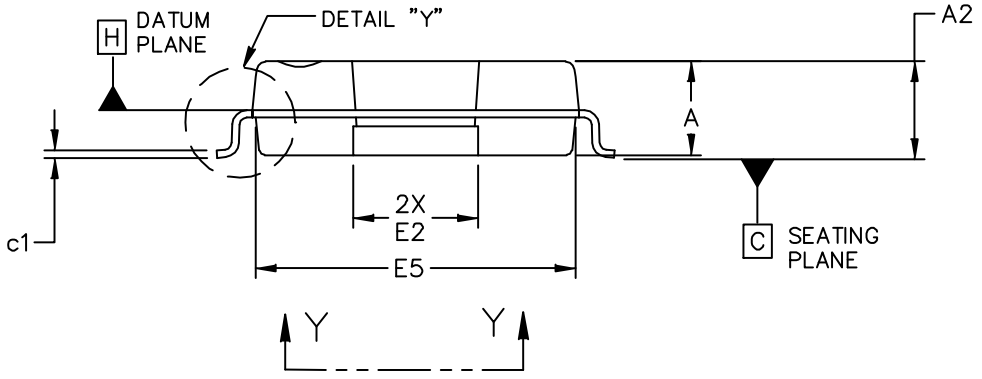

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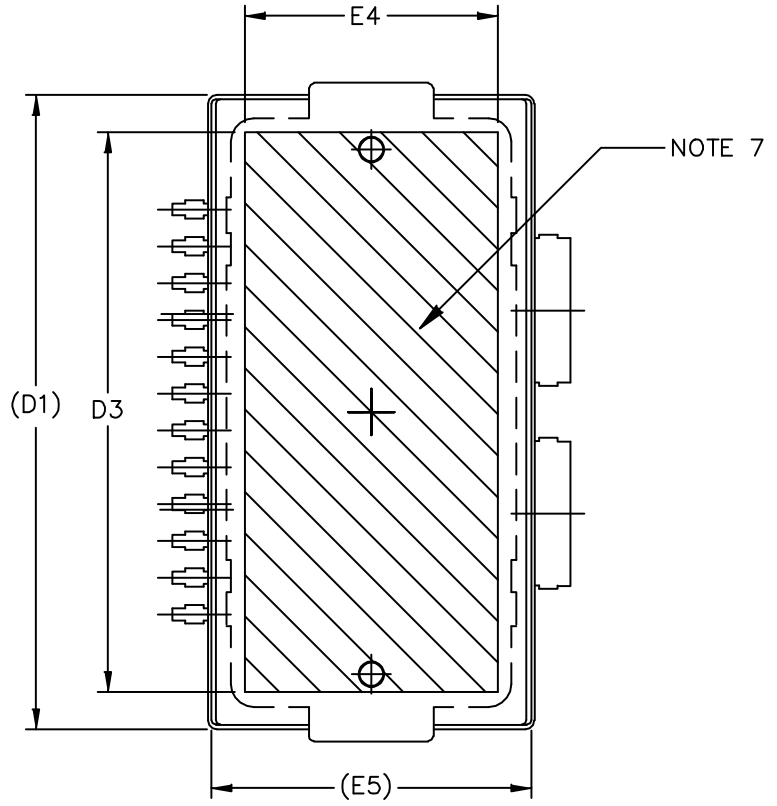
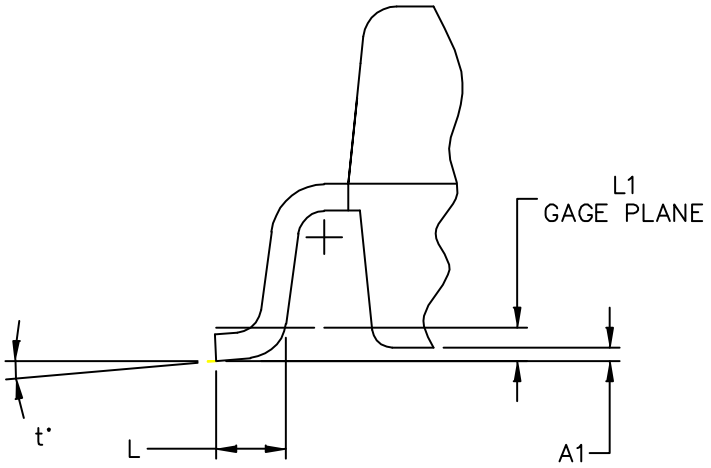


VIEW Y–Y



DETAIL "Y"

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over−Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3789: Clamping of High Power RF Transistors and RFICs in Over−Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2013	• Initial Release of Data Sheet

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