HARRIS SEMICONDUCTOR

RFW2N06RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors

May 1992

Features

- 2A, 60V
- $r_{DS}(on) = 0.160\Omega$
- UIS Rating Curve (Single Pulse)
- Design Optimized For 5 Volt Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Electrostatic Discharge Protected

Description

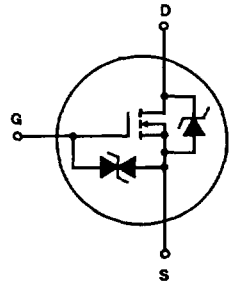
The RFW2N06RLE (TA9861) N-Channel logic level ESD protected power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFW2N06RLE was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor and relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFW2N06RLE is supplied in the 4-pin hexdip plastic package. (Similar to JEDEC outline TO-250)

Package

4-PIN HEXDIP
TOP VIEW

Terminal Diagram



6 LOGIC LEVEL POWER MOSFETs

Absolute Maximum Ratings ($T_C = +25^oC$)

			UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	+10, -5	V
Drain Current			
RMS Continuous	I_D	2	A
Pulsed Drain Current	I_{DM}	14	A
Single Pulse Avalance Rating	E_{AS}	Refer to UIS Curve	
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Power Dissipation			
$T_C = +25^oC$	P_D	1.09	W
Derate Above $+25^oC$	P_T	0.009	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2838.1**

Electrical Characteristics Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25mA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-1	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10V, V_{GS} = -5V		-	-	10	µA
				-	-	10	µA
On Resistance	$r_{DS(on)}$	I_D = 2A, V_{GS} = 5.0V, I_D = 2A, V_{GS} = 4.3V		-	-	160	mΩ
				-	-	200	mΩ
Turn-On Time	t_{on}	V_{DD} = 30V, I_D = 2A, R_L = 15, V_{GS} = 5V, R_{GS} = 25Ω		-	-	100	ns
Turn-On Delay Time	$t_{d(on)}$			-	13	-	ns
Rise Time	t_r			-	42	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	95	-	ns
Fall Time	t_f			-	45	-	ns
Turn-Off Time	t_{off}			-	-	200	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0 to 10V	V_{DD} = 48V, I_D = 2A, RL = 24Ω	-	20	30	nC
Gate Charge at 5V	Qg(5)	V_{GS} = 0 to 5V		-	11	16	nC
Threshold Gate Charge	Qg(th)	V_{GS} = 0 to 1V		-	0.6	1.0	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 2A, V_{DS} = 15V		-	-	4.3	V
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	535	-	pF
Output Capacitance	C_{oss}			-	175	-	pF
Reverse Transfer Capacitance	C_{rss}			-	32	-	pF
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30V, I_D = 2A, L = 0.21µH, R_L = 15Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	10	µJ
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	115	°C/W

Source-Drain Diode Ratings And Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 2A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/µs	-	-	200	ns

Performance Curves

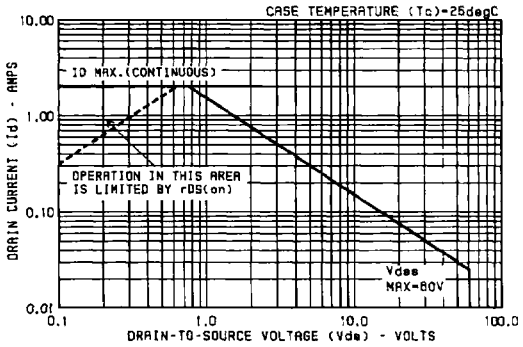


FIGURE 1. SAFE-OPERATING AREA CURVE

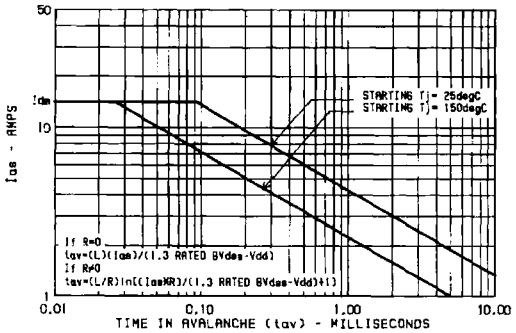


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

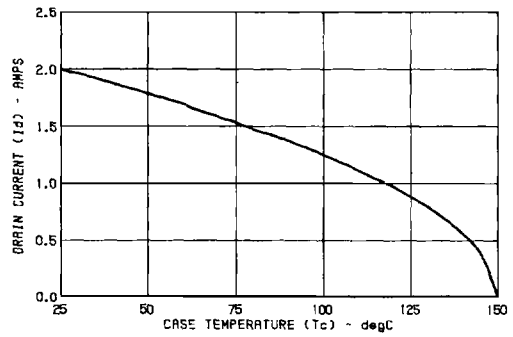


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

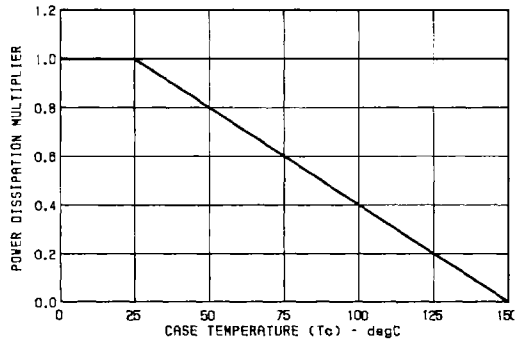


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

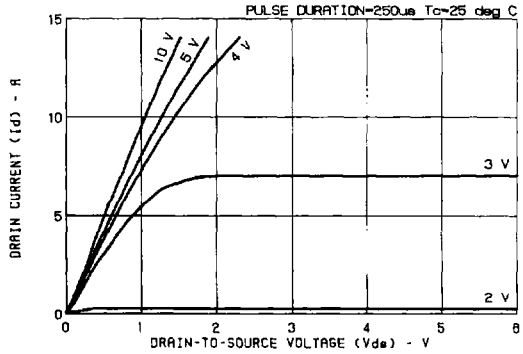


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

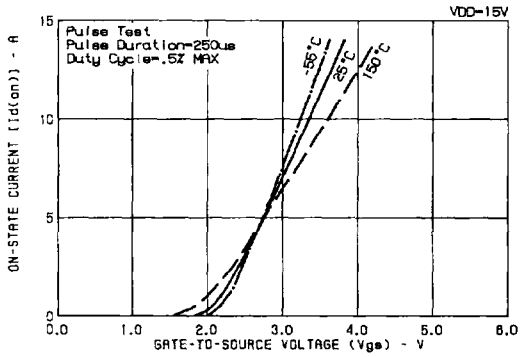


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Performance Curves (Continued)

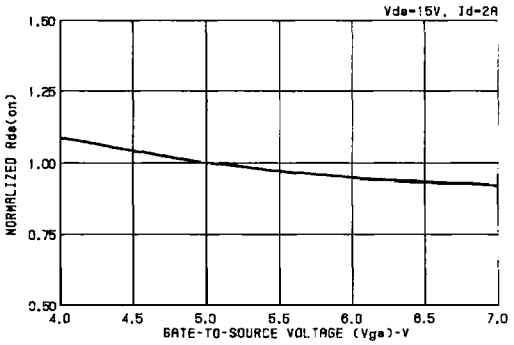


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs V_{gs}

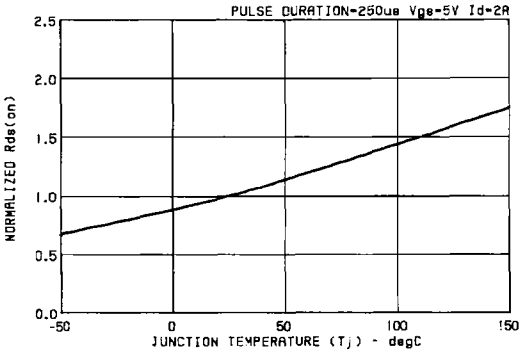


FIGURE 8. NORMALIZED $r_{DS(on)}$ vs JUNCTION TEMPERATURE

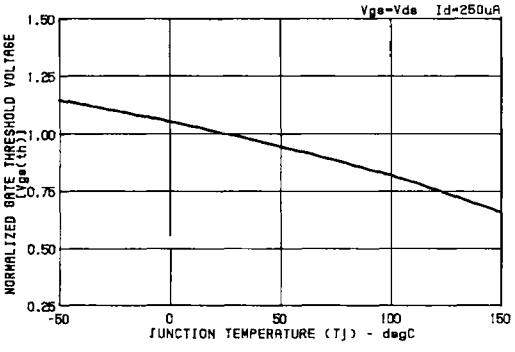


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

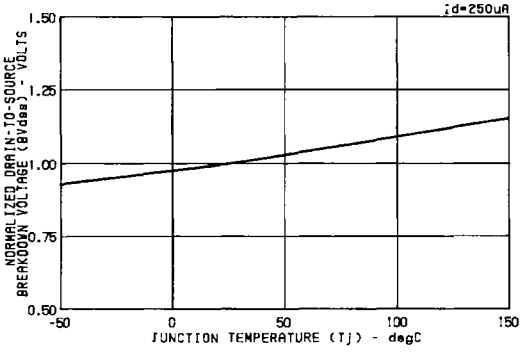


FIGURE 10. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

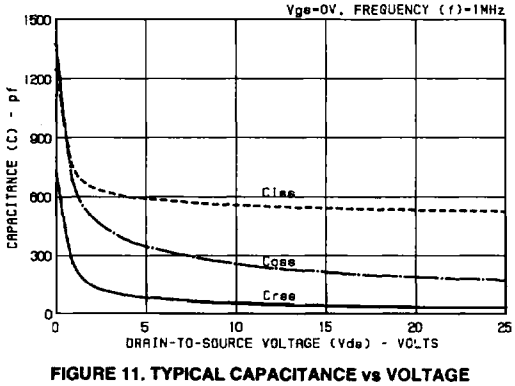


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

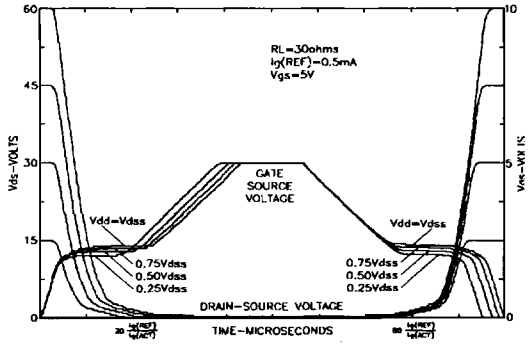


FIGURE 12. TYPICAL SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

Performance Curves (Continued)

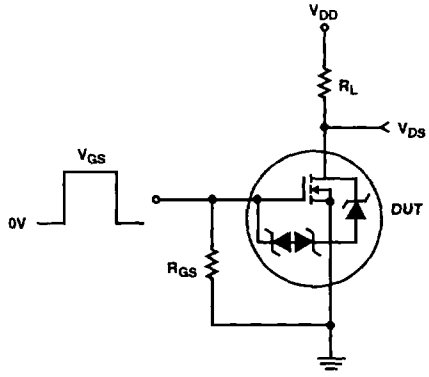


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUITS

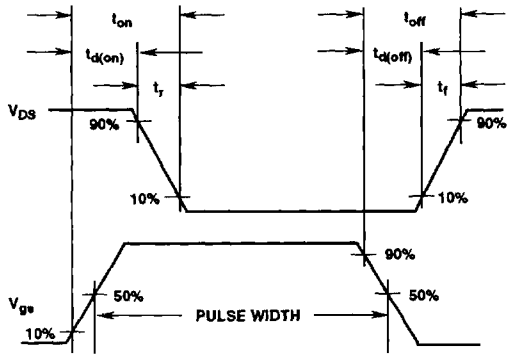


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

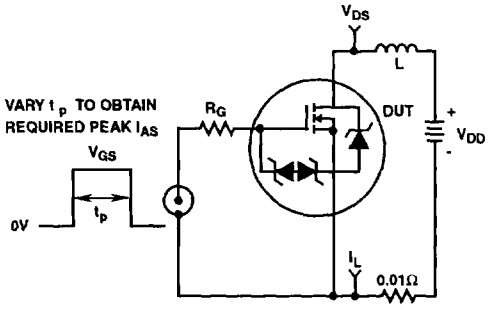


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

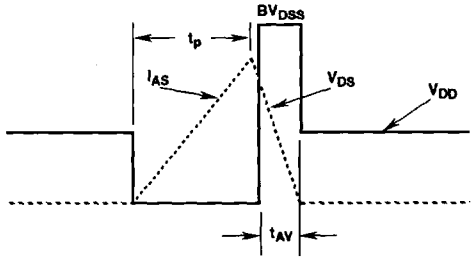


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS