MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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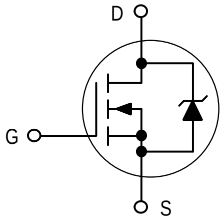
Advance Information

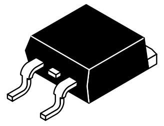
TMOS E-FET ™
High Energy Power FET
D^2PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

TMOS POWER FET
60 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.022 Ω

The D^2PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for medium voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

N–Channel





CASE 418B–03, Style 2
D^2PAK

New Features of TMOS 7

- Ultra Low On–Resistance Provides Higher Efficiency
- Reduced Gate Charge

Features Common to TMOS 7 and TMOS E–FETS

- Logic Level Gate Drive
- Avalanche Energy Specified
- Diode Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Industry Standard D^2PAK Surface Mount Package
- Surface Mount Package Available in 24 mm, 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	100	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	60 48 210	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	242 1.61 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 60 Vdc, V_{GS} = 5.0 Vdc, PEAK I_L = 60 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	 540	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.62 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

E–FET is a trademark of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 100 —	 — 135	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J =150°C)		I_{DSS}	 — —	 — —	 10 100	µAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 µAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 5.5	 2.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 30 Adc) (V_{GS} = 5.0 Vdc, I_D = 30 Adc)		$R_{DS(on)}$	 — —	 0.019 0.021	 0.022 0.024	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 60 Adc) (V_{GS} = 10 Vdc, I_D = 30 Adc, T_J = 150°C)		$V_{DS(on)}$	 — —	 — —	 1.6 1.5	Vdc
Forward Transconductance (V_{DS} = 8 Vdc, I_D = 15 Adc)		g_{FS}	30	35	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3000	4200	pF
Output Capacitance		C_{oss}	—	625	880	
Transfer Capacitance		C_{rss}	—	140	280	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 30 Adc, V_{GS} = 5.0 Vdc, R_G = 1.4 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	215	430	
Turn–Off Delay Time		$t_{d(off)}$	—	60	120	
Fall Time		t_f	—	130	260	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 30 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	67	90	nC
		Q_1	—	10	—	
		Q_2	—	42	—	
		Q_3	—	36	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	 (I_S = 30 Adc, V_{GS} = 0 Vdc) (I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	 — —	 0.81 0.65	 1.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs)	t_{rr}	—	155	—	ns
		t_a	—	100	—	
		t_b	—	55	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.87	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	 —	 7.5	 —	

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

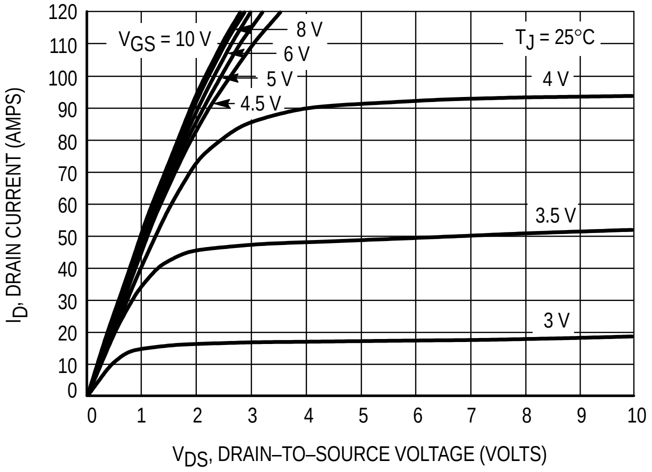


Figure 1. On–Region Characteristics

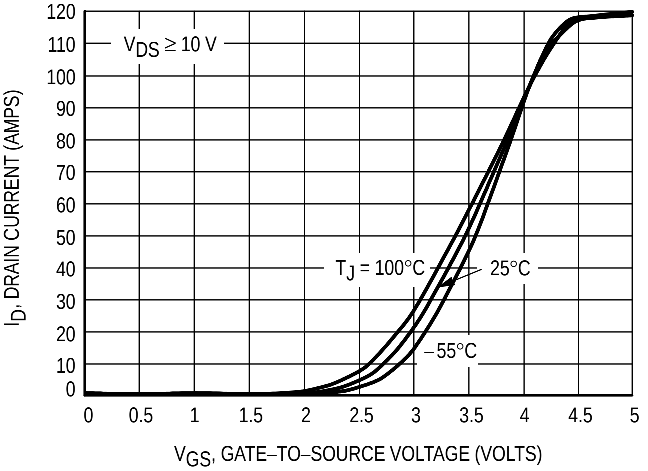


Figure 2. Transfer Characteristics

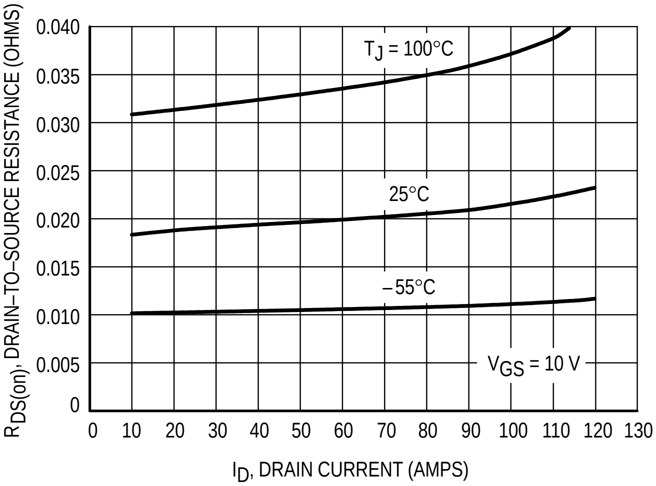


Figure 3. On–Resistance versus Drain Current and Temperature

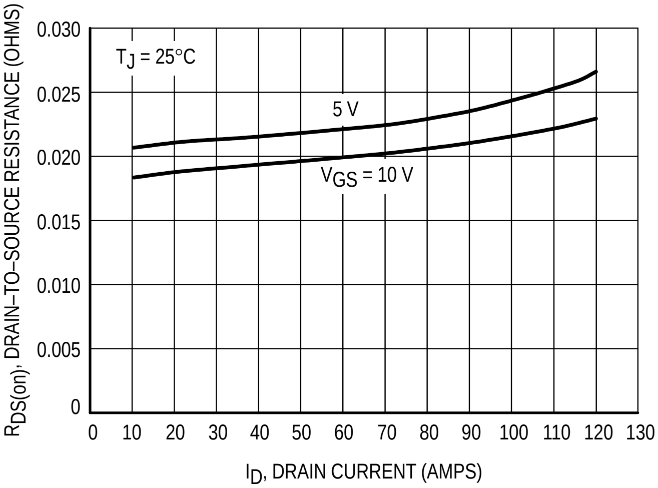


Figure 4. On–Resistance versus Drain Current and Gate Voltage

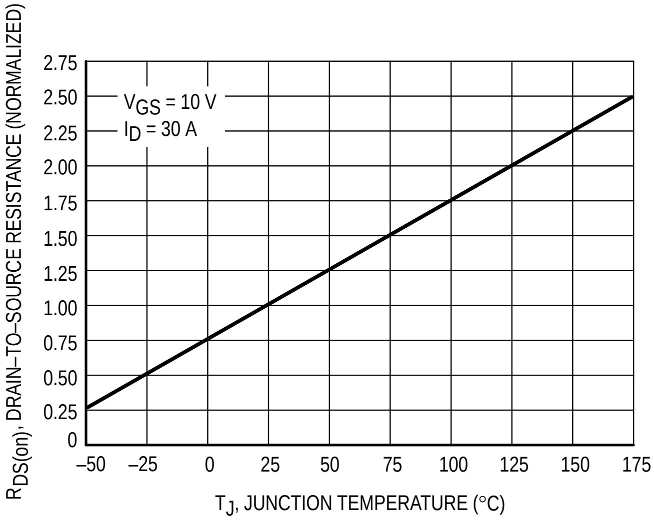


Figure 5. On–Resistance Variation with Temperature

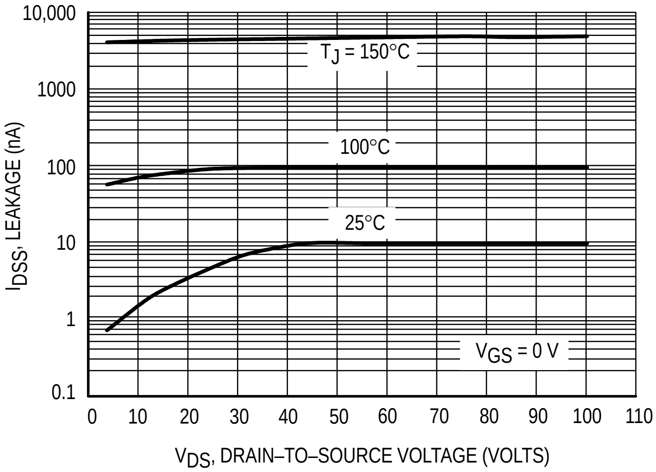


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \ln\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \ln\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

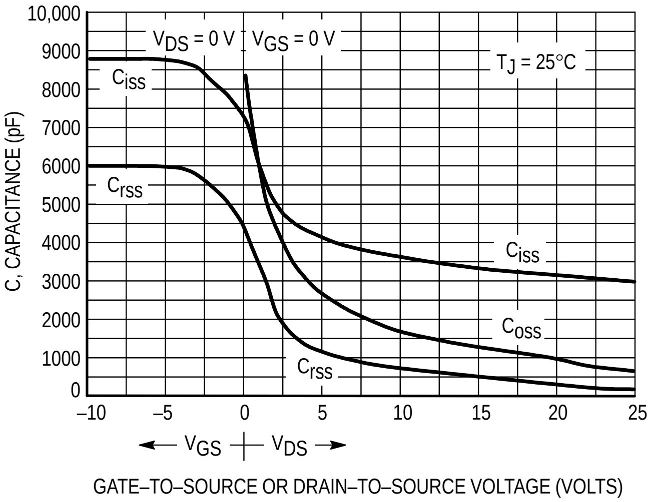


Figure 7. Capacitance Variation

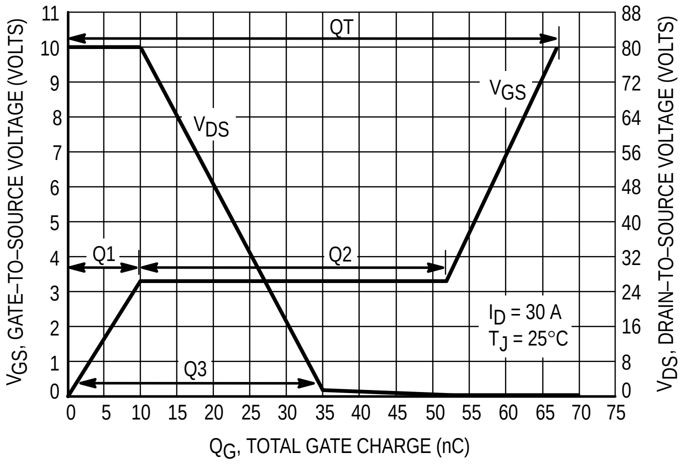


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

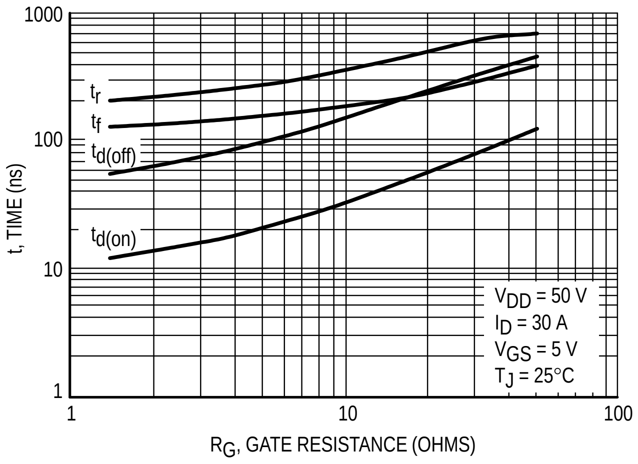


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

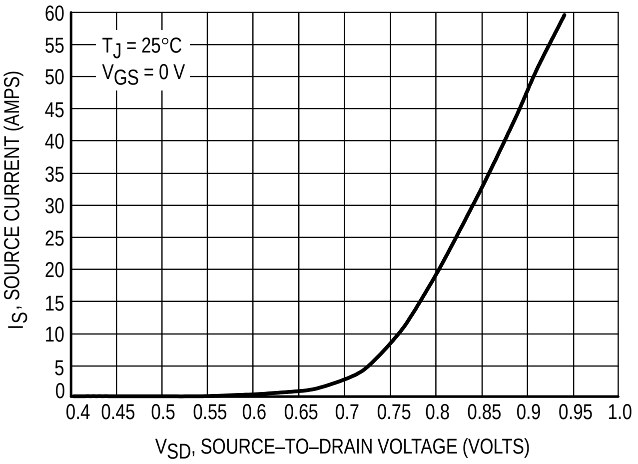


Figure 10. Diode Forward Voltage versus Current

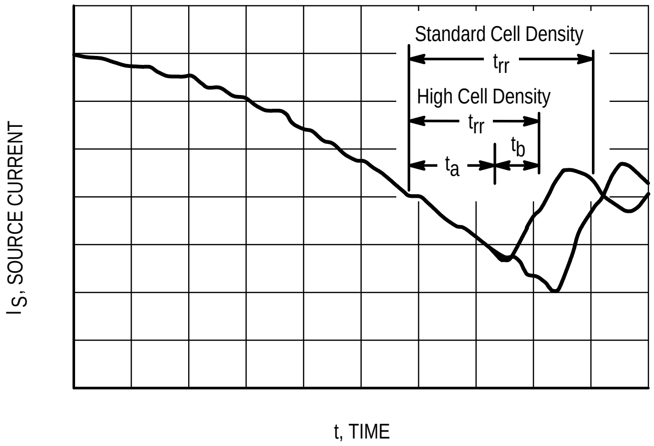


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

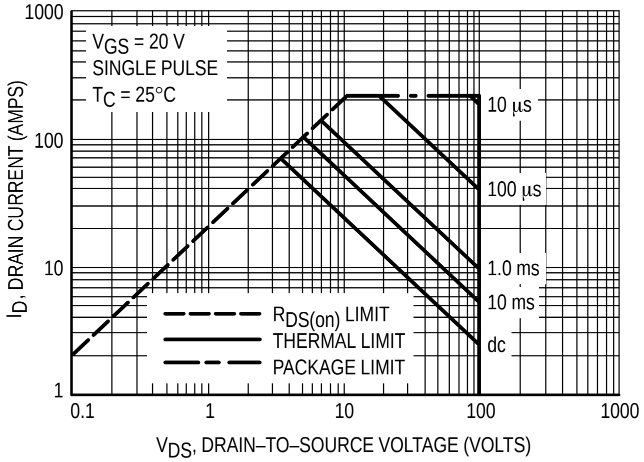


Figure 12. Maximum Rated Forward Biased Safe Operating Area

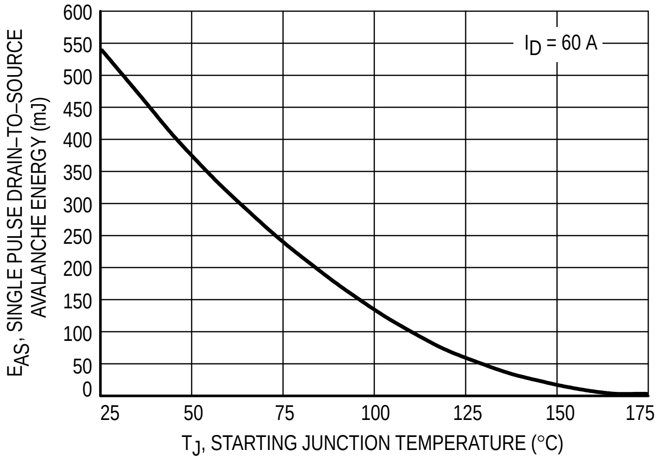


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

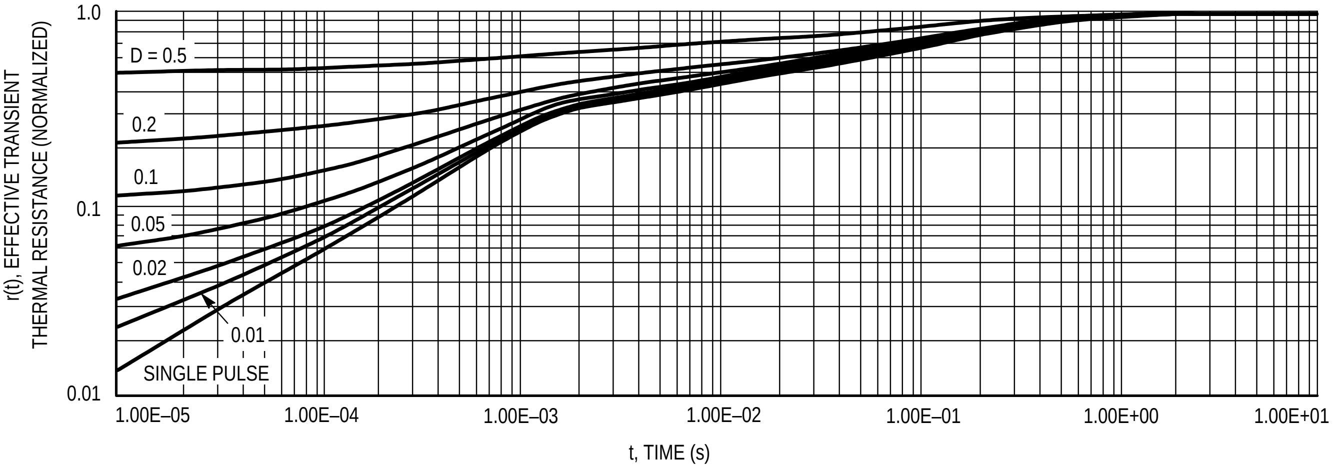


Figure 14. Thermal Response

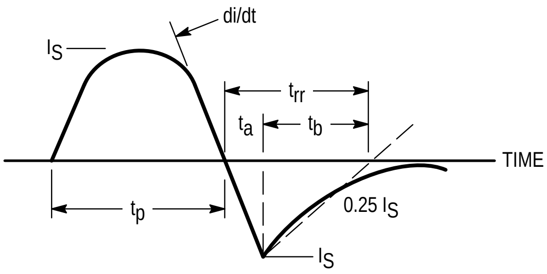
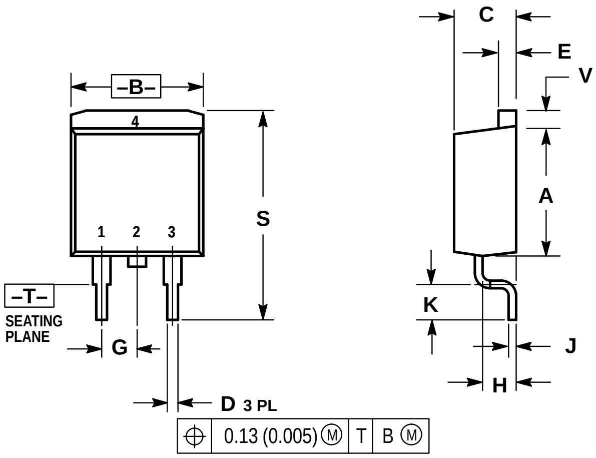


Figure 15. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

CASE 418B–03
ISSUE C

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