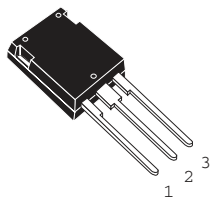
STY80NM60N

N-channel 600 V, 0.030 Ω, 74 A, MDmesh™ II Power MOSFET Max247

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STY80NM60N	650 V	< 0.035 Ω	74 A

- The worldwide best $R_{DS(on)}$ in Max247
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Max247

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

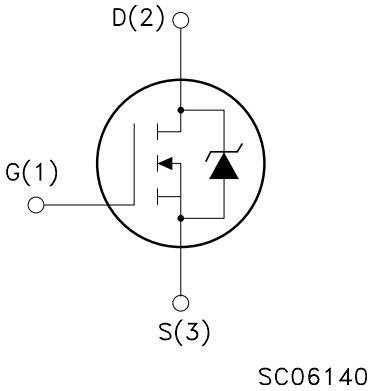


Table 1. Device summary

Order code	Marking	Package	Packaging
STY80NM60N	80NM60N	Max247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	600	V
V_{GS}	Gate- source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	74	A
I_D	Drain current (continuous) at T_C = 100 °C	46	A
I_{DM} (1)	Drain current (pulsed)	296	A
P_{TOT}	Total dissipation at T_C = 25 °C	447	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	–55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 74$ A, di/dt ≤ 400 A/µs, $V_{DSpeak} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.28	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	30	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	25	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25°C, $I_D = I_{AS}$, V_{DD} = 50 V)	2	J

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	600			V
dv/dt (1)	Drain source voltage slope	V_{DD} = 480 V, I_D = 74 A, V_{GS} = 10 V		48		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125 °C			10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 37 A		0.030	0.035	Ω

1. Characteristic value at turn off on inductive load.

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}=15 V, I_D = 37 A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		10100 455 26		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V		1300		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 74 A, V_{GS} = 10 V, *(see Figure 15)*		360 85 160		nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain		2.0		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300 V, I_D = 37 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 14)*		50 65 440 200		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				74 296	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 74 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 74 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 25 °C *(see Figure 16)*		700 25 65		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 74 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C *(see Figure 16)*		840 30 69		ns µC A

1. Pulse width limited by safe operating area .
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

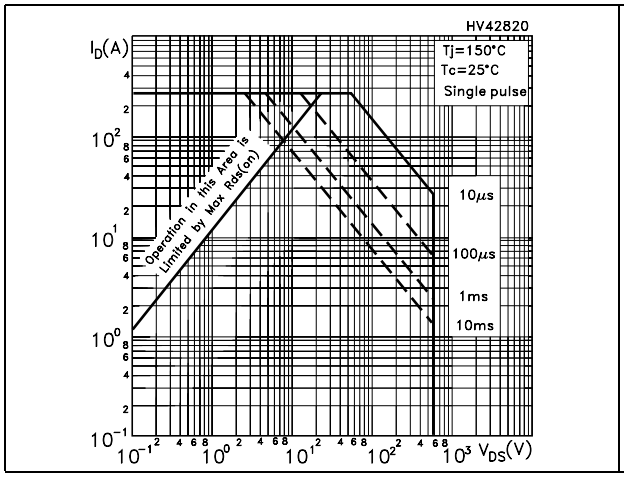


Figure 3. Thermal impedance

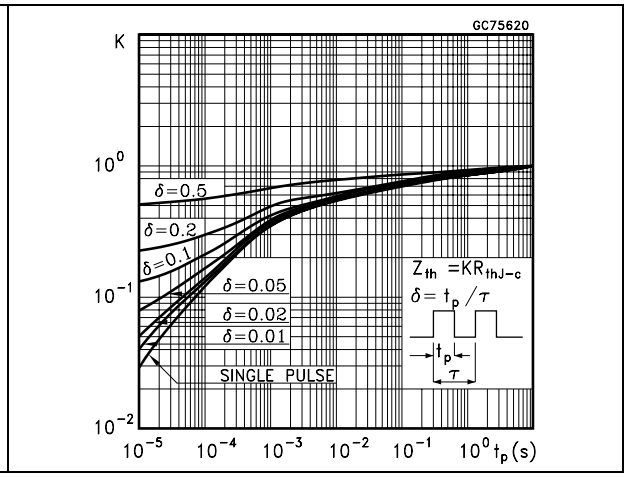


Figure 4. Output characteristics

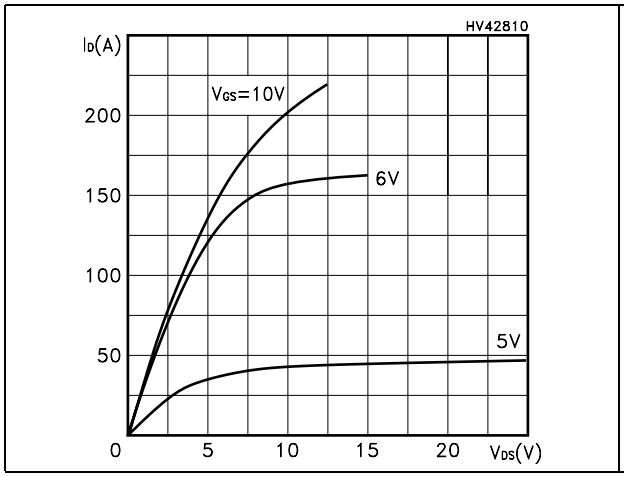


Figure 5. Transfer characteristics

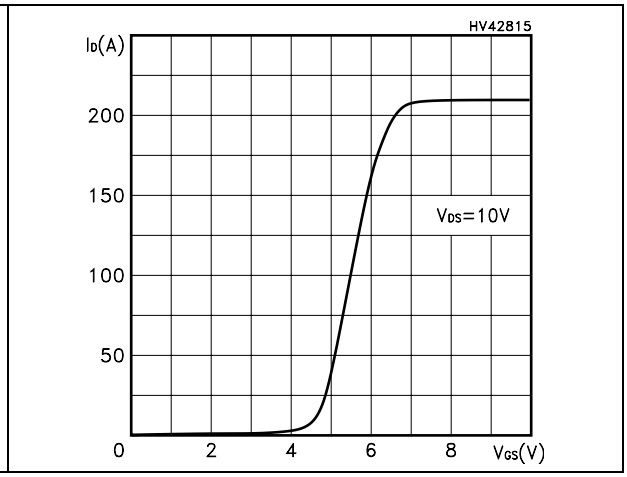


Figure 6. Transconductance

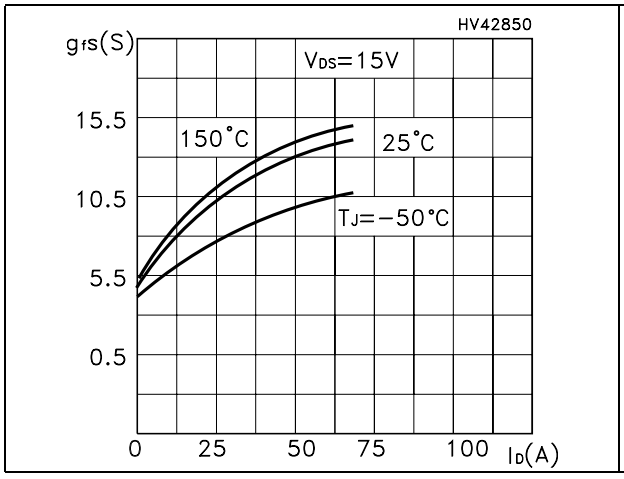


Figure 7. Static drain-source on resistance

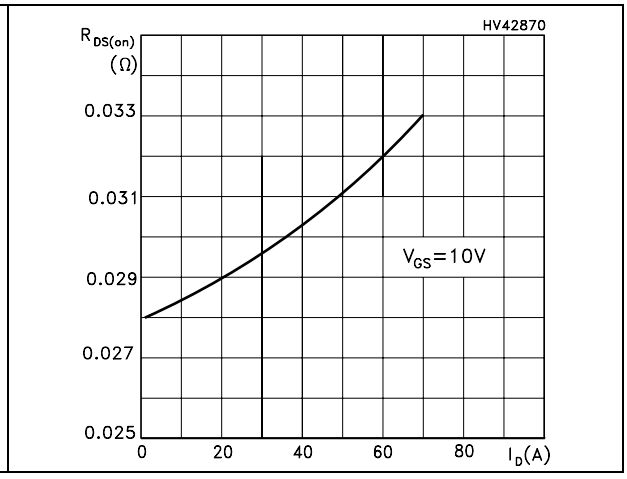


Figure 8. Gate charge vs gate-source voltage

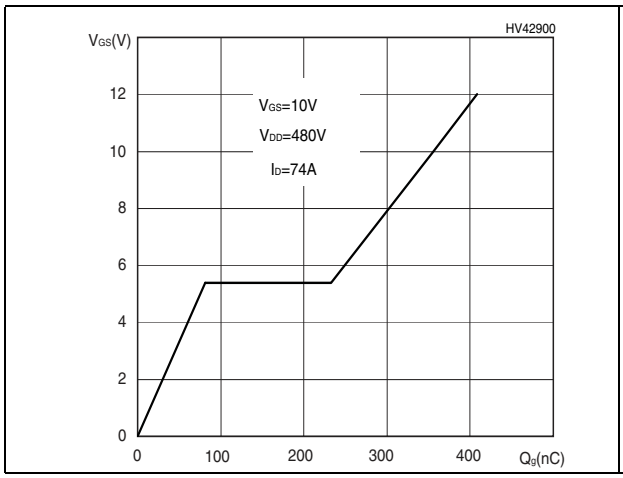


Figure 9. Capacitance variations

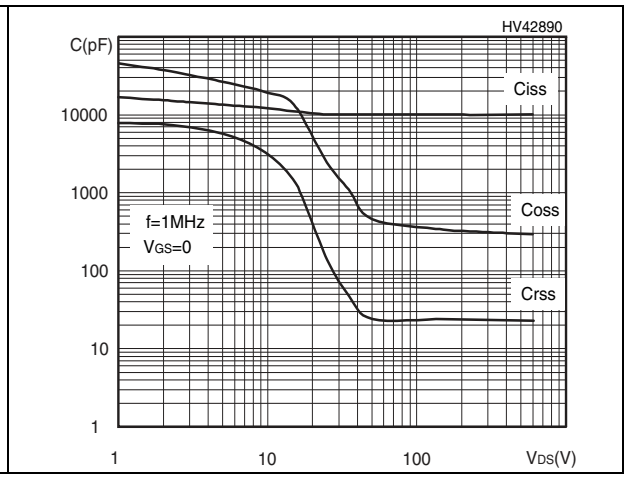


Figure 10. Normalized gate threshold voltage vs temperature

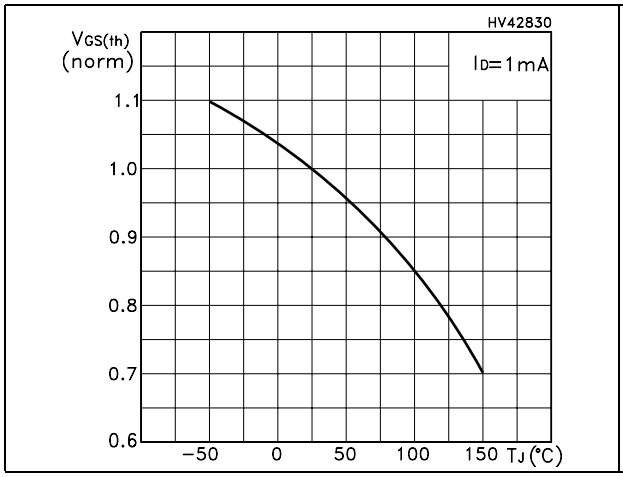


Figure 11. Normalized on resistance vs temperature

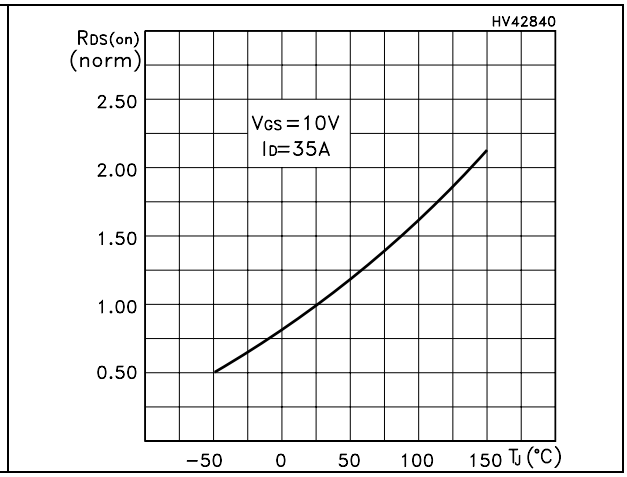


Figure 12. Source-drain diode forward characteristics

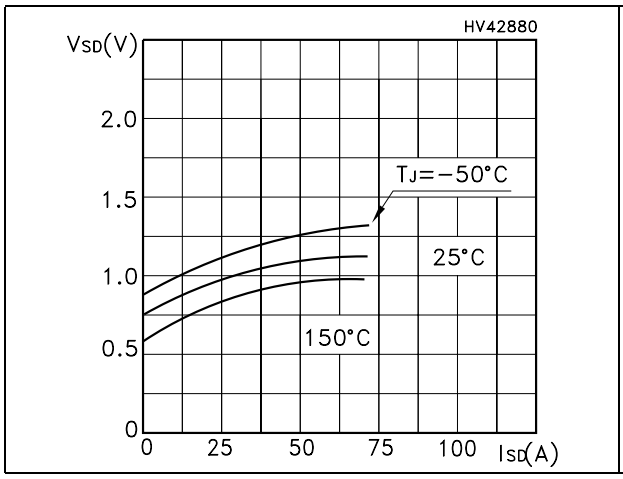
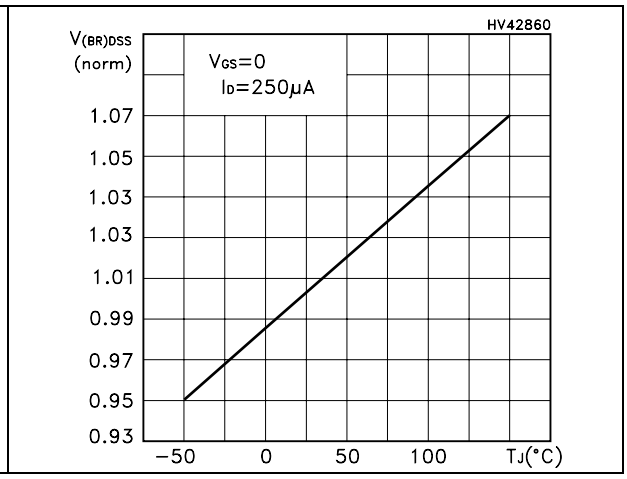


Figure 13. Normalized BV_{DSS} vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

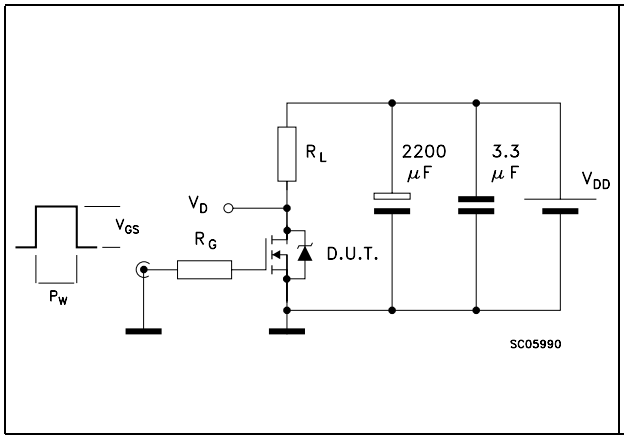


Figure 15. Gate charge test circuit

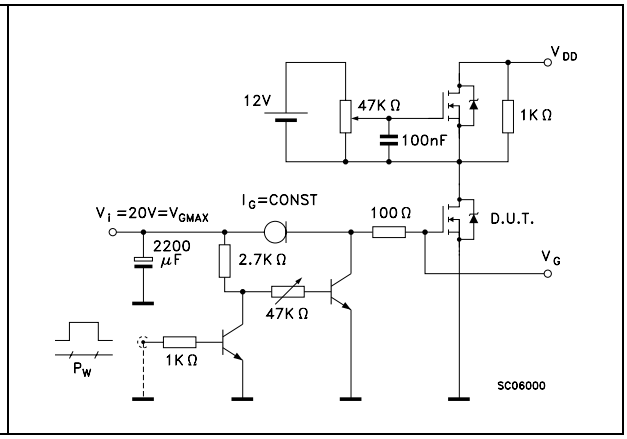


Figure 16. Test circuit for inductive load switching and diode recovery times

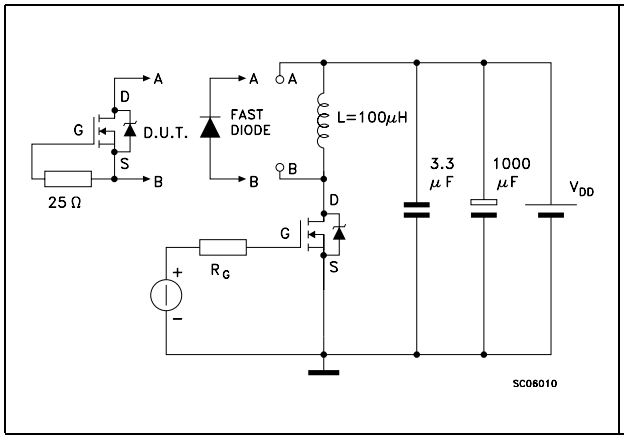


Figure 17. Unclamped inductive load test circuit

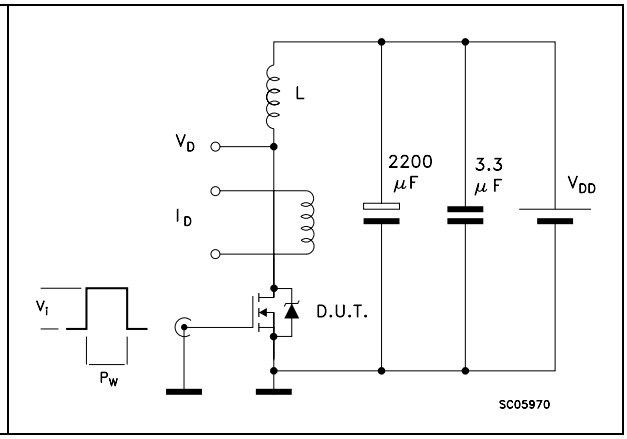


Figure 18. Unclamped inductive waveform

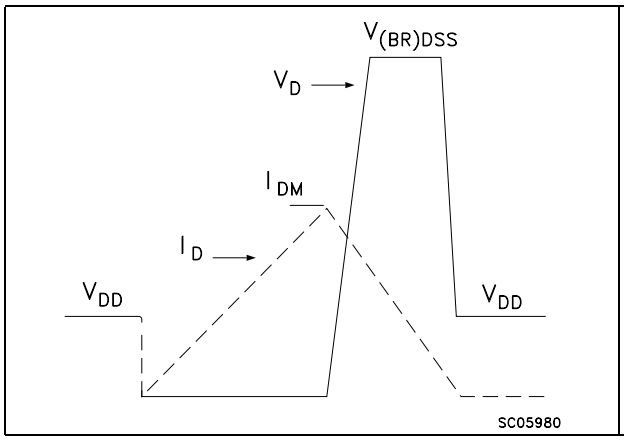
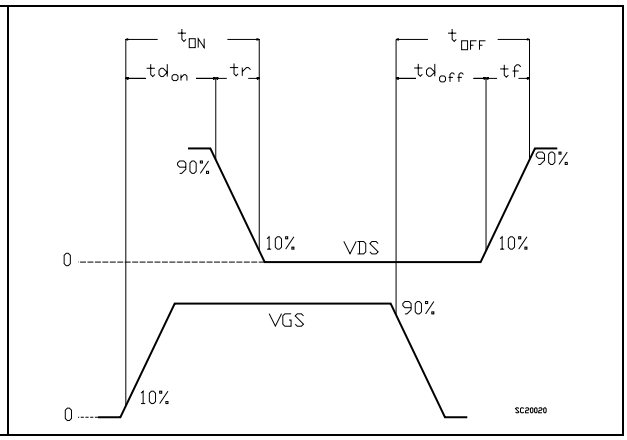


Figure 19. Switching time waveform



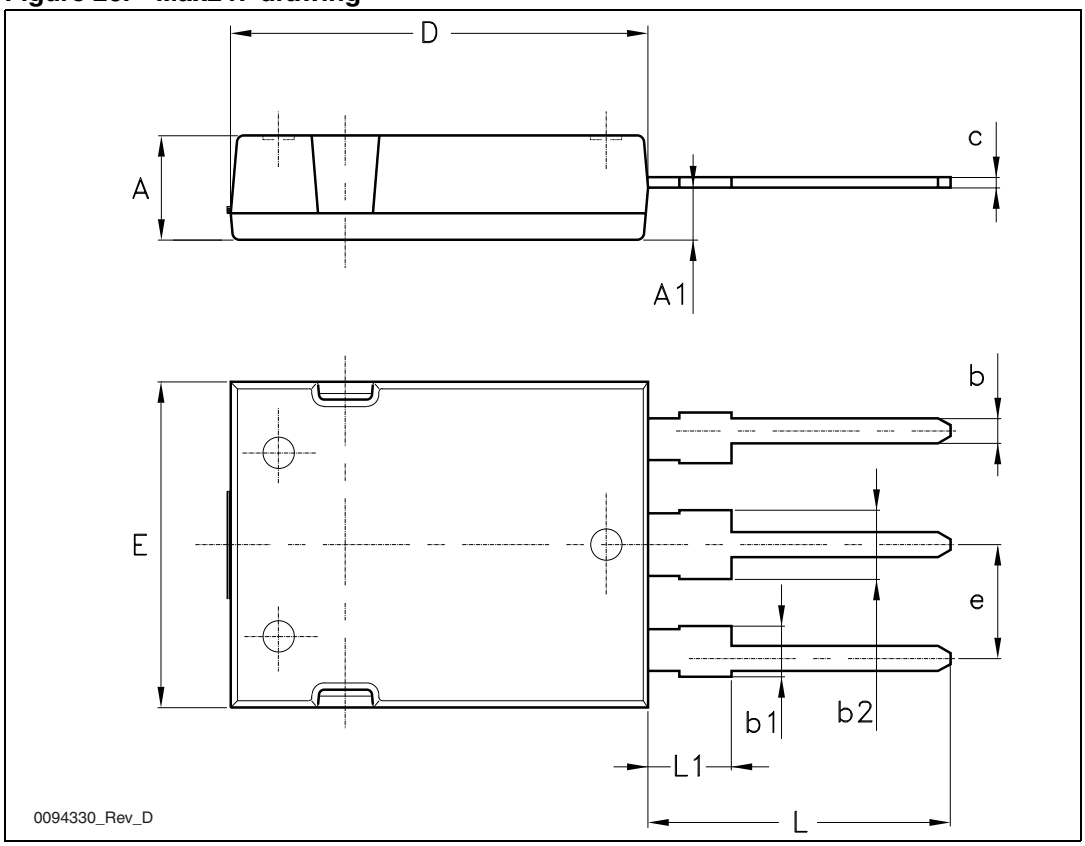
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. Max247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70		5.30
A1	2.20		2.60
b	1.00		1.40
b1	2.00		2.40
b2	3.00		3.40
c	0.40		0.80
D	19.70		20.30
e	5.35		5.55
E	15.30		15.90
L	14.20		15.20
L1	3.70		4.30

Figure 20. Max247 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Nov-2007	1	First release.
04-Dec-2007	2	Header has been corrected.
04-Aug-2008	3	Document status promoted: from preliminary data to datasheet.
14-Nov-2008	4	*Figure 13: Normalized BV_{DSS} vs temperature* has been corrected.
04-Feb-2009	5	*Figure 7: Static drain-source on resistance* has been corrected.
06-Jul-2011	6	Modified I_{DSS} value in *Table 5: On/off states*.

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