DS50PCI401EVK User Guide
PCI Express SMA Evaluation Kit

General Description:
The DS50PCI401EVK – PCI Express (PCIe) SMA evaluation kit provides a complete high bandwidth platform to evaluate the signal integrity and signal conditioning features of the National Semiconductor DS50PCI401 – Quad Lane PCI Express transceiver with Equalization and De-emphasis.

SMA edge launch connectors are used as the input and the output connections for this evaluation board. Commercially available adaptor boards can be purchased to facilitate connection to PCIe cables or backplane interconnects.

Features:

- Quad lane bi-directional transceiver up to 5.0 Gbps rate
- Signal conditioning on inputs and outputs for extended reach
- Adjustable receive equalization up to +26 dB gain
- Adjustable transmit de-emphasis up to −12 dB
- Adjustable transmit VOD (600 mVp-p to 1200 mVp-p)
- <0.15 UI of residual DJ at 5.0 Gbps with 40” FR4 trace
- Automatic de-emphasis scaling based on rate detect
- PCIe: Beacon signal pass-through,
- Adjustable electrical IDLE detect threshold
- Low power (100 mW/channel), per-channel power down
- Programmable via pin selection or SMBus interface
- Single supply operation at 2.5V ±5%
- >6 kV HBM ESD Rating
- 3.3V LVCMOS input tolerant for SMBus interface
- High speed signal flow–thru pinout package: 54-pin LLP (10 mm x 5.5 mm)

Applications:

- PCIe (2.5 Gbps / 5.0 Gbps)
- Will also support other AC coupled 8b/10b encoded serial standards under 5.0 Gbps

DS64BR401EVK Demo Kit Contents:

- End User License Agreement
- DS50PCI401EVK User Guide Rev.1.0
- DS50PCI401 Datasheet
- DS50PCI401EVK PCB

Ordering Information:

DEVICE: DS50PCI401SQ – QTY = 2000, DS50PCI401SQE – QTY = 250
SMA Evaluation Kit: DS50PCI401EVK

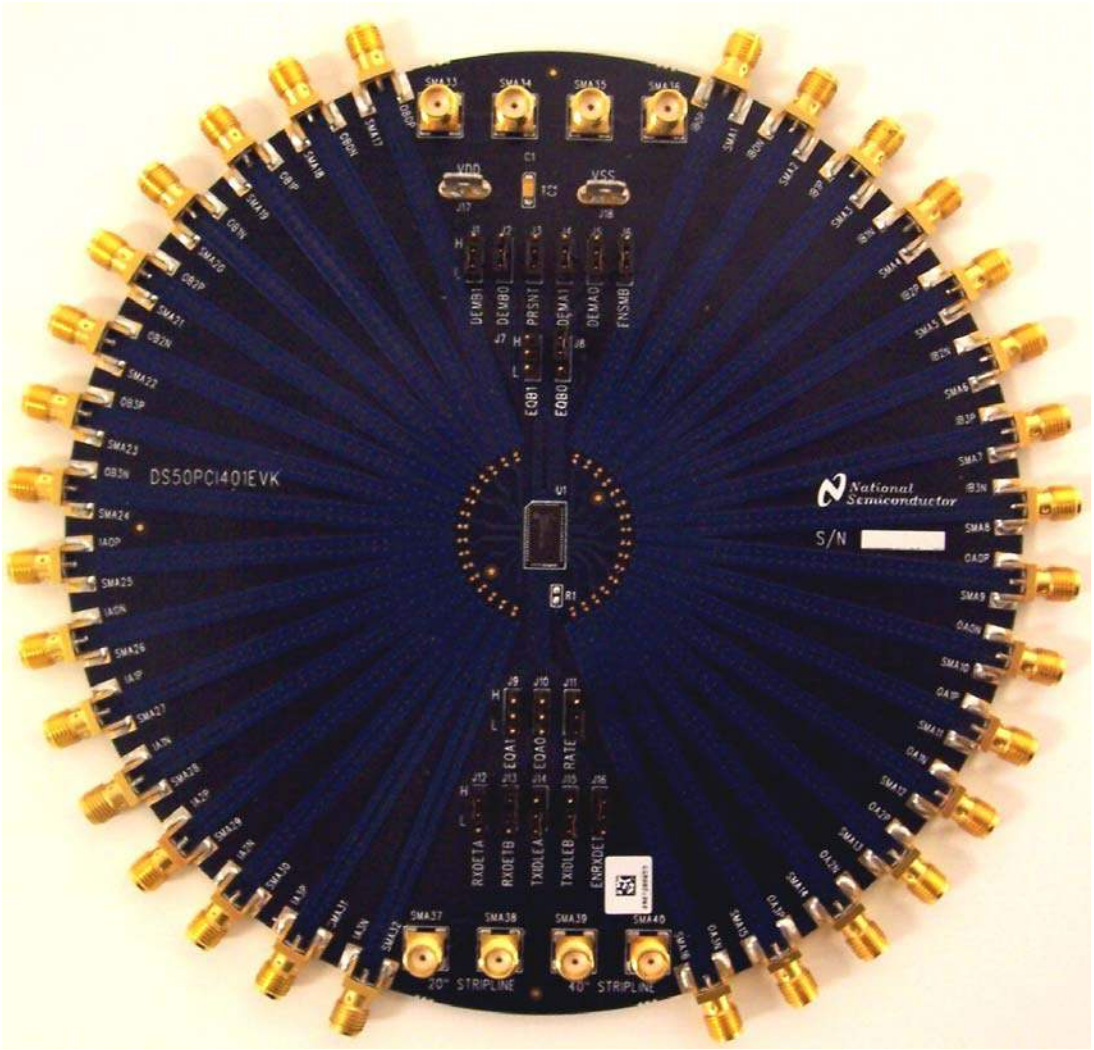


Figure 1. DS50PCI401EVK Evaluation Board

Quick Start Guide:

1. Connect -> 2.5V DC power to J17 and GND to J18. Verify supply voltage levels with a multi-meter prior to connection. VDD levels in excess of the Absolute Maximum will likely damage the device.
2. Attach 50 Ohm SMA cables to the board. Input and output cables must be AC coupled to most test equipment for optimum results. AC coupling can be accomplished with external units similar to the Picosecond Pulse Labs 5508-110. Alternatively, a location for on-board AC coupling is provided. The connecting trace between the 0402 SMT pads must be severed prior to capacitor installation.

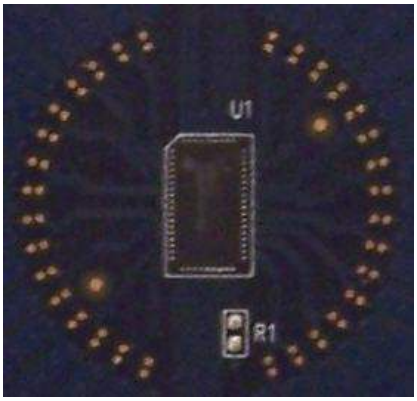


Figure 2. AC coupling location

3. Set EQ and DE level according to the attenuation characteristics of the inter-connect media.

Connection and Control Description

Component	Name	Level	Function
J17	VDD		DC Power – VIN direct to DS50PCI401
J18	VSS		GND – direct to DS50PCI401 and edge launch SMAs
J6	ENSMB	0	Optional SMBus access pins. See datasheet for additional information.
J1 - J2 and J4 - J5	DEM	00	Control pins for De-emphasis. (Default = 0 dB)
J7 - J8 and J9 - J10	EQ	FF	Control pins for Equalization. (Default = Bypass)
J3	PRSNT	0	Control pin for PCIe PRSNT signal.
J11	RATE		Control pin for RATE (2.5 Gbps or 5 Gbps).
J12, J13	RXDET	1	Control pins for RXDET (50 Ohm or Hi-Z to VDD).
J18	ENRXDET	1	Must be held HIGH for RXDET to operate.
J14, J15	TXIDLE	0	Control pins for TXIDLE

J17, J18 – Power Connection

VDD (2.375 – 2.625V) on J17 is needed for power. GND must also be connected to J18 / VSS.

J6 – SMBus Access

J6 is used to access the SMBus to configure the DS50PCI401. ENSMB should be tied low for external pin control. When ENSMB is tied high, SCL (clock input) and SDA (data input/output) are enabled.

Other Control Pins

Jumpers should be used to tie the control pins to 1-high (VDD), 0-low (GND) or F-float (NC). The EQA, EQB, DEMA, DEMB, RATE, TXIDLEA, and TXIDLEB are 3-level inputs. PRSNT is used to enable and disable the device and should be tied low (GND) for normal operation. RXDET is used to set the input termination impedance to VDD. Please refer to the tables below for detail information.

Equalization Control Pins (EQA/EQB)

EQA/B1	EQA/B0	Equalization Level	Recommend Media Length
F	F	Off	Bypass
1	1	4 dB at 2.5 GHz	8 inch FR4 or 0.7 meter (28AWG) PCIe cable
0	0	9.6 dB at 2.5 GHz	14 inch FR4 or 1-3 meters (28AWG) PCIe cable
F	0	11.4 dB at 2.5 GHz	20 inch FR4 or 5 meter (26AWG) PCIe cable
1	0	15.5 dB at 2.5 GHz	30 inch FR4 or 7 meter (24AWG) PCIe cable
F	1	17.0 dB at 2.5 GHz	40 inch FR4 or 9 meter (24AWG) PCIe cable
0	1	19.1 dB at 2.5 GHz	50 inch FR4 or 10 meter (24AWG) PCIe cable
0	F	20.6 dB at 2.5 GHz	15 meter (24AWG) PCIe cable
1	F	26.3 dB at 2.5 GHz	>15 meter (24AWG) PCIe cable

De-emphasis Control Pins (DEMA/DEMB)

DEMA1/B1	DEMA0/B0	De-emphasis Level	VOD Level
0	0	0 dB	VOD: 600 mV to 1200 mV
0	1	-3.5dB	VOD = 1000 mV
1	0	-6.0 dB	VOD = 1000 mV
1	1	-6.0 dB enhanced	VOD = 1000 mV
0	F	-9.0 dB enhanced	VOD = 1000 mV
1	F	-12.0 dB enhanced	VOD = 1000 mV
F	0	-9.0 dB enhanced	VOD = 1200 mV
F	1	-12.0 dB enhanced	VOD = 1400 mV
F	F	Reserved, don't use	

Rate Control Pins (RATE)

RATE	Functional Description
0	Set the De-emphasis pulse width duration for 2.5 Gbps (low rate)
1	Set the De-emphasis pulse width duration for 5.0 Gbps (high rate).
F	Enables the auto rate select function.

TX Output Control Pins (TXIDLEA/TXIDLEB)

TXIDLEA/B	Functional Description
0	Disables the signal detect/squelch function for all outputs A or B.
1	Forces all outputs to be muted (electrical idle).
F	Enables the signal detect/squelch function for all channels. Signal detect voltage level threshold can be adjusted with an external resistor on the SD_TH pin to GND. Default level is 130 mVp-p when SD_TH is floating. Please refer to Figure 1 in the datasheet for typical resistor value.

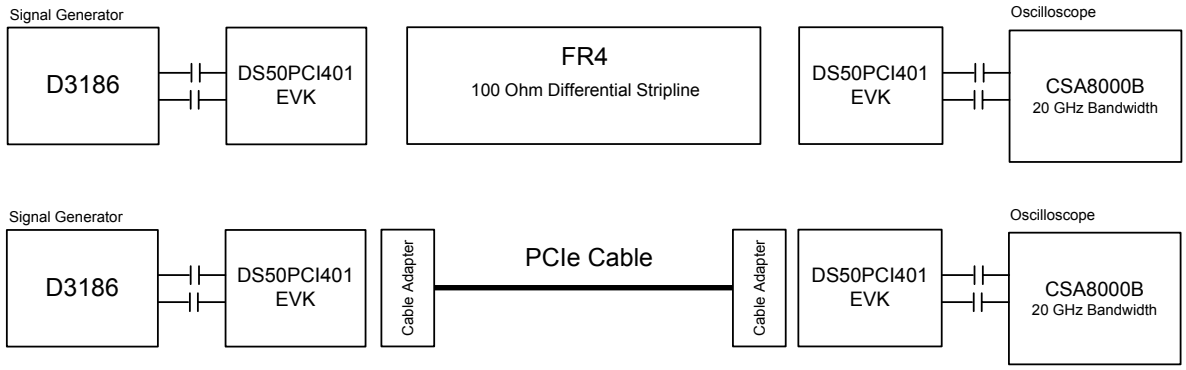
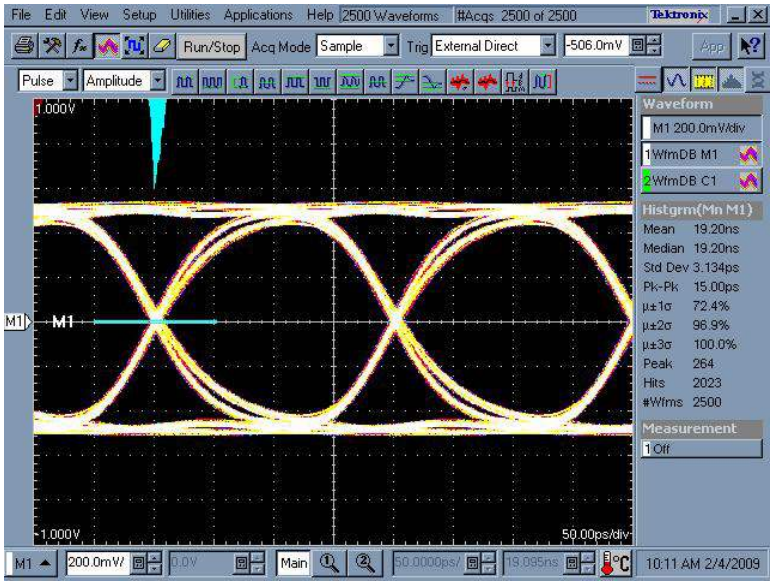


Figure 3. DS50PCI401EVK Equalization Test Setup

Typical Results:

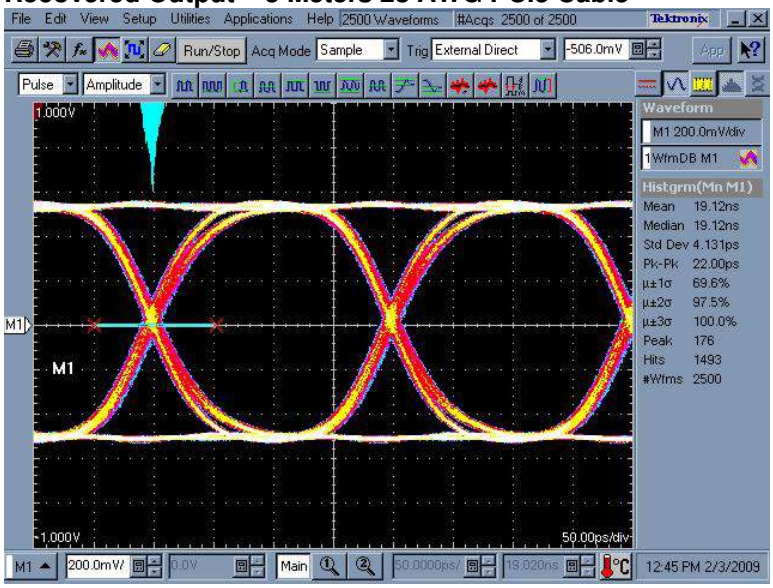
DS50PCI401 Device Performance with 3" EVK trace at 5.0 Gbps: OUTPUT (EVK Trace Only)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = FF (Bypass or Off)
DEM[1:0] = 00 (-0 dB with VOD = 1.0 Vp-p)

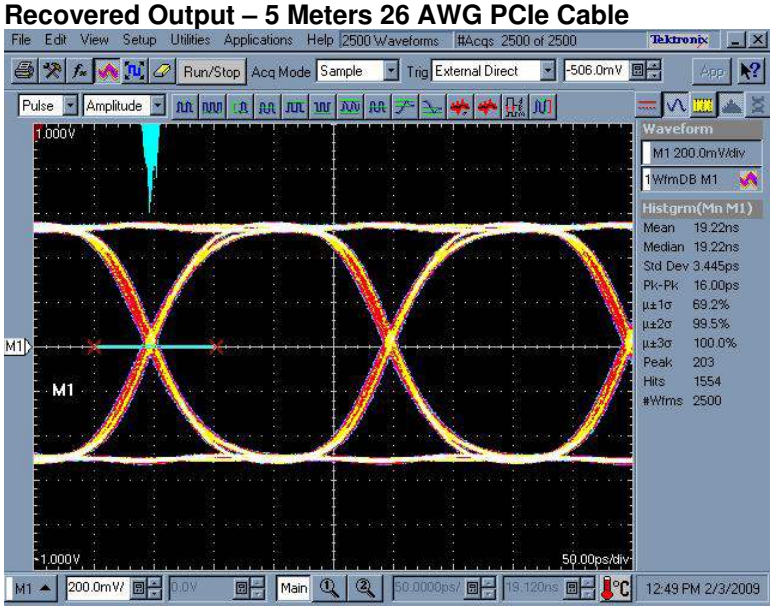
DS50PCI401 Equalization Performance at 5.0 Gbps:

Recovered Output – 3 Meters 28 AWG PCIe Cable



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = 00 (9.6 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

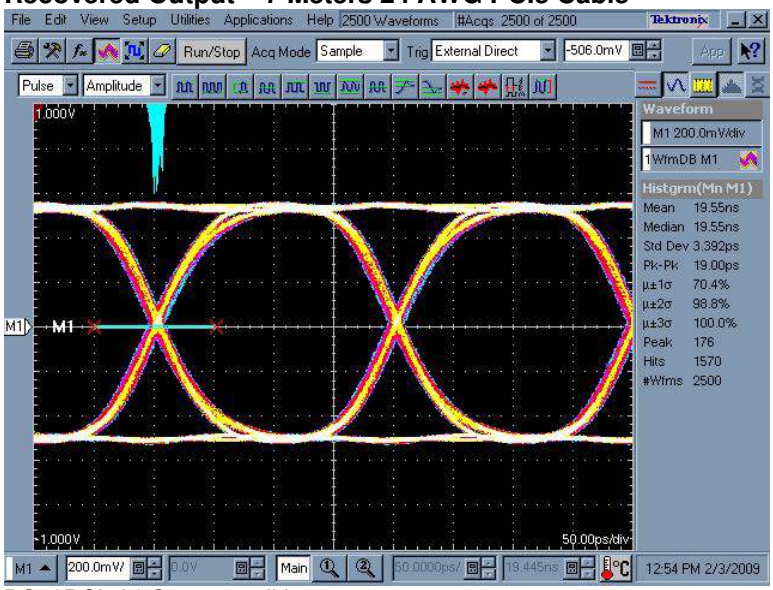
Recovered Output – 5 Meters 26 AWG PCIe Cable



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = F0 (11.4 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

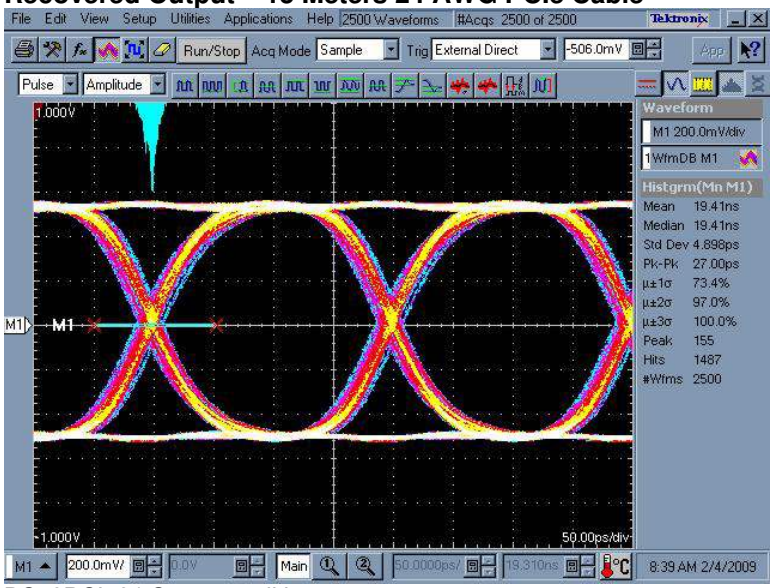
DS50PCI401 Equalization Performance at 5.0 Gbps:

Recovered Output – 7 Meters 24 AWG PCIe Cable



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = 10 (15.5 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

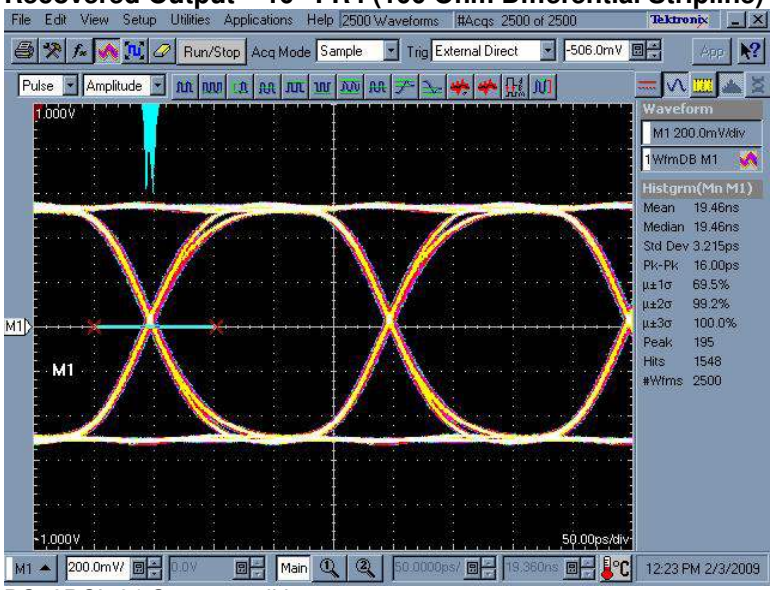
Recovered Output – 15 Meters 24 AWG PCIe Cable



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = 0F (20.6 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

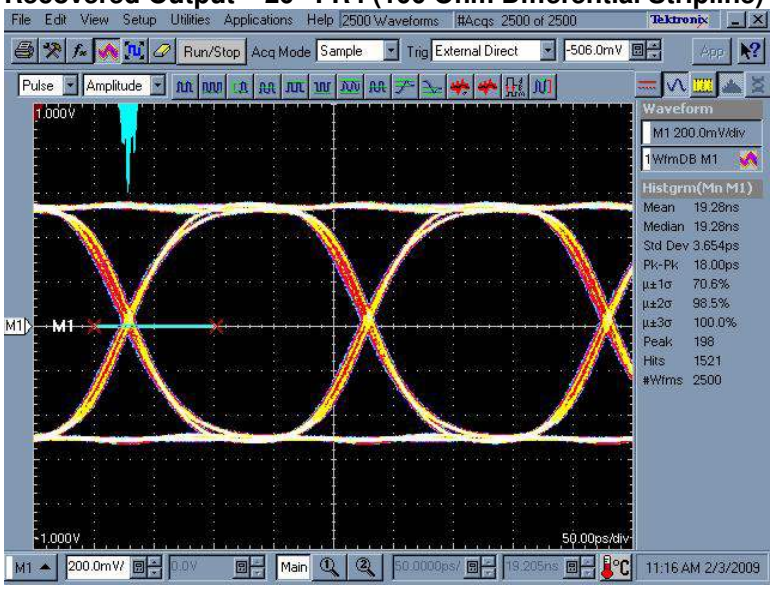
DS50PCI401 Equalization Performance at 5.0 Gbps:

Recovered Output – 10” FR4 (100 Ohm Differential Stripline)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = 11 (4 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

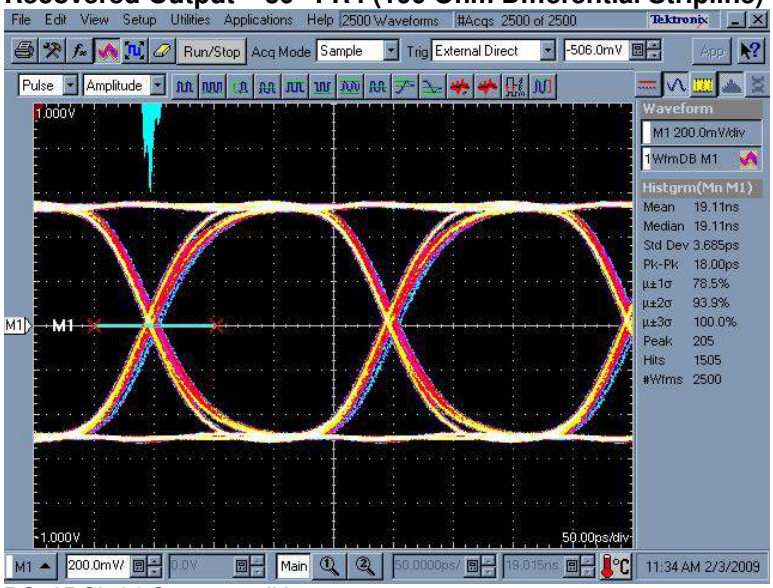
Recovered Output – 20” FR4 (100 Ohm Differential Stripline)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = F0 (11.4 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

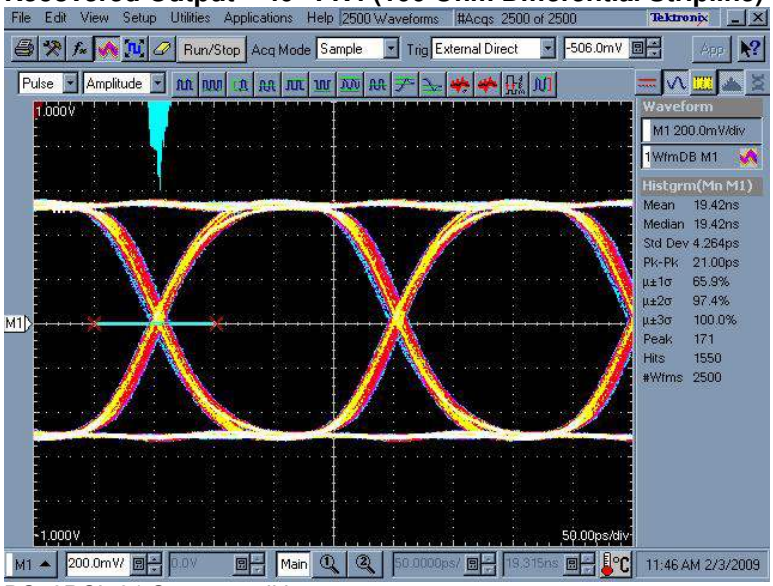
DS50PCI401 Equalization Performance at 5.0 Gbps:

Recovered Output – 30” FR4 (100 Ohm Differential Stripline)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = 10 (15.5 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

Recovered Output – 40” FR4 (100 Ohm Differential Stripline)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = F1 (17.0 dB at 2.5 GHz)
DEM[1:0] = 00 (0 dB with VOD = 1.0 Vp-p)

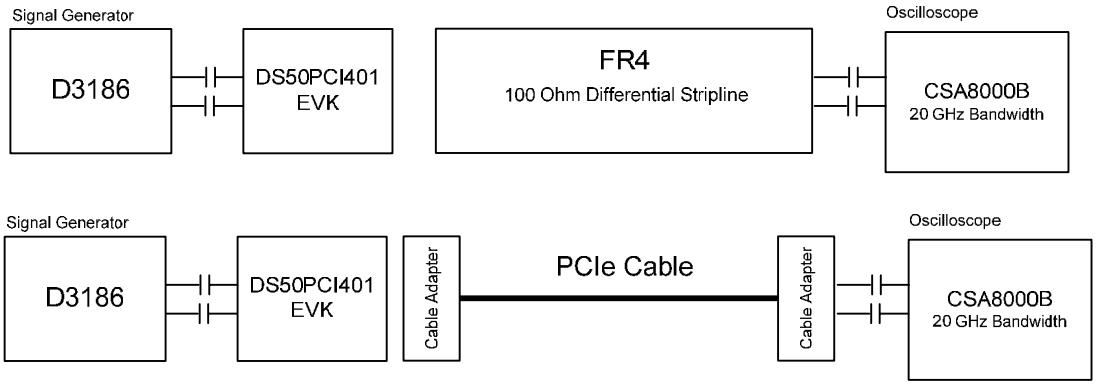
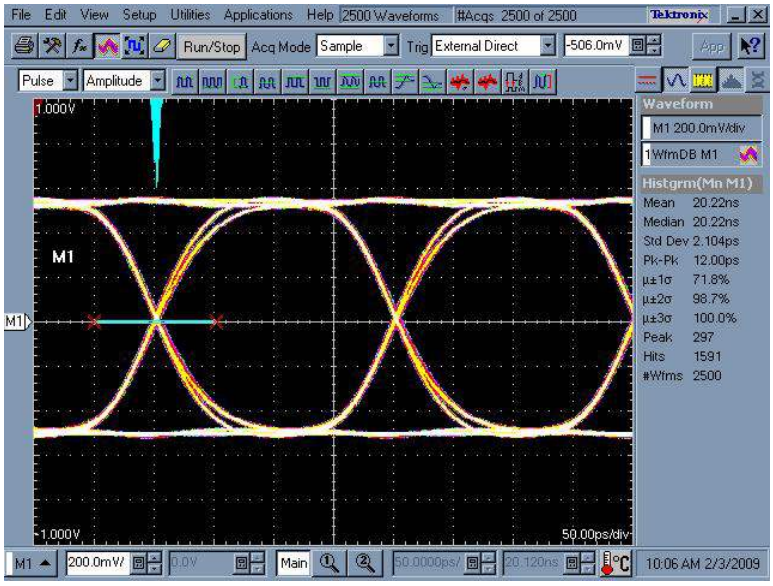


Figure 4. DS50PCI401EVK De-Emphasis Test Setup

Typical Results:

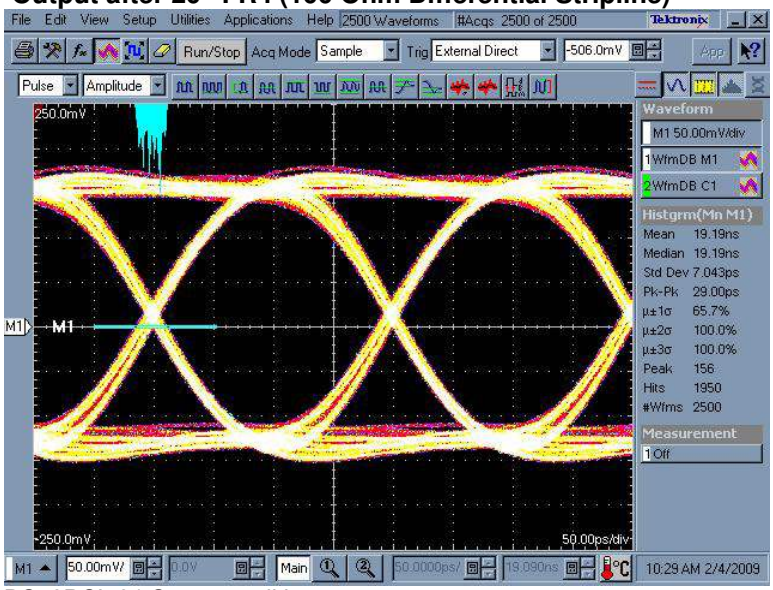
DS50PCI401 Device Performance with 3" EVK trace at 5.0 Gbps: OUTPUT (EVK Trace Only)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = FF (Bypass or Off)
DEM[1:0] = 00 (-0 dB with VOD = 1.0 Vp-p)

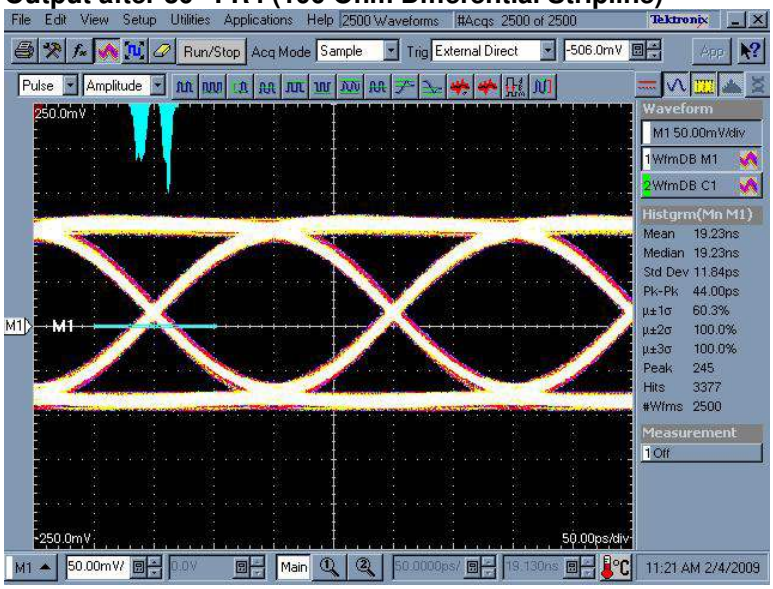
DS50PCI401 De-Emphasis Performance at 5.0 Gbps:

Output after 20” FR4 (100 Ohm Differential Stripline)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = FF (Bypass or Off)
DEM[1:0] = 11 (-6 dB enhanced)

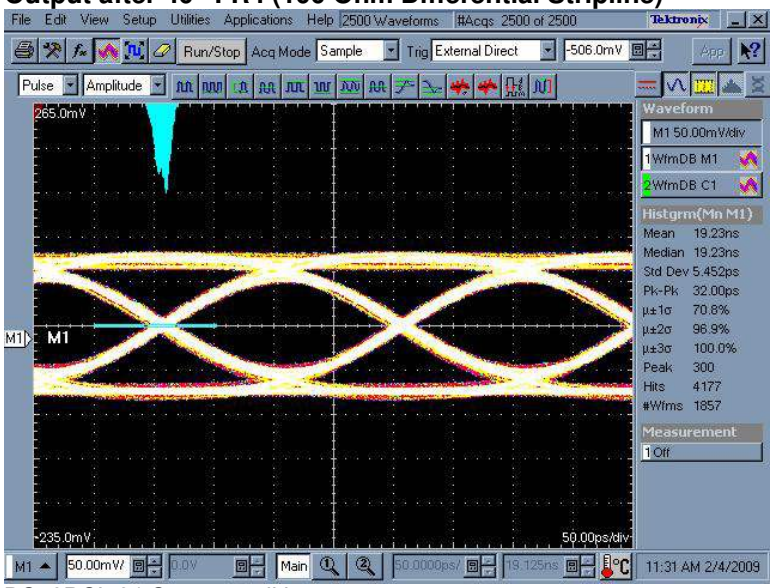
Output after 30” FR4 (100 Ohm Differential Stripline)



DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = FF (Bypass or Off)
DEM[1:0] = 0F (-9 dB enhanced)

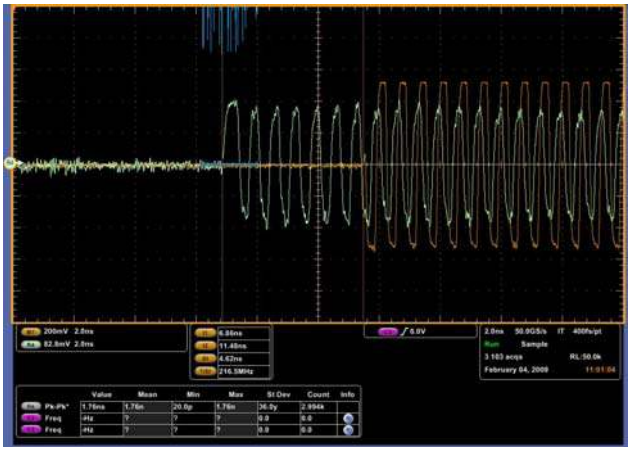
DS50PCI401 De-Emphasis Performance at 5.0 Gbps:

Output after 40” FR4 (100 Ohm Differential Stripline)

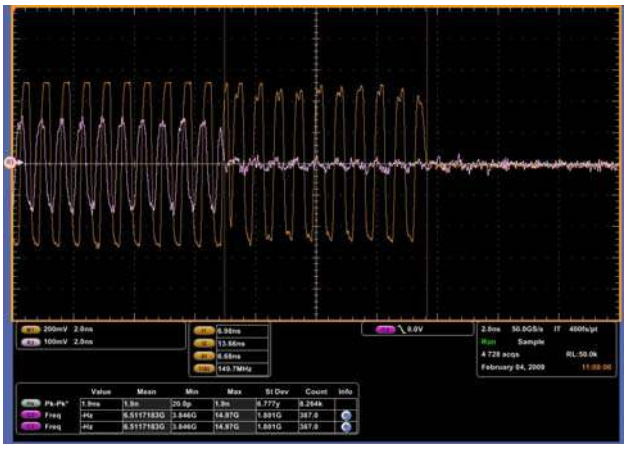


DS50PCI401 Setup condition:
Input Data: PRBS7
EQ[1:0] = FF (Bypass or Off)
DEM[1:0] = 1F (-12 dB enhanced)

Scope plots of Active - Idle through the DS50PCI401:

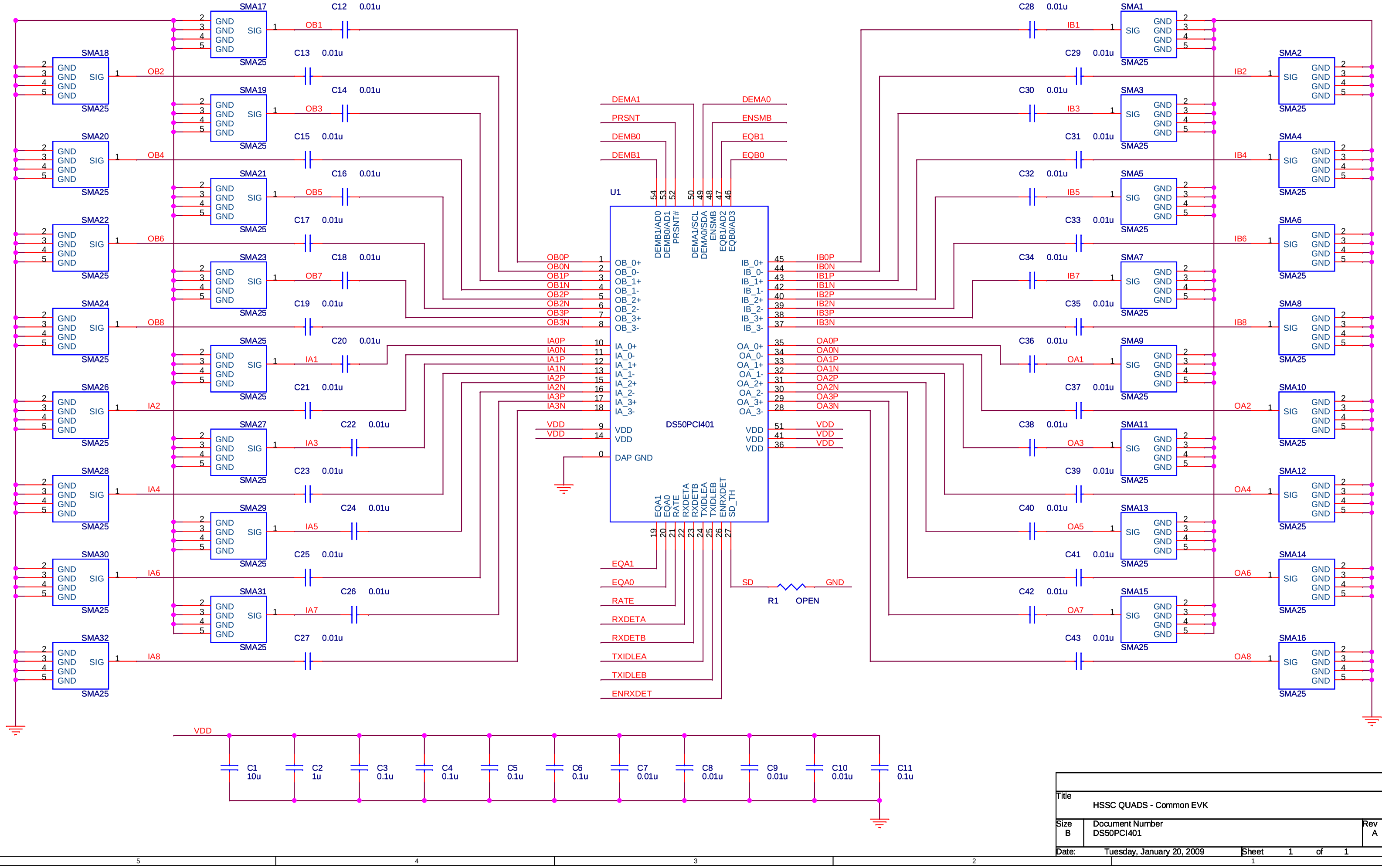


Idle to Active Response Time: ~ 4.6 ns



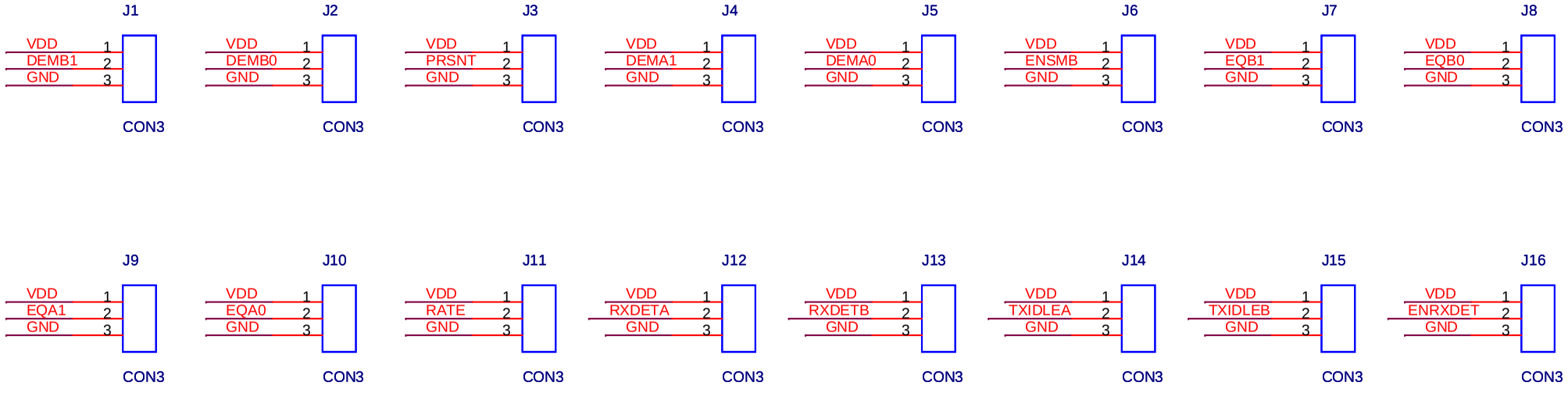
Active to Idle Response Time: ~ 6.7 ns

Figure 5. DS50PCI401EVK Active – Idle Response

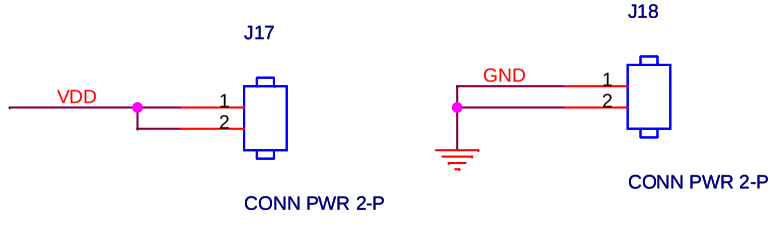


Title	HSSC QUADS - Common EVK	
Size B	Document Number DS50PCI401	Rev A
Date: Tuesday, January 20, 2009	Sheet 1 of 1	

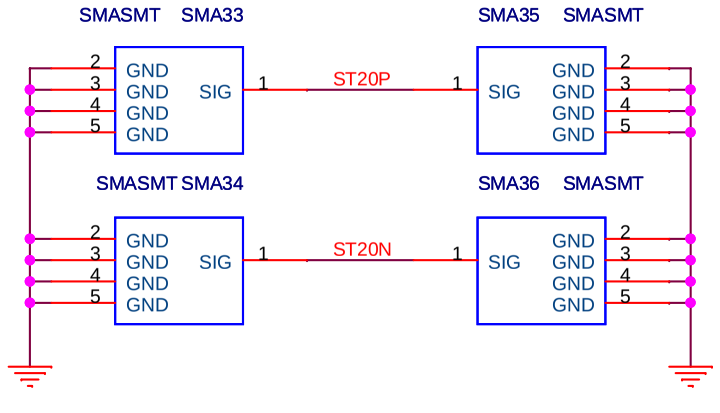
CONNECTOR	DS50PCI401	DS64BR401
J1	DEMB1	DEMB1
J2	DEMB0	DEMB0
J3	PRSNT	PWDN
J4	DEMA1	DEMA1
J5	DEMA0	DEMA0
J6	ENSMB	ENSMB
J7	EQB1	EQB1
J8	EQB0	EQB0
J9	EQA1	EQA1
J10	EQA0	EQA0
J11	RATE	RATE
J12	RXDETA	VOD0
J13	RXDETB	VOD1
J14	TXIDLEA	TXIDLEA
J15	TXIDLEB	TXIDLEB
J16	ENRXDET	NC



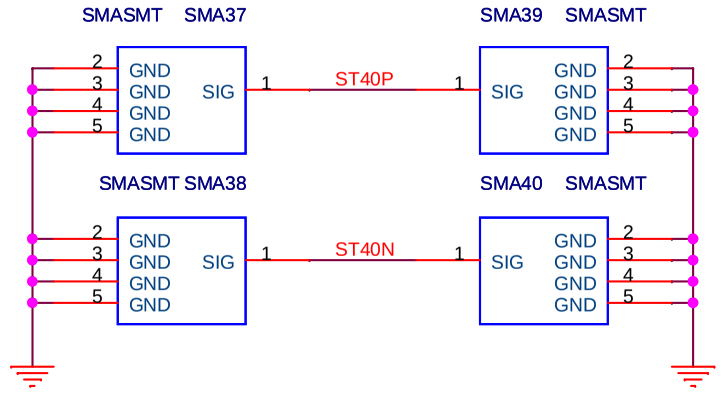
NOTE: Connector signal net names reference the DS50PCI401 design, but connections are common to all 4 EVK designs.



20" STRIPLINE TRACE



40" STRIPLINE TRACE



Title: HSSC QUADS - Common EVK			
Size: B	Document Number: COMMON		Rev: A
Date: Wednesday, February 11, 2009	Sheet 1 of 1		

Bill of Materials:

DS50PCI401EVK Interface Applications Rev. A
Bill of Materials
February 26, 2009

Item	Quantity	Reference	Part	Source
1	1	C1	10u	PCC2420CT-ND
2	1	C2	1u	PCC2257CT-ND
3	5	C3, C4, C5, C6, C11	0.1u	PCC13490CT-ND
4	4	C7, C8, C9, C10	0.01u	PCC2270CT-ND
5	16	J1, J2, J3, J4, J5, J6, J7, J8, J9 J10, J11, J12, J13, J14, J15, J16	CON3	WM6103-ND
6	2	J17, J18	CON2P	Keystone 1287-ST
7	32	SMA1, SMA2, SMA3, SMA4, SMA5, SMA6, SMA7, SMA8, SMA9, SMA10, SMA11, SMA12, SMA13, SMA14, SMA15, SMA16, SMA17, SMA18, SMA19, SMA20, SMA21, SMA22, SMA23, SMA24, SMA25, SMA26, SMA27, SMA28, SMA29, SMA30, SMA31, SMA32	SMA25	142-0701-821
8	8	SMA33, SMA34, SMA35, SMA36, SMA37, SMA38, SMA39, SMA40	SMASMT	142-0711-201
9	1	U1	DS50PCI401	NSC
10	1	R1	Do Not Stuff	
11	32	C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43	Do Not Stuff	

FAB/Manufacture Information:

The major fabrication highlights are listed below.

1. Utilize Nelco N4000-13EP for high speed signals.
2. Optimized SMA launch structure for Johnson edge launch connector.
3. Utilize a coplanar waveguide structure for reduced loss and enhanced metal coverage.

Material: Nelco N4000-13EP – ROHS compliant

Layer Stack Up:
1/2 oz. ---------- TOP
5.8 mils (Nelco)
1/2 oz. ----------GND
10 mils
1/2 oz. ---------- SIG
8 mils
1/2 oz. ----------GND
3 mils
1/2 oz. ----------VDD
8 mils
1/2 oz. ---------- SIG
10 mils
1/2 oz. ----------GND – Back Drill past this layer
5.8 mils
1/2 oz. ---------- BOT

Overall Thickness: 0.062” ± 0.004”
Adjust metal thickness on inner plane layers to meet overall thickness

Transmission Line Characteristics:

The TOP layer 50-ohm signals will be based on Figures 6 and 7 below. This shows a microstrip with a Width = 11 mil, Dielectric Height = 5.8 mil, Final Copper Thickness = 2.4 mil, and a Dielectric Constant = 3.2. The TOP layer 100-ohm signals will be based on Figure 8 on the following page. This shows an edge coupled differential microstrip with a Width = 7 mil, Dielectric Height = 5.8 mil, Finished Copper Thickness = 2.4 mil, Spacing = 8 mil, and a Dielectric Constant = 3.2.

Impedance Geometries:

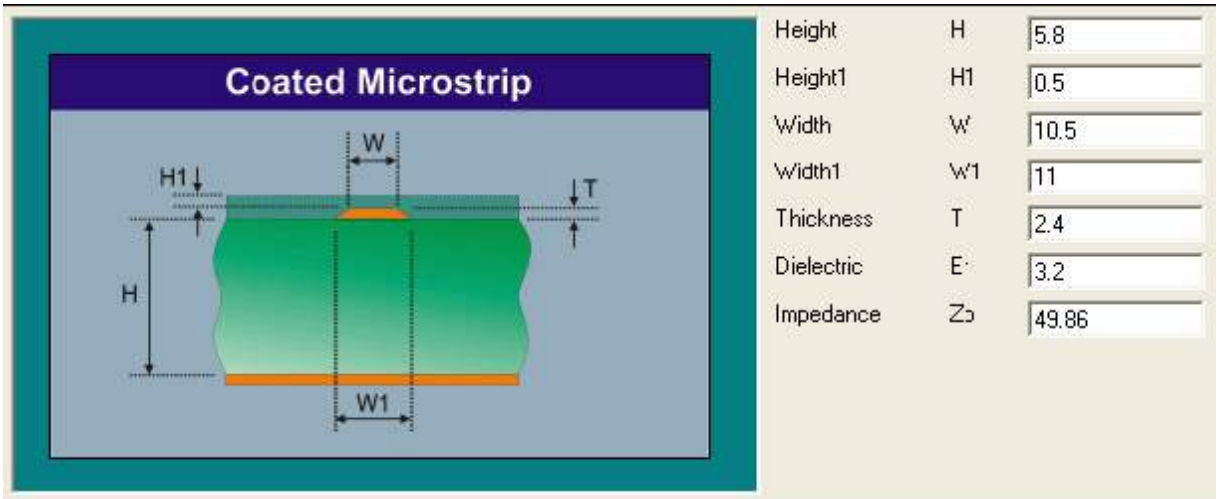


Figure 6. DS50PCI401EVK 50 Ohm Microstrip

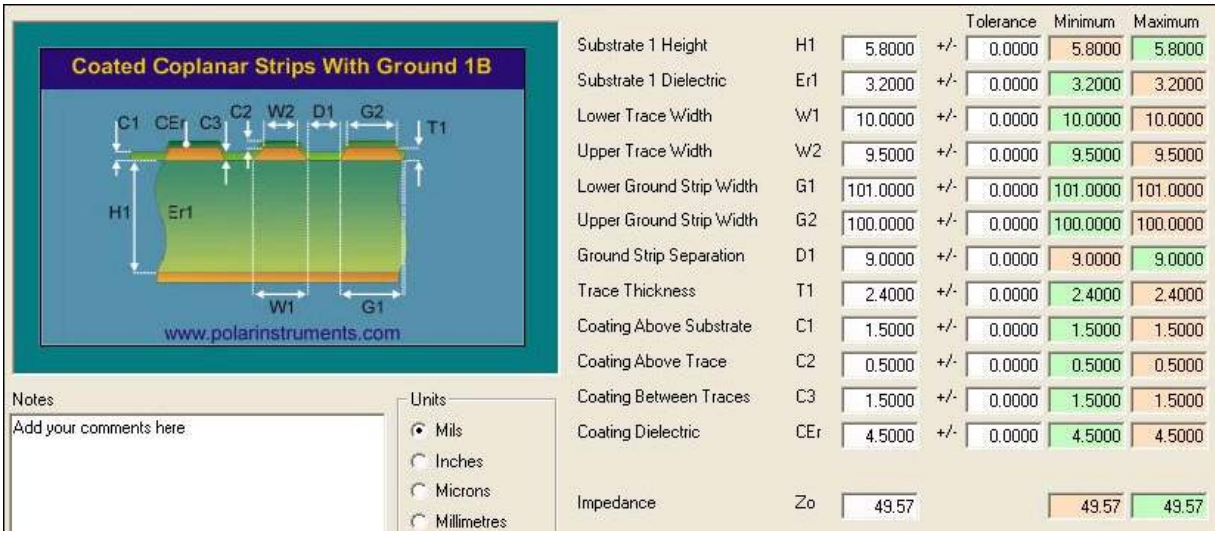


Figure 7. DS50PCI401EVK 50 Ohm Waveguide

Figure 8. DS50PCI401EVK 100 Ohm Differential Microstrip

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