

74HC125; 74HCT125

Quad buffer/line driver; 3-state

Rev. 7 — 4 February 2021

Product data sheet

1. General description

The 74HC125; 74HCT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($n\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - The 74HC125: CMOS levels
 - The 74HCT125: TTL levels
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|---------|---|----------|
| | Temperature range | Name | Description | Version |
| 74HC125D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HCT125D | | | | |
| 74HC125PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74HCT125PW | | | | |

4. Functional diagram

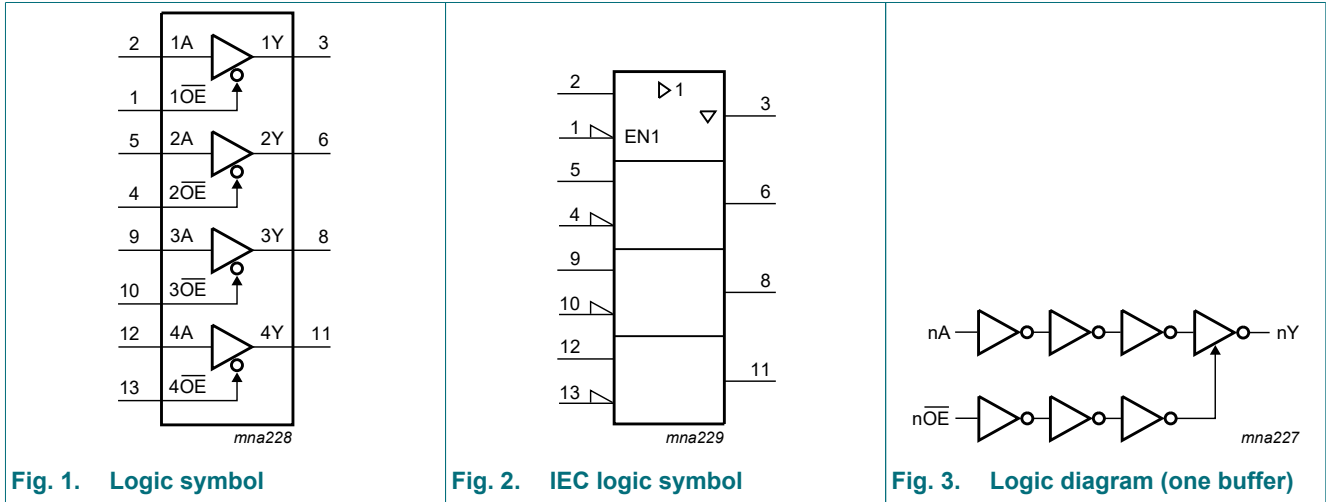


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one buffer)

5. Pinning information

5.1. Pinning

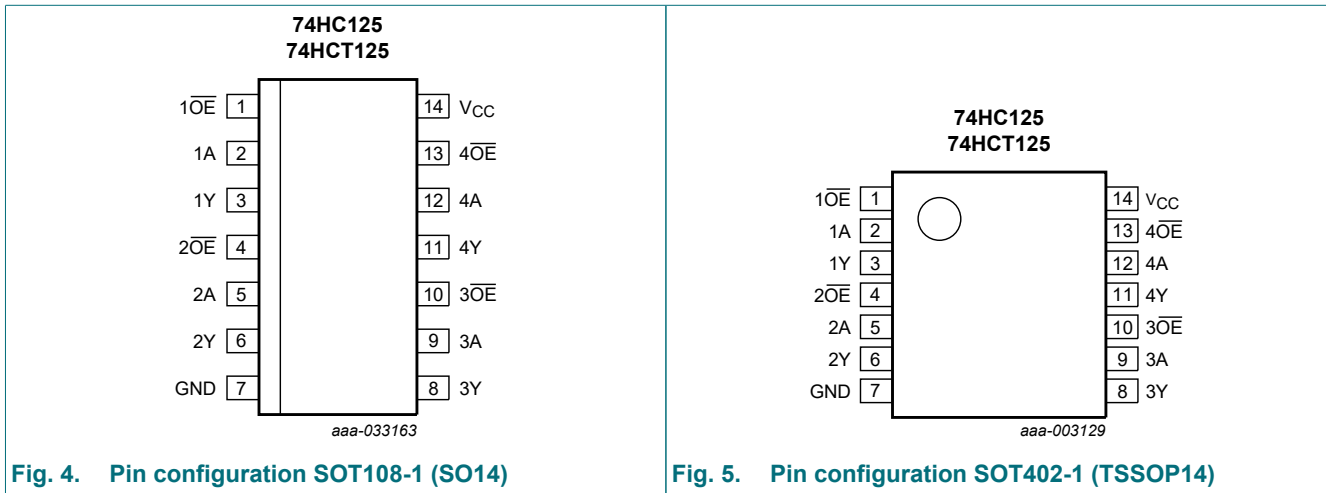


Fig. 4. Pin configuration SOT108-1 (SO14)

Fig. 5. Pin configuration SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------|--------------|----------------------------------|
| 1OE, 2OE, 3OE, 4OE | 1, 4, 10, 13 | output enable input (active LOW) |
| 1A, 2A, 3A, 4A | 2, 5, 9, 12 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| VCC | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Control | Input | Output |
|---------|-------|--------|
| nOE | nA | nY |
| L | L | L |
| | H | H |
| H | X | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_O | output current | $V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$ | - | ± 35 | mA |
| I_{CC} | supply current | | - | +70 | mA |
| I_{GND} | ground current | | - | -70 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC125 | | | 74HCT125 | | | Unit |
|---------------------|-------------------------------------|-------------------------|---------|------|----------|----------|------|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---------------------------|--|-------|------|------|------------------|------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC125 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| I _O = -7.8 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V | | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _O = 7.8 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V | | |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.5 | - | ±5.0 | - | ±10.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT125 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -6 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 6.0 mA | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | µA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND | - | - | ±0.5 | - | ±5.0 | - | ±10 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | - | 100 | 360 | - | 450 | - | 490 | µA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 8.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC125 | | | | | | | | | | |
| t_{pd} | propagation delay | nA to nY; see Fig. 6 [1] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 30 | 100 | - | 125 | - | 150 | ns |
| | | $V_{CC} = 4.5$ V | - | 11 | 20 | - | 25 | - | 30 | ns |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 9 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V | - | 9 | 17 | - | 21 | - | 26 | ns |
| t_{en} | enable time | nOE to nY; see Fig. 7 [2] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 41 | 125 | - | 155 | - | 190 | ns |
| | | $V_{CC} = 4.5$ V | - | 15 | 25 | - | 31 | - | 38 | ns |
| | | $V_{CC} = 6.0$ V | - | 12 | 21 | - | 26 | - | 32 | ns |
| t_{dis} | disable time | nOE to nY; see Fig. 7 [3] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 41 | 125 | - | 155 | - | 190 | ns |
| | | $V_{CC} = 4.5$ V | - | 15 | 25 | - | 31 | - | 38 | ns |
| | | $V_{CC} = 6.0$ V | - | 12 | 21 | - | 26 | - | 32 | ns |
| t_t | transition time | nY; see Fig. 6 [4] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 14 | 60 | - | 75 | - | 90 | ns |
| | | $V_{CC} = 4.5$ V | - | 5 | 12 | - | 15 | - | 18 | ns |
| | | $V_{CC} = 6.0$ V | - | 4 | 10 | - | 13 | - | 15 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ [5] | - | 22 | - | - | - | - | - | pF |
| 74HCT125 | | | | | | | | | | |
| t_{pd} | propagation delay | nA to nY; see Fig. 6 [1] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 15 | 25 | - | 31 | - | 38 | ns |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 12 | - | - | - | - | - | ns |
| t_{en} | enable time | nOE to nY; see Fig. 7 [2] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 15 | 28 | - | 35 | - | 42 | ns |
| t_{dis} | disable time | nOE to nY; see Fig. 7 [3] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 15 | 25 | - | 31 | - | 38 | ns |
| t_t | transition time | nY; see Fig. 6 [4] | - | 5 | 12 | - | 15 | - | 18 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC} - 1.5$ V [5] | - | 24 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_{en} is the same as t_{PZH} and t_{PZL} .

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[4] t_t is the same as t_{THL} and t_{TLH} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

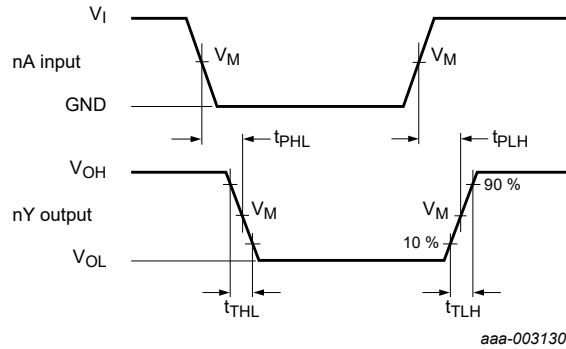
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

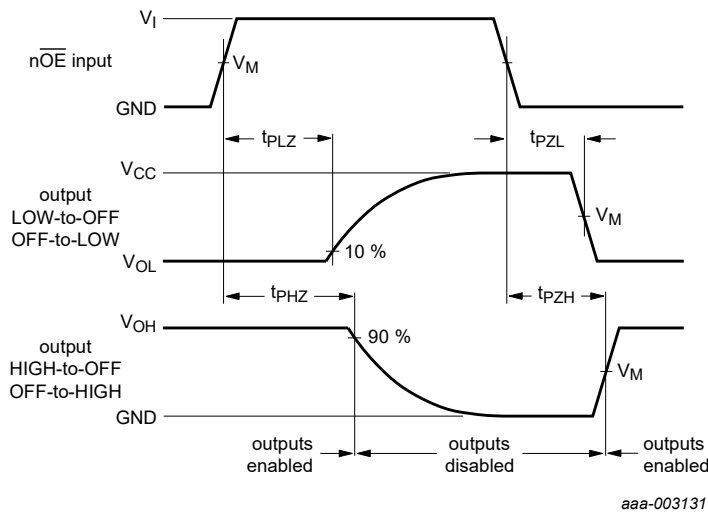
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Propagation delay input (nA) to output (nY)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Enable and disable times

Table 8. Measurement points

| Type | Input | Output |
|----------|-------------|-------------|
| | V_M | V_M |
| 74HC125 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT125 | 1.3 V | 1.3 V |

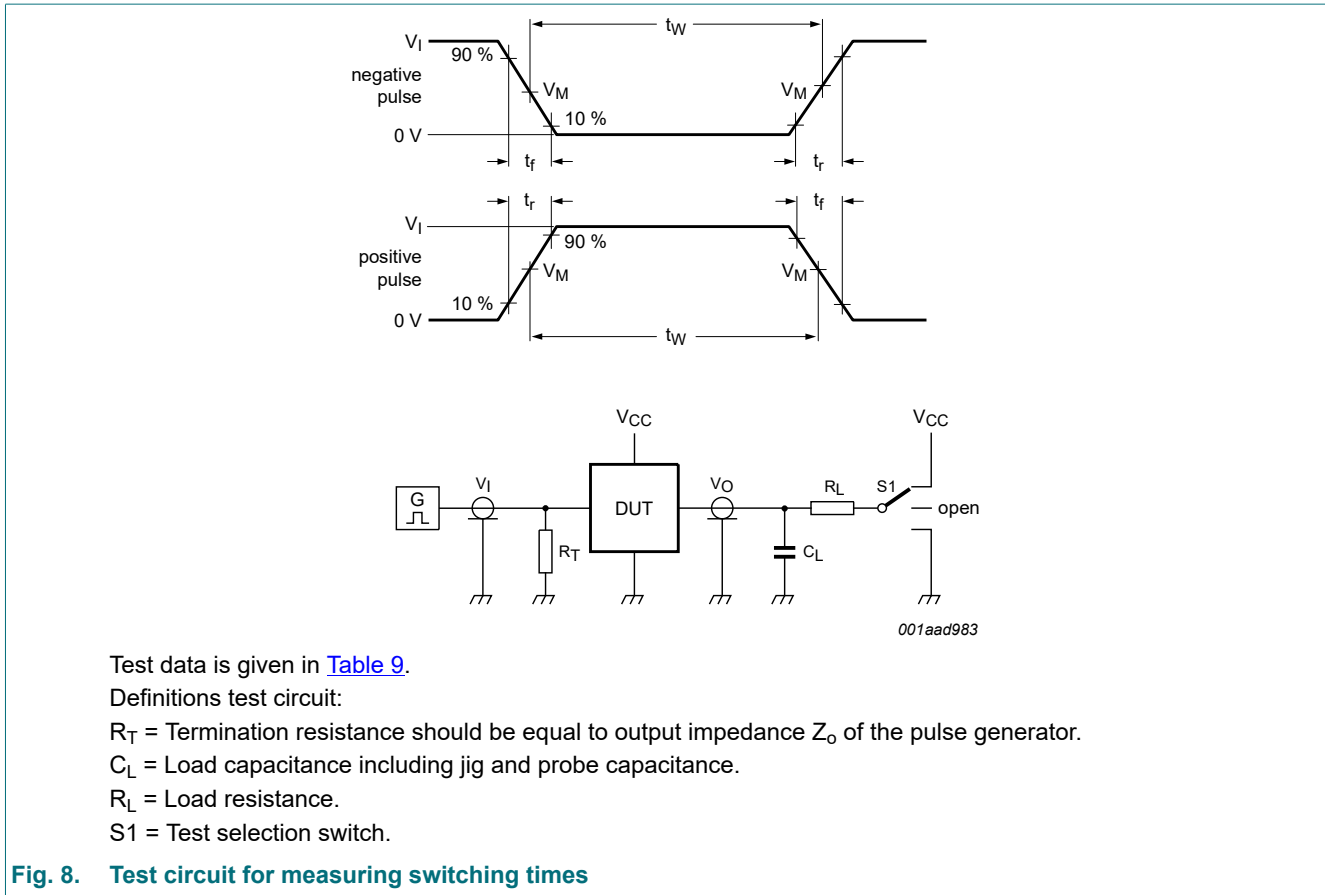


Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC125 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT125 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

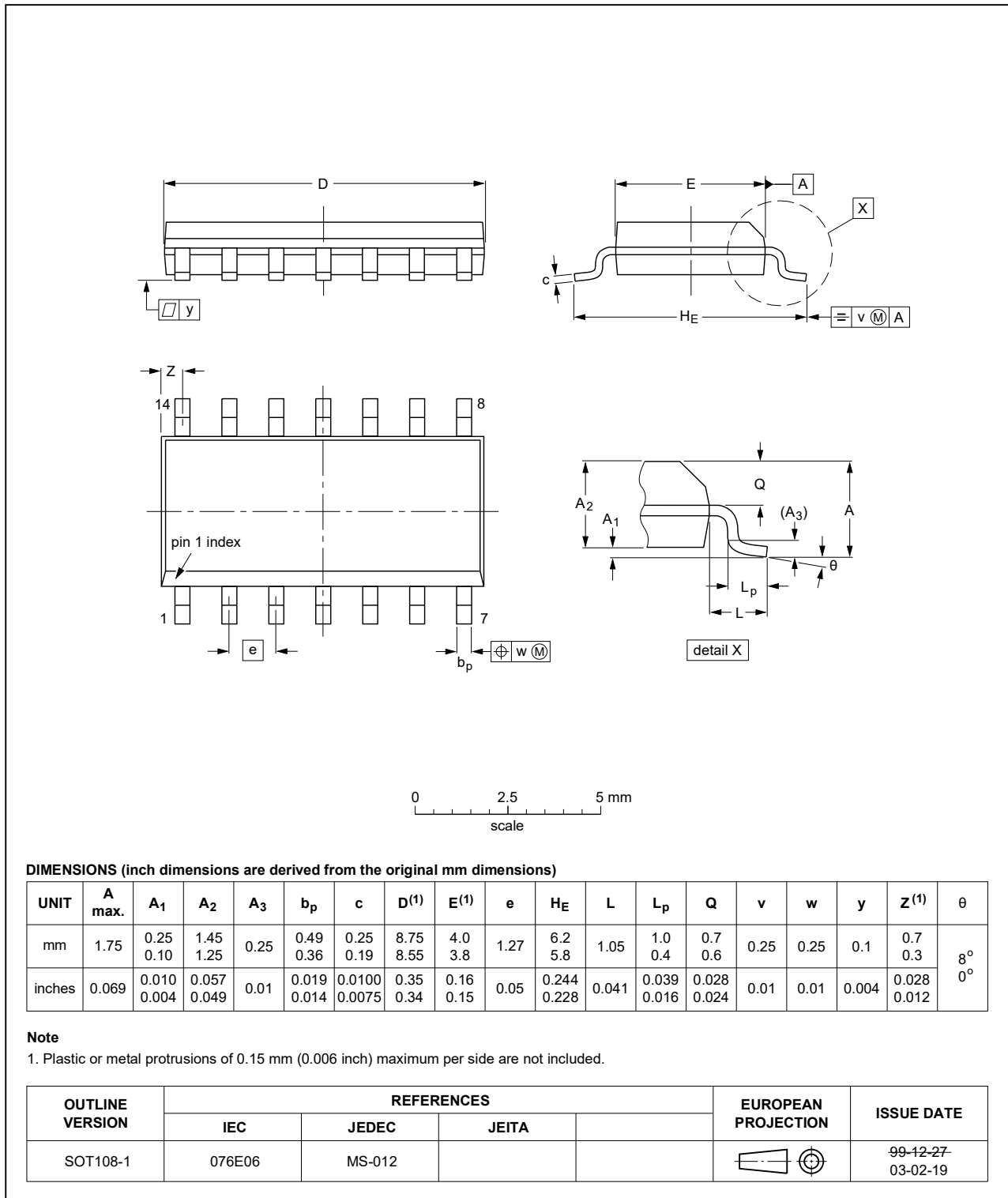


Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

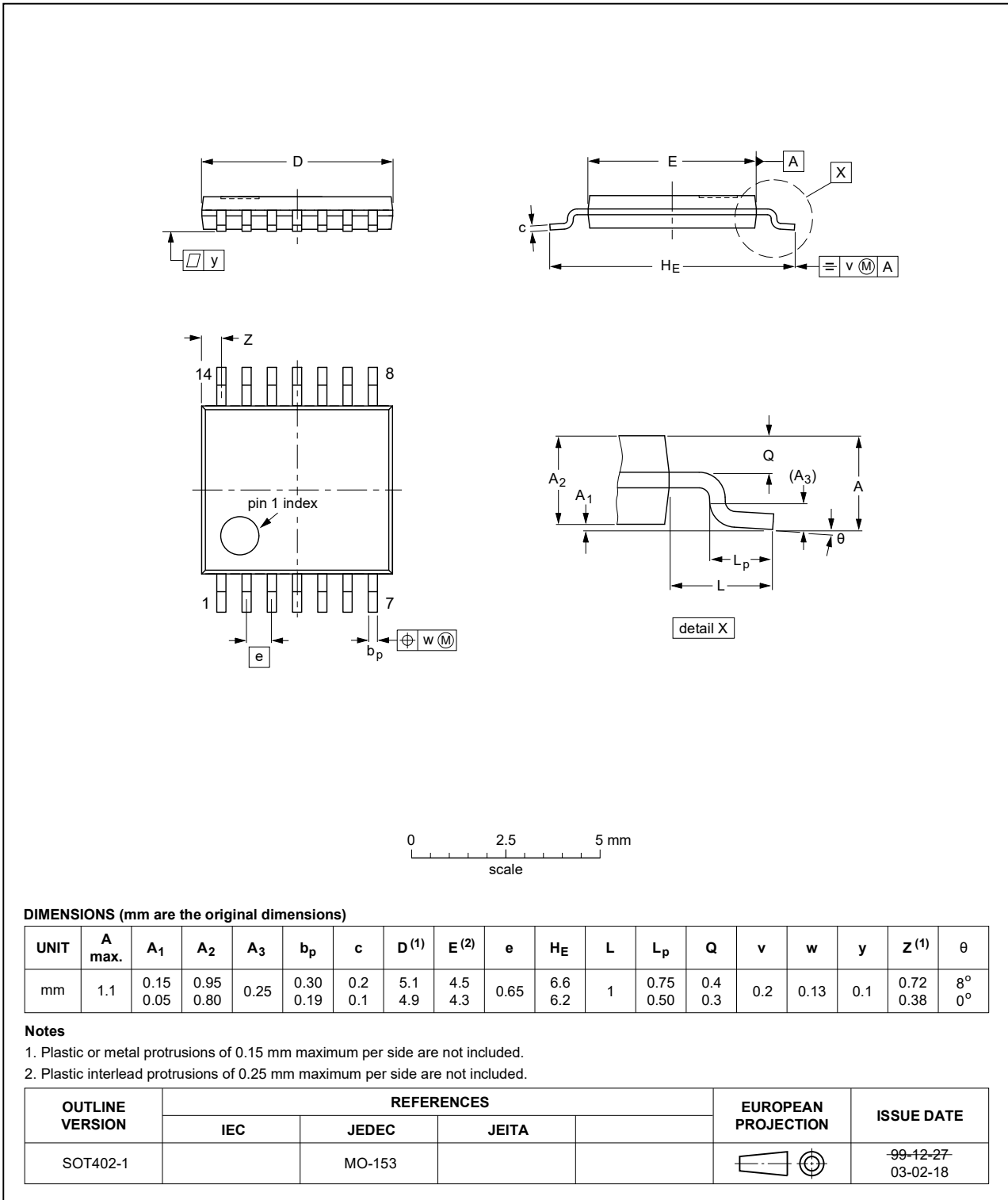


Fig. 10. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--|--------------------|---------------|---------------------|
| 74HC_HCT125 v.7 | 20210204 | Product data sheet | - | 74HC_HCT125 v.6 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HC125DB and 74HCT125DB (SOT337-1 / SSOP14) removed. Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. | | | |
| 74HC_HCT125 v.6 | 20151201 | Product data sheet | - | 74HC_HCT125 v.5 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC125N and 74HCT125N (SOT27-1) removed. | | | |
| 74HC_HCT125 v.5 | 20150119 | Product data sheet | - | 74HC_HCT125 v.4 |
| Modifications: | <ul style="list-style-type: none"> Table 7: Power dissipation capacitance condition for 74HCT125 is corrected. | | | |
| 74HC_HCT125 v.4 | 20130110 | Product data sheet | - | 74HC_HCT125 v.3 |
| Modifications: | <ul style="list-style-type: none"> New general description. | | | |
| 74HC_HCT125 v.3 | 20120827 | Product data sheet | - | 74HC_HCT125_CNV v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT125_CNV v.2 | 19970827 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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