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K22F Family Product Brief

Supports 120/100MHz devices with 128KB to 512KB Embedded Flash

Contents

1 K22F Family Introduction

The K22F microcontrollers are based on the ARM® Cortex™-M4 core and are the second generation of devices within the Kinetis K2x family, offering lower power and higher memory densities in smaller packages than before. The K22F devices have 100 MHz and 120 MHz performance options with an integrated single-precision floating-point unit. Embedded flash memory sizes range from 128 KB to 1 MB. Packages include 64-pin up to 144-pin LQFP and BGA options.

This product brief describes the K22F devices from 128 KB to 512 KB package options, from 64-pin up to 121-pin. For further information on other K2x family products, see www.freescale.com/kinetis.

2 Block Diagram

The following figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

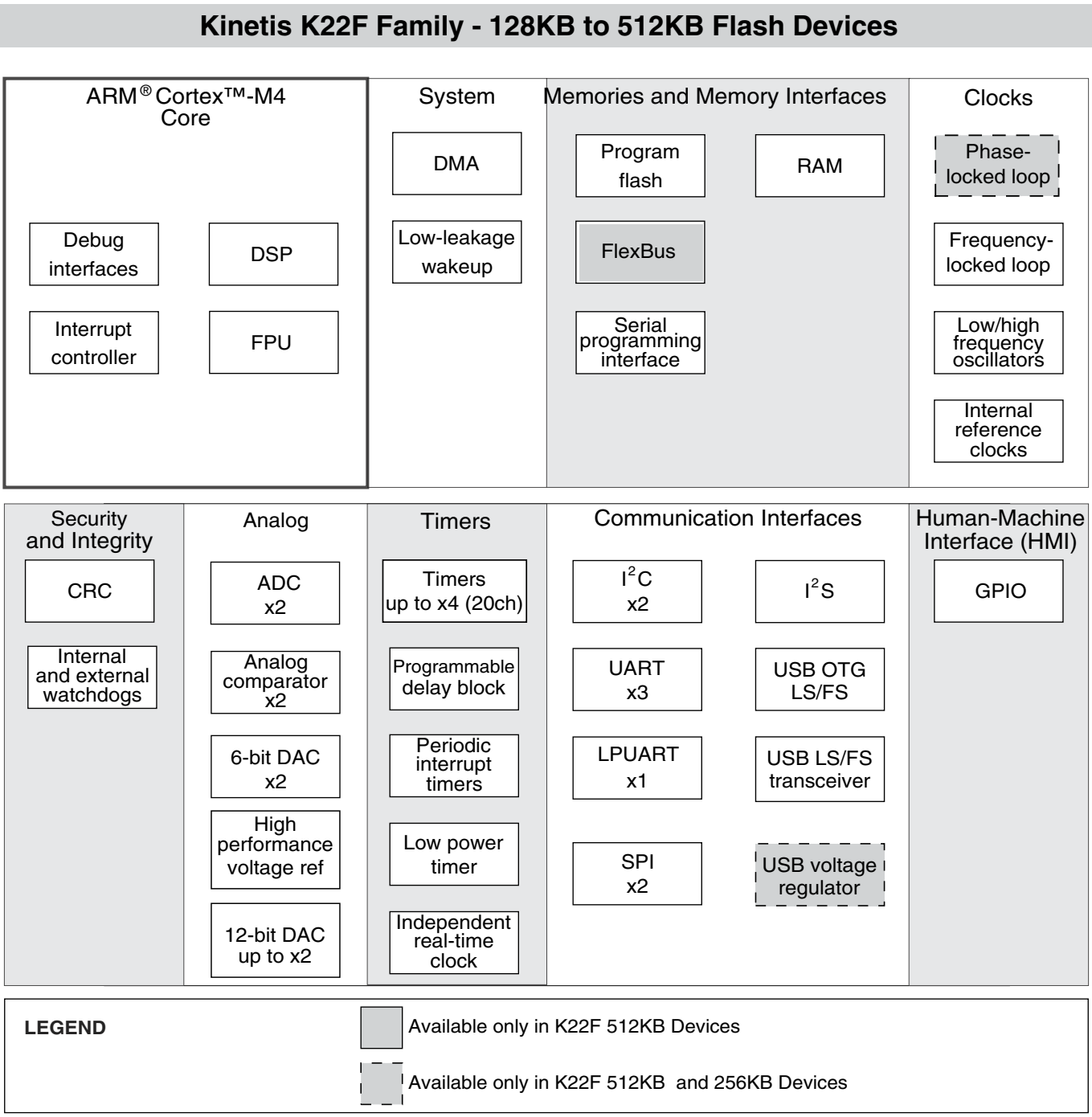

Figure 1. K22F Block Diagram

3 Features

3.1 K22F High-Level Feature Comparison

Table 1. K22F - 120MHz / 100MHz devices (128K to 512K)

Flash Memory	512KB	256KB	128KB
CPU Frequency	120MHz	120MHz	100MHz
Total SRAM	128KB	48KB	24KB
FlexBus	√	—	—
DMA	16-ch	16-ch	4-ch
USB Vreg	√	√	—
PLL	√	√	—
FlexTimers	2x8ch; 2x2ch	1x8ch; 2x2ch	1x8ch; 2x2ch
DAC	2x12-bit	1x12-bit	1x12-bit
I/Os w/ dig. Filter	16	8	8
121-BGA	√	√	√
100-LQFP	√	√	√
64-BGA[1]	—	√	√
64LQFP	√	√	√

1. This package offering is subject to removal.

3.2 K22F 128KB to 512KB Common Features

Table 2. K22F 128KB to 512KB Common Features

K22F Common Features			
Core/System Modules		**Timers Modules**	
CPU / Frequency	Cortex-M4	Motor Control/General purpose/PWM	up to 2x 8-ch[1]
DMA	up to 16-ch	Quad decoder/General purpose/PWM	2x 2-ch
Floating Point Unit	Single Precision	FTM External Clock	2
Debug	JTAG, SWD	Independent RTC (Vbat)	Yes
Trace	TPIU, FPB, DWT, ITM	Low Power Timer	1
Memory and Memory Interface		PDB	Yes
Flash Memory	up to 512KB	PIT	4-ch
Total SRAM	up to 128KB	**Communication Interfaces**	
Serial Programming Interface	Yes	UART	3 (1x w/ ISO7816 and High Baud rate)

Table continues on the next page...

Table 2. K22F 128KB to 512KB Common Features (continued)

K22F Common Features					
Clock Modules			DSPI	2
RTC Clock Out	Yes		I2C	2
MCG	Yes (FLL)		I2S	1
IRC	48MHz		LPUART	1
Internal Oscillators	32kHz / 4MHz		USB OTG LS/FS w/on chip PHY[2]	1
OSC	32-40kHz / 3-32MHz		USB Vreg	Optional (120mA)
RTC OSC	32KHz		**Human Machine Interface**	
Security and Integrity			GPIO (w/interrupts)	up to 81
Software Watchdog	Yes		NMI	Yes
Hardware Watchdog	Yes		**Operating Characteristics**	
CRC	Yes		Voltage Range	1.71-3.6V
Analog Modules			Temperature Range	-40-105ºC
ADC	2x 16-bit ADC			
12-bit DAC	up to 2			
Analog Comparators	2			
High precision voltage reference	1			

1. For the 256KB and 128KB flash devices: 1x 8-ch
2. Host function not supported in the 128 K flash-device 64-pin package.

3.3 K22F 128KB to 512KB of Flash Feature Differences Per Package

Table 3. K22F Differences

Feature	121XFBGA (DC)	100LQFP (LL)	64MAPBGA (MP)[1]	64LQFP (LH)
Memory Interface (Only in 512K Flash devices)				
External Bus Interface (FlexBus) (Addr/Data/CS)	32/32/6	21/16/5	—	18/16/2
Non-Muxed External Bus Interface (Flexbus) (Addr/Data/CS)	25/16/6; 25/8/6	21/16/5	—	—
Clock Modules				
RTC Wake-up	Yes[2]	No	No	No
Analog Modules				
ADC0 (SE:single-ended, DP:differential pair)	21ch SE + 4ch DP[3]	19ch SE + 4ch DP	14ch SE + 2ch DP	14ch SE + 2ch DP

Table continues on the next page...

Table 3. K22F Differences (continued)

Feature	121XFBGA (DC)	100LQFP (LL)	64MAPBGA (MP)[1]	64LQFP (LH)
ADC1 (SE:single-ended, DP:differential pair)	23ch SE + 3ch DP[4]	19ch SE + 3ch DP	12ch SE + 2ch DP	12ch SE + 2ch DP
Total ADC DP inputs	4	4	2	2
Total ADC SE inputs	38[5]	33	22	22
Analog Comparators Inputs (CMP0 / CMP1)	6 / 5[6]	5 / 4	5 / 4	5 / 4
Communication Interfaces				
DSPI chip selects per module (DSPI0 / DSPI1)	6 / 4	6 / 4	5 / 2	5 / 2
USB OTG LS/FS	yes	yes	yes[7]	yes[7]
Human Machine Interface				
GPIO (w/interrupts)	81[8]	66	40	40

1. 64MAPBGA package not available in the 512 KB device. Only available for 256 KB and 128 KB flash devices. This package offering is subject to removal.
2. Excluding the 128KB flash devices
3. For 256KB and 128KB flash devices: 19ch SE + 4ch DP
4. For 256KB flash devices: 22ch SE + 3ch DP. For 128KB flash devices: 20ch SE + 3ch DP.
5. For 256KB flash devices: 36. For 128KB flash devices: 34.
6. For 256KB and 128KB flash devices: 6 / 4.
7. USB device-only in the 128 KB flash devices
8. For 256KB flash devices: 70. For 128KB flash devices: 67.

3.4 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document. See the Part identification section for details on the part number format.

Table 4. K22F 128KB to 512KB orderable part numbers summary

Part number	CPU frequency	Pin count	Package	Flash	SRAM	DMA	GPIO	GPIO w/ digital filter
MK22FN512VDC12	120 MHz	121	BGA	512 KB	128 KB	16 ch	81	16
MK22FN512VLL12	120 MHz	100	LQFP	512 KB	128 KB	16 ch	66	8
MK22FN512VLH12	120 MHz	64	LQFP	512 KB	128 KB	16 ch	40	8
MK22FN256VDC12	120 MHz	121	BGA	256 KB	48 KB	16 ch	70	8
MK22FN256VLL12	120 MHz	100	LQFP	256 KB	48 KB	16 ch	66	8
MK22FN256VMP12[1]	120 MHz	64	BGA	256 KB	48 KB	16 ch	40	8
MK22FN256VLH12	120 MHz	64	LQFP	256 KB	48 KB	16 ch	40	8
MK22FN128VDC10	100 MHz	121	BGA	128 KB	24 KB	4 ch	67	8
MK22FN128VLL10	100 MHz	100	LQFP	128 KB	24 KB	4 ch	66	8
MK22FN128VMP10[1]	100 MHz	64	BGA	128 KB	24 KB	4 ch	40	8
MK22FN128VLH10	100 MHz	64	LQFP	128 KB	24 KB	4 ch	40	8

1. This package offering is subject to removal.

3.5 Feature highlights

3.5.1 Power Modes Description

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For Run and VLPR mode there is a corresponding wait and stop mode. Wait modes are similar to ARM® sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

Stop mode entry is not supported directly from HSRUN and requires transition to Run prior to an attempt to enter a stop mode.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 5. Chip power modes

Chip mode	Description	Core mode	Normal recovery method
Normal run	Default mode out of reset; on-chip voltage regulator is on.	Run	-
High Speed run	Allows maximum performance of chip. In this state, the MCU is able to operate at a faster frequency compared to normal run mode.	Run	-
Normal Wait - via WFI	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low Power Run)	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; internal oscillator provides a low power 4 MHz source for the core, the bus and the peripheral clocks.	Run	-
VLPW (Very Low Power Wait) -via WFI	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but LPTimer, RTC, CMP, DAC can be used. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt

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Table 5. Chip power modes (continued)

Chip mode	Description	Core mode	Normal recovery method
LLS3 (Low Leakage Stop3)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt[1]
LLS2 (Low Leakage Stop2)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. A portion of SRAM_U remains powered on (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt
VLLS3 (Very Low Leakage Stop3)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[3]
VLLS2 (Very Low Leakage Stop2)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_L is powered off. A portion of SRAM_U remains powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[3]
VLLS1 (Very Low Leakage Stop1)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 32-byteVBAT register file remain powered for customer-critical data.	Sleep Deep	Wakeup Reset[3]
VLLS0 (Very Low Leakage Stop 0)	Most peripherals are disabled (with clocks stopped), but LLWU and RTC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 32-byte VBAT register file remain powered for customer-critical data. The POR detect circuit can be optionally powered off.	Sleep Deep	Wakeup Reset[3]
BAT (backup battery only)	The chip is powered down except for the VBAT supply. The RTC and the 32-byte VBAT register file for customer-critical data remain powered.	Off	Power-up Sequence

1. Resumes normal run mode operation by executing the LLWU interrupt service routine.
2. Resumes normal run mode operation by executing the LLWU interrupt service routine.
3. Follows the reset flow with the LLWU interrupt flag set for the NVIC.

3.5.2 Power Targets

Power consumption estimates for K22F devices from 128 KB to 512 KB embedded flash are summarized in the table below.

NOTE

This is not an exhaustive list of the MCU power modes. See the respective data sheets for further information.

Table 6. Power consumption (at 25° C)

Power mode	Description	IDD			Unit	Wake-up time
		512 KB	256 KB	128 KB		
High-Speed Run mode[1]	All peripherals off, while 1	225	200	180	µA/MHz	NA
VLPR mode[2]	Compute operation, while 1	180	145	138	µA/MHz	NA
VLPS mode		9.0	5.2	4.2	µA	6 µs
LLS3 mode		4.5	2.9	2.6	µA	6 µs
VLLS3 mode		3.0	2.0	1.8	µA	65 µs
VLLS0 mode	POR disabled	180	160	150	nA	125 µs

1. For 512 KB and 256 KB flash devices 120 MHz core and system clock, 60 MHz bus clock, and 24 MHz flash clock. For 128 KB flash device 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock.
2. 4MHz core and system clock, 4MHz bus clock, and 1MHz flash clock.

3.6 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device. See the previous section for differences among the subset devices.

3.6.1 Core modules

3.6.1.1 ARM® Cortex®-M4 Core

- Supports up to 120 MHz frequency with 1.25DMIPS/MHz
- ARM® Core based on the ARMv7 Architecture & Thumb®-2 ISA
- Microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments
- Harvard bus architecture
- 3-stage pipeline with branch speculation
- Integrated bus matrix
- Integrated Digital Signal Processor (DSP)
- Configurable nested vectored interrupt controller (NVIC)
- Advanced configurable debug component
- Single Precision Floating Point Unit (SPFPU)

3.6.1.2 Nested Vectored Interrupt Controller (NVIC)

- Close coupling with Cortex-M4 core's Harvard architecture enables low latency interrupt handling
- Up to 120 interrupt sources
- Includes a single non-maskable interrupt
- 16 levels of priority, with each interrupt source dynamically configurable
- Supports nesting of interrupts when higher priority interrupts are activated
- Relocatable vector table

3.6.1.3 Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected
- Contains no programmer's model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

3.6.1.4 Debug Controller

- Serial Wire Debug (SWD) provides an external serial-wire bidirectional debug interface
- Debug Watchpoint and Trace (DWT) with the following functionality:
  - four comparators configurable as a hardware watchpoint, a PC sampler event trigger, or a data address sampler event trigger
  - several counters or a data match event trigger for performance profiling
  - configurable to emit PC samples at defined intervals or to emit interrupt event information
- Instrumentation Trace Macrocell (ITM) with the following functionality:
  - Software trace - writes directly to ITM stimulus registers can cause packets to be emitted
  - Hardware trace - packets generated by DWT are emitted by ITM
  - Time stamping - emitted relative to packets
- Test Port Interface Unit (TPIU) acts as a bridge between ITM and an off-chip Trace Port Analyzer
- Flash Patch and Breakpoints (FPB) implements hardware breakpoints and patches code and data from code space to system space

3.6.2 System modules

3.6.2.1 Power Management Control Unit (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required
- Available wake-up from power saving modes via RTC and external inputs
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

3.6.2.2 DMA Channel Multiplexer (DMA MUX)

- Up to 16 independently selectable DMA channel routers
- 4 periodic trigger sources available
- Each channel router can be assigned to 1 of 63 possible peripheral DMA sources

3.6.2.3 DMA Controller

- Up to 16 fully programmable channels with 32-byte transfer control descriptors
- Data movement via dual-address transfers for 8-, 16-, 32-, 128-, and 256-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes
- Support for major and minor nested counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration

3.6.2.4 System Clocks

- Frequency-locked loop (FLL)
  - Digitally-controlled oscillator (DCO)
  - DCO frequency range is programmable
  - Option to program DCO frequency for a 32,768 Hz external reference clock source
  - Internal or external reference clock can be used to control the FLL
  - 0.2% resolution using 32 kHz internal reference clock
- Phase-locked loop (PLL)
  - Voltage-controlled oscillator (VCO)
  - External reference clock is used to control the PLL
  - Modulo VCO frequency divider Phase/Frequency detector
  - Integrated loop filter
- Internal reference clock generator
  - Slow clock with nine trim bits for accuracy
  - Fast clock with four trim bits
  - Can be used to control the FLL
  - Either the slow or the fast clock can be selected as the clock source for the MCU
  - Can be used as a clock source for other on-chip peripherals
- External clock from the Crystal Oscillator (XOSC)
  - Can be used to control the FLL and/or the PLL
  - Can be selected as the clock source for the MCU
- External clock monitor with reset request capability
- Lock detector with interrupt request capability for use with the PLL
- Auto Trim Machine (ATM) for trimming both the slow and fast internal reference clocks
- Multiple clock source options available for most peripherals

3.6.3 Memories and Memory Interfaces

3.6.3.1 On-Chip Memory

- Security circuitry to prevent unauthorized access to RAM and flash contents
- Flash access control to protect proprietary software

3.6.3.2 External Bus Interface (FlexBus)

- Six independent, user-programmable chip-select signals that can interface with external SRAM, PROM, EPROM, EEPROM, flash, and other peripherals
- Supports up to 2 GB addressable space
- 8-, 16- and 32-bit port sizes with configuration for multiplexed or non-multiplexed address and data buses
- Byte-, word-, longword-, and 16-byte line-sized transfers
- Programmable address-setup time with respect to the assertion of chip select
- Programmable address-hold time with respect to the negation of chip select and transfer direction

3.6.3.3 Serial Programming Interface (EzPort)

- Same serial interface as, and subset of, the command set used by industry-standard SPI flash memories
- Ability to read, erase, and program flash memory
- Reset command to boot the system after flash programming

3.6.4 Security and Integrity

3.6.4.1 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit using 16/32-bit shift register
- User Configurable 16/32 bit CRC
- Programmable Generator Polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation
- Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in lsb format

3.6.4.2 Watchdog Timer (WDOG)

- Independent, configurable clock source input
- Write-once control bits with unlock sequence
- Programmable timeout period
- Ability to test watchdog timer and reset
- Windowed refresh option
- Robust refresh mechanism
- Cumulative count of watchdog resets between power-on resets
- Configurable interrupt on timeout

3.6.4.3 External Watchdog Monitor (EWM)

- Independent 1 kHz LPO clock source
- Output signal to gate an external circuit which is controlled by CPU service or external input

3.6.5 Analog

3.6.5.1 16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
  - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two's complement 16-bit sign-extended format
  - Single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

3.6.5.2 High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Comparator output supports:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered using external sample signal or scaled peripheral clock
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes

3.6.5.3 12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotocity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode
- Choice of asynchronous or synchronous updates
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

3.6.5.4 Voltage Reference (VREF)

- Programmable trim register with 0.5mV steps, automatically loaded with room temp value upon reset
- Programmable mode selection:
  - Off
  - Bandgap out (or stabilization delay)
  - Low-power buffer mode
  - Tight-regulation buffer mode
- 1.2V output at room temperature
- Dedicated output pin

3.6.6 Timers

3.6.6.1 Programmable Delay Block (PDB)

- Up to 15 trigger input sources and software trigger source
- Up to eight configurable PDB channels for ADC hardware trigger
  - One PDB channel is associated with one ADC.
  - One trigger output for ADC hardware trigger and up to eight pre-trigger outputs for ADC trigger select per PDB channel
  - Trigger outputs can be enabled or disabled independently.
  - One 16-bit delay register per pre-trigger output
  - Optional bypass of the delay registers of the pre-trigger outputs
  - Operation in One-Shot or Continuous modes
  - Optional back-to-back mode operation, which enables the ADC conversions complete to trigger the next PDB channel
  - One programmable delay interrupt
  - One sequence error interrupt
  - One channel flag and one sequence error flag per pre-trigger
  - DMA support
- Up to eight DAC interval triggers
  - One interval trigger output per DAC
  - One 16-bit delay interval register per DAC trigger output
  - Optional bypass the delay interval trigger registers
  - Optional external triggers
- Up to eight pulse outputs (pulse-out's)
  - Pulse-out's can be enabled or disabled independently.
  - Programmable pulse width

3.6.6.2 FlexTimers (FTM)

- Selectale FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Up to 4 fault inputs for global fault control
- Configurable channel polarity

- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

3.6.6.3 Programmable Interrupt Timers (PITs)

- Up to 4 general purpose interrupt timers
- Up to 4 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- DMA support

3.6.6.4 Low Power Timer

- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock (not available in low leakage power modes)
  - Secondary external reference clock (for example, 32 kHz crystal)
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare

3.6.6.5 Real-Time Clock (RTC)

- Independent power supply, POR and 32 kHz crystal oscillator
- 32-bit seconds counter with 32-bit alarm
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires VBAT POR to enable write access
  - Soft lock requires system reset to enable write/read access

3.6.7 Communication interfaces

3.6.7.1 USB On-The-Go Module (FS/LS)

- Complies with USB specification rev 2.0
- USB host mode
  - Supports enhanced-host-controller interface (EHCI)
  - Allows direct connection of FS/LS devices without an OHCI/UHCI companion controller
  - Supported by Linux and other commercially available operating systems
- USB device mode
  - Full-speed operation via the on-chip transceiver
  - Supports one upstream facing port
  - Supports four programmable, bidirectional USB endpoints, including endpoint 0
- Suspend mode/low power

- As host, firmware can suspend individual devices or the entire USB and disable chip clocks for low-power operation
- Device supports low-power suspend
- Remote wake-up supported for host and device
- Integrated with the processor's low power modes

- Includes an on-chip full-speed (12 Mbps) and low-speed (1.5 Mbps) transceiver

3.6.7.2 USB Voltage Regulator

- 5V regulator input typically provided by USB VBUS power
- 3.3V regulated output powers on-chip USB transceiver
- Output pin from regulator can be used to power external board components and source up to 120mA
- Eliminates cost of external LDO
- 3.3V regulated output can power MCU main power supply

3.6.7.3 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8-bit or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed transfers of large amounts of data
- Support for both transmit and receive by DMA

3.6.7.4 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and *SMBus Specification Version 2* features
- Up to 400 kbps with maximum bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt or DMA driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

3.6.7.5 UART

- Support for ISO 7816 protocol for interfacing with smartcards
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format

- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Parameterizable buffer support for one dataword for each transmit and receive
- Independent FIFO structure for transmit and receive
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection

3.6.7.6 LPUART

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Address match feature in receiver to reduce address mark wake-up ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low-power modes

3.6.7.7 Synchronous Serial Interface (I^2S)

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode intended for audio support
- Master or slave mode operation
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with up to 32 time slots
- Programmable data interface modes, such as I^2S, LSB aligned, and MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- AC97 support

3.6.8 Human-machine interface

3.6.8.1 General Purpose Input/Output (GPIO)

- Progammable glitch filter and interrupt with selectable polarity on select input pins
- Hysteresis and configurable pull up/down device on all input pins
- Configurable slew rate on all output pins
- Configurable drive strength on select output pins
- Independent pin value register to read logic level on digital pin

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow, full reel • P = Prequalification • K = Fully qualified, general market flow, 100 piece reel
K##	Kinetis family	• K22
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB • 512 = 512 KB
R	Silicon revision	• Z = Initial

Table continues on the next page...

Part identification

Field	Description	Values
		• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA[1](5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 XFBGA (8 mm x 8 mm) • DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel

1. This package offering is subject to removal.

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