2D_048_015A Data Sheet

2D_048_015A 48V 15W DC-DC Converter

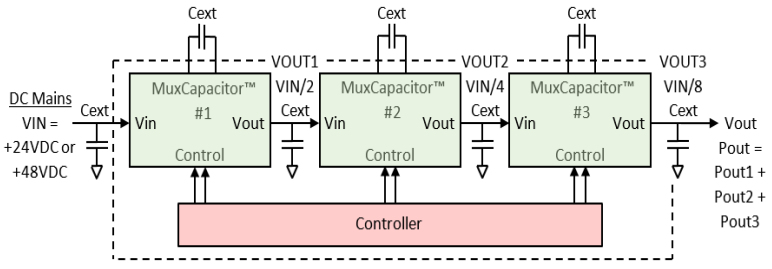
The Helix Semiconductors MuxCapacitor® 2D_048_015A is a member of the MxC® 200 family of monolithic configurable high voltage switch capacitor DC-DC converters targeted for use in both non-isolated and isolated, buck or boost converter applications. The 2D_048_015A supports seamless interface to low voltage PoL regulators to provide highly efficient DC-DC converter solutions with 24V to 57V input voltages for regulated or non-regulated PoL solutions. Consisting of three unique capacitive conversion stages, each capable of providing a separate output voltage, the 2D_048_015A can easily be configured to support systems with multiple voltage requirements. Intelligent timing & control optimize power delivery efficiency from no-load to maximum power.

Applications

- PoE: Wireless Access Points, Security Cameras, VoIP Phones
- IoT & IIoT Gateways
- Electric & Hybrid Automobiles
- Industrial Controllers, HVAC
- Telecom, Data Center Functions

Features

- 48V to 6V Input/Output Voltage
  - 3-stage MuxCap™, G=1/2 each
  - Up to 57V Input Voltage
  - Up to 3 outputs
- Up to 15W Output
  - Pout = Pout1 + Pout2 + Pout3
- Idle Operation: Active, No-Load
  - 1mW Non-Switching
  - 48mW Switching
- 48V to 12V peak efficiency of >97%
  - > 90% Efficiency @ 15W
- Maximizes PoL regulator efficiency
- Fault Detection
  - Output Over Current
  - Thermal Shutdown
- Evaluation Boards, Reference Designs
  - Voltage Buck
  - Unregulated and Regulated
- Package Options
  - 32 pin QFN, 5mm x 5mm
  - Wire Bond Die



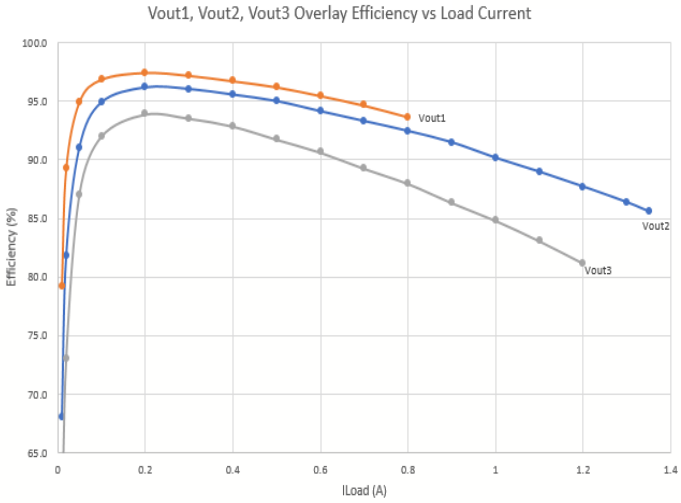


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Figure 1: 2D_048_015A QFN32 Pinout

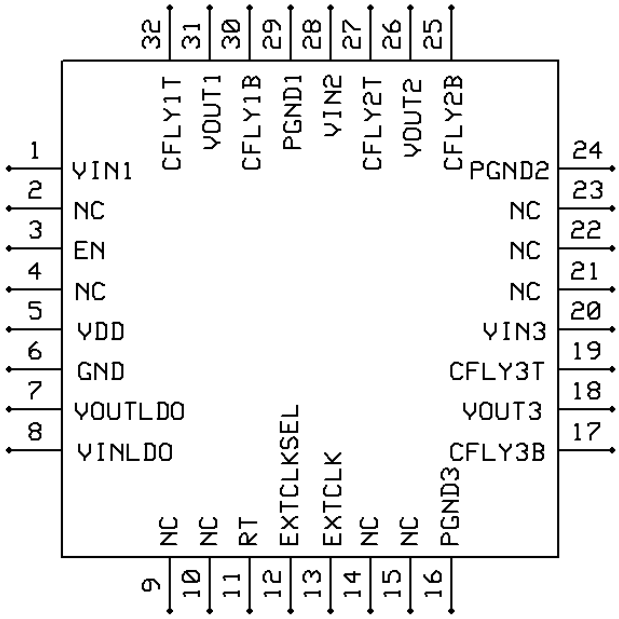


Table 1: 2D_048_015A Pin Assignments

Pin No.	Name	Description
1	VIN1	MuxCapacitor 1: DC input voltage supply pin
3	EN	Device Enable: Input Pin, Internal 2MΩ Pull-Down, 60Vmax 0 = Disable, 1 = Enable
5	VDD	Pre-Regulator: Output supply voltage pin Attach 0.1µF capacitor from VDD pin to GND
6	GND	GND for internal reference and analog circuitry
7	VOUTLDO	LDO: 5V Analog Output pin Attach 4.7µF capacitor from VOUTLDO pin to GND
8	VINLDO	LDO: Input supply voltage pin Connect VINLDO pin to VOUT1
11	RT	Charge Pump Frequency: Input Pin Add external resistor from RT pin to GND.
12	EXTCLKSEL	External Clock Sync Enable: Input Pin, Internal 2MΩ Pull-Down, 30Vmax 0 = Internal Clock, 1 = External Clock
13	EXTCLK	External Clock Sync: Input pin, Internal 2MΩ Pull-Down

16	PGND3	Power GND
17	CFLY3B	MuxCapacitor 3: Bottom of flying capacitor
18	VOUT3	MuxCapacitor 3: Output Pin Attach output capacitor from VOUT3 to PGND3.
19	CFLY3T	MuxCapacitor 3: Top of flying capacitor
20	VIN3	MuxCapacitor 3: DC input voltage supply pin
24	PGND2	Power GND
25	CFLY2B	MuxCapacitor 2: Bottom of flying capacitor
26	VOUT2	MuxCapacitor 2: Output Pin Attach output capacitor from VOUT2 to PGND2.
27	CFLY2T	MuxCapacitor 2: Top of flying capacitor
28	VIN2	MuxCapacitor 2: DC input voltage supply pin
29	PGND1	Power GND
30	CFLY1B	MuxCapacitor 1: Bottom of flying capacitor
31	VOUT1	MuxCapacitor 1: Output Pin Attach output capacitor from VOUT1 to PGND1.
32	CFLY1T	MuxCapacitor 1: Top of flying capacitor
2,4,9,10, 14,15,21, 22,23	NC	No Connect
	Thermal Pad	Power GND

2 Absolute Maximum Ratings

The 2D_048_015A can be exposed to the following extremes without permanent damage to device operation. Performance is not guaranteed at these extremes. Continuous operation at these extremes reduces long term reliability.

Table 2: 2D_048_015A Absolute Maximum Ratings

Pin	Min	Max	Unit
VIN1, EN	-0.3	62	V
VIN2, VIN3	-0.3	31	V
VINLDO	-0.3	15	V
EXTCLK	-0.3	30	V
VOUTLDO, VDD, EXTCLKSEL, RT	-0.3	6	V
GND to PGND	-0.3	0.3	V
ESD Voltage: Human Body Model		2	kV
ESD Voltage: Charge coupled Model		500	V
ESD Voltage: Machine Model		200	V
Storage temperature	-40	125	°C
Junction Temperature	-40	125	°C

3 Recommended Operating Conditions

The 2D_048_015A chip is designed to operate within the design limits specified in the Parametric Specifications when the conditions of the following table are not exceeded.

Table 3: 2D_048_015A Recommended Operating Conditions

Definition	Min	Max	Unit
Input Voltage	20	57	V
Output Power	0	15	W
EN	0	57	V
EXTCLK	0	29	V
EXTCLKSEL, RT	0	5.5	V
Junction Temperature	-40	125	°C

4 Electrical Specifications

The electrical characteristics of the Helix Semiconductors 2D_048_015A is tested according to the following criteria:

Unless otherwise stated, these specifications apply over:

20V < VIN1 < 57V, 10V < VIN2 & VIN3 < 28.5V,

4.5V < VOUTLDO < 5.5, Fsw=100kHz, -40˚C < TJ < 85˚C.

Notes:

1. Min and Max values are valid over Operating Conditions, unless otherwise stated.
2. Typ values are valid at typical Operating Conditions and typical process Parameters.
3. Guaranteed by Design.

Table 4: 2D_048_015A Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
60V MuxCapacitor Voltage Divider: VIN1/VOUT1						
Vout	Output Voltage	VIN=48V, Po=0W, Note 3.		24		V
Iout	Output Current	Note 3.			0.65	A
Rsw	Switch Rdson			600		mΩ
30V MuxCapacitor Voltage Divider: VIN2/VOUT2 and VIN3/VOUT3						
Vout	Output Voltage	VIN=24V, Po=0W, Note 3.		12		V
Iout	Output Current	Note 3.			1	A
Rsw	Switch Rdson			300		mΩ
VOUTLDO						
VoutLDO	Output Voltage			5		V
Under Voltage Lockout						
UVVoutS+	VOUTLDO Start	5V Rising Trip Level	4.4	4.6	4.8	V
UVVoutS-	VOUTLDO Stop	5V Falling Trip Level	4.1	4.2	4.3	V
EN+	Enable On Thresh.	Enable Rising Trip Level	1.14	1.2	1.26	V
EN1	Enable Off Thresh.	Enable Falling Trip Level	0.95	1.0	1.05	V
Clock Generator						
Fsw	Switching Frequency	RT=402KΩ,95kHz RT=174KΩ, 220kHz		95	230	kHz
Thermal Shutdown						
TSD	Thermal Shutdown	Note 3.		145		°C
Hyst	Hysteresis	Note 3.		20		°C

Figure 2: VOUT1, VOUT2, VOUT3 Efficiency

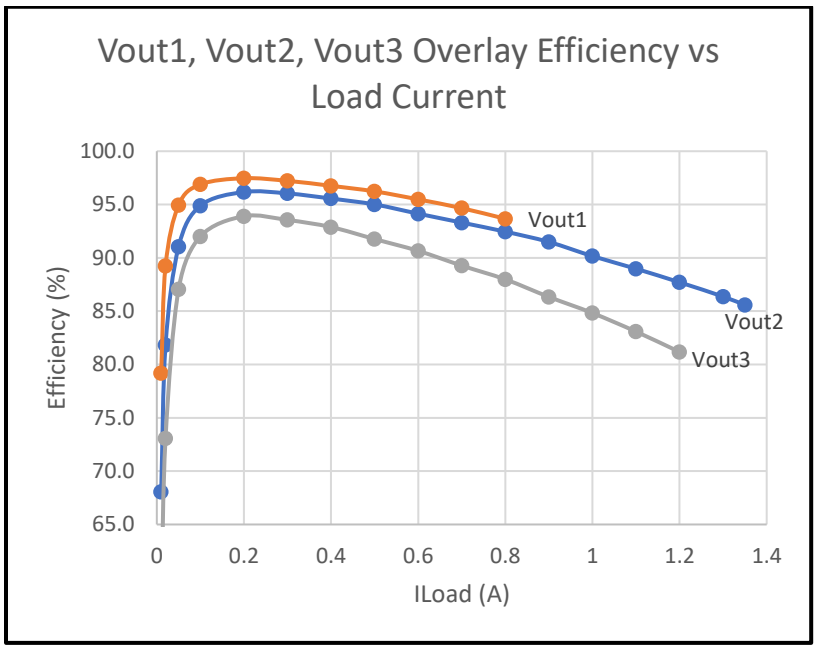


Figure 3: VOUT vs Frequency Efficiency

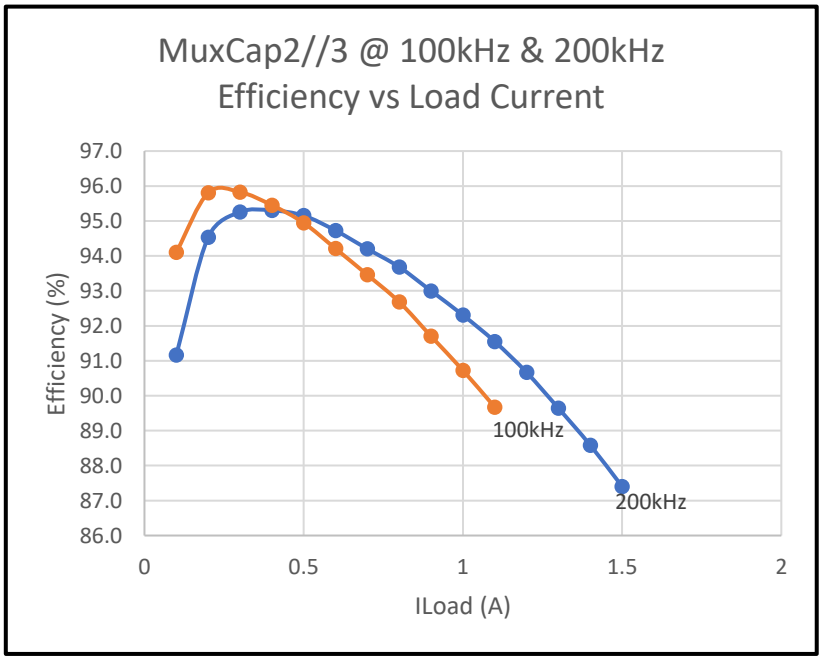
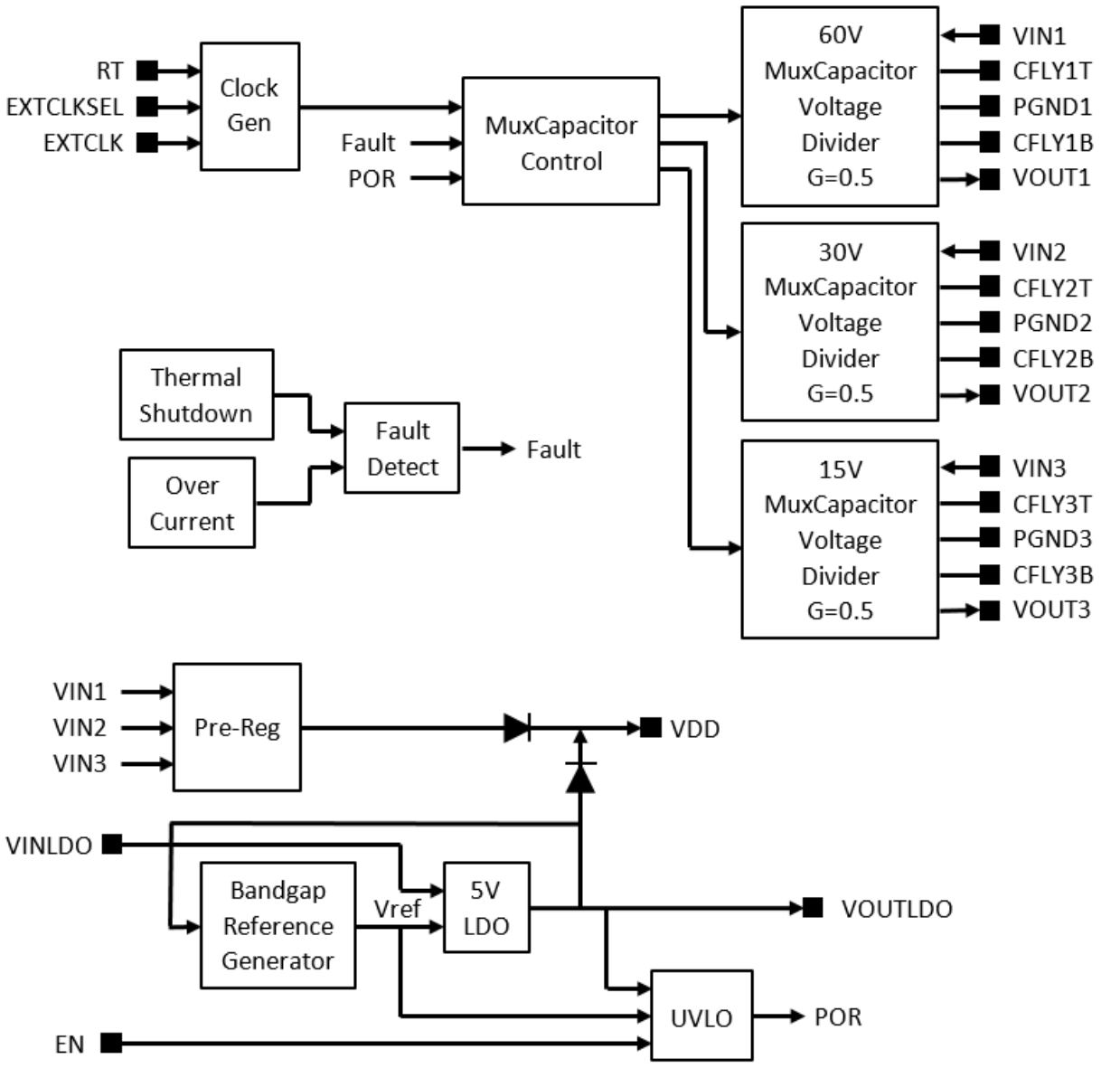


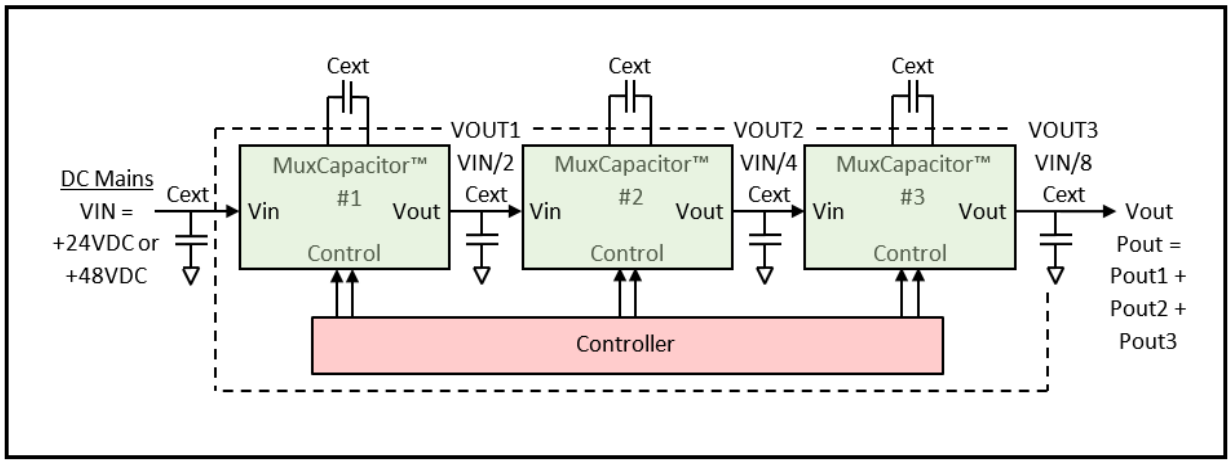
Figure 4: 2D_048_015A Block Diagram



5 Functional Description

The Helix Semiconductors 2D_048_015A DC-DC MuxCapacitor IC is an easy to use, highly efficient DC voltage divider. It combines three MuxCapacitor Voltage Dividers to reduce the input voltage allowing the use of lower voltage / lower cost PoL regulators.

Figure 5: 2D_048_015A Functional Block Diagram



Each MuxCapacitor stage has its own input and output pins allowing for multiple configurations. All three stages can be connected in series for access to intermediate voltage reduction outputs. Or, the MuxCapacitor stages can be wired in parallel for added output current capability and efficiency.

5.1 MuxCapacitor Voltage Divider

The 2D_048_015A Muxcapacitor Voltage Dividers (MCVD) divide the DC voltage present at the VIN1 pin to reduced voltages at the VOUT1, VOUT2, and VOUT3 pins which provides the input voltage to an external POL regulator.

The MCVD is comprised of three stages, each with a gain of ½.

Each MCVD uses an external flying capacitor, an internal switching circuit, and an external hold capacitor. The switching device is configured to operate the corresponding voltage reduction circuit at charging and discharging phases from a two-phase non-overlapping on-chip clock generator.

Each MuxCapacitor contains over-current protection. The over-current protection automatically resets once the over-current condition clears. This feature is active at startup enhancing the soft-start ramp-up at each VOUTx.

5.2 Low Drop-Out Voltage Regulator

An integrated 5V LDO provides the supply voltage for the analog circuits. The 5V LDO is powered from the VINLDO pin. The VINLDO supply voltage range is 7-15V.

The 5V LDO uses the bandgap output as the reference voltage to generate the desired output voltage.

5.3 Under-Voltage Lockout and POR

The integrated under-voltage lockout circuit monitors the voltages at the 5V LDO output, and the Enable pin. It ensures that the MuxCapacitor outputs remain in the off state whenever one of these signals drop below the set thresholds. Normal operation resumes once these signals rise above their thresholds. The Power-On Ready (POR) signal is generated when each signal reaches their valid logic level. When the POR is asserted the Soft-Start sequence starts. All the UVLO comparators except the enable circuit are disabled when enable is low to achieve the ultra-low power dissipation.

5.4 Clock Generator

The integrated clock generator's switching frequency is programmed with an external resistor (402KΩ typical) connected from the RT pin to GND. The MuxCapacitor switching frequency (Fsw) is calculated as:

Fsw (kHz) = 38,190 / External RT Resistor (Kohms)

This clock signal can be synchronized to an external clock by using the EXTCLK pin. Switching activity at the EXTCLK pin enables the internal synchronizer. When the synchronizer is enabled (EXTCLKSEL = 1), the MuxCapacitor clock will track the EXTCLK pin switching rate. As the EXTCLK pin frequency slows down, the MuxCapacitor clock slows down. The EXTCLK signal is derived from the external POL's switch drive signal. This allows the MuxCapacitors to save power as the external switcher slows down due to reduced load demand. The MuxCapacitor switching frequency is ¼ the EXTCLK frequency.

5.5 Thermal Shutdown

Temperature sensing is included and provides the signal to an over temperature detector. The trip threshold is set to 145°C. When trip threshold is exceeded, thermal shutdown turns off the MuxCapacitor outputs and resets the internal soft start.

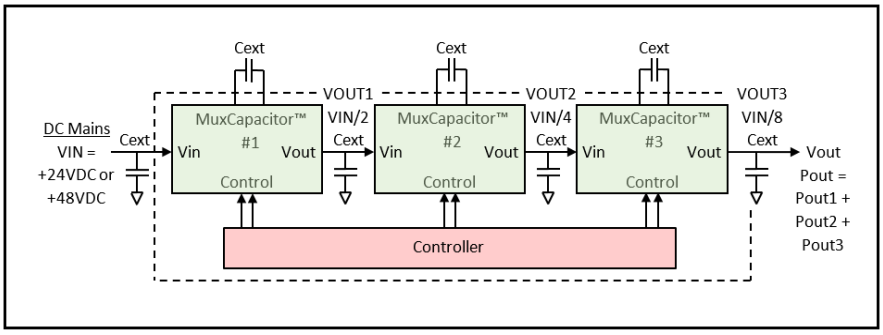
The restart is automatically initiated when the sensed temperature drops down within the normal operating range. A 20°C hysteresis is incorporated into the thermal shutdown threshold. The thermal shutdown circuit is disabled when enable is low to achieve the ultra-low power dissipation.

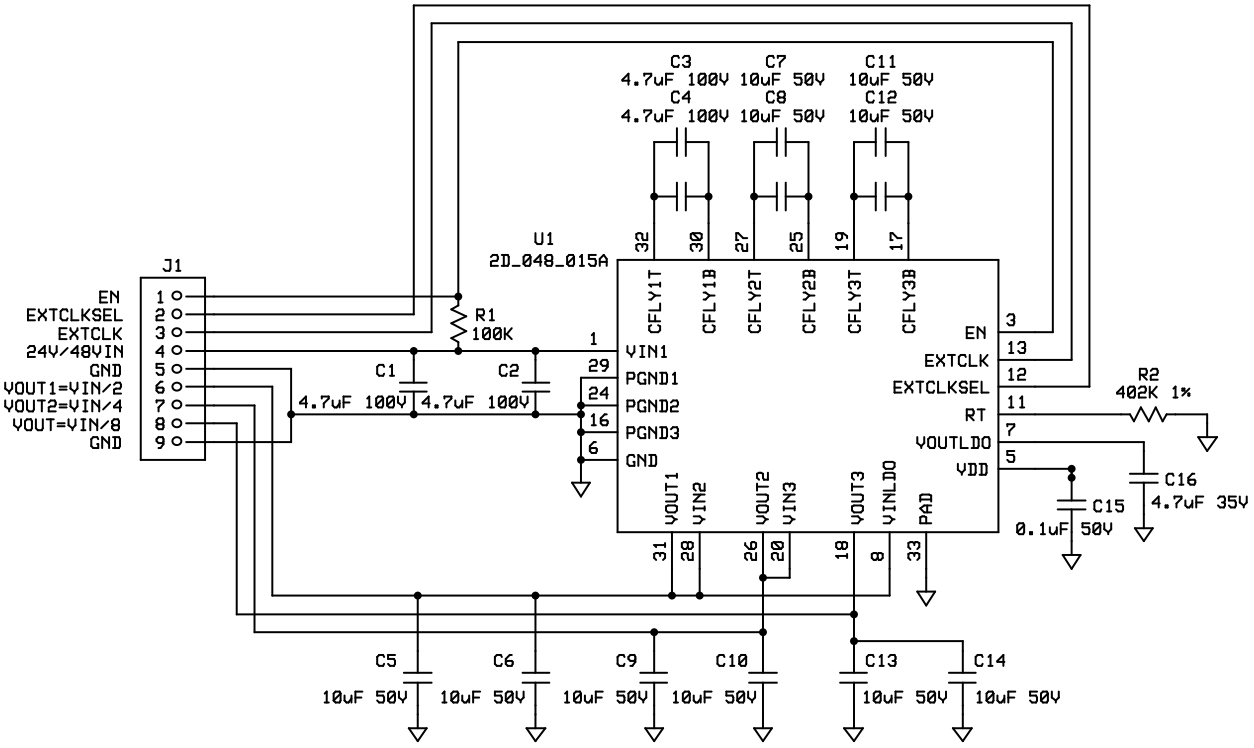
6 Reference System Application

The following system diagrams provide 15W application schematics. The 2D_048_015A is first shown as a simple DC-DC voltage reduction circuit. Each MuxCapacitor stage performs a G=1/2 voltage reduction. Additionally, each MuxCapacitor output can be tapped to provide an intermediate voltage. While the total power drawn from the 2D_048_015A cannot exceed 15W where Pout = Pout1 + Pout2 + Pout3, each MuxCapacitor cell has a maximum output current. The Iout_max for VOUT1 cannot exceed 0.5A. The Iout_max for VOUT2 and VOUT3 cannot exceed 1A individually.

Efficiency and delivered power are dependent on application circuit implementation, capacitor components, RT frequency and thermal management. Consult the factory for additional design information.

Figure 6: 2D_048_015A Application Schematic





MxC 290-EB9-C

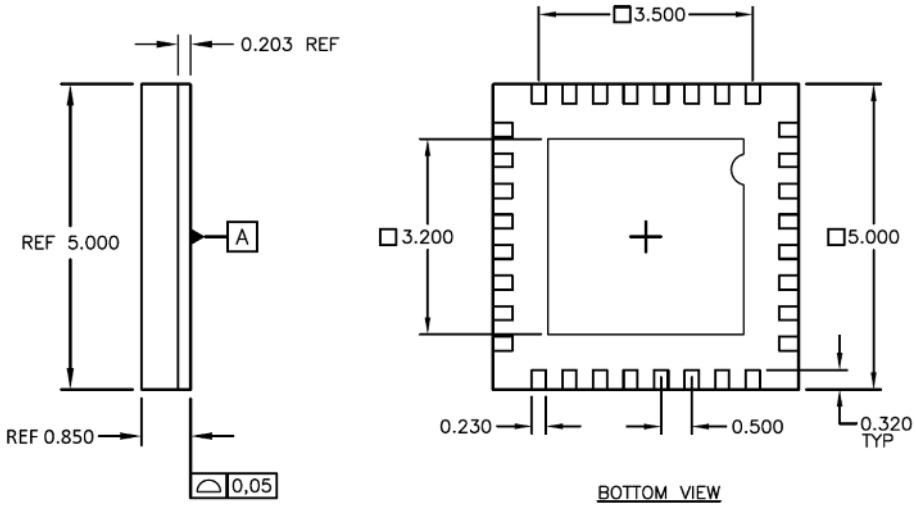
7 Package Drawings

The available packages for the 2D_048_015A are shown in the following drawings.

7.1 QFN32 Package

The 2D_048_015A is packaged in a 32-pin 5mm x 5mm QFN package as shown below.

Figure 7: 2D_048_015A QFN32 Package Drawing



7.2 Wire-bond Die

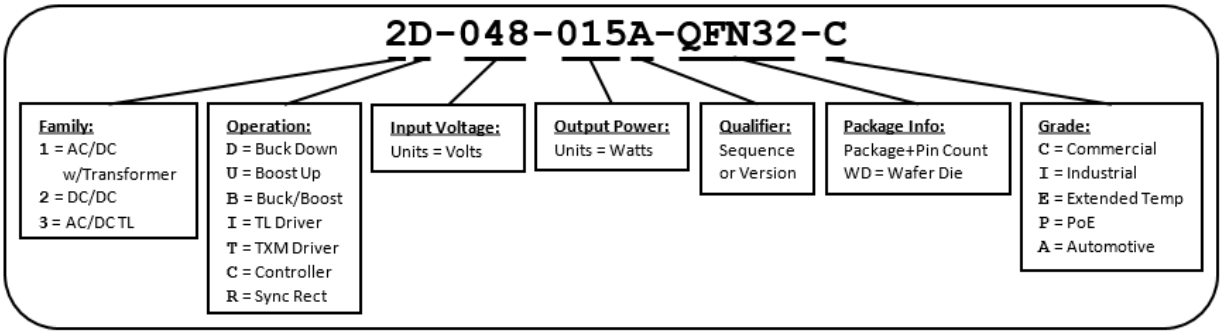
The 2D_048_015A is available in die form. Please contact factory for information regarding die sales.

8 Ordering Information

Refer to the following table for package option ordering information.

Table 5: 2D_048_015A Ordering Information

Part Number	Description	Package
2D-048-015A-QFN32-C	32 pin 5mm x 5mm QFN	QFN
2D-048-015A-WD-C	Wire Bond Die	Die
MxC 290-EB9-C	9-Pin Three Output Evaluation Board	Eval Board



This product is covered by one or more Helix Semiconductors patents.

Patent http://www.helixsemiconductors.com/pages/company/trademarksandpatents

Table 6: Revision History

Date	Revision	Description
1.30.19	1	Initial release
2.2.19	2	Miscellaneous edits
3.4.19	3	Patent disclosure

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