# PI3VDP1430

## Dual Mode DisplayPort to HDMI Level shifter and Re-driver

### Features

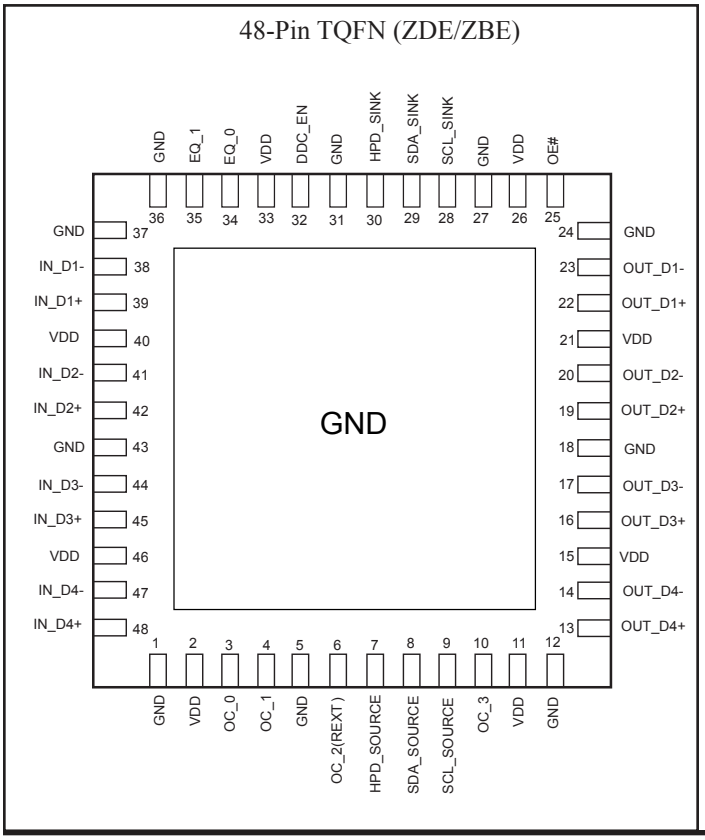
- Re-drives HDMI1.4a signal across long PCB trace
- Converts low-swing AC coupled differential input to HDMI™ rev 1.4a compliant open-drain current steering Rx terminated differential output
- HDMI level shifting operation up to 2.97Gbps per lane (297MHz pixel clock) for stereo video
- Integrated 50-ohm termination resistors for AC-coupled differential inputs.
- Enable/Disable feature to turn off TMDS outputs to enter low-power state.
- 3.3 Power supply required.
- Integrated ESD protection to 8kV contact on all high speed I/O pins (IN_x and OUT_x) per IEC61000-4-2 test spec, level 4
- DDC level shifters from 5V from sink side down to 3.3V on source side
- Level shifter for HPD signal from HDMI/DVI connector
- Integrated pull-down on HPD_sink input guarantees "input low" when no display is plugged in
- Packaging (Pb-Free & Green)
  - 48 TQFN, 7mm x 7mm (ZBE)

### Description

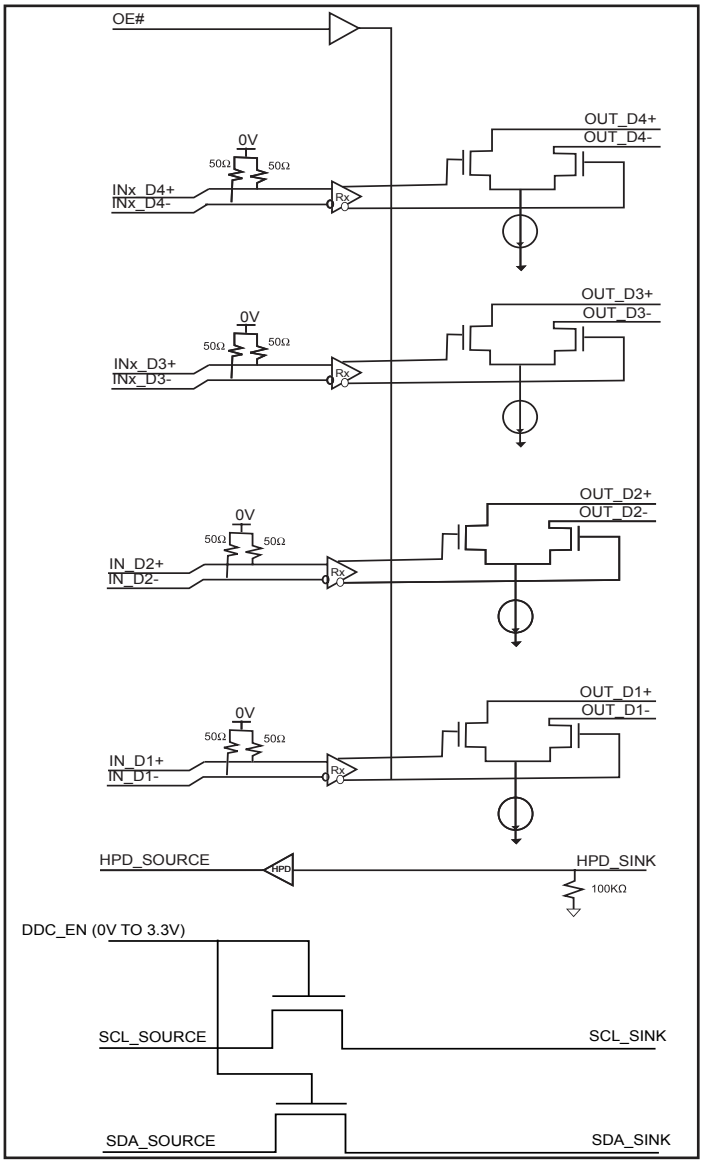
Pericom Semiconductor's PI3VDP1430 provides the ability to use a Dual-mode DP transmitter in HDMI™ mode. This flexibility provides the user a choice of how to connect to their favorite display. All signal paths accept AC coupled video signals. The PI3VDP1430 converts this AC coupled signal into an HDMI rev 1.4a compliant signal with proper signal swing. This conversion is automatic and transparent to the user.

The PI3VDP1430 supports up to 2.97Gbps, which provides stereo video functionality as described in the HDMI 1.4a specification.

### Pin Configuration




### Block Diagram



## Pin Assignment

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>OE#</td><td>I</td><td>5.5V tolerant low-voltage single-ended input<br>Enable for level shifter path
<table>
<tr><td>OE#</td><td>IN_D Termination</td><td>OUT_D Outputs</td></tr>
<tr><td>1</td><td>>100KΩ</td><td>High-Z</td></tr>
<tr><td>0</td><td>50Ω</td><td>Active</td></tr>
</table></td></tr>
<tr><td>IN_D4+</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D4–</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D3+</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D3–</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D2+</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D2–</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D1+</td><td>I</td><td>Differential input</td></tr>
<tr><td>IN_D1–</td><td>I</td><td>Differential input</td></tr>
<tr><td>OUT_D4+</td><td>O</td><td>TMDS Differential output</td></tr>
<tr><td>OUT_D4–</td><td>O</td><td>TMDS Differential output</td></tr>
<tr><td>OUT_D3+</td><td>O</td><td>TMDS Differential output</td></tr>
<tr><td>OUT_D3–</td><td>O</td><td>TMDS Differential output</td></tr>
<tr><td>OUT_D2+</td><td>O</td><td>TMDS Differential output</td></tr>
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<tr><td>OUT_D1–</td><td>O</td><td>TMDS Differential output</td></tr>
</table>

**(Continued)**

| Pin Name | Type | Description |
|---|---|---|
| HPD_SINK | 5V tolerance single-ended input | Low Frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage High indicates "plugged" state; voltage low indicated "unplugged". HPD_SINK is pulled down by an integrated 100K ohm put-down resistor. |
| HPD_SOURCE | 3.3V single-ended output | HPD_SOURCE: 0V to 3.3V (nominal) output signal. This is level-shifted version of the HPD_SINK signal. |
| SCL_SOURCE | Single-ended 3.3V open-drain DDC I/O | 3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SCL_SINK through voltage-limiting integrated NMOS passgate. |
| SDA_SOURCE | Single-ended 3.3V open-drain DDC I/O | 3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SDA_SINK through voltage-limiting integrated NMOS passgate. |
| SCL_SINK | Single-ended 5V open-drain DDC I/O | 5V DDC Clock I/O. Pulled up by external termination to 5V. Connected to SCL_SOURCE through voltage-limiting integrated NMOS passgate. |
| SDA_SINK | Single-ended 5V open-drain DDC I/O | 5V DDC Data I/O. Pulled up by external termination to 5V. Connected to SDA_SOURCE through voltage-limiting integrated NMOS passgate. |
| DDC_EN | 5.0V tolerant Single-ended input | Enables bias voltage to the DDC passgate level shifter gates. (May be implemented as a bias voltage connection to the DDC pass gates themselves.)<br>DDC_EN: 0V → Passgate: Disabled<br>DDC_EN: 3.3V → Passgate: Enabled |
| VDD | 3.3V DC Supply | 3.3V ± 10% |
| OC_2<br>(REXT) | 3.3V single-ended control input | Acceptable connections to OC_1 (REXT) pin are: Resistor to GND; Resistor to 3.3V; NC. (Resistor should be 0-ohm). |
| OC_3 | Analog connection to external component or supply | Acceptable connections to OC_3 pin are: short to 3.3V or to GND; NC. |
| OC_0<br>OC_1<br>EQ_0<br>EQ_1 | Output and Input jitter elimination control | Control pins are to enable Jitter elimination features. For normal operation these pins are tied GND or to VDD. Please see the truth tables for more information. |

**Table 1: Truth Table**

| OC_3[1] | OC_2[1] | OC_1[1] | OC_0[1] | Vswing (mV) | Pre/De-emphasis |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 500 | 0 |
| 0 | 0 | 0 | 1 | 600 | 0 |
| 0 | 0 | 1 | 0 | 750 | 0 |
| 0 | 0 | 1 | 1 | 1000 | 0 |
| 0 | 1 | 0 | 0 | 500 | 0 |
| 0 | 1 | 0 | 1 | 500 | 1.5dB |
| 0 | 1 | 1 | 0 | 500 | 3.5dB |
| 0 | 1 | 1 | 1 | 500 | 6dB |
| 1 | 0 | 0 | 0 | 400 | 0 |
| 1 | 0 | 0 | 1 | 400 | 3.5dB |
| 1 | 0 | 1 | 0 | 400 | 6dB |
| 1 | 0 | 1 | 1 | 400 | 9dB |
| 1 | 1 | 0 | 0 | 1000 | 0 |
| 1 | 1 | 0 | 1 | 1000 | -3.5dB |
| 1 | 1 | 1 | 0 | 1000 | -6dB |
| 1 | 1 | 1 | 1 | 1000 | -9dB |

**Table 2: Truth Table**

| EQ_1[1] | EQ_0[1] | Equalization @ 1.25GHz (dB) |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 6 |
| 1 | 0 | 9 |
| 1 | 1 | 12 |

**Notes:**
1) These signals have internal 100kohm pull-ups.

## Absolute Maximum Ratings (Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +5V
DC Input Voltage.....–0.5V to $V_{DD}$
DC Output Current .....120mA
Power Dissipation .....1.0W

**Note:** Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Thermal Characteristics

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $T_{Jmax}$ | Junction Temperature | 125 | °C |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 23.65 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 9.1 | |

## Electrical Characteristics

### Table 3: Power Supplies and Temperature Range

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| VDD | Power Supply | 2.89 | 3.3 | 3.6 | V | |
| ICC | Max Current | | | 100 | mA | Total current from VDD 3.3V supply when de-emphasis/pre-emphasis is set to 0dB. |
| ICCQ | Standby Current Consumption | | | 2 | mA | OE# = HIGH |
| TCASE | Case temperature range for operation with spec. | -40 | | 85 | Celcius | |

**Table 4: OE# Description**

| OE# | Device State | Comments |
|---|---|---|
| Asserted (low voltage) | Differential input buffers and output buffers enabled. Input impedance = 50Ω | Normal functioning state for IN_D to OUT_D level shifting function. |
| Unasserted (high voltage) | Low-power state.<br><br>Differential input buffers and termination are disabled. Differential inputs are in a high-impedance state.<br><br>OUT_D level-shifting outputs are disabled.<br>OUT_D level-shifting outputs are in high-impedence state.<br>Internal bias currents are turned off. | Intended for lowest power condition when:<br>• No display is plugged in or<br>• The level shifted data path is disabled<br><br>HPD_SINK input and HPD_SOURCE output are not affected by OE# SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE# |

**Table 5: Differential Input Characteristics for IN_D and RX_IN signals**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| Tbit | Unit Interval | 360 | | | ps | Tbit is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal Tbit at 2.5 Gbps=400ps. 360ps=400ps-10% |
| $V_{RX-DIFFp-p}$ | Differential Input Peak to Peak Voltage | 0.175 | | 1.2 | V | VRX-DIFFp-p=2'\|VRX-D+ x VRX-D-\| Applies to IN_D and RX_IN signals |
| $T_{RX-EYE}$ | Minimum Eye Width at IN_D input pair | 0.8 | | | Tbit | The level shifter may add a maximum of 0.02UI jitter |
| $V_{CM-AC-pp}$ | AC Peak Common Mode Input Voltage | | | 100 | mV | VCM-AC-pp = \|VRX-D+ + VRX-D-\|/2 - VRX-CM-DC.<br>VRX-CM-DC = DC(avg) of\|VRX-D+ + VRX-D-\|/2<br>VCM-AC-pp includes all frequencies above 30 kHz. |
| $Z_{RX-DC}$ | | 40 | 50 | 60 | Ω | Required IN_D+ as well as IN_D- DC impedance (50Ω ± 20% tolerance). |
| $V_{RX-Bias}$ | | 0 | | 2.0 | V | Intended to limit power-up stress on chipset's PCIE output buffers. |
| $Z_{RX-HIGH-Z}$ | | 100 | | | kΩ | Differential inputs must be in a high impedance state when OE# is HIGH. |

## TMDS Outputs

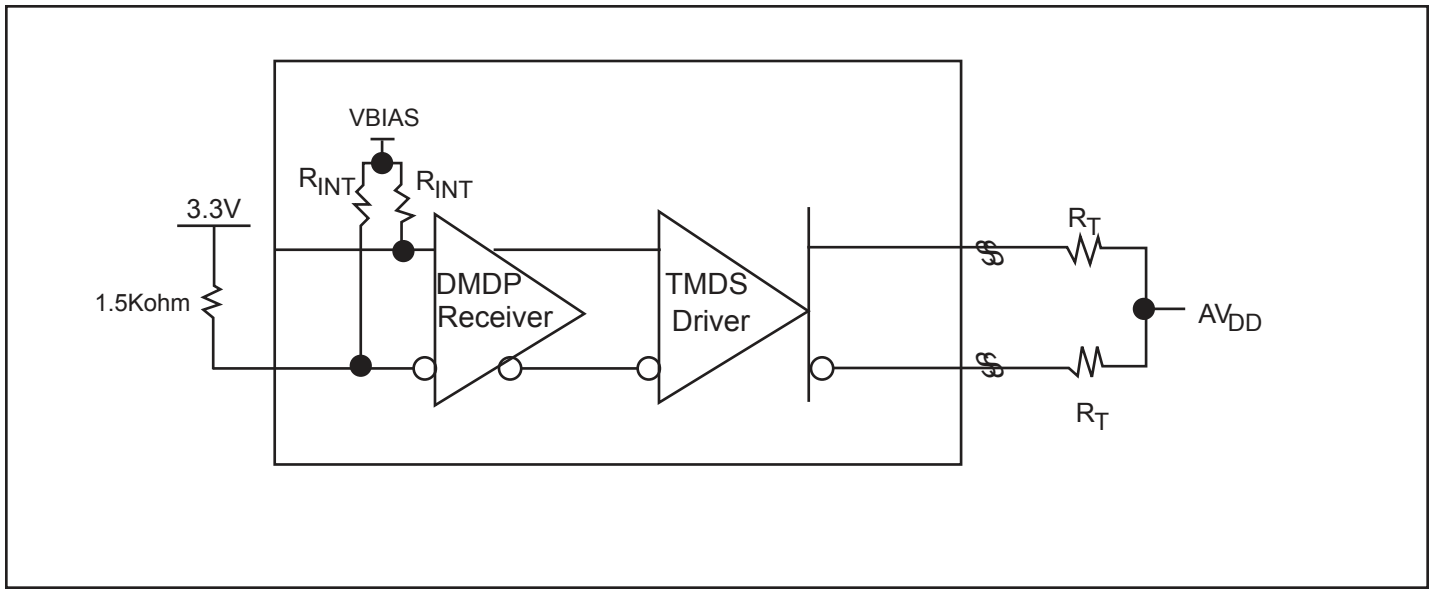
The level shifter's TMDS outputs are required to meet HDMI 1.4a specifications.
The HDMI 1.4a Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.4 specification.

**Table 6: Differential Output Characteristics for TMDS_OUT signals**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_H$ | Single-ended high level output voltage | VDD-10mV | VDD | VDD+10mV | V | VDD is the DC termination voltage in the HDMI or DVI Sink. VDD is nominally 3.3V |
| $V_L$ | Single-ended low level output voltage | VDD-600mV | VDD-500mV | VDD-400mV | V | The open-drain output pulls down from VDD. |
| $V_{SWING}$ | Single-ended output swing voltage | 450mV | 500mV | 600mV | V | Swing down from TMDS termination voltage (3.3V ± 10%) |
| $I_{OFF}$ | Single-ended current in high-Z state | | | 50 | µA | Measured with TMDS outputs pulled up to VDD Max _(3.6V) through 50Ω resistors. |
| $T_R$ | Rise time | 125ps | | 0.4Tbit | ps | Max Rise/Fall time @2.7Gbps = 148ps. 125ps = 148-15% |
| $T_F$ | Fall time | 125ps | | 0.4Tbit | ps | Max Rise/Fall time @2.7Gbps = 148ps. 125ps = 148-15% |
| $T_{SKEW-INTRA}$ | Intra-pair differential skew | | | 30 | ps | This differential skew budget is in addition to the skew presented between D+ and D- paired input pins. HDMI revision 1.3 source allowable intra-pair skew is 0.15Tbit. |
| $T_{SKEW-INTER}$ | Inter-pair lane-to-lane output skew | | | 100 | ps | This lane-to-lane skew budget is in addition to skew between differential input pairs |
| $T_{JIT}$ | Jitter added to TMDS signals | | | 25 | ps | Jitter budget for TMDS signals as they pass through the level shifter. 25ps = 0.056 Tbit at 2.25 Gb/s |

## TMDS Output Oscillation Elimination

The inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. Pericom recommends to add a 1.5Kohm pull-up to the Clock input.




**TMDS Input Fail-Safe Recommendation**

**Table 8: HPD Input Characteristics**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{IH-HPD}$ | Input High Level | 2.0 | 5.0 | 5.3 | V | Low-speed input changes state on cable plug/unplug |
| $V_{IL-HPD}$ | HPD_sink Input Low Level | 0 | | 0.8 | V | |
| $I_{IN-HPD}$ | HPD_sink Input Leakage Current | | | 70 | µA | Measured with HPD_sink at $V_{IH-HPD}$ max and $V_{IL-HPD}$ min |
| $V_{OH-HPDB}$ | HPD_sink Output High-Level | 2.5 | | $V_{DD}$ | V | $V_{DD}$ = 3.3V ± 10% |
| $V_{OL-HPDB}$ | HPD_sink Output Low-Level | 0 | | 0.02 | V | |
| $T_{HPD}$ | HPD_sink to HPD_source propagation delay | | | 200 | ns | Time from HPD_sink changing state to HPD_source changing state. Includes HPD_source rise/fall time |
| $T_{RF-HPDB}$ | HPD_source rise/ fall time | 1 | | 20 | ns | Time required to transition from $V_{OH-HPDB}$ to $V_{OL-HPDB}$ or from $V_{OL-HPDB}$ to $V_{OH-HPDB}$ |

**Table 9: OE# Input and DDC_EN**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | 2.0 | | VDD | V | TMDS enable input changes state on cable plug/unplug |
| $V_{IL}$ | Input Low Level | 0 | | 0.8 | V | |
| $I_{IN}$ | Input Leakage Current | | | 10 | µA | Measured with input at $V_{IH-EN}$ max and $V_{IL-EN}$ min |

**Table 10: Termination Resistors**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $R_{HPD}$ | HPD_sink input pull-down resistor. | 80K | 100k | 120K | Ω | Guarantees HPD_sink is LOW when no display is plugged in. |

## Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each $V_{DD}$ pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four $V_{DD}$ pins on our part, if there is more or less $V_{DD}$ pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of $V_{DD}$ pins. On top of 0.1µF decoupling capacitors on each $V_{DD}$ pins, it is recommended to put a 10µF decoupling capacitor near our part's $V_{DD}$, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

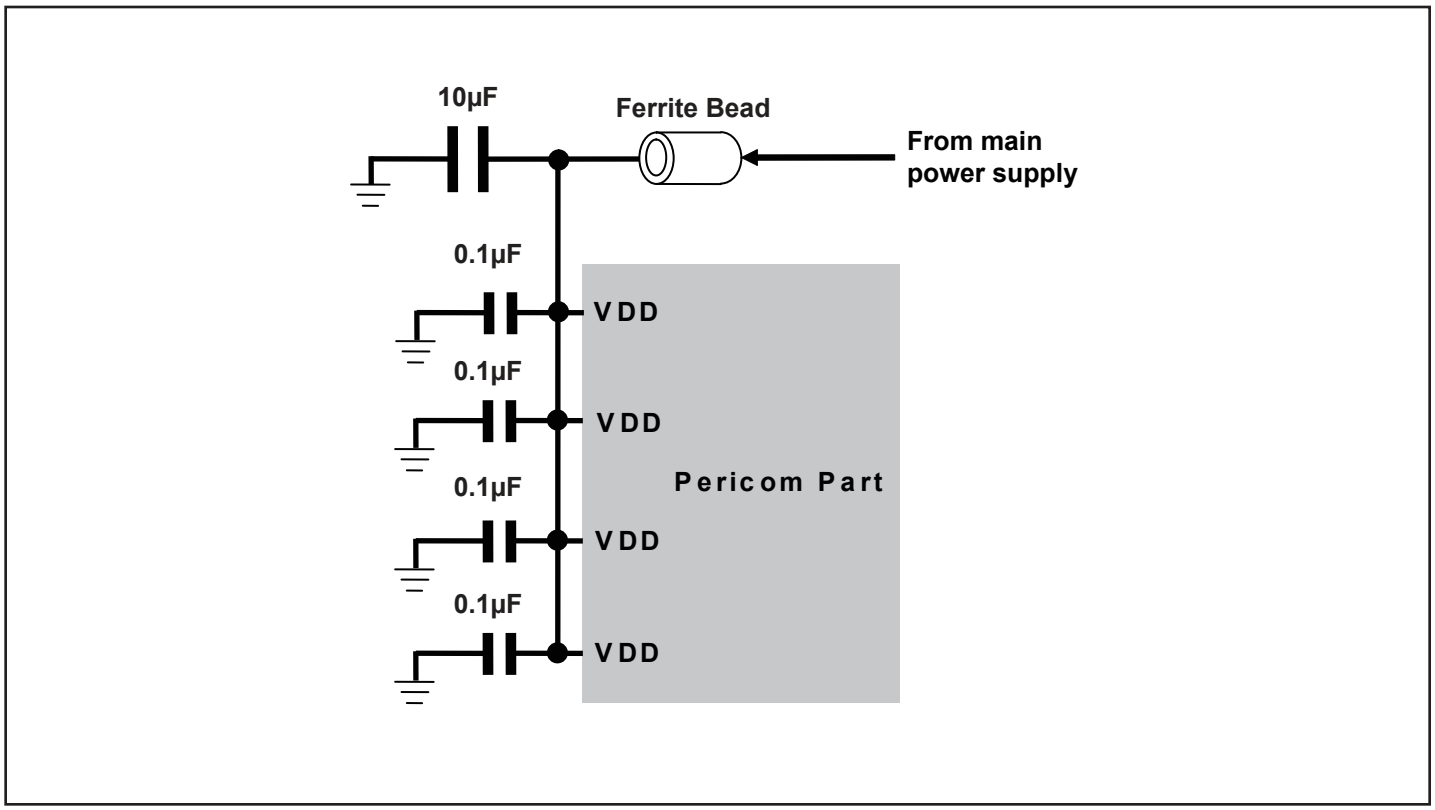



**Figure 1 Recommended Power Supply Decoupling Circuit Diagram**

## Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

## Layout and Decoupling CapacitorPlacement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each $V_{DD}$ pin.
ii. $V_{DD}$ and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to $V_{DD}$ and GND planes directly.
iv. Trace should be as wide as possible
v. Trace should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same $V_{DD}$ and GND planes. Since large current flowing on our $V_{DD}$ or GND planes will generate a potential variation on the $V_{DD}$ or GND of our part.

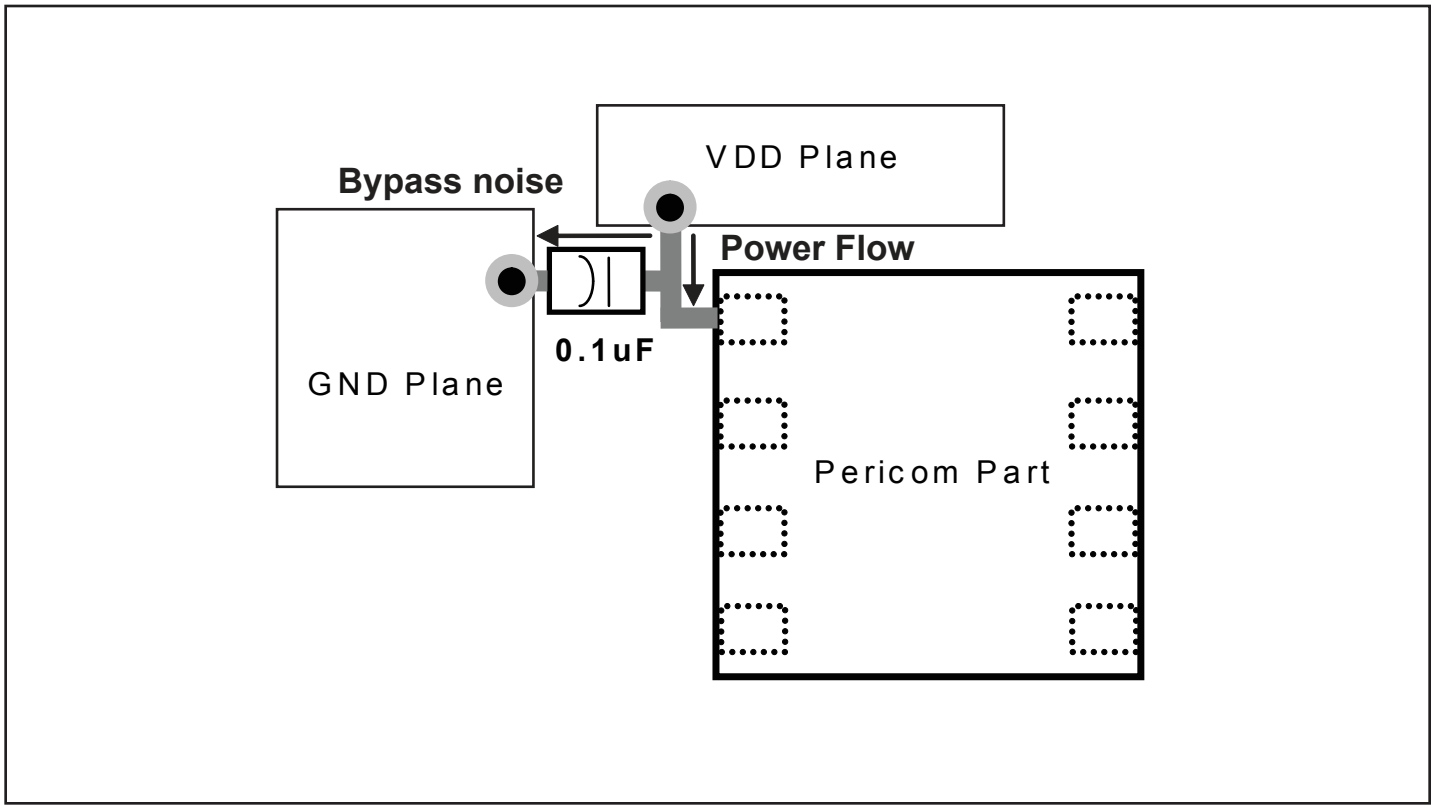
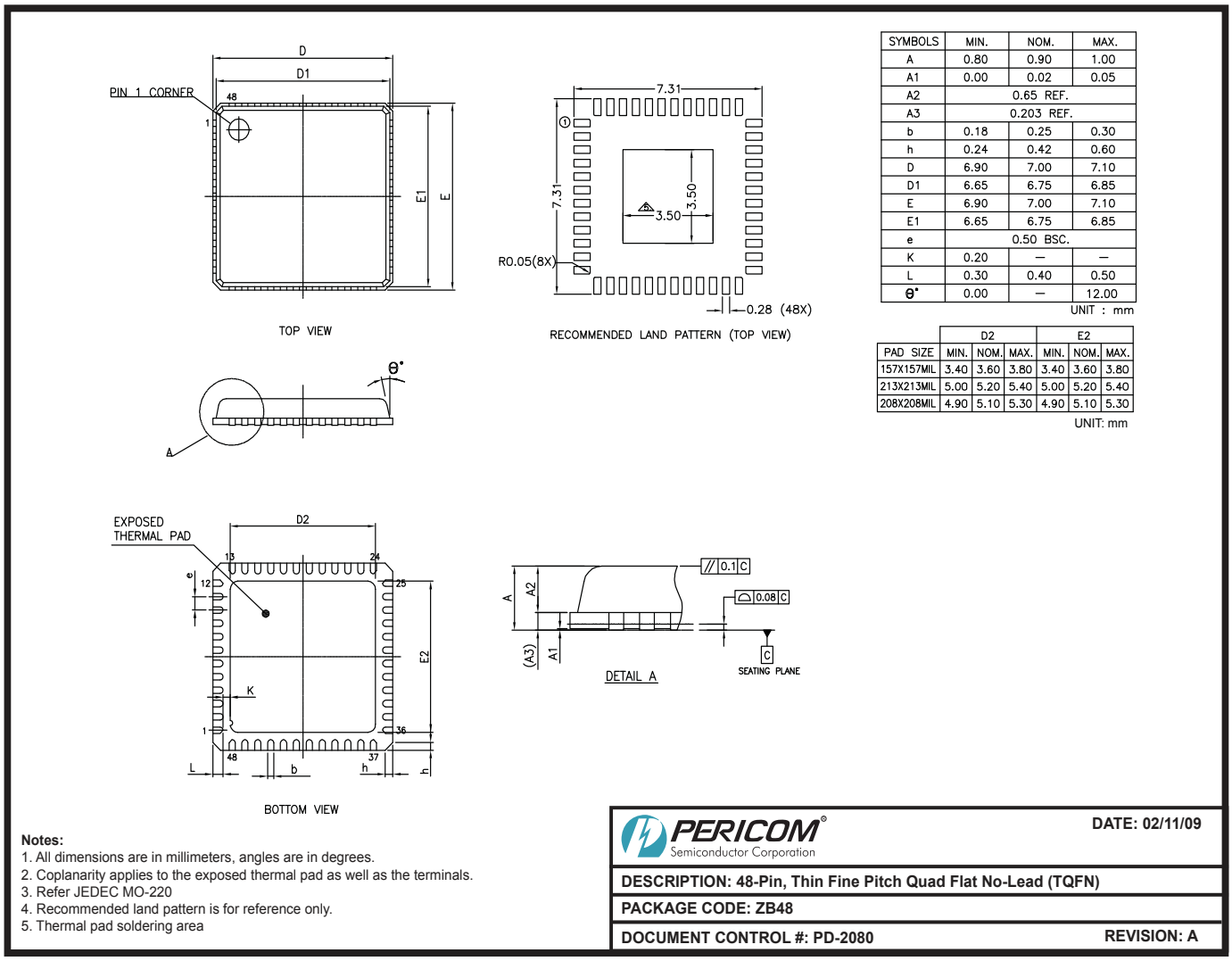



**Figure 2 Layout and Decoupling Capacitor Placement Diagram**

## Package Mechanical : 48-pin TQFN




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | | 0.65 REF. | |
| A3 | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| h | 0.24 | 0.42 | 0.60 |
| D | 6.90 | 7.00 | 7.10 |
| D1 | 6.65 | 6.75 | 6.85 |
| E | 6.90 | 7.00 | 7.10 |
| E1 | 6.65 | 6.75 | 6.85 |
| e | | 0.50 BSC. | |
| K | 0.20 | — | — |
| L | 0.30 | 0.40 | 0.50 |
| θ° | 0.00 | — | 12.00 |

UNIT : mm

| | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| PAD SIZE | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| 157X157MIL | 3.40 | 3.60 | 3.80 | 3.40 | 3.60 | 3.80 |
| 213X213MIL | 5.00 | 5.20 | 5.40 | 5.00 | 5.20 | 5.40 |
| 208X208MIL | 4.90 | 5.10 | 5.30 | 4.90 | 5.10 | 5.30 |

UNIT: mm

**Notes:**
1. All dimensions are in millimeters, angles are in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area

PERICOM Semiconductor Corporation

**DATE: 02/11/09**

**DESCRIPTION: 48-Pin, Thin Fine Pitch Quad Flat No-Lead (TQFN)**

**PACKAGE CODE: ZB48**

**DOCUMENT CONTROL #: PD-2080** **REVISION: A**

**Note:**
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php
- The epad size is 5.1 x 5.1 mm

## Ordering Information

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI3VDP1430ZBE | ZBE | 48-pin Pb-free & Green, TQFN |

**Notes:**

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel