

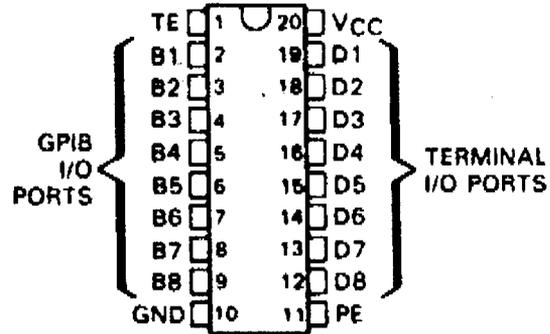
# GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

← D2525

## MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (VCC = 0)

DUAL IN-LINE PACKAGE  
(TOP VIEW)



### FUNCTION TABLES

EACH DRIVER

EACH RECEIVER

INPUTS			OUTPUT	INPUTS			OUTPUT
D	TE	PE	B	D	TE	PE	D
H	H	H	H	L	L	X	L
L	H	X	L	H	L	X	H
H	X	L	Z <sup>†</sup>	X	H	X	Z
X	L	X	Z <sup>†</sup>				

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

<sup>†</sup> This is the high-impedance state of a normal 3-state output modified by the internal resistors to VCC and ground.

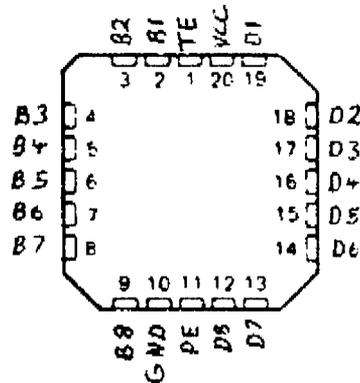
### description

The SN75160B 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when VCC = 0 volts. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.  
-55°C to 100°C.

*95160B  
SN75160B... FT Package  
(TOP VIEW)*



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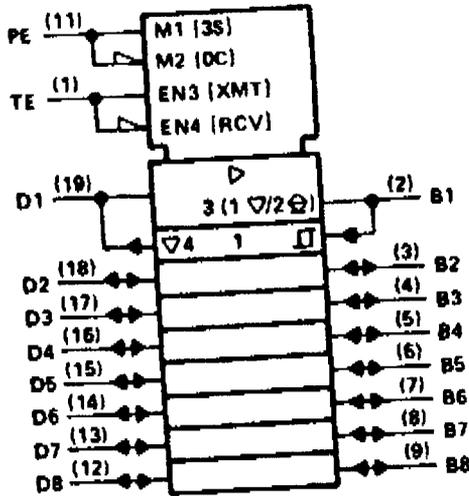


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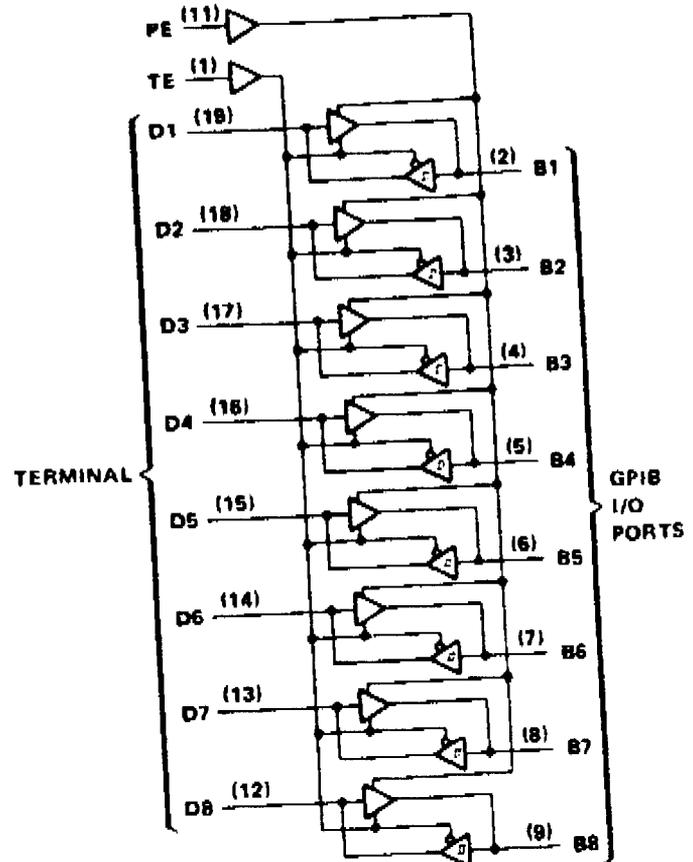
# SN75160B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

logic symbol<sup>1</sup>

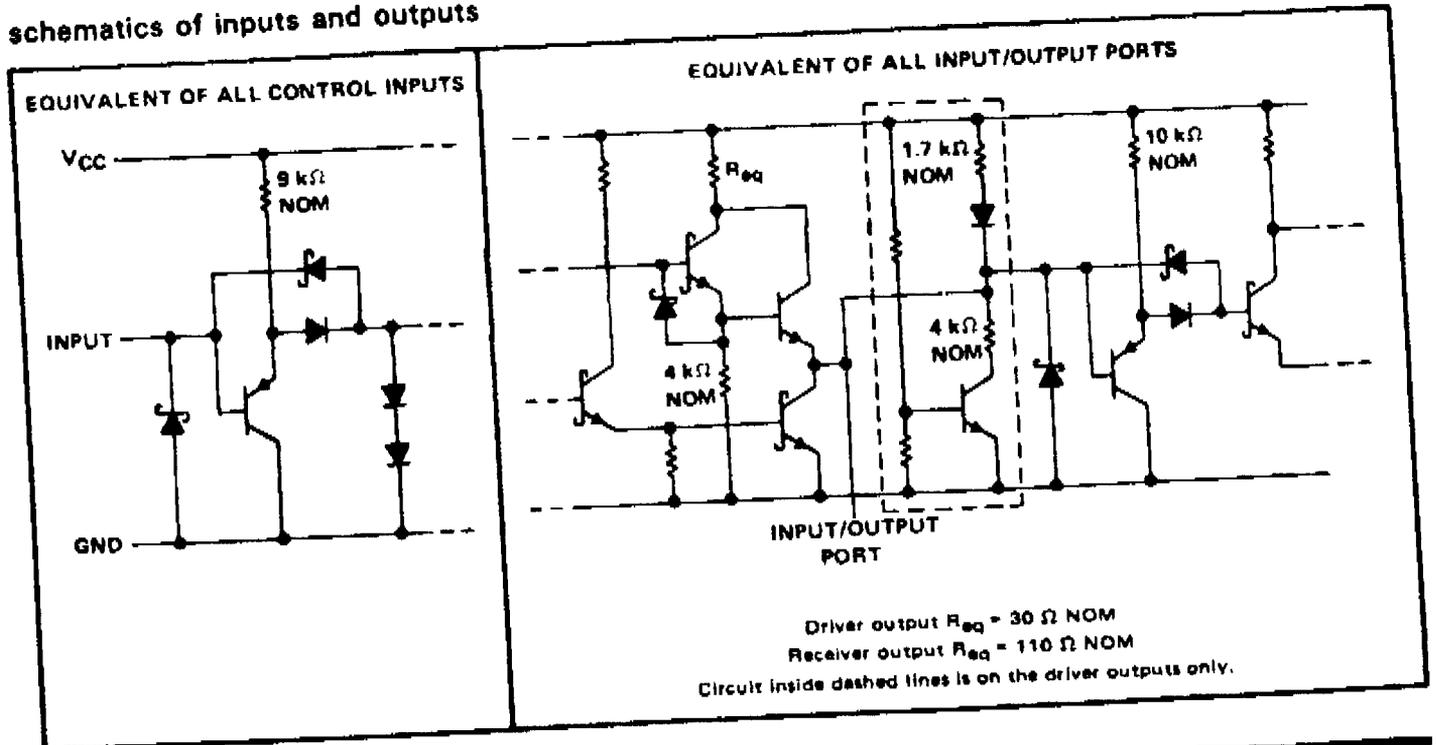


<sup>1</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 ▽ Designates 3-state outputs.  
 ⊕ Designates passive-pullup outputs.

logic diagram (positive logic)



schematics of inputs and outputs



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SN95160B SN75160B

# OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
<del>DW package</del>	<del>1125 mW</del>
J package	1375 mW
FK package	1375-1150 mW
Operating free-air temperature range	-55°C to 70°C 100°C
Storage temperature range	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C

- NOTES 1. All voltage values are with respect to network ground terminal.  
 2. For operation above 25°C free-air temperature, derate the DW package at the rate of 0.0 mW/°C, the N package at the rate of 0.2 mW/°C, and the J package at the rate of 11.0 mW/°C. In the J package, SN75160B chips are alloy mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.75	5	5.25	V
High-level input voltage, V <sub>IH</sub> , PE & TE	2			V
Low-level input voltage, V <sub>IL</sub> , PE & TE			0.8	V
High-level output current, I <sub>OH</sub>	Bus ports with pull-ups active		-5.2	mA
	Terminal ports		-800	μA
Low-level output current, I <sub>OL</sub>	Bus ports		48	mA
	Terminal ports		16	mA
Operating free air temperature, T <sub>A</sub>	-55		70	°C

HIGH-level input voltage, V <sub>IH</sub> , Bus & Terminal	25°C	2	V
	Full Range	2.1	V
Low-level input voltage, V <sub>IL</sub> , Bus & Terminal	25°C	.8	V
	Full Range	.7	V



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# OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SN95160B

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT	
V <sub>IK</sub>	Input clamp voltage		I <sub>I</sub> = -18 mA, V <sub>CC</sub> = Min.		-0.8	-1.5	V	
V <sub>HYS</sub>	Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	Bus	V <sub>CC</sub> = 5V	0.4	0.65		V	
V <sub>OH</sub>	High-level output voltage	Terminal	I <sub>OH</sub> = -800 μA, TE at 0.8 V, V <sub>CC</sub> = Min.	2.7	3.5		V	
		Bus	I <sub>OH</sub> = -5.2 mA, PE and TE at 2 V, V <sub>CC</sub> = Min.	2.5	3.3			
V <sub>OL</sub>	Low-level output voltage	Terminal	I <sub>OL</sub> = 16 mA, TE at 0.8 V, V <sub>CC</sub> = Min.		0.3	0.5	V	
		Bus	I <sub>OL</sub> = 48 mA, TE at 2 V, V <sub>CC</sub> = Min.		0.35	0.5		
I <sub>I</sub>	Input current at maximum input voltage	Terminal	V <sub>I</sub> = 5.5 V, V <sub>CC</sub> = Max.		0.2	100	μA	
I <sub>IH</sub>	High-level input current	Terminal	V <sub>I</sub> = 2.7 V, V <sub>CC</sub> = Max.		0.1	20	μA	
I <sub>IL</sub>	Low-level input current	Terminal	V <sub>I</sub> = 0.5 V, V <sub>CC</sub> = Max.		-10	-100	μA	
V <sub>I/O(bus)</sub>	Voltage at bus port		Driver disabled V <sub>CC</sub> = 5V	I <sub>I(bus)</sub> = 0 I <sub>I(bus)</sub> = -12 mA	2.5	3.0	3.7	V
I <sub>I/O(bus)</sub>	Current into bus port	Power on	Driver disabled V <sub>CC</sub> = 5V	V <sub>I(bus)</sub> = -1.5 V to 0.4 V		-1.3		
				V <sub>I(bus)</sub> = 0.4 V to 2.5 V		0	-3.2	
				V <sub>I(bus)</sub> = 2.5 V to 3.7 V			+2.5	
				V <sub>I(bus)</sub> = 3.7 V to 5 V		0	-3.2	
				V <sub>I(bus)</sub> = 5 V to 5.5 V		0.7	2.5	
				V <sub>I(bus)</sub> = 0 V to 2.5 V			+40	
I <sub>OS</sub>	Short-circuit output current	Terminal	V <sub>CC</sub> = Max.		-15	-35	-75	mA
		Bus	V <sub>CC</sub> = Max.		-25	-50	-125	
I <sub>CC</sub>	Supply current		No load V <sub>CC</sub> = Max.	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
C <sub>I/O(bus)</sub>	Bus-port capacitance		V <sub>CC</sub> = 5 V to 0 V. f = 1 MHz	V <sub>I/O</sub> = 0 to 2 V.		30		pF

<sup>†</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

switching characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 15 pF, T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Terminal	Bus	C <sub>L</sub> = 30 pF. See Figure 1		14	20	ns
t <sub>PHL</sub>					14	20	
t <sub>PLH</sub>	Bus	Terminal	C <sub>L</sub> = 30 pF. See Figure 2		10	20	ns
t <sub>PHL</sub>					15	22	
t <sub>PZH</sub>	TE	Bus	See Figure 3		25	35	ns
t <sub>PHZ</sub>					13	22	
t <sub>PZL</sub>					22	35	
t <sub>PLZ</sub>					22	32	
t <sub>PZH</sub>	TE	Terminal	See Figure 4		20	30	ns
t <sub>PHZ</sub>					12	20	
t <sub>PZL</sub>					23	32	
t <sub>PLZ</sub>				19	30		
t <sub>en</sub>	PE	Bus	See Figure 5		15	22	ns
t <sub>dis</sub>					13	20	

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PARAMETER MEASUREMENT INFORMATION

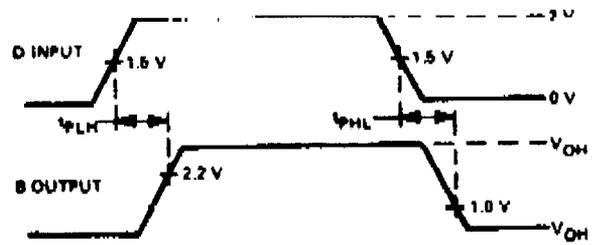
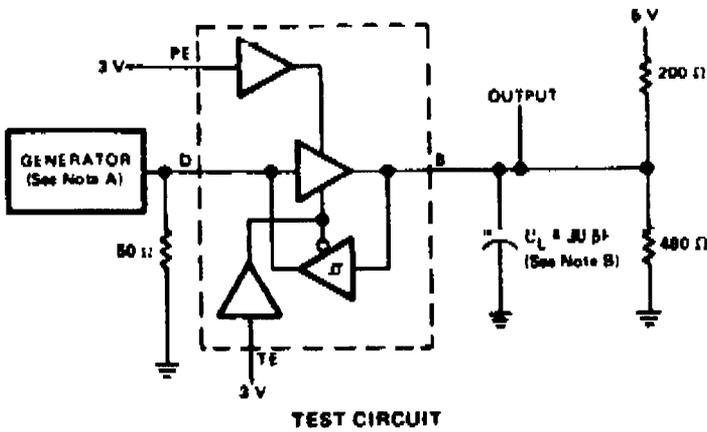


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

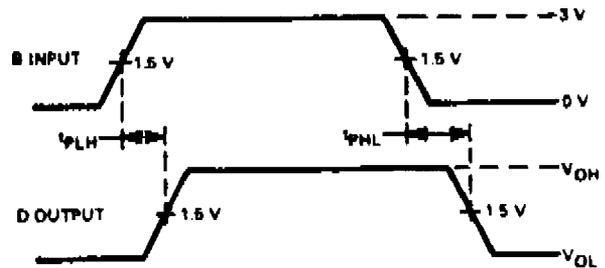
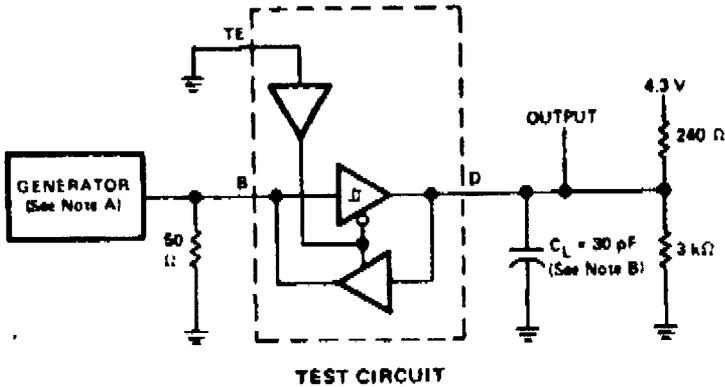


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

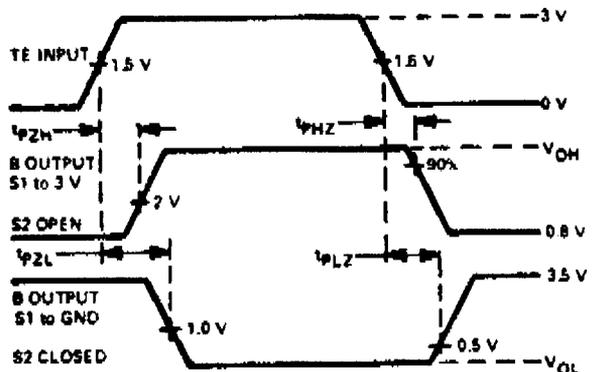
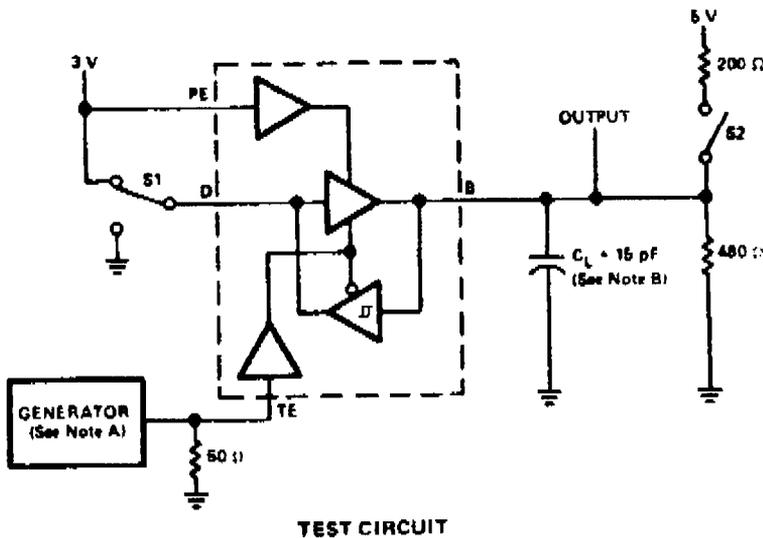


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  8 ns,  $t_f \leq$  6 ns,  $Z_{out} = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

6 ns



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PARAMETER MEASUREMENT INFORMATION

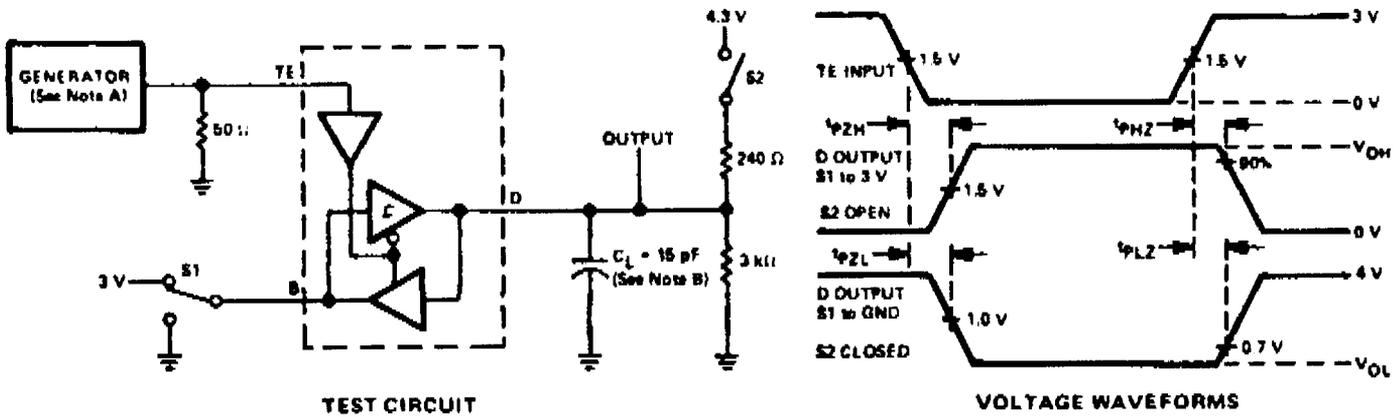


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

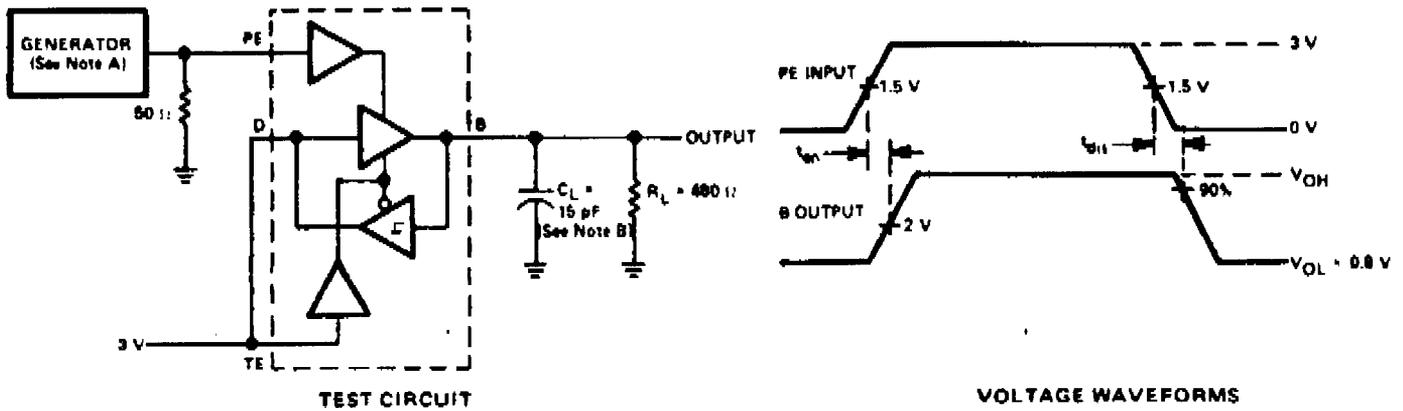


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_f \leq$  6 ns,  $t_r \leq$  6 ns,  $Z_{out} = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance

6 ns

**TYPICAL CHARACTERISTICS**

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE  
 vs  
 HIGH-LEVEL OUTPUT CURRENT

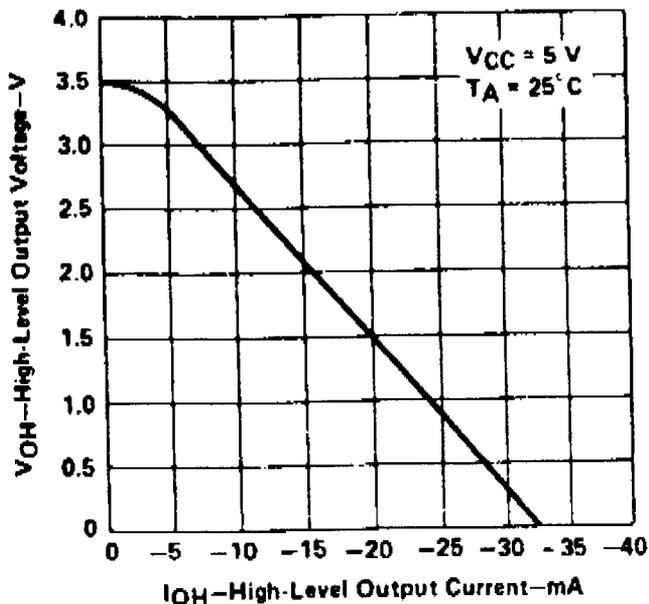


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

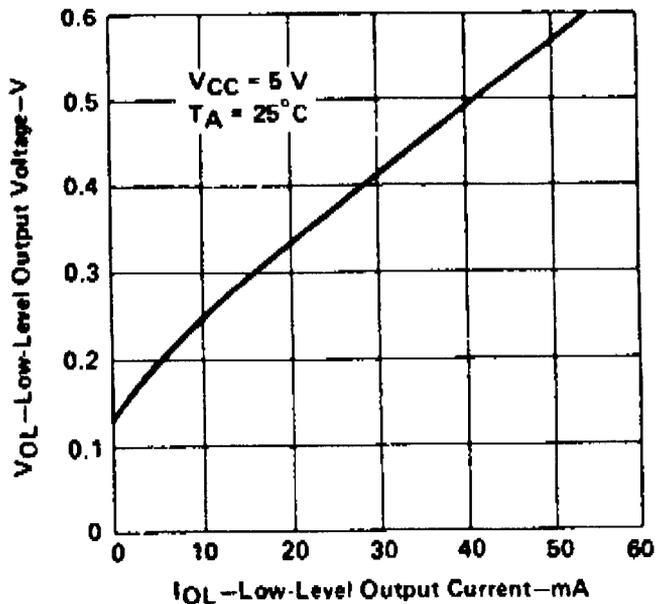


FIGURE 7

TERMINAL OUTPUT VOLTAGE  
 vs  
 BUS INPUT VOLTAGE

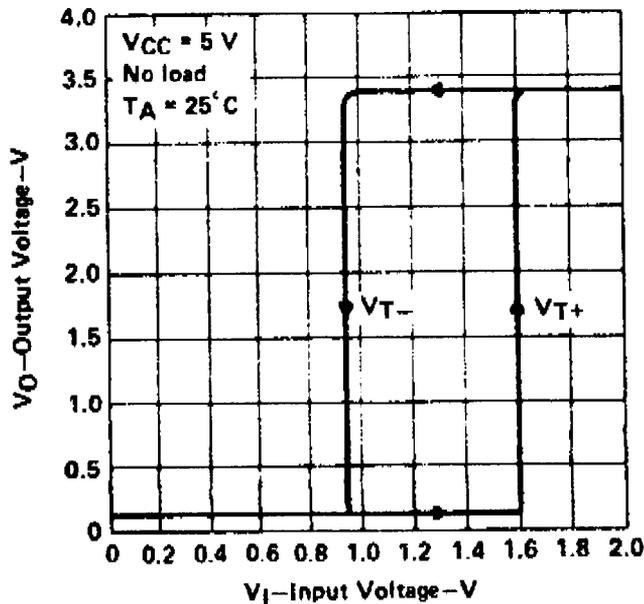


FIGURE 8



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**TYPICAL CHARACTERISTICS**

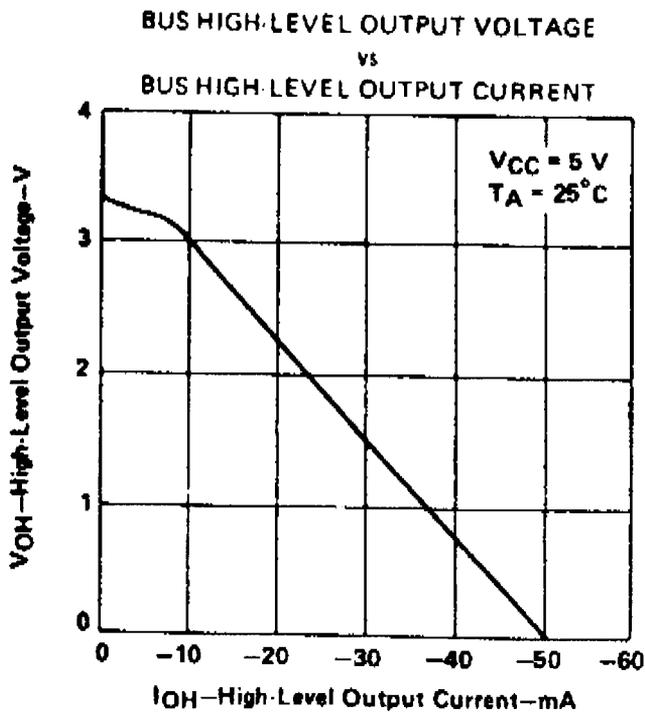


FIGURE 9

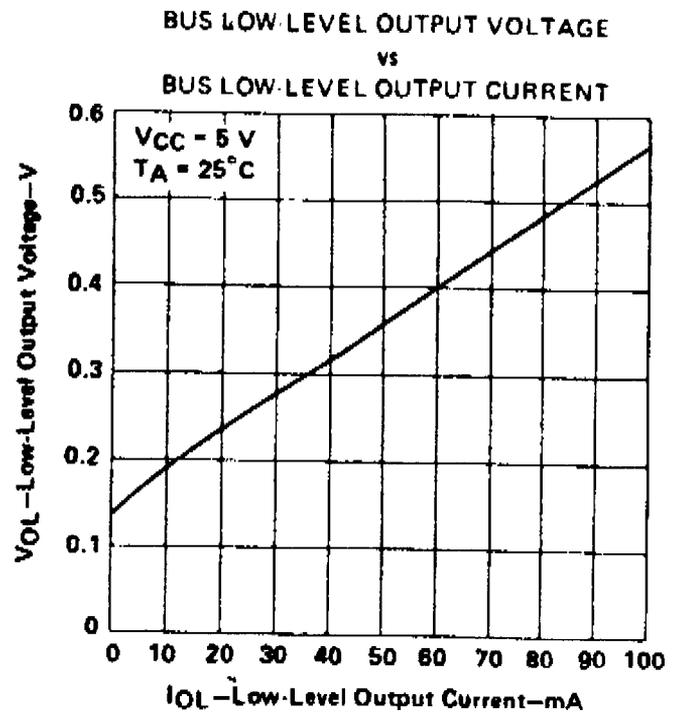


FIGURE 10

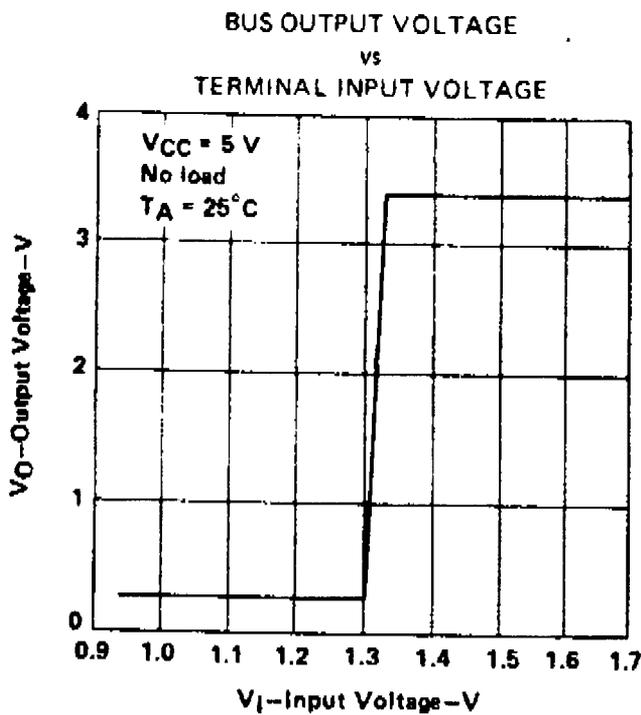


FIGURE 11

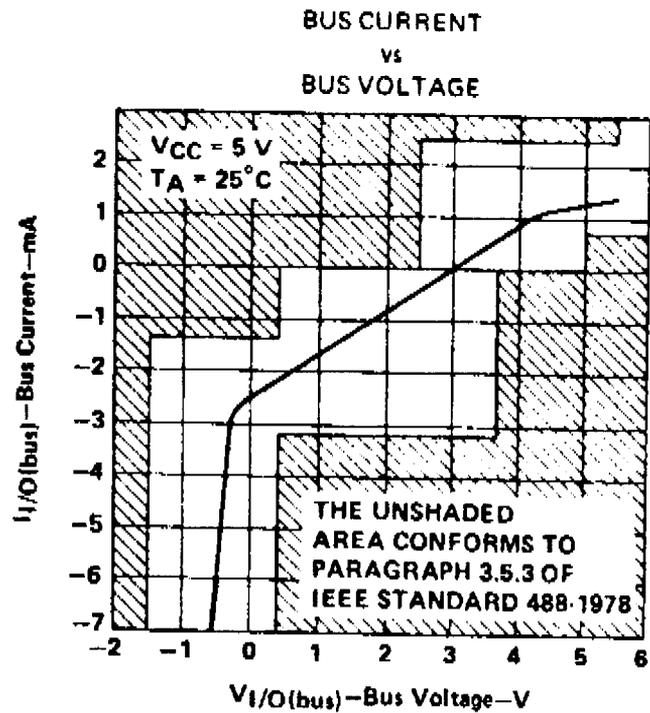


FIGURE 12