

TIBPALR19L8C, TIBPALR19R4C, TIBPALR19R6C, TIBPALR19R8C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

D2709, DECEMBER 1982 - REVISED AUGUST 1989

- High-Performance Operation . . . 30 MHz
- Preload Capability on Output Registers
- DIP Options Include Both 300-mil Plastic and 600-mil Ceramic
- Dependable Texas Instruments Quality and Reliability

DEVICE	I/O INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
*PALR19L8	11	2	2	0	6
*PALR19R4	11	0	0	4 (3-state buffers)	4
*PALR19R6	11	0	0	6 (3-state buffers)	2
*PALR19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type input registers. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

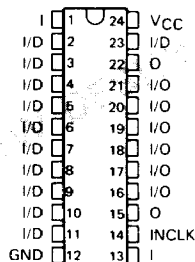
A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

INPUT REGISTER FUNCTION TABLE

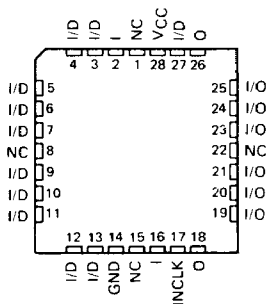
INPUT		OUTPUT OF INPUT REGISTER	
INCLK	D	H	L
↑	L	L	L
L	X	Q ₀	Q ₀

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975. PAL is a registered trademark of Monolithic Memories Inc.

TIBPALR19L8*
JW OR NT PACKAGE
(TOP VIEW)



TIBPALR19L8*
FN PACKAGE
(TOP VIEW)

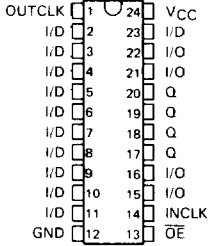


NC—No internal connection

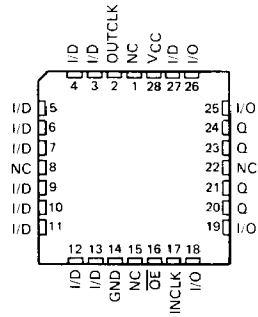
Pin assignments in operating mode

TIBPALR19R4C, TIBPALR19R6C, TIBPALR19R8C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

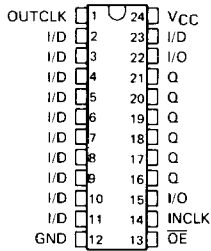
TIBPALR19R4'
JW OR NT PACKAGE
(TOP VIEW)



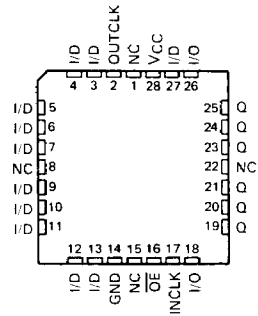
TIBPALR19R4'
FN PACKAGE
(TOP VIEW)



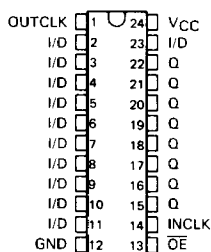
TIBPALR19R6'
JW OR NT PACKAGE
(TOP VIEW)



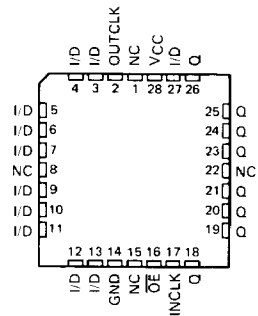
TIBPALR19R6'
FN PACKAGE
(TOP VIEW)



TIBPALR19R8'
JW OR NT PACKAGE
(TOP VIEW)



TIBPALR19R8'
FN PACKAGE
(TOP VIEW)

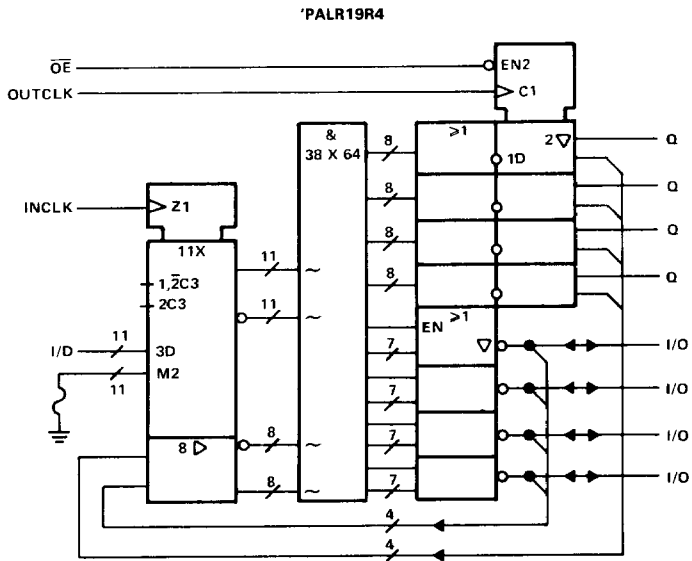
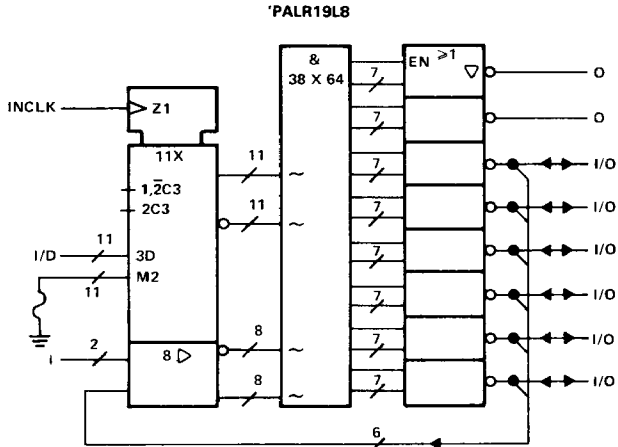


Pin assignments in operating mode

NC—No internal connection

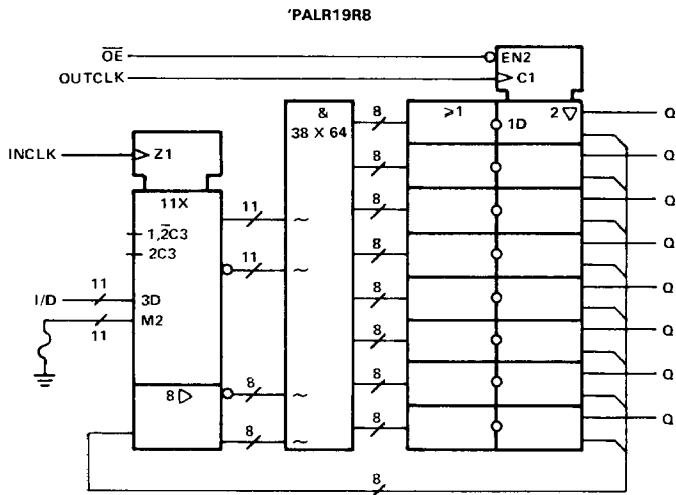
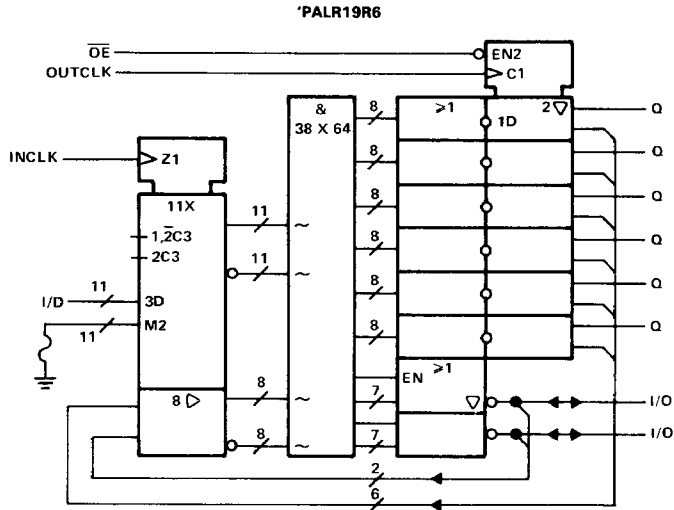
TIBPALR19L8C, TIBPALR19R4C
HIGH-PERFORMANCE REGISTERED-INPUT PAL[®] CIRCUITS

functional block diagrams (positive logic)



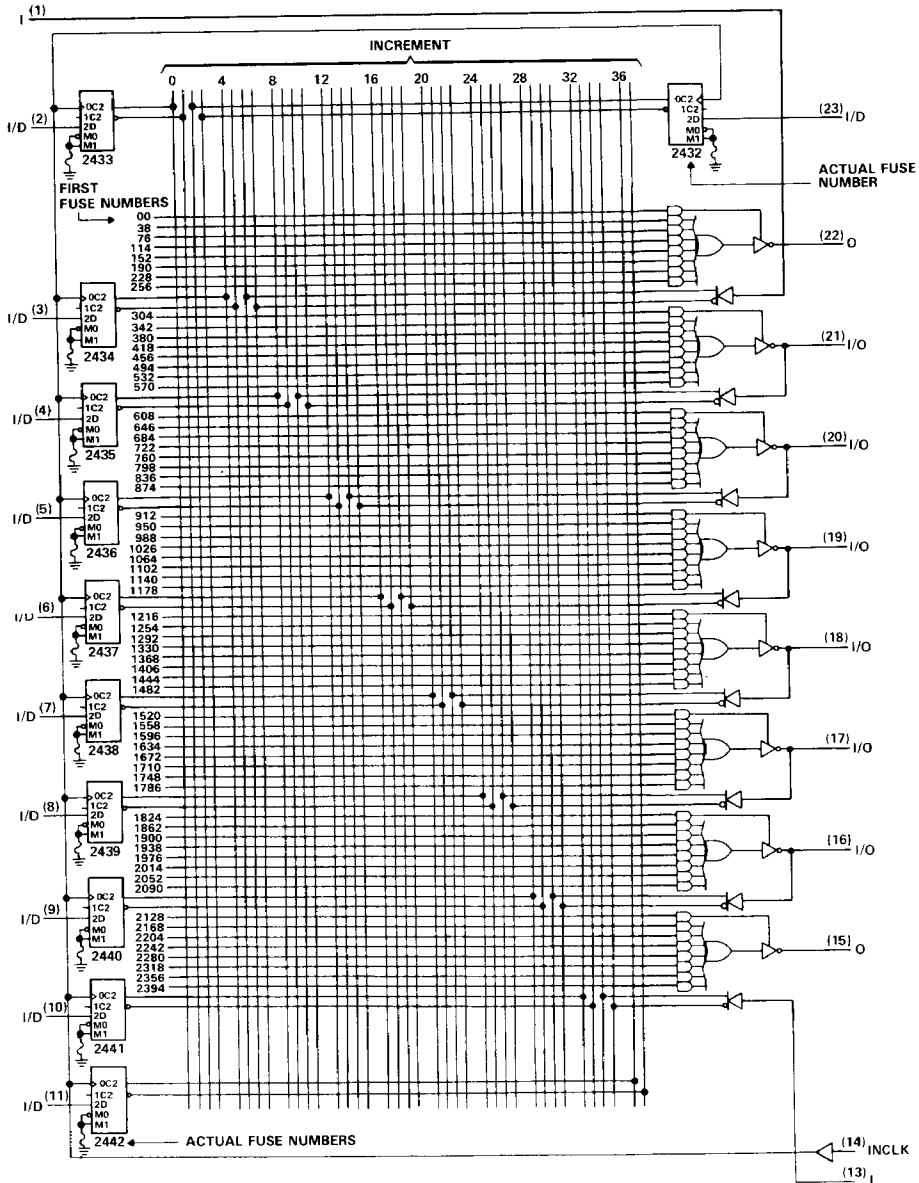
TIBPALR19R6C, TIBPALR19R8C
HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

functional block diagrams (positive logic)



TIBPALR19L8C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

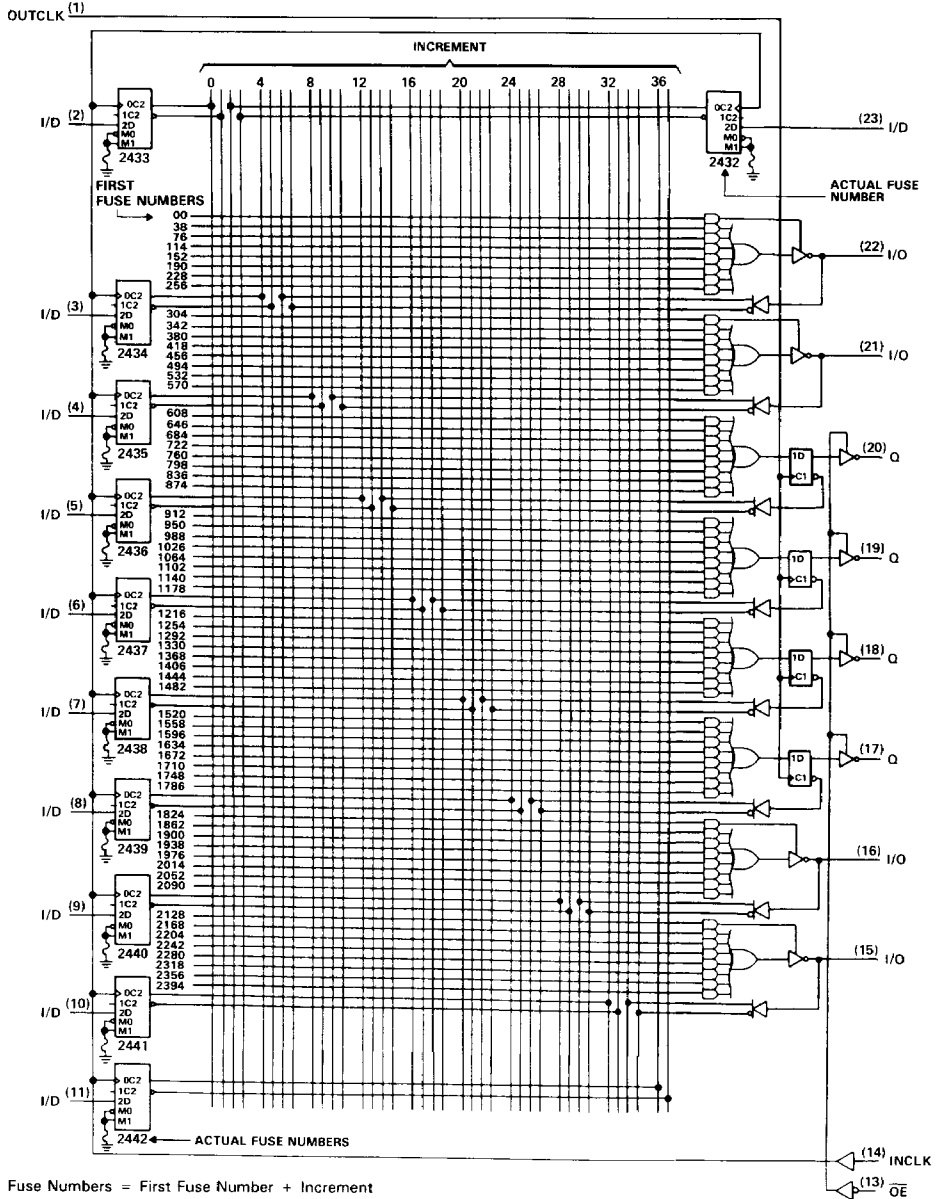
logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TIBPALR19R4C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

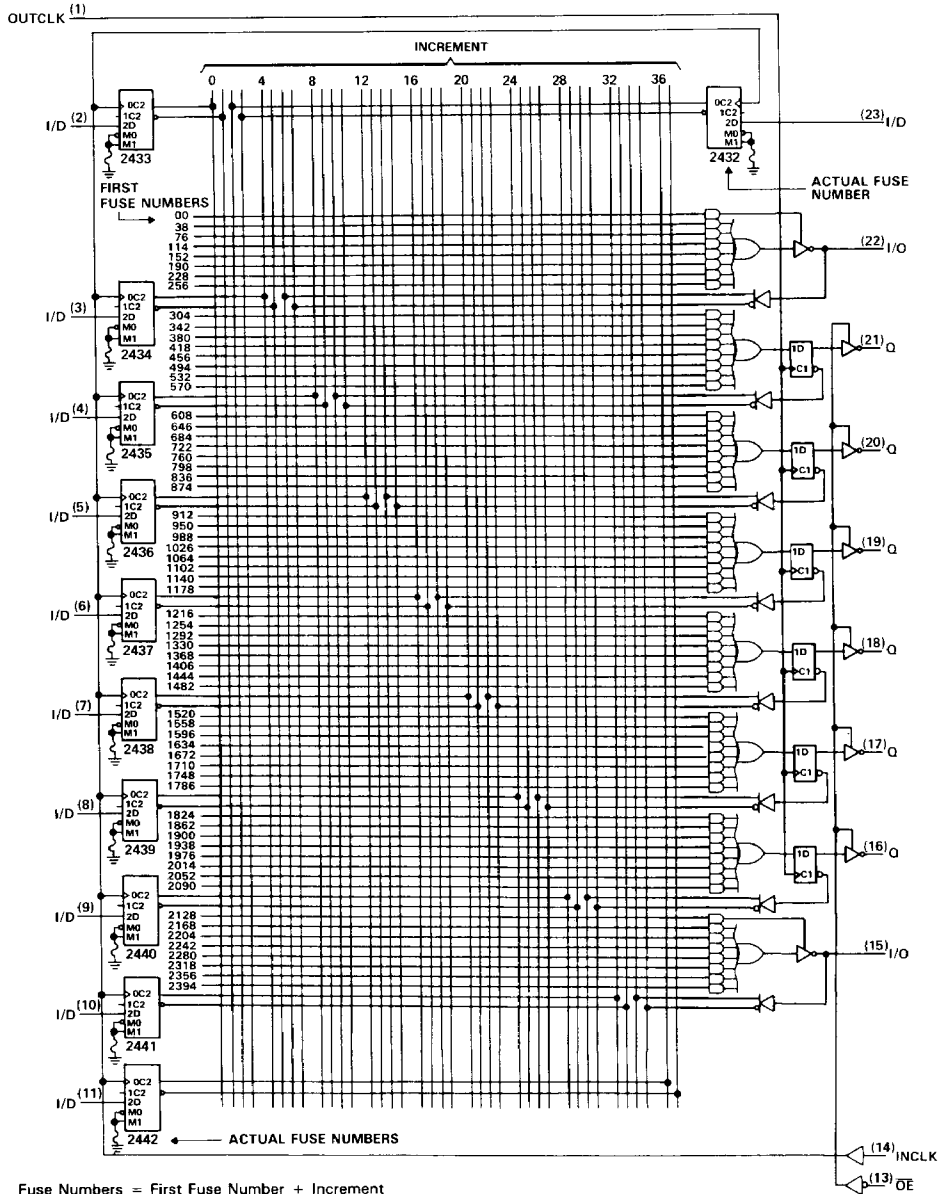
logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TIBPALR196C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

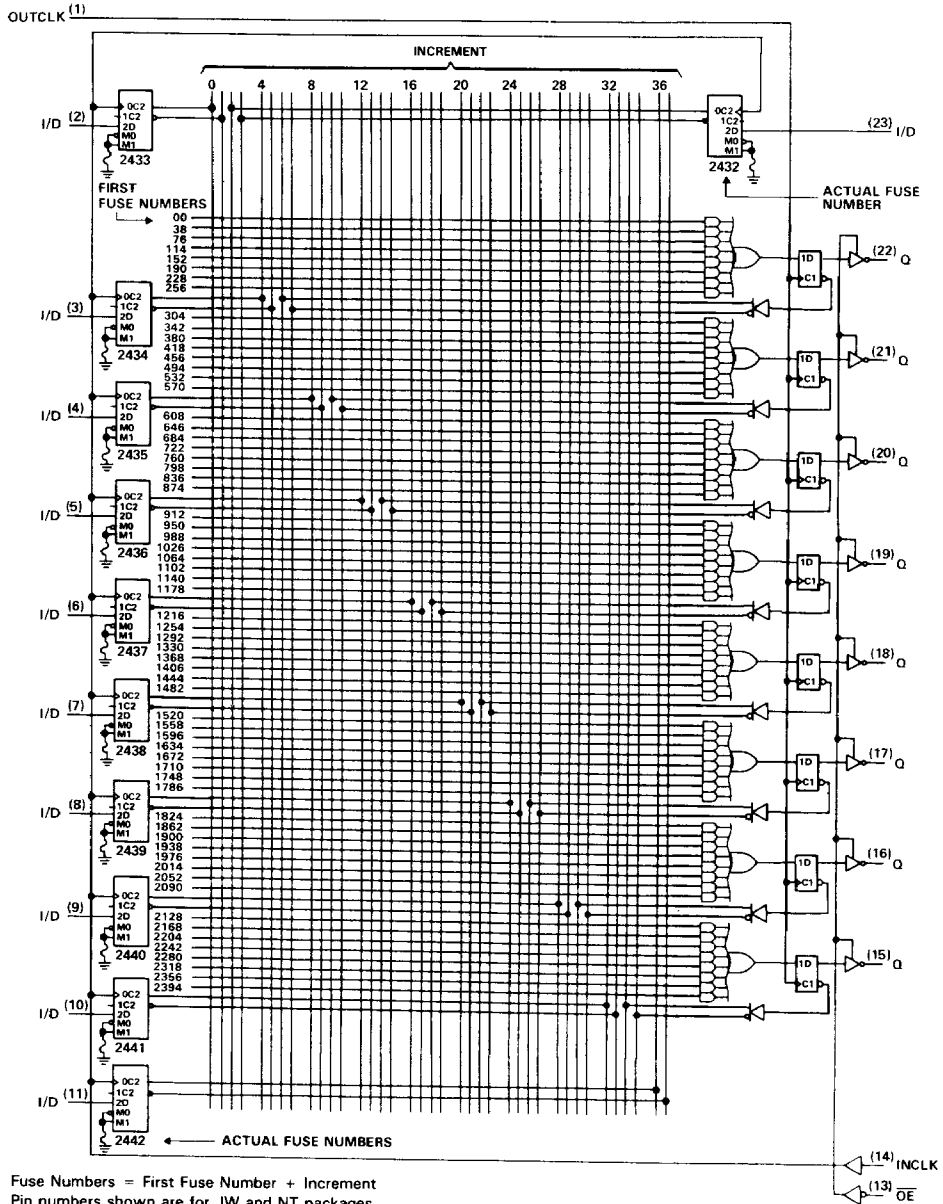
logic diagram (positive logic)



Fuse Numbers = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

TIBPALR19R8C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

logic diagram (positive logic)



TIBPALR19L8C, TIBPALR19R4C, TIBPALR19R6C, TIBPALR19R8C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to a disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	INCLK	0	30	MHz
		OUTCLK	0	30	
t_w	Pulse duration, clock	INCLK high	15		ns
		INCLK low	15		
		OUTCLK high	15		
		OUTCLK low	15		
t_{su}	Setup time	Data before INCLK↑	10		ns
		Data before OUTCLK↑	25		
		INCLK↑ before OUTCLK↑ (See Note 2)	25		
t_h	Hold time	Data after INCLK↑	5		ns
		Data after OUTCLK↑	0		
T_A	Operating free-air temperature	0		70	°C

NOTE 2: This setup time ensures the output registers will see stable data from the input registers.

TIBPALR19L8C, TIBPALR19R4C, TIBPALR19R6C, TIBPALR19R8C HIGH-PERFORMANCE REGISTERED-INPUT PAL® CIRCUITS

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IJK}		V _{CC} = 4.75 V,	I _I = -18 mA			-1.5	V
V _{OH}		V _{CC} = 4.75 V,	I _{OH} = -3.2 mA	2.4	3.3		V
V _{OL}		V _{CC} = 4.75 V,	I _{OL} = 24 mA		0.35	0.5	V
I _{OZH}	Outputs	V _{CC} = 5.25 V,	V _{IH} = 2.7 V			20	μA
	I/O ports					100	
I _{OZL}	Outputs	V _{CC} = 5.25 V,	V _{IH} = 0.4 V			-20	μA
	I/O ports					-250	
I _I	OE Input	V _{CC} = 5.25 V,	V _I = 5.5 V			0.2	mA
	I/D Inputs					0.1	
	All others					0.1	
I _{IH}	OE Input	V _{CC} = 5.25 V,	V _I = 2.7 V			40	μA
	I/D Inputs					20	
	All others					20	
I _{IL}	OE Input	V _{CC} = 5.25 V,	V _I = 0.4 V			-0.4	mA
	I/D Inputs					-0.6	
	All others					-0.2	
I _O [‡]		V _{CC} = 5.25 V,	V _O = 2.25 V	-30		-125	mA
I _{CC}		V _{CC} = 5.25 V,	V _I = 0 V, Outputs open		150	210	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
f _{max}	INCLK [†]	I/O, 0	R1 = 500 Ω, R2 = 500 Ω, C _L = 50 pF, See Figure 1	30			MHz
t _{pd}	I, I/O	I/O, 0			15	25	ns
t _{pd}	I/D [§]	I/O, 0			20	35	ns
t _{pd}	INCLK [†]	I/O, 0			20	35	ns
t _{pd}	OUTCLK [†]	Q			10	20	ns
t _{en}	OE [†]	Q			10	20	ns
t _{en}	I, I/O	I/O, 0			14	25	ns
t _{en}	I/D [§]	I/O, 0			27	40	ns
t _{en}	INCLK [†]	I/O, 0			27	40	ns
t _{dis}	OE [†]	Q			11	20	ns
t _{dis}	I, I/O	I/O, 0			12	25	ns
t _{dis}	I/D [§]	I/O, 0			13	30	ns
t _{dis}	INCLK [†]	I/O, 0			13	25	ns

[†]All typical values are V_{CC} = 5 V, T_A = 25°C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

[§]Input configured as an input buffer.

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programming information

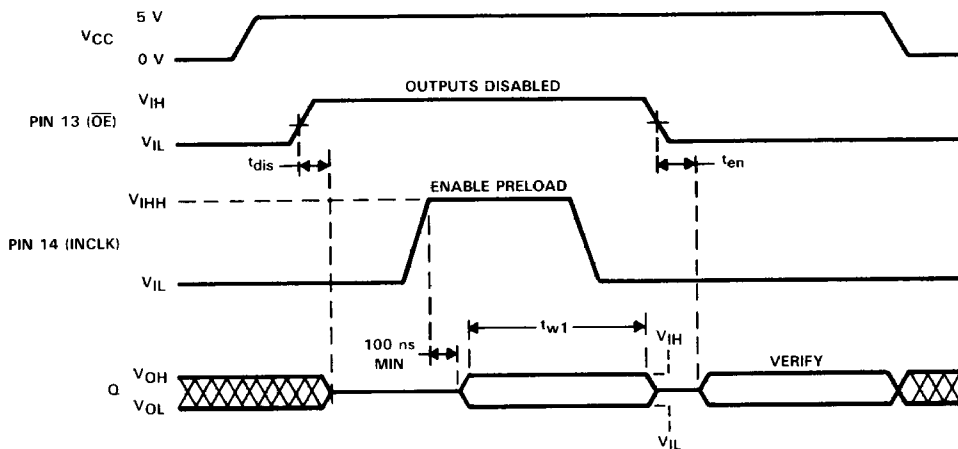
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

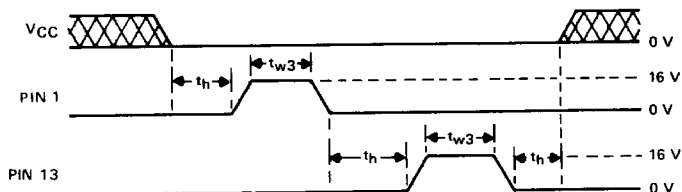
preload procedure for registered outputs (see Note 3)

- Step 1 Pin 13 to V_{IH} , Pin 1 to V_{IL} , and V_{CC} to 5 volts.
- Step 2 Pin 14 to V_{IHH}
- Step 3 At Q outputs, apply V_{IL} to preload a low and V_{IH} to preload a high.
- Step 4 Pin 14 to V_{IL} .
- Step 5 Remove the voltages applied to the outputs.
- Step 6 Pin 13 to V_{IL}
- Step 7 Check the output states to verify preload.

preload waveforms (see Note 3)

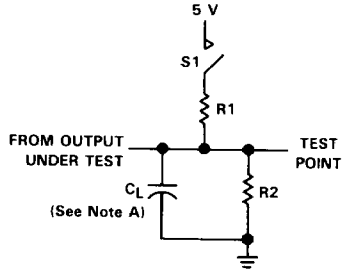


security fuse programming (see Note 3)

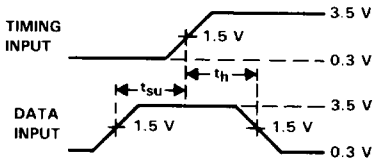


NOTE 3: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

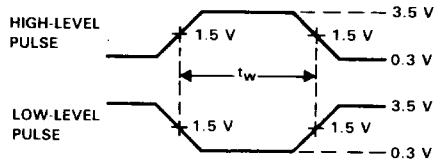
PARAMETER MEASUREMENT INFORMATION



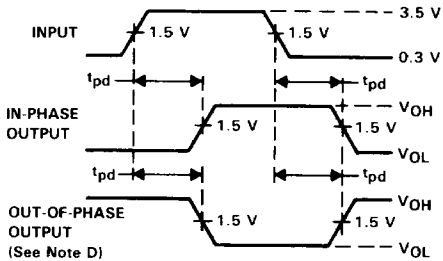
**LOAD CIRCUIT FOR
THREE-STATE OUTPUTS**



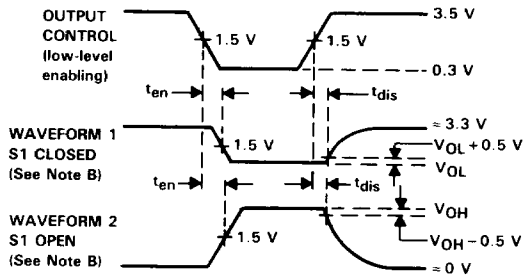
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1