

FEATURES

192-Bit Pixel Port Allows 2048 × 2048 × 24 Screen Resolution
360 MHz, 24-Bit True-Color Operation
Triple 8-Bit D/A Converters
8:1 Multiplexing
Onboard PLL
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Internal Voltage Reference
Standard 8-Bit MPU I/O Interface
DAC-DAC Matching: Typ 2%, Adjustable to 0.02%
+5 V CMOS Monolithic Construction
304-Pin PQFP Package

APPLICATIONS

Ultrahigh Resolution Color Graphics
Image Processing
Drives 24-Bit Color 2K × 2K Monitors

GENERAL DESCRIPTION

The ADV7129 is a complete analog output, video DAC on a single CMOS (ADV®) monolithic chip. The part is specifically designed for use in the highest resolution graphics and imaging systems. The ultimate level of integration, comprised of 360 MHz triple 8-bit DACs, a programmable pixel port, an internal voltage reference and an onboard PLL, makes the ADV7129 the only choice for the very highest level of performance and functionality.

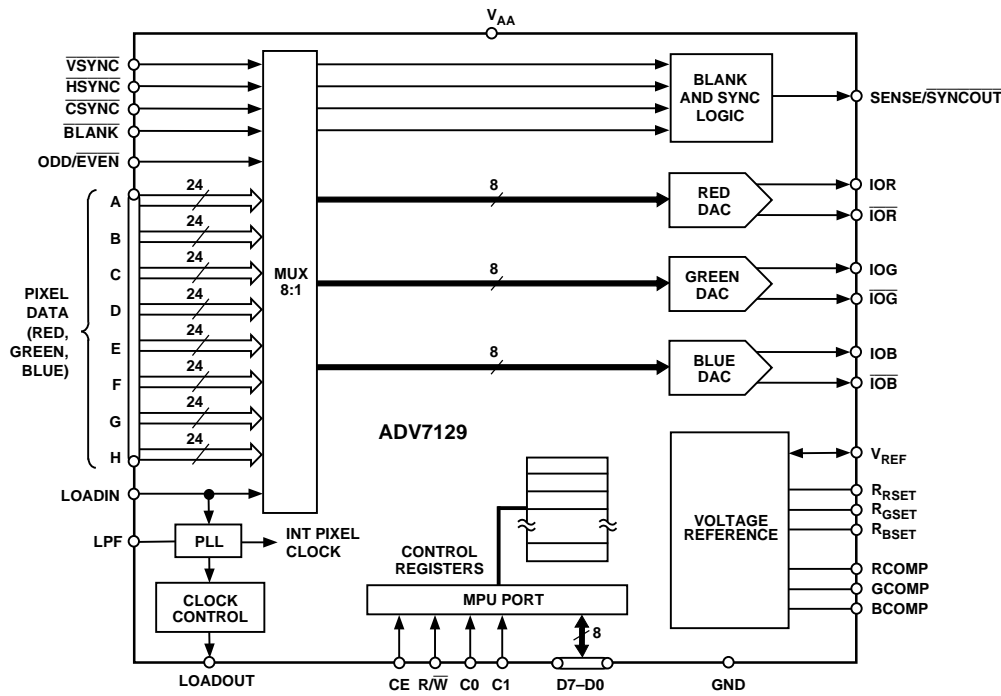
The device consists of three high speed, 8-bit, video D/A converters (RGB). An onboard phase locked loop clock generator is provided to provide high speed operation without requiring high speed external crystal or clock circuitry.

The part is fully controlled through the MPU port by the onboard command registers. This MPU port may be updated at any time without causing sparkle effects on the screen.

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FUNCTIONAL BLOCK DIAGRAM



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REV. 0

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ADV7129—SPECIFICATIONS ($V_{AA}^1 = +5\text{ V}$, $V_{REF} = +1.235\text{ V}$, $R_{RSET}, R_{GSET}, R_{BSET} = 280\ \Omega$, $R_L = 25\ \Omega$, $C_L = 10\ \text{pF}$. All specifications T_{MIN} to T_{MAX}^2 unless otherwise noted.)

All Versions	Conditions ¹	Min	Typ	Max	Units
STATIC PERFORMANCE³ Resolution (Each DAC) Accuracy (Each DAC) Integral Nonlinearity Differential Nonlinearity Gray Scale Error	Guaranteed Monotonic			8 ± 1 ± 1 ± 5	Bits LSB LSB % Gray Scale Binary Coding
DIGITAL INPUTS Input High Voltage, V_{INH} Input Low Voltage, V_{INL} Input Current, I_{IN} Input Capacitance, C_{IN}	$V_{IN} = 0.4\text{ V}$ or 2.4 V	2.0 GND - 0.5		$V_{AA} + 0.5$ 0.8 ± 10	V V μA pF
DIGITAL OUTPUTS Output High Voltage, V_{OH} Output Low Voltage, V_{OL} Floating-State Leakage Current Floating-State Output Capacitance	$I_{OH} = -400\ \mu\text{A}$ $I_{OL} = 3.2\ \text{mA}$	2.4		0.4 ± 10	V V μA pF
ANALOG OUTPUTS Gray Scale Current Range Output Current White Level Relative to Black Black Level Relative to Blank Blank Level, Sync Disabled LSB Size DAC to DAC Matching Output Compliance, V_{OC} Output Impedance, R_{OUT} Output Capacitance, C_{OUT}		10		60	mA
		50.16	52.80	55.44	mA
		4.1	4.32	4.54	mA
		0	5	50	μA
			223		μA
			2	5	%
		0		1.4	V
			10		k Ω
			20		pF
VOLTAGE REFERENCE Voltage Reference Range, V_{REF} Input Current, I_{VREF}	$V_{REF} = 1.234\text{ V}$ for Specified Performance	1.14	1.235	1.30	V
			5		μA
POWER REQUIREMENTS V_{AA} I_{AA}^4 I_{AA}^4 Power Supply Rejection Ratio	Analog Current Digital Current @ 360 MHz		5	160 200	V mA mA
				360 400	mA mA
				0.12	%/%
DYNAMIC PERFORMANCE Clock and Data Feedthrough ⁵ Glitch Impulse DAC to DAC Crosstalk ⁶			-30		dB
			50		pV secs
			-23		dB

NOTES

¹ $\pm 5\%$ for all versions.

²Temperature range (T_{MIN} to T_{MAX}), 0°C to $+70^\circ\text{C}$, T_J (Silicon Junction Temperature) $\leq 100^\circ\text{C}$.

³Static performance is measured with the Gain Error Registers set to 00H (disabled).

⁴ I_{AA} is measured with a typical dynamic pattern, satisfying the absolute maximum current spec for the DACs.

⁵Clock and Data Feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough. TTL input values are 0 V to 3 V, with input rise/fall times $\geq 3\text{ ns}$, measured at the 10% and 90% points. Timing reference points are at 50% for inputs and outputs.

⁶DAC to DAC crosstalk is measured by holding one DAC high while the other two DACs are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING SPECIFICATIONS ($V_{AA}^2 = +5\text{ V}$, $V_{REF} = +1.235\text{ V}$, $R_{RSET}, R_{GSET}, R_{BSET} = 280\ \Omega$, $R_L = 25\ \Omega$ for IOG, IOR, IOB, $C_L = 10\text{ pF}$. All specifications T_{MIN} to T_{MAX}^3 unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Units
CLOCK CONTROL & PIXEL PORT⁴					
LOADIN Clocking Rate, f_{LCLK}		10		45	MHz
LOADIN Cycle Time, t_1		16.67			ns
LOADIN Low Time, t_2		6.67			ns
LOADIN High Time, t_3		6.67			ns
LOADIN to LOADOUT Delay, t_4			5		ns
Pixel Setup Time, t_5		1	0		ns
Pixel Hold Time, t_6		4	2		ns
MPU PORT					
$\overline{R/W}$, C0, C1 Setup Time, t_7		10	2.5		ns
$\overline{R/W}$, C0, C1 Hold Time, t_8		10	0.5		ns
\overline{CE} Low Time, t_9		25			ns
\overline{CE} High Time, t_{10}		25			ns
\overline{CE} Asserted to Data-Bus Driven, t_{11}		2	5		ns
\overline{CE} Asserted to Data-Bus Valid, t_{12}				20	ns
\overline{CE} Negated to Data-Bus Invalid, t_{13}		1			ns
\overline{CE} Negated to Data-Bus Three Stated, t_{14}				15	ns
Write Data (D7–D0) Setup Time, t_{15}		10			ns
Write Data (D7–D0) Hold Time, t_{16}		10			ns
ANALOG OUTPUTS⁵					
Analog Output Delay, t_{17}	@ 360 MHz		5		ns
Analog Output Rise/Fall Time, t_{18}			0.8		ns
Analog Output Transition Time, t_{19}			25		ns
RGB Analog Output Skew, t_{SK}				1.5	ns
Pipeline Delay, t_{PD}			19		PCLKs
PLL PERFORMANCE⁶					
Jitter (1σ)	(LOADIN = 45 MHz)		55		ps rms

NOTES

¹TTL inputs values are 0 V to 3 V with input rise/fall times ≥ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. Databus (D7–D0) loaded as shown in Figure 1. Digital output load for SENSE ≤ 30 pF.

² $\pm 5\%$ for all versions.

³Temperature range (T_{MIN} to T_{MAX}), 0°C to +70°C.

⁴Pixel Port consists of the following inputs: Pixel Inputs: RED [A-H], BLUE [A-H], GREEN [A-H].

⁵Output Delay is measured from the 50% rising edge of LOADIN to the 50% point of full-scale transition on the A pixel. t_{17} includes the analog delay due to DACs and internal gate transitions plus the pipeline stages delay. The output delay for pixels B-H will be the output delay to the A pixel (t_{17}) plus the appropriate number of clock cycles. Output rise/fall time is measured between the 10% and 90% points of full-scale transition. Settling time is measured from the 50% point of full-scale transition to the output remaining within 1%. (Settling Time does not include clock and data feedthrough.)

⁶Jitter is measured by triggering on the output clock, delayed by 15 μ s and then measuring the time period from the trigger edge to the next edge of the output clock after the delay. This measurement is repeated multiple times and the rms value is determined.

Specifications subject to change without notice.

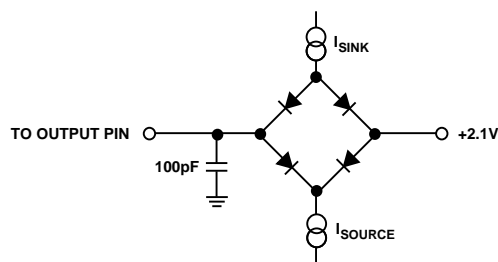


Figure 1. LOADIN vs. Pixel Input Data

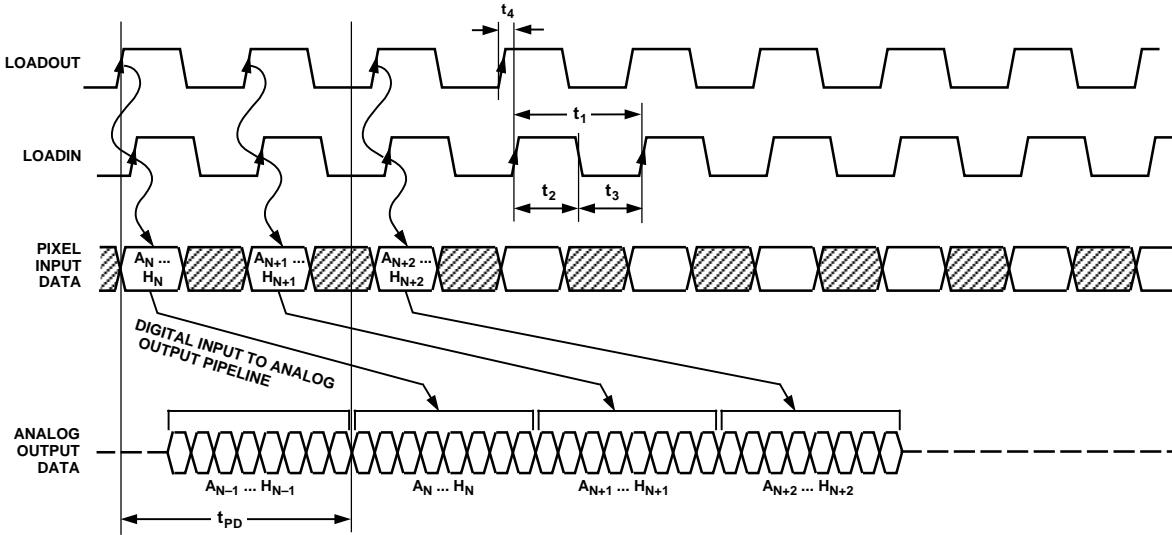


Figure 2. LOADIN vs. Pixel Input Data

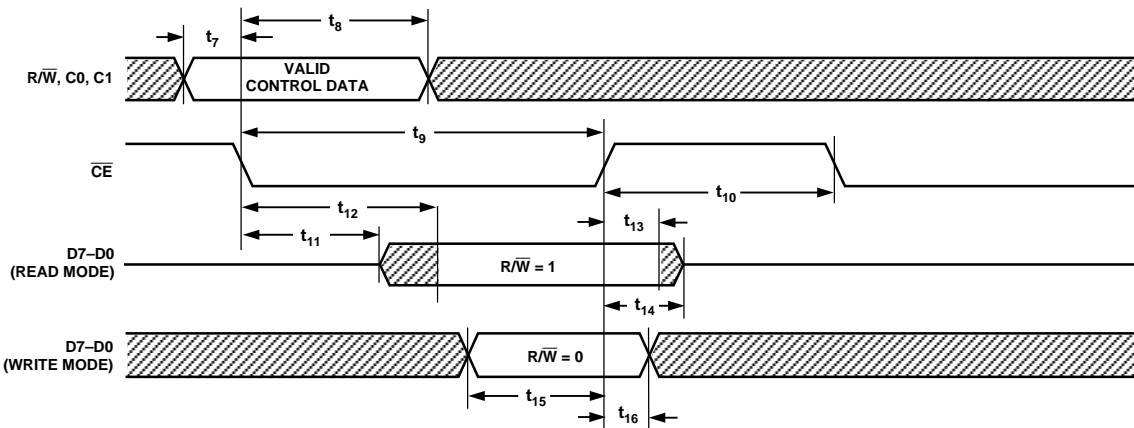
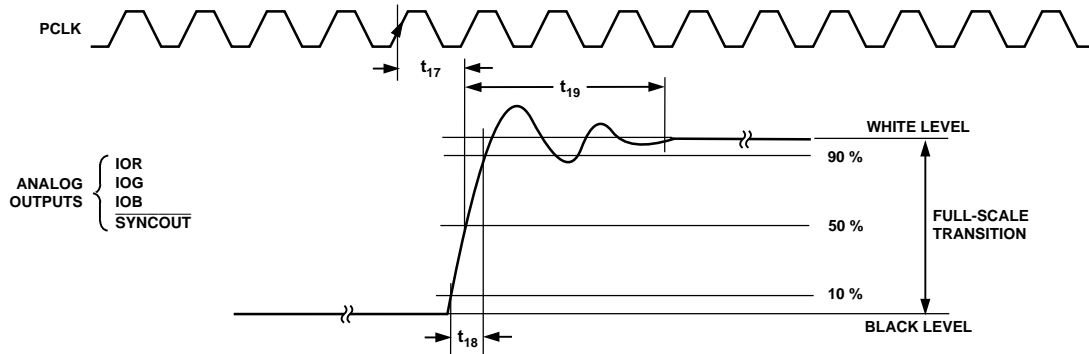


Figure 3. Microprocessor Port (MPU) Interface Timing



NOTE:
 THIS DIAGRAM IS NOT TO SCALE.
 FOR THE PURPOSES OF CLARITY, THE ANALOG OUTPUT WAVEFORM IS MAGNIFIED IN TIME AND AMPLITUDE W.R.T THE CLOCK WAVEFORM.
 SYNCOUT IS A DIGITAL VIDEO OUTPUT SIGNAL.
 t₁₇ IS THE ONLY RELEVANT TIMING SPECIFICATION FOR SYNCOUT.

Figure 4. Analog Output Response vs. LOADIN

ABSOLUTE MAXIMUM RATINGS¹

V _{AA} to GND	7 V
Voltage on Any Digital Pin	GND - 0.5 V to V _{AA} + 0.5 V
Ambient Operating Temperature (T _A)	0°C to +70°C
Storage Temperature (T _S)	-65°C to +150°C
Junction Temperature (T _J)	+150°C
Lead Temperature (Soldering, 10 sec)	+260°C
Vapor Phase Soldering (1 minute)	+220°C
Analog Outputs to GND ²	GND - 0.5 V to V _{AA}
Current on Any DAC Output	60 mA

NOTES

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

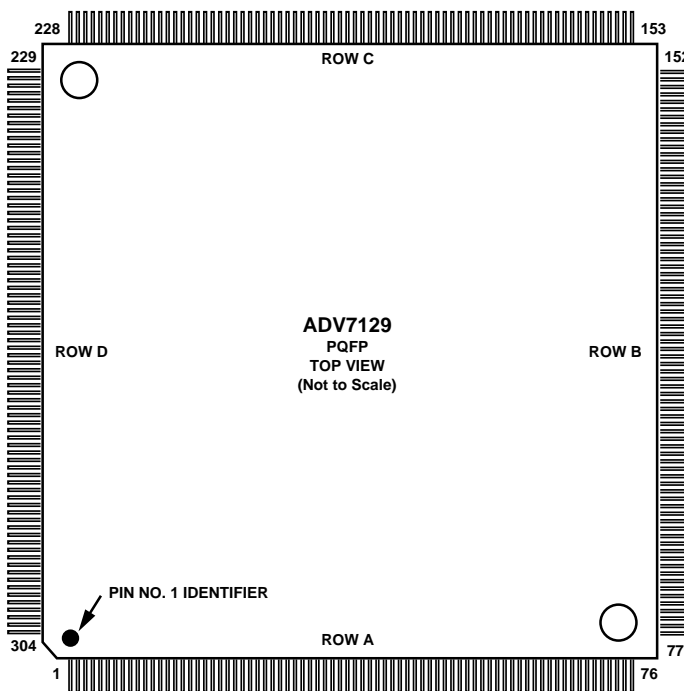
²Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE*

Model	Temperature Range	Package Option
ADV7129KS	0°C to +70°C	S-304

*Due to the specialized nature and application of this part, it is not automatically available to order. Please contact your local sales office for details.

304-LEAD PQFP PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7129 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADV7129

PIN ASSIGNMENTS

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	GND	41	G4 _C	81	GND	121	B4 _E
2	GND	42	G4 _B	82	GND	122	B4 _D
3	GND	43	G4 _A	83	G1 _A	123	B4 _C
4	GND	44	V _{AA}	84	G0 _H	124	B4 _B
5	GND	45	GND	85	G0 _G	125	B4 _A
6	GND	46	V _{AA}	86	G0 _F	126	B3 _H
7	R0 _E	47	GND	87	G0 _E	127	B3 _G
8	R0 _D	48	G3 _H	88	G0 _D	128	B3 _F
9	R0 _C	49	G3 _G	89	G0 _C	129	B3 _E
10	R0 _B	50	G3 _F	90	G0 _B	130	B3 _D
11	R0 _A	51	G3 _E	91	G0 _A	131	B3 _C
12	G7 _H	52	G3 _D	92	B7 _H	132	B3 _B
13	G7 _G	53	G3 _C	93	B7 _G	133	B3 _A
14	G7 _F	54	G3 _B	94	B7 _F	134	B2 _H
15	G7 _E	55	G3 _A	95	B7 _E	135	B2 _G
16	G7 _D	56	G2 _H	96	B7 _D	136	B2 _F
17	G7 _C	57	G2 _G	97	B7 _C	137	B2 _E
18	G7 _B	58	G2 _F	98	B7 _B	138	B2 _D
19	G7 _A	59	G2 _E	99	B7 _A	139	B2 _C
20	G6 _H	60	G2 _D	100	B6 _H	140	B2 _B
21	G6 _G	61	G2 _C	101	B6 _G	141	B2 _A
22	G6 _F	62	G2 _B	102	B6 _F	142	B1 _H
23	G6 _E	63	G2 _A	103	B6 _E	143	B1 _G
24	G6 _D	64	G1 _H	104	B6 _D	144	B1 _F
25	G6 _C	65	G1 _G	105	B6 _C	145	B1 _E
26	G6 _B	66	G1 _F	106	B6 _B	146	B1 _D
27	G6 _A	67	G1 _E	107	B6 _A	147	GND
28	G5 _H	68	G1 _D	108	B5 _H	148	GND
29	G5 _G	69	G1 _C	109	B5 _G	149	GND
30	G5 _F	70	G1 _B	110	B5 _F	150	GND
31	G5 _E	71	GND	111	B5 _E	151	GND
32	G5 _D	72	GND	112	B5 _D	152	GND
33	G5 _C	73	GND	113	B5 _C	153	GND
34	G5 _B	74	GND	114	B5 _B	154	GND
35	G5 _A	75	GND	115	B5 _A	155	GND
36	G4 _H	76	GND	116	V _{AA}	156	GND
37	G4 _G	77	GND	117	GND	157	GND
38	G4 _F	78	GND	118	B4 _H	158	GND
39	G4 _E	79	GND	119	B4 _G	159	B1 _C
40	G4 _D	80	GND	120	B4 _F	160	B1 _B

*No Connect.

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
161	B1 _A	197	R _{BIAS}	233	GND	269	LOADOUT
162	B0 _H	198	SENSE/ <u>SYNCOUT</u>	234	GND	270	R4 _B
163	B0 _G	199	V _{REF}	235	R6 _H	271	R4 _A
164	B0 _F	200	GND	236	R6 _G	272	R3 _H
165	B0 _E	201	D0	237	R6 _F	273	R3 _G
166	B0 _D	202	D1	238	R6 _E	274	R3 _F
167	B0 _C	203	D2	239	R6 _D	275	R3 _E
168	B0 _B	204	D3	240	R6 _C	276	R3 _D
169	B0 _A	205	GND	241	R6 _B	277	R3 _C
170	<u>BLANK</u>	206	V _{AA}	242	R6 _A	278	R3 _B
171	<u>HSYNC</u>	207	D4	243	R5 _H	279	R3 _A
172	<u>VSYNC</u>	208	D5	244	R5 _G	280	R2 _H
173	<u>ODD/EVEN</u>	209	D6	245	R5 _F	281	R2 _G
174	NC*	210	<u>D7</u>	246	V _{AA}	282	R2 _F
175	GND	211	<u>CE</u>	247	GND	283	R2 _E
176	GND	212	R/ <u>W</u>	248	V _{AA}	284	R2 _D
177	<u>IOB</u>	213	C0	249	GND	285	R2 _C
178	IOB	214	C1	250	R5 _E	286	R2 _B
179	R _{BSET}	215	R7 _H	251	R5 _D	287	R2 _A
180	B _{COMP}	216	R7 _G	252	R5 _C	288	R1 _H
181	V _{AA}	217	R7 _F	253	R5 _B	289	R1 _G
182	V _{AA}	218	R7 _E	254	R5 _A	290	R1 _F
183	<u>BBIAS</u>	219	R7 _D	255	R4 _H	291	R1 _E
184	<u>IOG</u>	220	R7 _C	256	R4 _G	292	R1 _D
185	IOG	221	R7 _B	257	R4 _F	293	R1 _C
186	R _{GSET}	222	R7 _A	258	R4 _E	294	R1 _B
187	G _{COMP}	223	GND	259	R4 _D	295	R1 _A
188	V _{AA}	224	GND	260	R4 _C	296	R0 _H
189	V _{AA}	225	GND	261	GND	297	R0 _G
190	<u>GBIAS</u>	226	GND	262	GND	298	R0 _F
191	<u>IOR</u>	227	GND	263	V _{AA}	299	GND
192	IOR	228	GND	264	LPF	300	GND
193	R _{RSET}	229	GND	265	GND	301	GND
194	R _{COMP}	230	GND	266	LOADIN	302	GND
195	V _{AA}	231	GND	267	GND	303	GND
196	V _{AA}	232	GND	268	<u>CSYNC</u>	304	GND

*No Connect.

PIN DESCRIPTION

Mnemonic	Function
R7–R0[A . . . H]	Red Pixel Port Inputs (TTL Compatible Inputs). Eight sets of eight bits latched on the rising edge of LOADIN.
G7–G0[A . . . H]	Green Pixel Port Inputs (TTL Compatible Inputs). Eight sets of eight bits latched on the rising edge of LOADIN.
B7–B0[A . . . H]	Blue Pixel Port Inputs (TTL Compatible Inputs). Eight sets of eight bits latched on the rising edge of LOADIN.
$\overline{\text{BLANK}}$	Composite Blank (TTL Compatible Input). This video control signal drives the analog outputs to the blanking level. When $\overline{\text{BLANK}}$ is at logic “0,” the pixel inputs are ignored. Pedestal selection is controlled by Bit CR15 of Command Register 1. $\overline{\text{BLANK}}$ is latched on the rising edge of LOADIN.
ODD/ $\overline{\text{EVEN}}$	Odd/Even Field Input (TTL Compatible Input). This input indicates which field of the frame is being displayed. An even field is selected by setting ODD/ $\overline{\text{EVEN}}$ to logical “0.” An odd field is selected by setting ODD/ $\overline{\text{EVEN}}$ to logical “1.” ODD/ $\overline{\text{EVEN}}$ should be changed only during vertical blank.
$\overline{\text{HSYNC}}$	Horizontal-Sync Input (TTL Compatible Input). This control signal is latched on the rising edge of LOADIN.
$\overline{\text{VSYNC}}$	Vertical-Sync Input (TTL Compatible Input). This control signal is latched on the rising edge of LOADIN.
$\overline{\text{CSYNC}}$	Composite-Sync Input (TTL Compatible Input). This video control signal drives the analog outputs to the $\overline{\text{SYNC}}$ level. It is only asserted during the blanking period and does not override any other control or data input. CR14, CR13 or CR12 of Command Register 1 must be set together with CR11 or Command Register 1 to decode $\overline{\text{SYNC}}$ onto the IOR/ $\overline{\text{IOR}}$, IOG/ $\overline{\text{IOG}}$ or IOB/ $\overline{\text{IOB}}$ analog outputs, otherwise the $\overline{\text{SYNC}}$ input is ignored.
$\overline{\text{CE}}$	Chip Enable Input (TTL Compatible Input). This input must be set to logic “0” when writing or reading over the data bus (D7–D0). Internally, data is latched on the rising edge of $\overline{\text{CE}}$.
R/ $\overline{\text{W}}$	Read/Write pin (TTL Compatible Input). This signal is latched on the falling edge of $\overline{\text{CE}}$. A high level indicates a read operation and a low level indicates a write operation.
C0, C1	Register select pins (TTL Compatible Inputs). These inputs select which MPU port register is selected for writing or reading. Data is latched on the falling edge of $\overline{\text{CE}}$.
D7–D0	Data Bus (TTL Compatible Input/Output Bus). Data, including color palette values and device control information is written to and read from the device over this 8-bit, bidirectional databus. Any unused bits of the data bus should be terminated through a resistor to either the digital power plane (V_{CC}) or GND.
LOADIN	Pixel Data Load Input (TTL Compatible Input). This input latches the multiplexed pixel data, including $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, and ODD/ $\overline{\text{EVEN}}$ into the device. This rising edge of this signal is used to latch in the video signal inputs. It is also used as a reference frequency to generate an $8 \times$ multiple pixel clock using the fixed reference onboard PLL.
LOADOUT	Pixel Data Load Output (TTL Compatible Output). This digital output is PCLK/8. If the onboard phase lock loop is used, it has the same phase as LOADIN.
LPF	Low-Pass Filter Pin. This pin stabilizes the internal PLL. The following network is recommended.

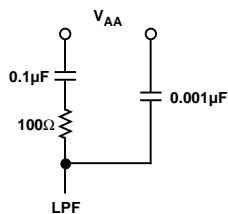


Figure 5.

Mnemonic	Function
IOR, IOG, IOB	Red, Green & Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into doubly terminated 50 Ω or 75 Ω loads.
$\overline{\text{IOR}}, \overline{\text{IOG}}, \overline{\text{IOB}}$	Differential Red, Green & Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into doubly terminated 50 Ω or 75 Ω loads. If the complementary outputs are not required, then these outputs should be tied to GND.
R _{COMP}	Red Compensation pin. This pin should be bypassed to V _{AA} with 0.01 μF capacitor.
G _{COMP}	Green Compensation pin. This pin should be bypassed to V _{AA} with 0.01 μF capacitor.
B _{COMP}	Blue Compensation pin. This pin should be bypassed to V _{AA} with 0.01 μF capacitor.
R _{RSET} , R _{GSET} , R _{BSET}	DAC Output Full-Scale Adjust Control (Analog Input): A resistor from this pin to ground sets the current in the DACs. The current in the DACs is set according to the equations: $I_{OUT} = 12,950 \times V_{REF}/R_{SET} \text{ (}\overline{\text{SYNC}} \text{ not encoded on the DAC Output)}$ $I_{OUT} = 18,137 \times V_{REF}/R_{SET} \text{ (}\overline{\text{SYNC}} \text{ encoded on the DAC Output)}$ <p>To generate RS 343-A video levels on the DAC outputs, a resistor value of 280 Ω is recommended for doubly terminated 50 Ω lines. Any combination of R_{SET} value, DAC termination resistor and programming of $\overline{\text{SYNC}}$ and pedestal are possible provided that the maximum DAC current and the DAC output compliance specifications are adhered to.</p> <p>For example, in a doubly terminated 50 Ω system with no $\overline{\text{SYNC}}$ or pedestal encoded on the DAC outputs, an R_{SET} value of 280 Ω gives a DAC full-scale output of 52.8 mA, i.e., a white-to-black value of 1.4 V. This example would give a 6 dB reduction in noise and feedthrough on the DAC outputs (compared to a 0.7 V full-scale value), but may require a 0.5X splitter at the monitor.</p>
R _{BIAS}	Red Bias node. This node should be decoupled to V _{AA} with a 0.01 μF capacitor.
G _{BIAS}	Green Bias node. This node should be decoupled to V _{AA} with a 0.01 μF capacitor.
B _{BIAS}	Blue Bias node. This node should be decoupled to V _{AA} with a 0.01 μF capacitor.
SENSE/ $\overline{\text{SYNCOU}}$	Comparator Sense Output (TTL Compatible Output). This output will be logic “1” if one or more of the analog outputs exceeds the internal voltage of the SENSE comparator circuit. It can be used to determine the absence of a CRT monitor. The value of the SENSE Output corresponds to the current pixel at the outputs. The output can drive one CMOS load. This pin can alternately be programmed to be a TTL sync output which is a delayed version of $\overline{\text{CSYNC}}$.
V _{REF}	Voltage Reference (Analog Input/Output): This should always have a 0.1 μF decoupling capacitor attached between V _{REF} and V _{AA} . If nothing else is connected then the DACs are driven by the internal voltage reference. If it is required to use a more accurate reference, then this pin acts as an overdrive input. An external 1.235 V voltage reference such as the AD1580 or equivalent is recommended to drive this input. (Note: It is not recommended to use a resistor network to generate the voltage reference.)
V _{AA}	Power Supply (+5 V ± 5%). The part contains multiple power supply pins, all should be connected together to one common +5 V filtered analog power supply.
GND	Analog Ground. The part contains multiple ground pins, all should be connected together to the system’s ground plane.

ADV7129

(continued from page 1)

The ADV7129 supports 24-bit true-color formats where screen resolution is the primary design goal. The individual Red, Green and Blue pixel input ports allow true-color image rendition at resolutions of $2048 \times 2048 \times 24$ bit.

The ADV7129 is capable of generating RGB video output signals that are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

An internal voltage reference is also provided to simplify system design.

The ADV7129 is fabricated in a +5 V CMOS process.

The ADV7129 is packaged in a 304-pin PQFP package.

CIRCUIT DETAILS AND OPERATION

Digital video or pixel data is latched into the ADV7129 over the pixel port. The data is multiplexed and latched into the three 8-bit digital-to-analog converters (DACs) and output as an RGB video signal.

The ADV7129 can be broken into three sections for purposes of clarity of explanation:

1. Pixel port and clock control circuit.
2. MPU port, registers and cursor.
3. Digital-to-analog converters and video outputs.

Pixel Port and Clock Circuits

The pixel port of the ADV7129 is directly interfaced to the video/graphics pipeline of a computer graphics subsystem. It is connected directly through a gate array to the video RAM of the system's frame buffer. The pixel port of the ADV7129 consists of:

Color Data: RED, GREEN, BLUE

Pixel Controls: $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, $\overline{\text{BLANK}}$

The associated clocking signals for the pixel port include:

Clock Input LOADIN

Clock Output LOADOUT

Pixel Port (Color Data)

The ADV7129 has 192 color data inputs. This supports 24-bit true color with 8:1 multiplexing.

Color data is always latched on the rising edge of LOADIN. LOADOUT is generated internally by the ADV7129. The frequency of LOADOUT is the internal clock frequency (PCLK) divided by 8.

Other pixel data signals latched into the part by LOADIN include $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{VSYNC}}$ and $\overline{\text{CSYNC}}$.

$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, $\overline{\text{BLANK}}$

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ video control signals drive the analog outputs to the blanking and sync levels respectively. These are latched on the rising edge of LOADIN. The $\overline{\text{SYNC}}$ information can be encoded onto any of the IOG, IOR or IOB analog outputs by setting Bits CR12, CR13 or CR14 of Command Register 1 to logic "1."

The $\overline{\text{SYNC}}$ information is ignored if Bits CR12, CR13 and CR14 of Command Register 1 are set to logic "0."

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ information can be decoded onto the inverted outputs by setting CR10 and CR11 of Command Register 1 to logic level "1."

SENSE

If any one or more of the analog outputs, IOG, IOR and IOB, exceed the internal voltage reference level (due to absence of CRT), SENSE is set to logic "1." The SENSE output can drive one CMOS load and can be used to determine the absence of a CRT monitor.

CLOCK CONTROL CIRCUIT

The ADV7129 has an integrated clock control circuit. This circuit is capable of generating the internal clocking signals.

A lower frequency external clock generator is used by enabling the onboard PLL. This fixed multiple PLL is used to speed up LOADIN by a factor of 8. This onboard $8 \times$ clock multiplier is activated by setting Bit CR20 of Command Register 2 from logic "0" to logic "1." It must be set up after power-up.

MICROPROCESSOR (MPU) PORT

The ADV7129 supports a standard MPU interface. All the functions of the part are controlled via this MPU port. Direct access is gained to the address register and all the control registers as well as the cursor palette. The following sections describe the setup for reading and writing to all of the devices' registers.

MPU Interface

The MPU interface consists of a bidirectional, 8-bit wide databus and interface control signals $\overline{\text{R/W}}$, $\overline{\text{CE}}$, C1, C0. Two write operations are required to set up the lower 8 bits and higher 2 bits of the Address Register.

Register Mapping

The ADV7129 contains a number of onboard registers including the Address Register, Command Registers and Gain Error Registers. Control Lines C1-C0 determine whether the Address Register is being pointed to (upper or lower bytes) or whether the other registers are being accessed.

The $\overline{\text{R/W}}$ and $\overline{\text{CE}}$ control inputs allow read and write access. All registers can be read and written to.

Power-On Reset

After power-up, the ADV7129 must be set to perform a reset operation. This is achieved by resetting the PLL (a low to high transition on Bit CR20 of Command Register 2). This initializes the pixel port such that the pixel sequence ABCDEFGH starts at A. This reset can be performed as the registers are being initialized. The Command Registers power up in an indeterminate state and must be set up for the required operation. The power-on is activated when V_{AA} goes from 0 V to 5 V. This is active for 1 μs . The ADV7129 should not be accessed during this period.

Register Accesses

The MPU can write to or read from all of the ADV7129s' registers. Figure 6 shows the Control Registers and C1-C0 Control Input Truth Table. The read/write timing is controlled by the $\overline{\text{CE}}$ and $\overline{\text{R/W}}$ inputs. The Address Register determines which Control Register is being accessed.

The registers can be addressed directly by two write cycles to set up the high and low bytes of Address Register and then by a read or write cycle of the MPU.

REGISTER PROGRAMMING

The following section describes each register, including Address Register and each of the Control Registers in terms of its configuration.

Address Register (A10–A0)

As illustrated previously, the C1–C0 inputs, in conjunction with the Address Register specify which control register, or palette RAM location is accessed by the MPU port. The Address Register is 16 bits wide and can be read from as well as written to.

CONTROL REGISTERS

A large bank of registers can be accessed using the Address register and C1–C0. Access is made first by writing the Address Register with the appropriate address to point to the particular Control Register, and then performing an MPU access to the Control Register.

ADDRESS REGISTER (A10–A0)																																	
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>C1</th> <th>C0</th> <th>R/W</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>WRITE TO ADDRESS REGISTER (LOWER BYTE)</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>WRITE TO ADDRESS REGISTER (UPPER BYTE)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>WRITE TO REGISTERS</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>READ FROM ADDRESS REGISTER (LOWER BYTE)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>READ FROM ADDRESS REGISTER (UPPER BYTE)</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>READ FROM REGISTERS</td> </tr> <tr> <td>1</td> <td>1</td> <td>X</td> <td>RESERVED</td> </tr> </tbody> </table>	C1	C0	R/W		0	0	0	WRITE TO ADDRESS REGISTER (LOWER BYTE)	0	1	0	WRITE TO ADDRESS REGISTER (UPPER BYTE)	1	0	0	WRITE TO REGISTERS	0	0	1	READ FROM ADDRESS REGISTER (LOWER BYTE)	0	1	1	READ FROM ADDRESS REGISTER (UPPER BYTE)	1	0	1	READ FROM REGISTERS	1	1	X	RESERVED
C1	C0	R/W																															
0	0	0	WRITE TO ADDRESS REGISTER (LOWER BYTE)																														
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0	1	1	READ FROM ADDRESS REGISTER (UPPER BYTE)																														
1	0	1	READ FROM REGISTERS																														
1	1	X	RESERVED																														
(A10–A0)	REGISTER ACCESS																																
4FF–412	RESERVED																																
411	COMMAND REGISTER 2																																
410	RESERVED																																
40F	RESERVED																																
40E	RESERVED																																
40D	RESERVED																																
40C	RESERVED																																
40B	RESERVED																																
40A	RESERVED																																
409	RESERVED																																
408	RESERVED																																
407	BLUE DAC GAIN ERROR REGISTER																																
406	GREEN DAC GAIN ERROR REGISTER																																
405	RED DAC GAIN ERROR REGISTER																																
004	RESERVED																																
403	RESERVED																																
402	RESERVED																																
401	RESERVED																																
400	COMMAND REGISTER 1																																
000–3FF	RESERVED																																

Figure 6. Control Registers

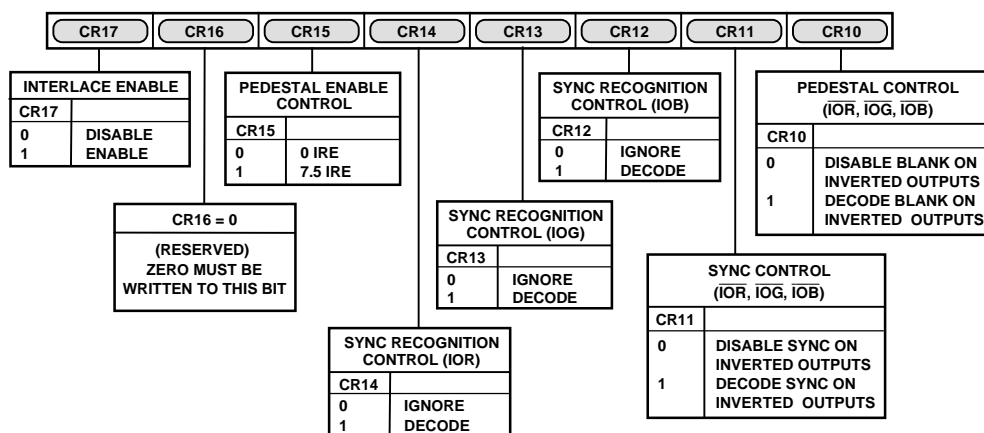


Figure 7. Command Register 1

COMMAND REGISTER 1 (CR1)

(Address Register (A10–A0) = 400H)

This register contains a number of control bits as shown in the diagram. CR1 is an 8-bit wide register.

Figure 7 shows the various operations under the control of CR1. This register can be read from as well as written to. Bit CR16 is reserved and should be set to logic “1.”

COMMAND REGISTER 1-BIT DESCRIPTION

BLANK Control on Inverted Outputs (CR10):

This bit specifies whether the video $\overline{\text{BLANK}}$ is to be decoded onto the inverted analog outputs or ignored.

SYNC Control on Inverted Outputs (CR11)

This bit specifies whether the video $\overline{\text{SYNC}}$ is to be decoded onto the inverted analog outputs or ignored.

SYNC Recognition on Blue (CR12)

This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be decoded onto the IOB analog output or ignored.

SYNC Recognition on Green (CR13)

This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be decoded onto the IOG analog output or ignored.

SYNC Recognition on Red (CR14)

This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be decoded onto the IOR analog output or ignored.

Pedestal Enable Control (CR15)

This bit specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be generated on the video outputs.

Display Mode Control (CR17)

This bit controls whether the display is interlaced or noninterlaced.

ADV7129

COMMAND REGISTER 2 (CR2)

(Address Register (A10-A0) = 411H)

This register contains a number of control bits as shown in the diagram. CR2 is an 8-bit wide register. CR27, CR24, CR22 and CR21 are reserved and should be set to logic “0.” Figure 8 shows the various operations under the control of CR2. This register can be read from as well as written to.

COMMAND REGISTER 2-BIT DESCRIPTION

PLL Control (CR20)

This bit resets the PLL divider when set to logic “0” and releases it when set to logic “1.”

SYNCOUT Control (CR23)

This bit is an enable for SYNCOUT. If this bit is set to logic “1,” the SENSE output becomes a pipelined version of $\overline{\text{CSYNC}}$. Otherwise the SENSE output remains unaffected.

SENSE Bit (CR25)

This output bit is used to determine the absence of a CRT monitor. When CR25 is set to logic “1,” a CRT is not present. With some diagnostic code, the presence of loading on the individual RGB lines can be determined. The reference is generated by a voltage divider from the external voltage reference on the V_{REF} pin. For the proper operation, the following levels should be applied to the comparator by the IOR, IOG and IOB outputs:

DAC Low Voltage ≤ 250 mV.

DAC High Voltage ≥ 450 mV.

VCO Override Bit (CR26)

This bit is used to override the VCO and set the PLL to the lowest frequency possible. If the external LOADIN source takes some time before it reaches its required frequency, the internal PLL can become unstable as it tries to track to a varying LOADIN signal. The VCO override bit can be set to logic level “0” and then released (set to logic level “1”) to allow the VCO to track to the input after it has stabilized. It is required to allow 200 μs before the VCO override bit is released.

GAIN ERROR REGISTERS

(Address Register (A10-A0) = 405H-407H)

The Red, Green and Blue Gain Error Registers allow the user to compensate for any channel-to-channel variations in the video output system. They control internal resistors from each of the three DAC outputs to GND, i.e., they appear in parallel with the external termination resistor across the DAC outputs. This allows the RGB output voltages to be adjusted as the value of R_{INT} is varied. A logic “1” on any of the control bits GR06 to GR00 switches in the appropriate resistor. A logic “0” disables or open circuits the resistor. Bit GR07 of the Gain Error Register enables or disables the Gain Error Adjust. Figure 9 shows the typical resistor values for these internal resistances versus R_{SET} .

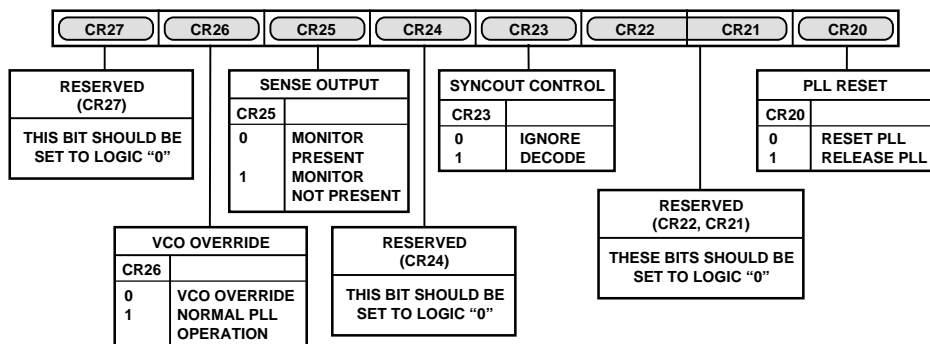


Figure 8. Command Register 2

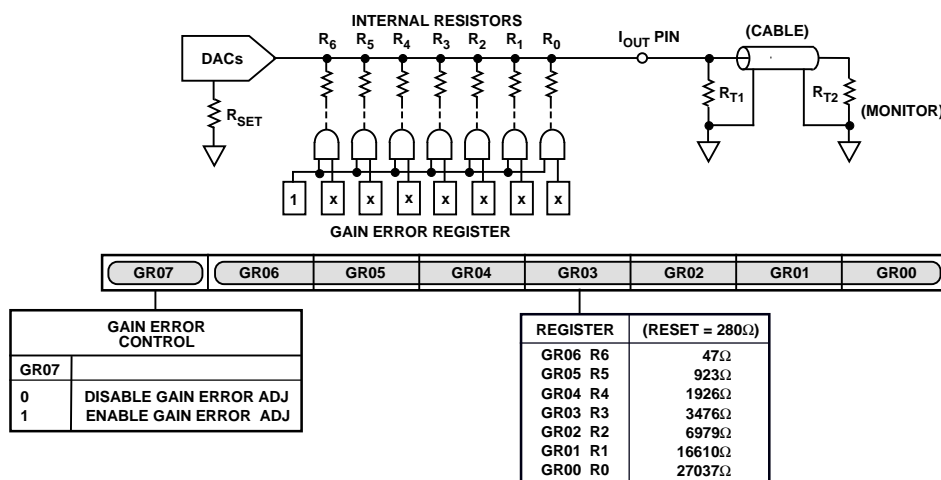


Figure 9. Gain Error Register

DIGITAL-TO-ANALOG CONVERTERS (DACs) AND VIDEO OUTPUTS

The ADV7129 contains three high speed video DACs. The DAC outputs are represented as the three primary analog color signals IOR (red video), IOG (green video) and IOB (blue video).

DACs and Analog Outputs

The part contains three matched 8-bit digital-to-analog converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either IOR, IOG, IOB (bit = "1") or IOR, IOG, IOB (bit = "0"). Normally IOR, IOG, & IOB are connected to GND.

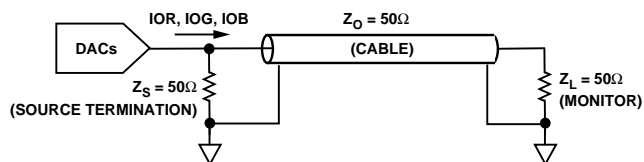


Figure 10. DAC Output Termination (Doubly Terminated 50 Ω Load)

The analog video outputs are high impedance current sources. Each of these three RGB current outputs are specified to directly drive a 25 Ω load (doubly-terminated 50 Ω).

Reference Input and R_{SET}

An external 1.235 V voltage reference is preferred to set up the analog outputs of the ADV7129. The reference voltage is connected to the V_{REF} input. In the absence of an external reference, the on-chip voltage reference is internally connected to the V_{REF} pin. The internal reference will set up the DAC currents, although with slightly less accuracy.

A resistor R_{SET} is connected between the R_{SET} (R_{RSET}, R_{GSET}, R_{BSET}) input of the part and ground. An R_{SET} value of 280 Ω corresponds to the generation of two times RS-343A video levels into a doubly-terminated 50 Ω load. Figure 11 illustrates the resulting video waveform and the Video Output Truth Table illustrates the corresponding control input stimuli. On the ADV7129 SYNC can be encoded on any of the analog signals, however in practice, SYNC is generally encoded on either the IOG output or on all of the video outputs.

Any combination of R_{SET}, DAC termination resistors and programming of SYNC and pedestal are possible provided that the maximum DAC current of 60 mA and the DAC output compliance specifications are adhered to. The following tables show the current levels for different values of R_{SET} resistors and R_{LOAD} termination.

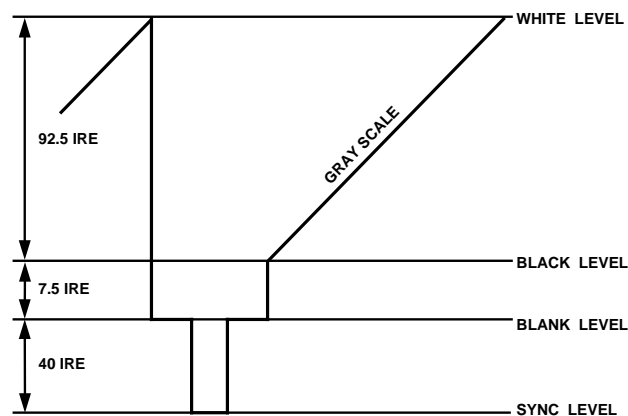


Figure 11. Composite Video Waveform SYNC Decoded; Pedestal = 7.5 IRE

Table I. Video Output Truth Table ($R_{SET} = 398 \Omega$, $R_{LOAD} = 37.5 \Omega$)

Description	O/P with Sync Enabled (mA)	O/P with Sync Disabled (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	FFH
VIDEO	Video + 9.05	Video + 1.44	1	1	Data
VIDEO to BLANK	Video + 1.44	Video + 1.44	0	1	Data
BLACK LEVEL	9.05	1.44	1	1	00H
BLACK to BLANK	1.44	1.44	0	1	00H
BLANK LEVEL	7.62	0	1	0	xxH
SYNC LEVEL	0	0	0	0	xxH

Table II. Video Output Truth Table ($R_{SET} = 560 \Omega$, $R_{LOAD} = 25 \Omega$)

Description	O/P with Sync Enabled (mA)	O/P with Sync Disabled (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	40	28.57	1	1	FFH
VIDEO	Video + 13.6	Video + 2.14	1	1	Data
VIDEO to BLANK	Video + 2.16	Video + 2.14	0	1	Data
BLACK LEVEL	13.6	2.14	1	1	00H
BLACK to BLANK	2.14	2.14	0	1	00H
BLANK LEVEL	11.44	0	1	0	xxH
SYNC LEVEL	0	0	0	0	xxH

Table III. Video Output Truth Table ($R_{SET} = 280 \Omega$, $R_{LOAD} = 25 \Omega$)

Description	O/P with Sync Disabled (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	52.8	0	0	FFH
VIDEO	Video + 0	0	0	Data
VIDEO to BLACK	Video + 0	0	0	Data
BLACK LEVEL	0	0	0	xxH

APPENDIX I BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7129 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The “Recommended Analog Circuit Layout” (see Figure 12) shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7129 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7129 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7129, the analog output traces, and all the digital signal traces leading up to the ADV7129. The analog ground plane should be separated from the system ground plane by a ferrite bead.

Power Planes

The ADV7129 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7129.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7129 power pins and voltage reference circuitry. Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 μF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7129 must have at least one 0.1 μF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7129 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used,

the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7129 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7129 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7129 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Inputs, especially Pixel Data Inputs and clocking signals (LOADOUT, LOADIN, etc.) should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the analog outputs should each have a 50 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7129 so as to minimize reflections.

There are a number of precautions that the user can take to minimize the effects of data feedthrough.

- a. Apply external filtering to the DAC outputs.
- b. Reduce input voltage risetime. From experiments, it has been seen that a reduction from 2 ns to 4 ns gives significant improvement.
- c. Reduce input voltage swing. A reduction from 5 V to 3 V gives significant improvement.
- d. Use series resistors on the pixel inputs (e.g., 100 Ω).
- e. The part can be run at $2\times$ DAC current levels as shown in the DAC output. The differential outputs can then be connected through a differential to single balun transformer to eliminate common-mode noise. A phase splitter should be used to reduce the $2\times$ levels to $1\times$ at the monitor end.

ADV7129

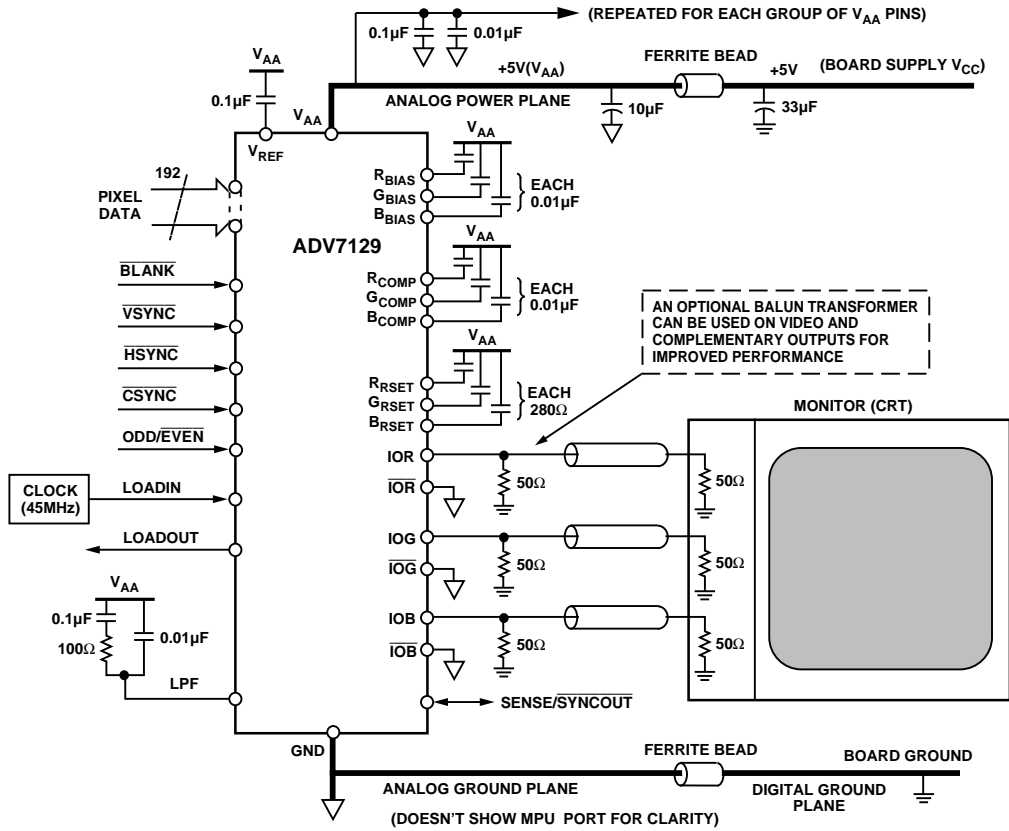


Figure 12. Typical Connection Diagram

APPENDIX II
THERMAL AND ENVIRONMENTAL CONSIDERATIONS

The ADV7129 is a very highly integrated monolithic silicon device. This high level of integration inevitably leads to consideration of thermal and environmental conditions which the ADV7129 must operate in. Reliability of the device is enhanced by keeping it as cool as possible. In order to avoid destructive damage to the device, the absolute maximum junction temperature must never be exceeded. Certain applications, depending on ambient temperature and pixel data rates may require forced air cooling or external heatsinks. The following data is intended as a guide in evaluating the operating conditions of a particular application so that optimum device and system performance is achieved.

It should be noted that information on package characteristics published herein may not be the most up to date at the time of reading this. Advances in package compounds and manufacture will inevitably lead to improvements in the thermal data. Please contact your local sales office for the most up-to-date information.

Package Characteristics

Junction-to-Case (θ_{JC}) Thermal Resistance for this particular part is:

$$\theta_{JC} = 8.9^{\circ}C/W$$

(Note: θ_{JC} is independent of airflow.)

The maximum silicon junction temperature should be limited to 100°C. Temperatures greater than this will reduce long-term device reliability. To ensure that the silicon junction tempera-

ture stays within prescribed limits, the addition of an external heatsink can be used if the junction temperature is brought beyond the maximum limit.

Junction-to-Ambient (θ_{JA}) Thermal Resistance for this particular part is:

$$\theta_{JA} = 25.9^{\circ}C/W \text{ (Still Air)}$$

θ_{JA} = will significantly decrease in air flow.

Thermal Model

The junction temperature of the device in a specific application is given by:

$$T_j = T_A + P_D (\theta_{JC} + \theta_{CA}) \tag{1}$$

or

$$T_j = T_A + P_D (\theta_{JA}) \tag{2}$$

where:

T_j = Junction Temperature of Silicon (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipation (W)

θ_{JC} = Junction to Case Thermal Resistance (°C/W)

θ_{CA} = Case to Ambient Thermal Resistance (°C/W)

θ_{JA} = Junction to Ambient Thermal Resistance (°C/W)

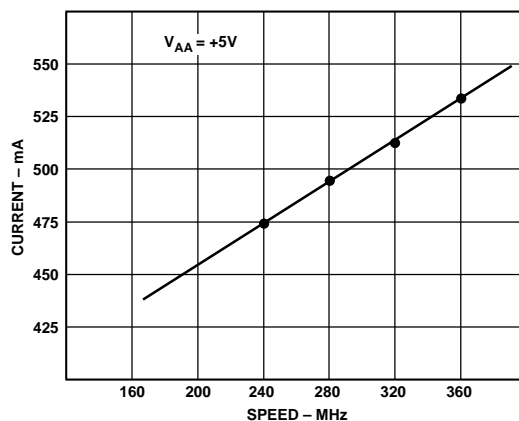


Figure 13. Supply Current vs. Frequency

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**304-Lead Plastic Quad Flatpack
(S-304)**

