>10 W, GaN Power Amplifier, 0.01 GHz to 1.1 GHz

Data Sheet **HMC1099**

FEATURES

- **High saturated output power (P_{SAT}): 40.5 dBm typical**
- **High small signal gain: 18.5 dB typical**
- **High power added efficiency (PAE): 69% typical**
- **Instantaneous bandwidth: 0.01 GHz to 1.1 GHz**
- **Supply voltage: V_{DD} = 28 V at 100 mA**
- **Internal prematching**
  - **Simple and compact external tuning for optimal performance**
- **32-lead, 5 mm × 5 mm, LFCSP package: 25 mm²**

APPLICATIONS

- **Extended battery operation for public mobile radios**
- **Power amplifier stage for wireless infrastructures**
- **Test and measurement equipment**
- **Commercial and military radars**
- **General-purpose transmitter amplification**

GENERAL DESCRIPTION

The HMC1099 is a gallium nitride (GaN), broadband power amplifier delivering >10 W with up to 69% PAE across an instantaneous bandwidth of 0.01 GHz to 1.1 GHz, and with a ±0.5 dB typical gain flatness.

The HMC1099 is ideal for pulsed or continuous wave (CW) applications, such as wireless infrastructure, radars, public mobile radios, and general-purpose amplification.

The HMC1099 amplifier is externally tuned using low cost, surface-mount components and is available in a compact LFCSP package.

Multifunction pin names may be referenced by their relevant function only.

FUNCTIONAL BLOCK DIAGRAM

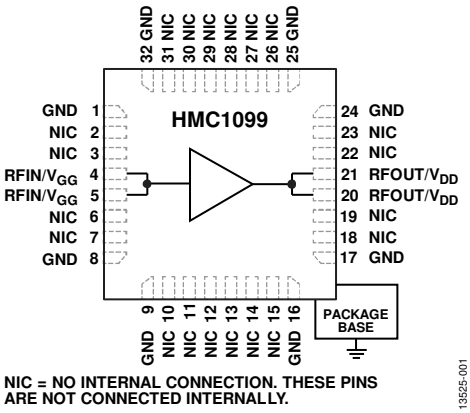

Figure 1.

Rev. A

Document Feedback

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Technical Support
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REVISION HISTORY

12/2016—Rev. 0 to Rev. A

Changed HCP-32-2 to CG-32-1 ..... Throughout
Updated Outline Dimensions 16
Changes to Ordering Guide 16

1/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = 28 V, I_{DD} = 100 mA, frequency range = 0.01 GHz to 0.4 GHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		0.4	GHz	
GAIN						
Small Signal Gain		18	20		dB	
Gain Flatness			±1		dB	
RETURN LOSS						
Input			12		dB	
Output			15		dB	
POWER						
Output Power for 4 dB Compression	P4dB		40		dBm	
Power Gain for P4dB Compression			15		dB	
Saturated Output Power	P_{SAT}		40.5		dBm	>10 W saturated output power
Power Gain for P_{SAT}			13		dB	
Power Added Efficiency	PAE		73		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		49		dBm	Measurement taken at P_{OUT}/tone = 30 dBm
NOISE FIGURE			8		dB	
TOTAL SUPPLY CURRENT	I_{DD}		100		mA	Adjust the gate bias control voltage (V_{GG}) between −8 V to 0 V to achieve an I_{DD} = 100 mA typical

T_A = 25°C, V_{DD} = 28 V, I_{DD} = 100 mA, frequency range = 0.4 GHz to 0.7 GHz.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.4		0.7	GHz	
GAIN						
Small Signal Gain		16.5	18.5		dB	
Gain Flatness			±0.25		dB	
RETURN LOSS						
Input			9.5		dB	
Output			14		dB	
POWER						
Output Power for 4 dB Compression	P4dB		40.5		dBm	
Power Gain for P4dB Compression			14		dB	
Saturated Output Power	P_{SAT}		40.5		dBm	>10 W saturated output power
Power Gain for P_{SAT}			13		dB	
Power Added Efficiency	PAE		69		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		48		dBm	Measurement taken at P_{OUT}/tone = 30 dBm
NOISE FIGURE			5.5		dB	
TOTAL SUPPLY CURRENT	I_{DD}		100		mA	Adjust the gate bias control voltage (V_{GG}) between −8 V to 0 V to achieve an I_{DD} = 100 mA typical

T_A = 25°C, V_{DD} = 28 V, I_{DD} = 100 mA, frequency range = 0.7 GHz to 1.1 GHz.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.7		1.1	GHz	
GAIN						
Small Signal Gain		16.5	18.5		dB	
Gain Flatness			±0.5		dB	
RETURN LOSS						
Input			12		dB	
Output			17		dB	
POWER						
Output Power for 4 dB Compression	P4dB		41.5		dBm	
Power Gain for P4dB Compression			14		dB	
Saturated Output Power	P_{SAT}		41.5		dBm	>10 W saturated output power
Power Gain for P_{SAT}			13.5		dB	
Power Added Efficiency	PAE		69		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		47		dBm	Measurement taken at P_{OUT}/tone = 30 dBm
NOISE FIGURE			5		dB	
TOTAL SUPPLY CURRENT	I_{DD}		100		mA	Adjust the gate bias control voltage (V_{GG}) between −8 V to 0 V to achieve an I_{DD} = 100 mA typical

TOTAL SUPPLY CURRENT BY V_{DD}

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT	I_{DD}					Adjust the gate bias control voltage (V_{GG}) between −8 V to 0 V to achieve an I_{DD} = 100 mA typical
V_{DD} = 24 V			100		mA	
V_{DD} = 28 V			100		mA	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Rating
Drain Bias Voltage (V_{DD})	32 V dc
Gate Bias Voltage (V_{GG})	−8 V to 0 V dc
Radio Frequency (RF) Input Power (RFIN)	33 dBm
Maximum Forward Gate Current	4 mA
Maximum Voltage Standing Wave Ratio (VSWR)[2]	6:1
Channel Temperature	225°C
Maximum Peak Reflow Temperature (MSL3)[3]	260°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 89 mW/°C Above 85°C)	12.5 W
Thermal Resistance (Junction to Back of Paddle)	11.2°C/W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 1B, passed 500 V

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the Absolute Maximum Rating is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] Restricted by maximum power dissipation.
[3] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

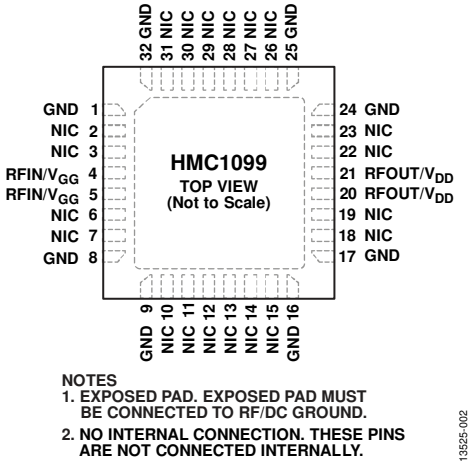

Figure 2. Pin Configuration

Table 6. Pad Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 17, 24, 25, 32	GND	Ground. These pins must be connected to RF/dc ground. See Figure 3 for the GND interface schematic.
2, 3, 6, 7, 10 to 15, 18, 19, 22, 23, 26 to 31	NIC	No Internal Connection. These pins are not connected internally. However, all data was measured with these pins connected to RF/dc ground externally.
4, 5	RFIN/V_{GG}	RF Input (RFIN)/Gate Bias Control Voltage (V_{GG}). This pin is a multifunction pin. The RFIN/V_{GG} pin is dc-coupled with internal prematching and requires external matching to 50 Ω, as shown in Figure 38. See Figure 4 for the RFIN/V_{GG} interface schematic.
20, 21	RFOUT/V_{DD}	RF Output (RFOUT)/Drain Bias Voltage (V_{DD}). This is a multifunction pin. The RFOUT/V_{DD} pin is dc-coupled and requires external matching to 50 Ω, as shown in Figure 38. See Figure 4 for the RFOUT/V_{DD} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface

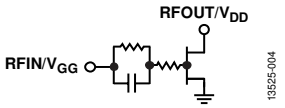

Figure 4. RFIN/V_{GG} and RFOUT/V_{DD} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

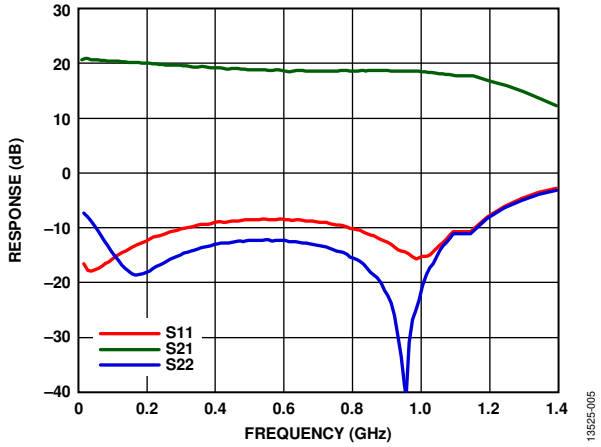

Figure 5. Response (Gain and Return Loss) vs. Frequency

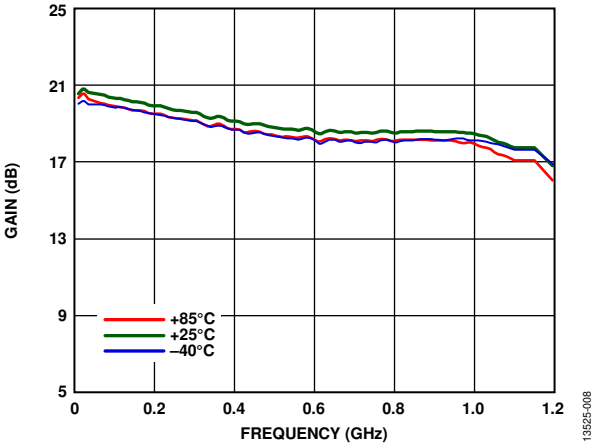

Figure 8. Gain vs. Frequency at Various Temperatures

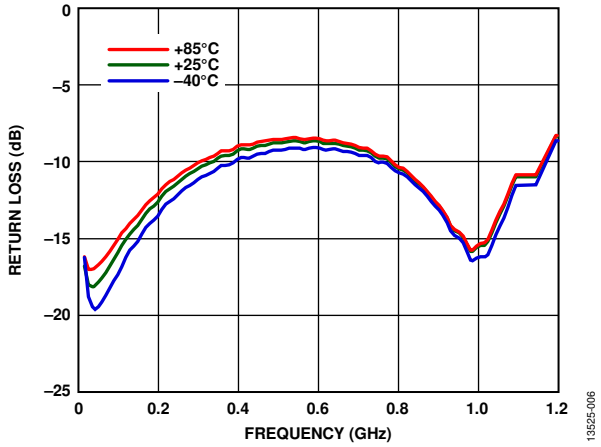

Figure 6. Input Return Loss vs. Frequency at Various Temperatures

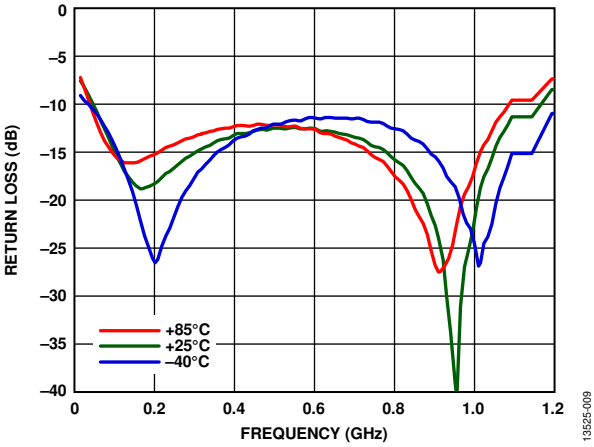

Figure 9. Output Return Loss vs. Frequency at Various Temperatures

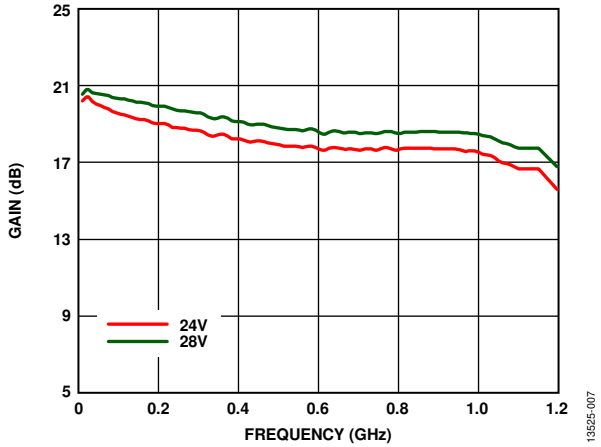

Figure 7. Gain vs. Frequency at Various Supply Voltages

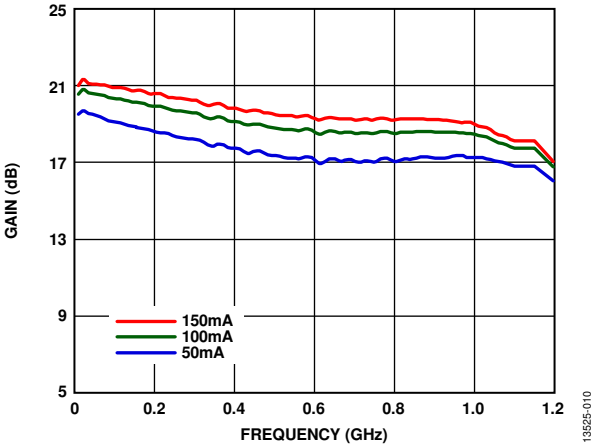

Figure 10. Gain vs. Frequency at Various Supply Currents

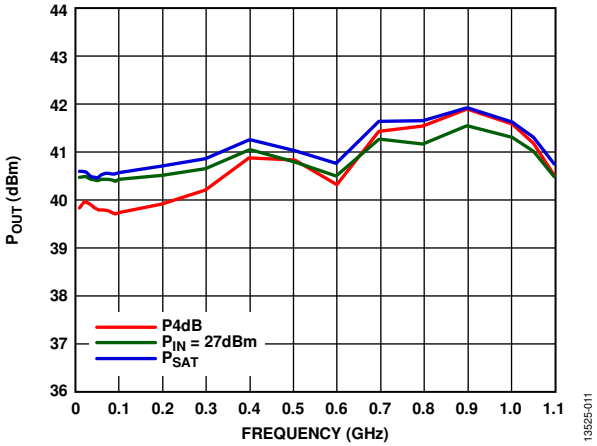

Figure 11. Power Output (P_{OUT}) vs. Frequency

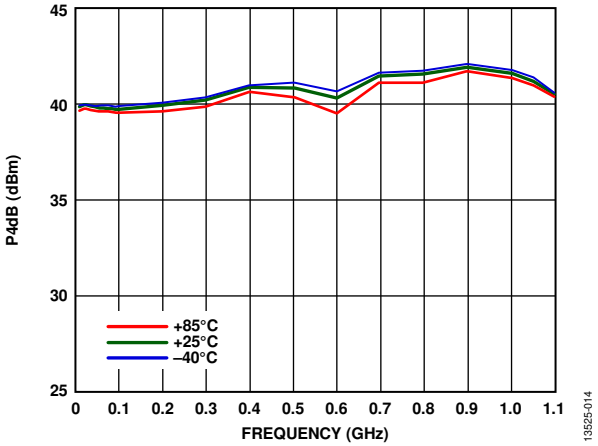

Figure 14. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Temperatures

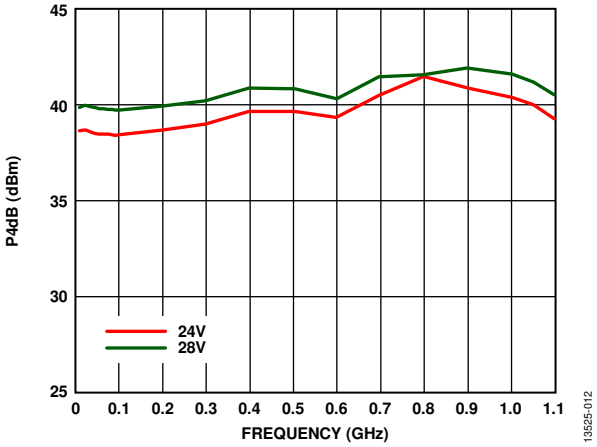

Figure 12. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Supply Voltages

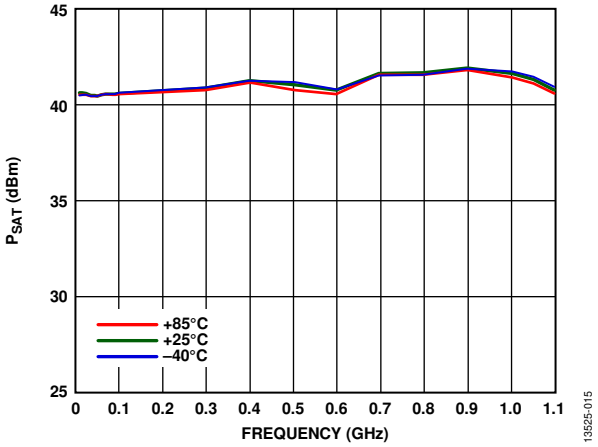

Figure 15. Saturated Output Power (P_{SAT}) vs. Frequency at Various Temperatures

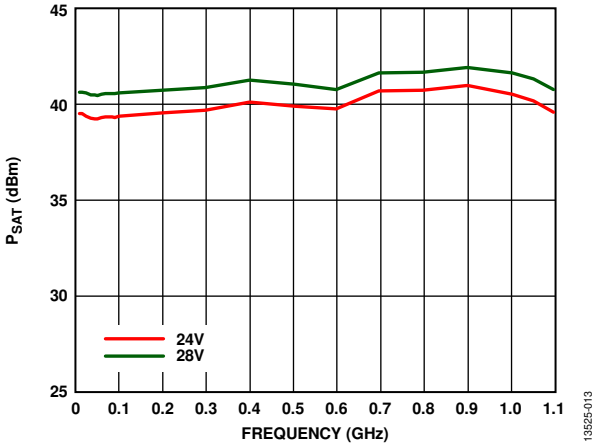

Figure 13. Saturated Output Power (P_{SAT}) vs. Frequency at Various Supply Voltages

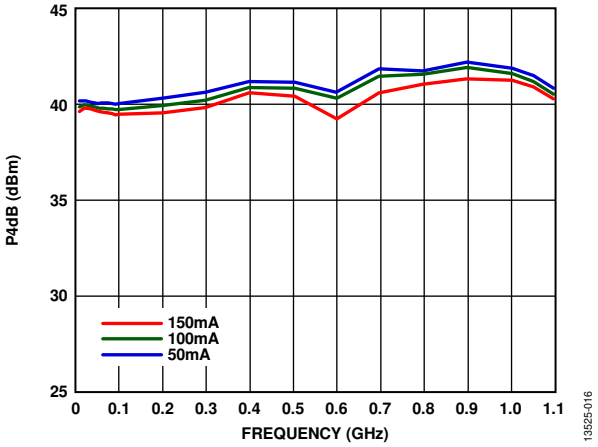

Figure 16. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Supply Currents

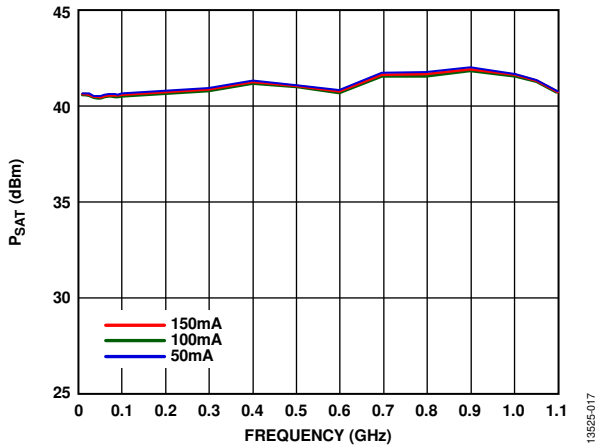

Figure 17. Saturated Output Power (P_{SAT}) vs. Frequency at Various Supply Currents

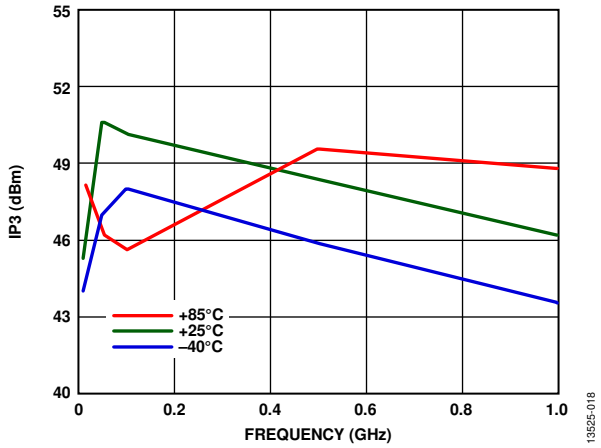

Figure 18. Output Third-Order Intercept (IP3) vs. Frequency at Various Temperatures, P_{OUT}/Tone = 30 dBm

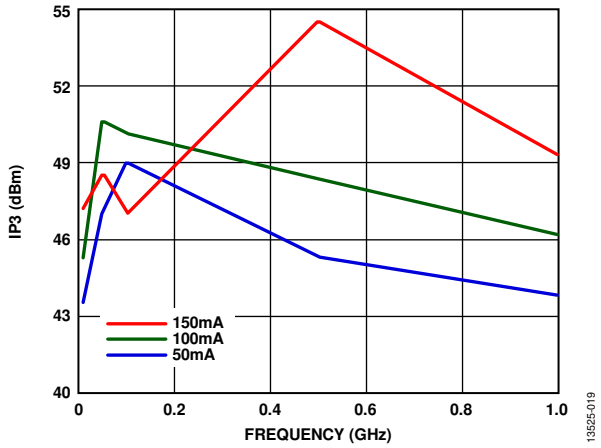

Figure 19. Output Third-Order Intercept (IP3) vs. Frequency at Various Supply Currents, P_{OUT}/Tone = 30 dB

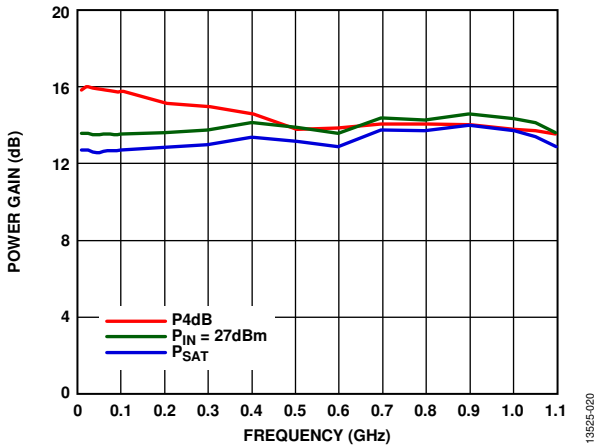

Figure 20. Power Gain vs. Frequency

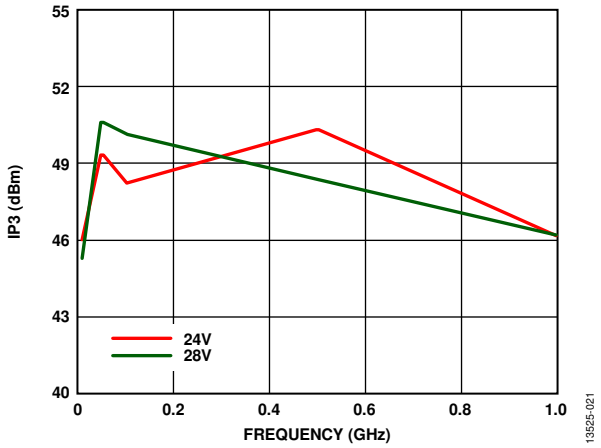

Figure 21. Output Third-Order Intercept (IP3) vs. Frequency at Various Supply Voltages, P_{OUT}/Tone = 30 dBm

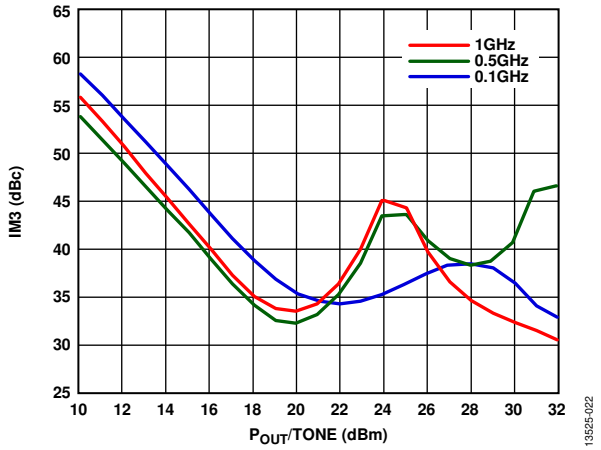

Figure 22. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/TONE at V_{DD} = 24 V

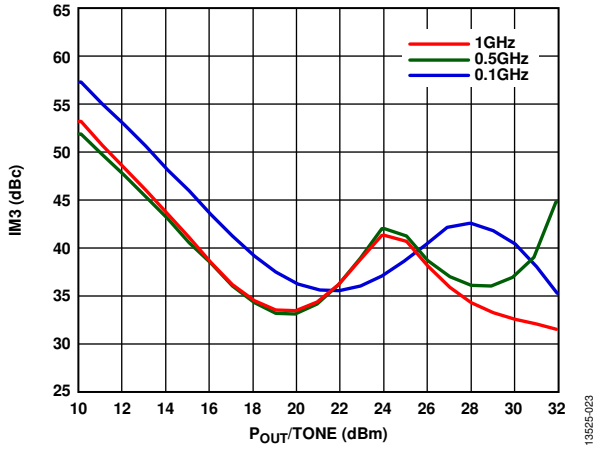

Figure 23. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/TONE at V_{DD} = 28 V

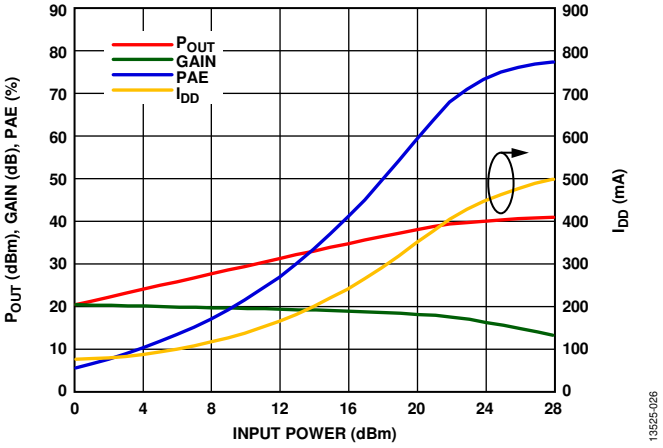

Figure 26. Power Output (P_{OUT}), GAIN, Power Added Efficiency (PAE), and Total Supply Current (I_{DD}) vs. Input Power at 0.1 GHz

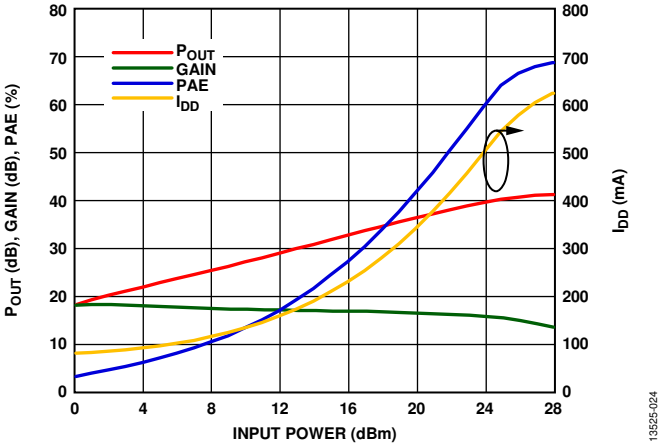

Figure 24. Power Output (P_{OUT}), GAIN, Power Added Efficiency (PAE), and Total Supply Current (I_{DD}) vs. Input Power at 0.5 GHz

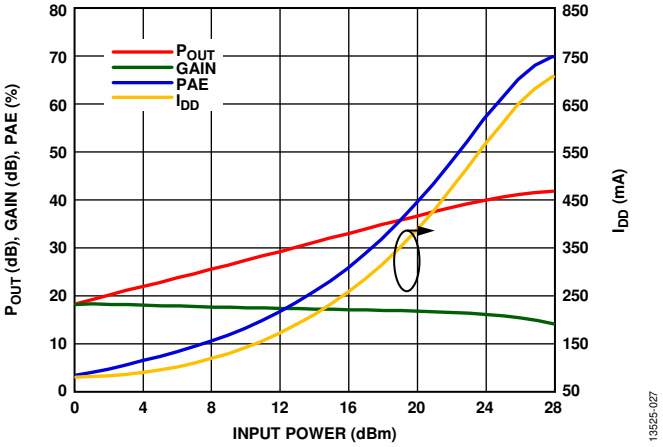

Figure 27. Power Output (P_{OUT}), GAIN, Power Added Efficiency (PAE), and Total Supply Current (I_{DD}) vs. Input Power at 1 GHz

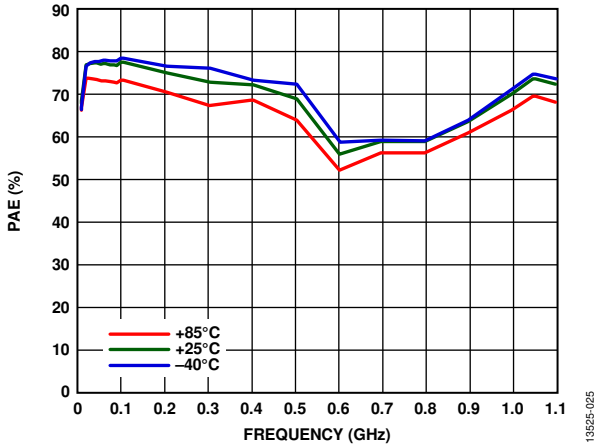

Figure 25. Power Added Efficiency (PAE) vs. Frequency at Various Temperatures

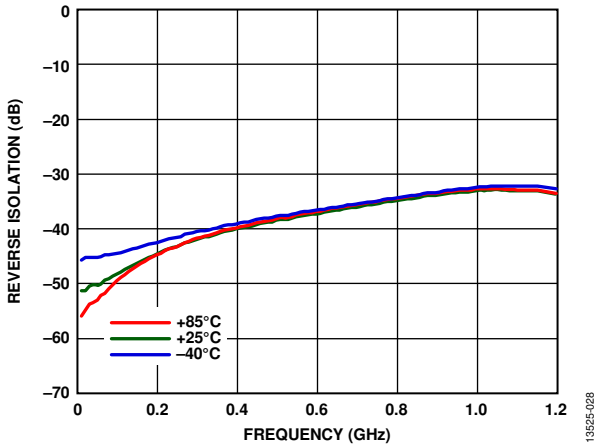

Figure 28. Reverse Isolation vs. Frequency at Various Temperatures

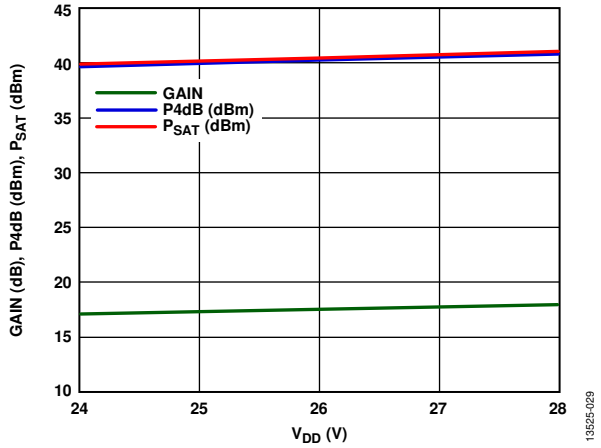

Figure 29. Gain, Output Power for 4 dB Compression (P4dB), and Saturated Output Power (P_{SAT}) vs. Supply Voltage (V_{DD}) at 0.5 GHz

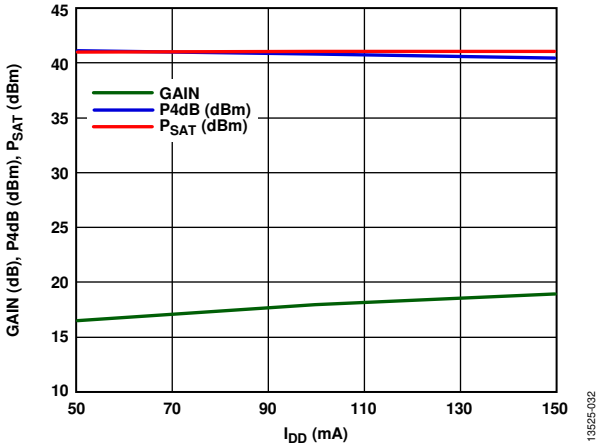

Figure 32. Gain, Output Power for 4 dB Compression (P4dB), and Saturated Output Power (P_{SAT}) vs. Supply Current (I_{DD}) at 0.5 GHz

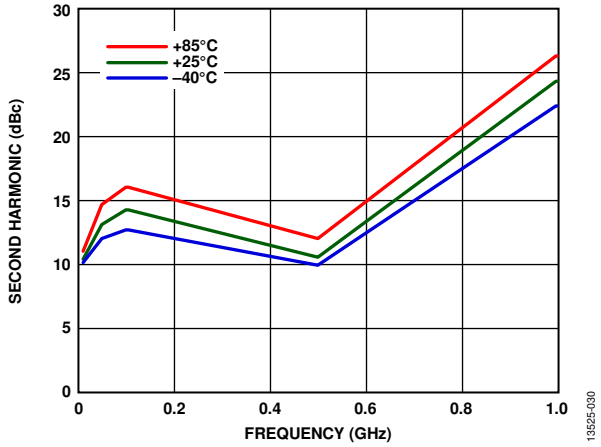

Figure 30. Second Harmonic vs. Frequency at Various Temperatures

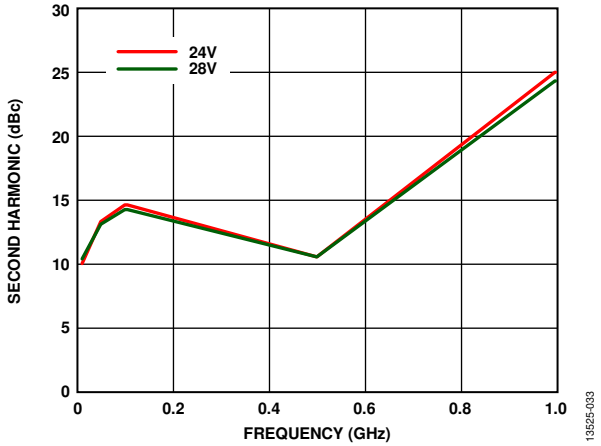

Figure 33. Second Harmonic vs. Frequency at Various Supply Voltages

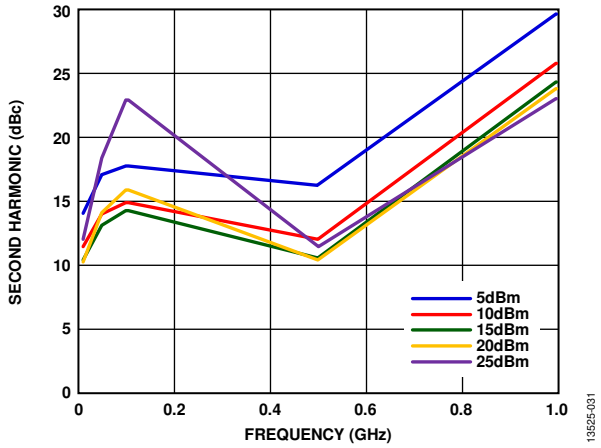

Figure 31. Second Harmonic vs. Frequency at Various Input Power Levels

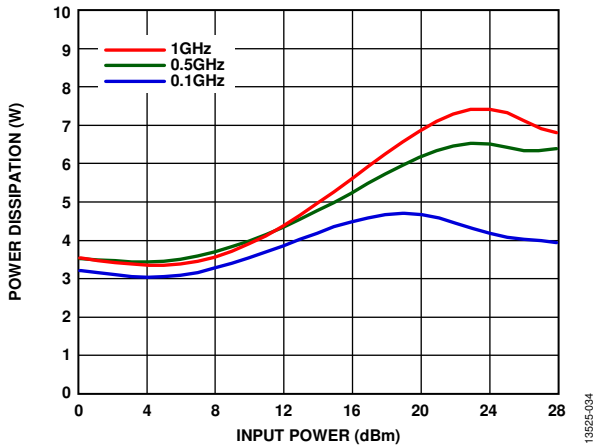

Figure 34. Power Dissipation vs. Input Power at Various Frequencies

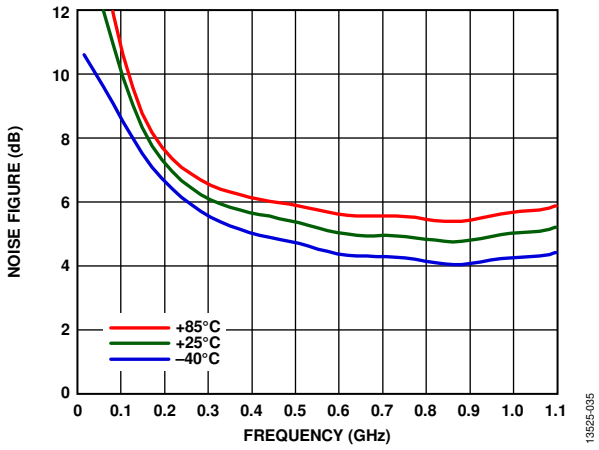

Figure 35. Noise Figure vs. Frequency at Various Temperatures

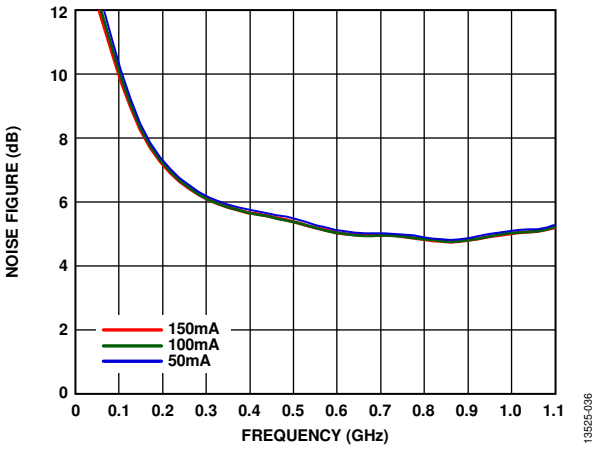

Figure 37. Noise Figure vs. Frequency at Various Supply Currents

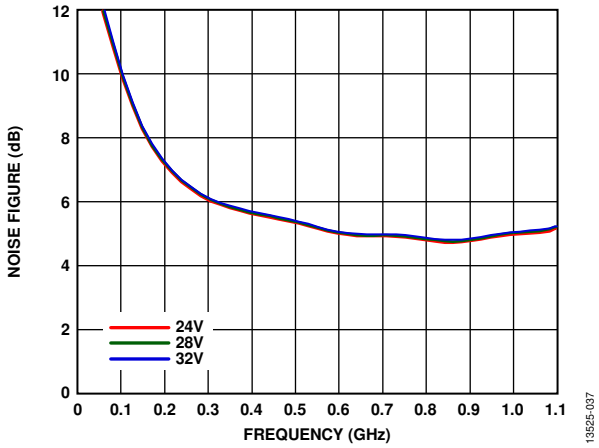

Figure 36. Noise Figure vs. Frequency at Various Supply Voltages

THEORY OF OPERATION

The HMC1099 is a >10 W, gallium nitride (GaN), power amplifier that consists of a single gain stage that effectively operates like a single field effect transistor (FET). The device is internally prematched so that a simple, external matching network optimizes the performance across the entire operating frequency range. The recommended dc bias conditions put the device in deep Class AB operation, resulting in high saturated output power (40.5 dBm typical) at improved levels of power efficiency (69% typical).

APPLICATIONS INFORMATION

The drain bias voltage is applied through the RFOUT/V_{DD} pin, and the gate bias voltage is applied through the RFIN/V_{GG} pin. For operation of a single application circuit across the entire frequency range, it is recommended to use the external matching components specified in the typical application circuit (L1, C1, L3, and C8) shown in Figure 38. If operation is only required across a narrower frequency range, performance may be optimized additionally through the implementation of alternate matching networks. Capacitive bypassing of V_{DD} and V_{GG} is recommended.

The recommended power-up bias sequence follows:

1. Connect to the GND pin.
2. Set V_{GG} to −8 V to pinch off the drain current.
3. Set V_{DD} to 28 V (drain current is pinched off).
4. Adjust V_{GG} more positive (approximately −2.5 V to −3.0 V) until a quiescent of I_{DD} = 100 mA is obtained.
5. Apply the RF signal.

The recommended power-down bias sequence follows:

1. Turn off the RF signal.
2. Set V_{GG} to −8 V to pinch off the drain current.
3. Set V_{DD} to 0 V.
4. Set V_{GG} to 0 V.

All measurements for this device were taken using the typical application circuit, configured as shown in the assembly diagram (see Figure 38). The bias conditions shown in the electrical specifications table (see Table 1 to Table 3) are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the HMC1099 under other bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section.

The evaluation printed circuit board (PCB) provides the HMC1099 in its typical application circuit, allowing easy operation using standard dc power supplies and 50 Ω RF test equipment.

TYPICAL APPLICATION CIRCUIT

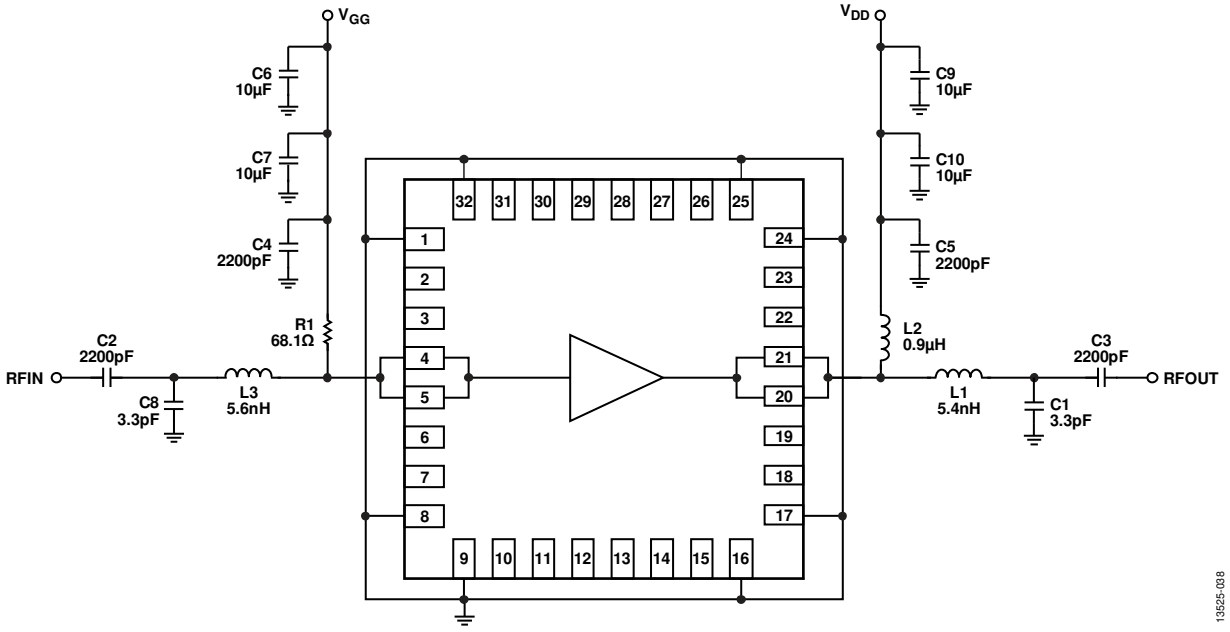

Figure 38. Typical Application Circuit

EVALUATION PCB

Use RF circuit design techniques for the circuit board used in the application. Provide 50 Ω impedance for the signal lines and directly connect the package ground leads and exposed paddle to the ground plane, similar to that shown in Figure 39. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 39 is available from Analog Devices, Inc., upon request.

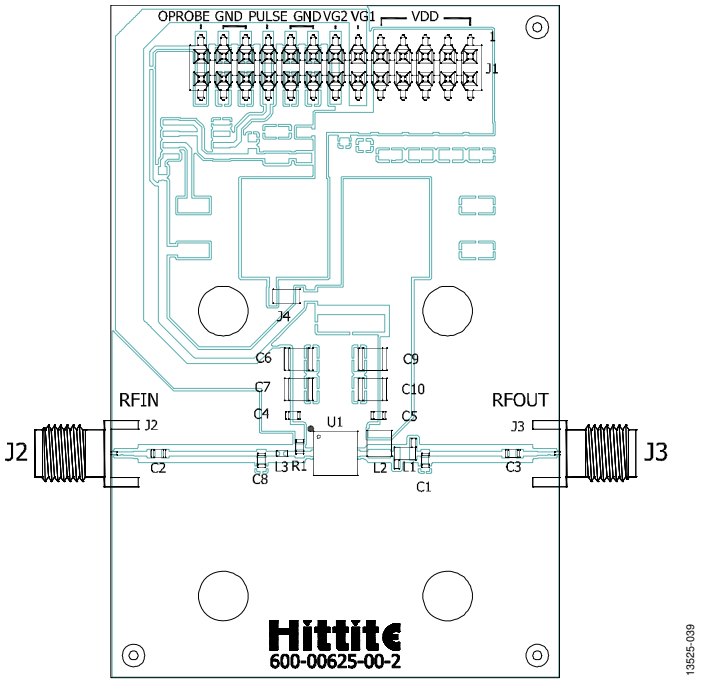

Figure 39. Evaluation Printed Circuit Board

BILL OF MATERIALS

Table 7. Bill of Materials for Evaluation PCB EV1HMC1099LP5D

Item	Description
J2, J3	SMA connectors
J1	DC pin
J4	Preform jumper
C1, C8	3.3 pF capacitors, 0603 package
C2 to C5	2200 pF capacitors, 0603 package
C6, C7, C9, C10	10 µF capacitors, 1210 package
L1	5.4 nH inductor, 0906 package
L2	0.9 µH inductor, 1008 package
L3	5.6 nH inductor, 0402 package
R1	68.1 Ω resistor, 0603 package
U1	HMC1099LP5DE
PCB	600-00625-00-2 evaluation PCB, circuit board material: Rogers 4350 or Arlon 25FR

OUTLINE DIMENSIONS

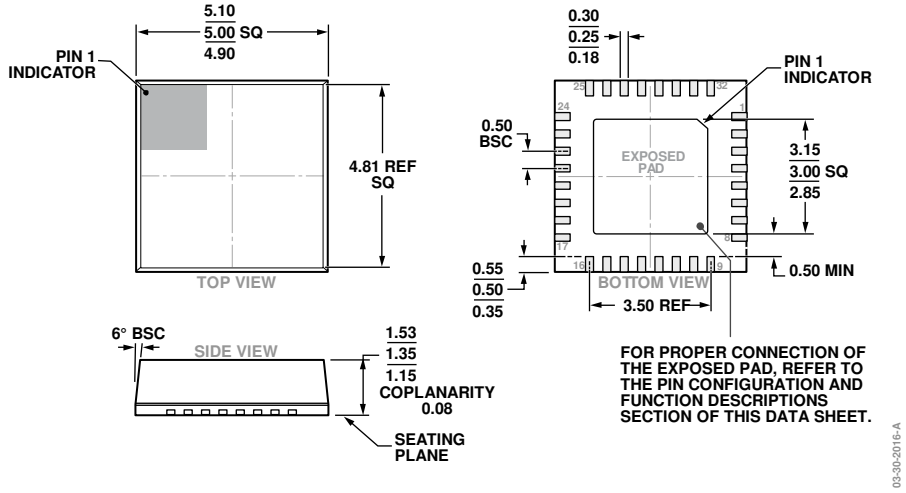

Figure 40. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.34 mm Package Height
(CG-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature	MSL Rating[3]	Description[4]	Package Option	Branding[5]
HMC1099LP5DE	−40°C to +85°C	MSL3	32-Lead LFCSP_CAV	CG-32-1	H1099 XXXX
HMC1099LP5DETR	−40°C to +85°C	MSL3	32-Lead LFCSP_CAV	CG-32-1	H1099 XXXX
EV1HMC1099LP5D			Evaluation PCB		

[1] The HMC1099LP5DE and the HMC1099LP5DETR are LFCSP premolded copper alloy lead frame and RoHS Compliant.
[2] When ordering the evaluation board only, reference the model number, EV1HMC1099LP5D.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC1099LP5DE and the HMC1099LP5DETR are nickel palladium gold (NiPdAu).
[5] The 4-digit lot number for the HMC1099LP5DE and the HMC1099LP5DETR are represented by XXXX.

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