Data Sheet, V1.0, Feb 2005

TC1100

32-Bit Single-Chip Microcontroller

Advance Information

Microcontrollers

Never stop thinking.

Edition 2005-02

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Previous Version:	none
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Controller Area Network (CAN): License of Robert Bosch GmbH

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Advance Information

32-Bit Single-Chip Microcontroller **TC1100**
TriCore™ Family

1 Summary of Features

- High Performance 32-bit TriCore™ V1.3 CPU with 4-Stage Pipeline
- Floating Point Unit (FPU)
- Dual Issue super-scalar implementation
  - MAC Instruction maximum triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- Memory Management Unit (MMU)
- On-chip Memory
  - 28-Kbyte Data Memory (SPRAM)
  - 32-Kbyte Code Memory (SPRAM)
  - 16-Kbyte Instruction Cache (ICACHE)
  - 4-Kbyte Data Cache (DCACHE)
  - 64-Kbyte SRAM Data Memory Unit (DMU)
  - 16-Kbyte Boot ROM
- On-chip Bus Systems
  - 64-bit High Performance Local Memory Bus (LMB) for fast access between caches and on-local memories and FPI Interface
  - On-chip Flexible Peripheral Interconnect Bus (FPI) for interconnections of functional units
- DMA Controller with 8 channels for data transfer operations between peripheral units and memory locations
- One high speed Micro Link Interface (MLI0) for controller communication and emulation
- Flexible External Bus Interface Unit (EBU) to access external data memories
- One Multifunctional General Purpose Timer Unit (GPTU) with three 32-bit timer/counters
- One Capture and Compare unit (CCU61) for PWM signal generation with
  - 3-channel, 16 bit Capture and Compare unit
  - 1-channel, 16 bit Compare unit
- Two Asynchronous/Synchronous Serial Channels (ASC0/1) with baud-rate generator, parity, framing and overrun error detection, support FIFO and IrDA data transmission
- Two High Speed Synchronous Serial Channels (SSC0/1) with programmable data length, FIFO support and shift direction
- Inter-IC (IIC) module with two physical IIC buses
- Digital I/O ports with 3.3 V I/O capabilities

- Level 2 On-chip Debug Support
- Power Management System
- Clock Generation Unit with PLL
- Maximum CPU and Bus clock frequency at 150 MHz without MMU and 120 MHz with MMU
- Ambient temperature under bias: -40° to +85°C
- P-LBGA-208 package

2 General Device Information

2.1 Block Diagram

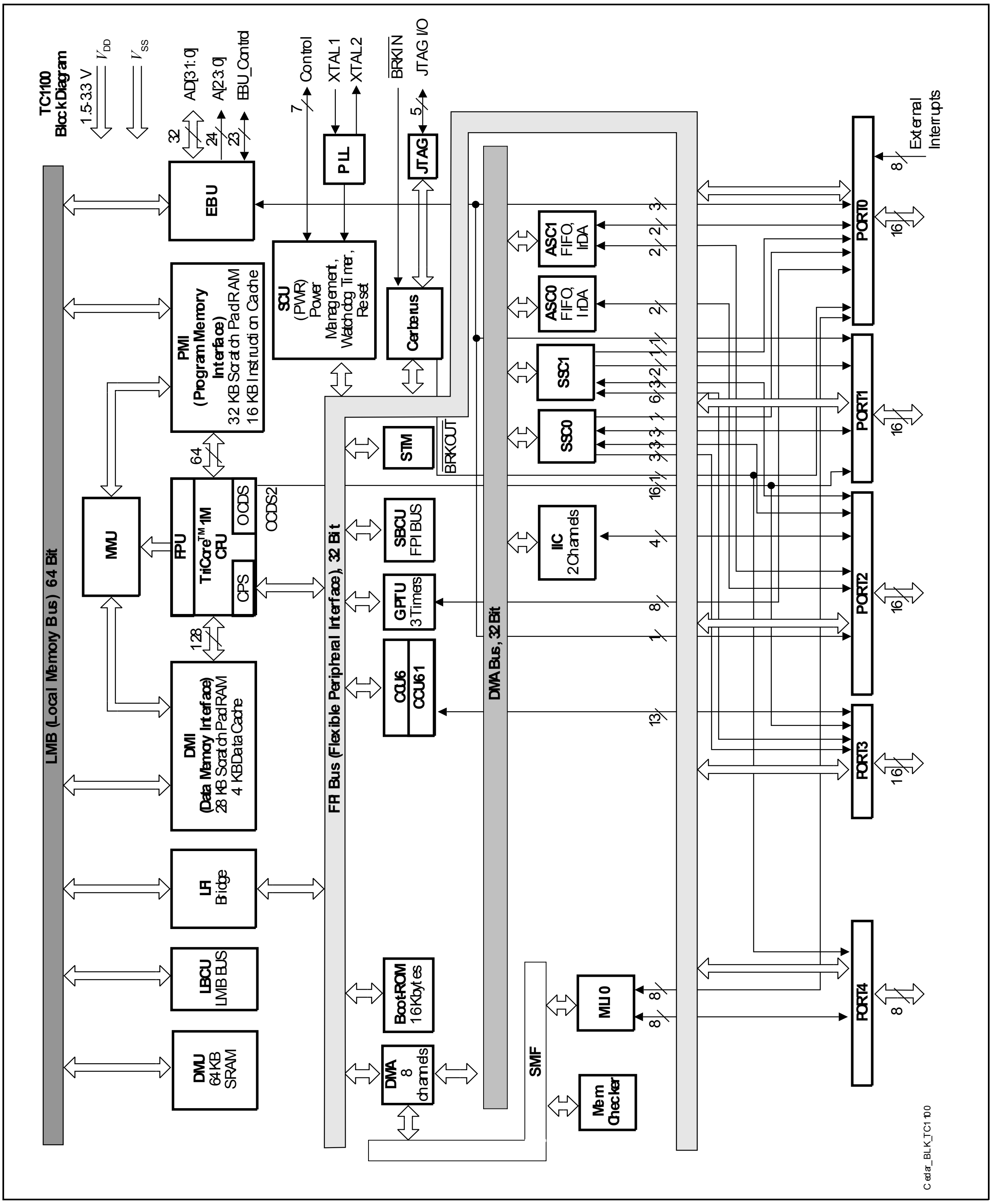


Figure 2-1 TC1100 Block Diagram

2.2 Logic Symbol

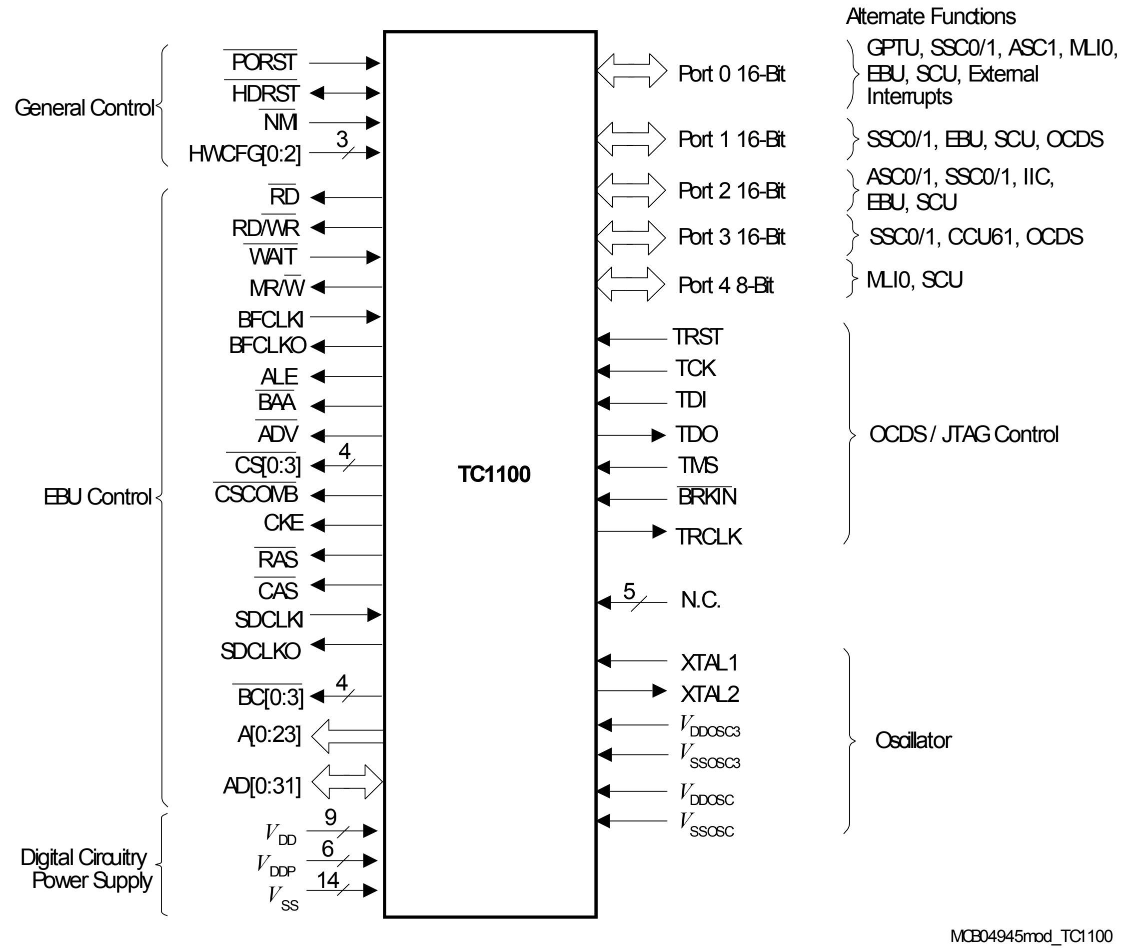
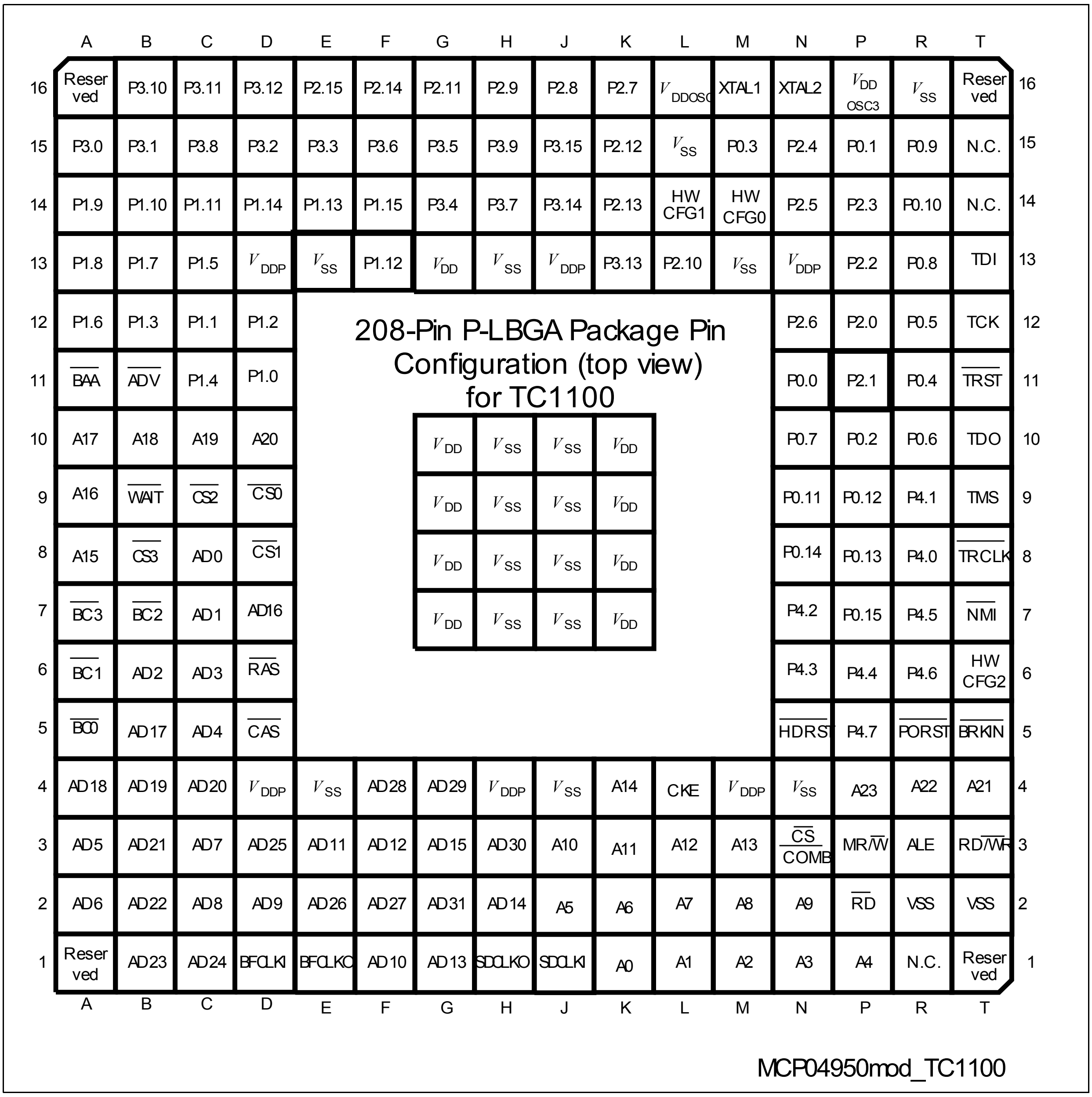


Figure 2-2 TC1100 Logic Symbol

2.3 Pin Configuration



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	
16	Reserved	P3.10	P3.11	P3.12	P2.15	P2.14	P2.11	P2.9	P2.8	P2.7	V_{DDOSC}	XTAL1	XTAL2	V_{DD} OSC3	V_{SS}	Reserved	16
15	P3.0	P3.1	P3.8	P3.2	P3.3	P3.6	P3.5	P3.9	P3.15	P2.12	V_{SS}	P0.3	P2.4	P0.1	P0.9	N.C.	15
14	P1.9	P1.10	P1.11	P1.14	P1.13	P1.15	P3.4	P3.7	P3.14	P2.13	HW CFG1	HW CFG0	P2.5	P2.3	P0.10	N.C.	14
13	P1.8	P1.7	P1.5	V_{DDP}	V_{SS}	P1.12	V_{DD}	V_{SS}	V_{DDP}	P3.13	P2.10	V_{SS}	V_{DDP}	P2.2	P0.8	TDI	13
12	P1.6	P1.3	P1.1	P1.2									P2.6	P2.0	P0.5	TCK	12
11	$\overline{\text{BAA}}$	$\overline{\text{ADV}}$	P1.4	P1.0									P0.0	P2.1	P0.4	$\overline{\text{TRST}}$	11
10	A17	A18	A19	A20			V_{DD}	V_{SS}	V_{SS}	V_{DD}			P0.7	P0.2	P0.6	TDO	10
9	A16	$\overline{\text{WAIT}}$	$\overline{\text{CS2}}$	$\overline{\text{CS0}}$			V_{DD}	V_{SS}	V_{SS}	V_{DD}			P0.11	P0.12	P4.1	TMS	9
8	A15	$\overline{\text{CS3}}$	AD0	$\overline{\text{CS1}}$			V_{DD}	V_{SS}	V_{SS}	V_{DD}			P0.14	P0.13	P4.0	$\overline{\text{TRCLK}}$	8
7	$\overline{\text{BC3}}$	$\overline{\text{BC2}}$	AD1	AD16			V_{DD}	V_{SS}	V_{SS}	V_{DD}			P4.2	P0.15	P4.5	$\overline{\text{NMI}}$	7
6	$\overline{\text{BC1}}$	AD2	AD3	$\overline{\text{RAS}}$									P4.3	P4.4	P4.6	HW CFG2	6
5	$\overline{\text{BC0}}$	AD17	AD4	$\overline{\text{CAS}}$									$\overline{\text{HDRST}}$	P4.7	$\overline{\text{PORST}}$	$\overline{\text{BRKIN}}$	5
4	AD18	AD19	AD20	V_{DDP}	V_{SS}	AD28	AD29	V_{DDP}	V_{SS}	A14	CKE	V_{DDP}	V_{SS}	A23	A22	A21	4
3	AD5	AD21	AD7	AD25	AD11	AD12	AD15	AD30	A10	A11	A12	A13	$\overline{\text{CS}}$ COMB	MR/$\overline{\text{W}}$	ALE	RD/$\overline{\text{WR}}$	3
2	AD6	AD22	AD8	AD9	AD26	AD27	AD31	AD14	A5	A6	A7	A8	A9	$\overline{\text{RD}}$	VSS	VSS	2
1	Reserved	AD23	AD24	BFCLKI	BFCLKO	AD10	AD13	SDCLKO	SDCLKI	A0	A1	A2	A3	A4	N.C.	Reserved	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	

Figure 2-3 TC1100 Pins: P-BGA-208 Package (top view)

2.4 Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P0		I/O		**Port 0** Port 0 is a 16-bit bi-directional general purpose I/O port that can be alternatively used for GPTU, ASC1, SSC0/ 1, MLI0, EBU and SCU.	
P0.0	N11	I/O	PUC	GPTU_0	GPTU input/output line 0
		I/O		RXD1B	ASC1 receiver input/output B
P0.1	P15	I/O	PUC	GPTU_1	GPTU input/output line 1
		O		TXD1B	ASC1 transmitter output B
P0.2	P10	I/O	PUC	GPTU_2	GPTU input/output line 2
P0.3	M15	I/O	PUC	GPTU_3	GPTU input/output line 3
P0.4	R11	I/O	PUC	GPTU_4	GPTU input/output line 4
		I		SLSI1	SSC1 Slave Select input
		O		BREQ	EBU Bus Request Output
P0.5	R12	I/O	PUC	GPTU_5	GPTU input/output line 5
		I		$\overline{\text{HOLD}}$	EBU Hold Request Input
		O		BRKOUT_B	OCDS Break Out B
P0.6	R10	I/O	PUC	GPTU_6	GPTU input/output line 6
		I/O		HLDA	EBU Hold Acknowledge Input/Output
		O		SLSO0_0	SSC0 Slave Select output 0
P0.7	N10	I/O	PUC	GPTU_7	GPTU input/output line 7
		O		SLSO1_0	SSC1 Slave Select output 0
P0.8	R13	I	PUC	REQ0	External Trigger Input 0
		O		TCLK0A	MLI0 transmit channel clock output A
P0.9	R15	I	PUC	TREADY0A	MLI0 transmit channel ready input A
		I		REQ1	External Trigger Input 1
P0.10	R14	I	PUC	REQ2	External Trigger Input 2
		O		TVALID0A	MLI0 transmit channel valid output A
P0.11	N9	I	PUC	REQ3	External Trigger Input 3
		O		TDATA0A	MLI0 transmit channel data output A
P0.12	P9	I	PUC	RCLK0A	MLI0 receive channel clock input A
		I		REQ4	External Trigger Input 4
P0.13	P8	I	PUC	REQ5	External Trigger Input 5
		O		RREADY0A	MLI0 receive channel ready output A
P0.14	N8	I	PUC	REQ6	External Trigger Input 6
		I		RVALID0A	MLI0 receive channel valid input A
P0.15	P7	I	PUC	REQ7	External Trigger Input 7
		I		RDATA0A	MLI0 receive channel data input A

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD1)	Functions	
P1		I/O		**Port 1** Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for OCDS L2, SSC0/1, EBU and SCU.	
P1.0	D11	I	PUC	SWCFG0	Software configuration 0
		O		OCDSA_0	OCDS L2 Debug Line A0
P1.1	C12	I	PUC	SWCFG1	Software configuration 1
		O		OCDSA_1	OCDS L2 Debug Line A1
P1.2	D12	I	PUC	SWCFG2	Software configuration 2
		O		OCDSA_2	OCDS L2 Debug Line A2
P1.3	B12	I	PUC	SWCFG3	Software configuration 3
		O		OCDSA_3	OCDS L2 Debug Line A3
P1.4	C11	I	PUC	SWCFG4	Software configuration 4
		O		OCDSA_4	OCDS L2 Debug Line A4
P1.5	C13	I	PUC	SWCFG5	Software configuration 5
		O		OCDSA_5	OCDS L2 Debug Line A5
P1.6	A12	I	PUC	SWCFG6	Software configuration 6
		O		OCDSA_6	OCDS L2 Debug Line A6
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1]	Functions	
P1.15	F14	I O I O	PUC	SLSI0 RMW SWCFG15 OCDSA_15	SSC0 Slave Select Input EBU Read Modify Write Software configuration 15 OCDS L2 Debug Line A15
P2		I/O		**Port 2** Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1, SSC0/1, IIC, EBU and SCU.	
P2.0	P12	I/O O	PUC	RXD0 CSEMU	ASC0 receiver input/output line EBU Chip Select Output for Emulator Region
P2.1	P11	O I	PUC	TXD0 TESTMODE	ASC0 transmitter output line Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0	SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0	SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0	SSC0 clock input/output line
P2.5	N14	I/O	PUC	MRST1A	SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O	PUC	MTSR1A	SSC1 master transmit/slave receive input/output A
P2.7	K16	I/O	PUC	SCLK1A	SSC1 clock input/output line A
P2.8	J16	I/O	PUC	RXD1A	ASC1 receiver input/output line A
P2.9	H16	O	PUC	TXD1A	ASC1 transmitter output line A
P2.10	L13	—	PUC	—	
P2.11	G16	—	PUC	—	
P2.12	K15	I/O O	—	SDA0 SLSO0_3	IIC Serial Data line 0 SSC0 Slave Select output 3
P2.13	K14	I/O O	—	SCL0 SLSO1_3	IIC clock line 0 SSC1 Slave Select output 3
P2.14	F16	I/O O	—	SDA1 SLSO0_4	IIC Serial Data line 1 SSC0 Slave Select output 4
P2.15	E16	I/O O	—	SCL1 SLSO1_4	IIC clock line 1 SSC1 Slave Select output 4

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	**Pin**	**In Out**	**PU/ PD**[1]	**Functions**	
P3		I/O		**Port 3** Port 3 is a 16-bit bi-directional general purpose I/O port that can be alternatively used for CCU61, SSC0/1 and OCDS Level 2 debug lines.	
P3.0	A15	O	PUC	OCDSB_0	OCDS L2 Debug Line B0
		O		COUT61_3	CCU61 compare channel 3 output
P3.1	B15	O	PUC	OCDSB_1	OCDS L2 Debug Line B1
		I/O		CC61_0	CCU61 input/output of capture/ compare channel 0
P3.2	D15	O	PUC	OCDSB_2	OCDS L2 Debug Line B2
		O		COUT61_0	CCU61 output of capture/compare channel 0
P3.3	E15	O	PUC	OCDSB_3	OCDS L2 Debug Line B3
		I/O		CC61_1	CCU61 input/output of capture/ compare channel 1
P3.4	G14	O	PUC	OCDSB_4	OCDS L2 Debug Line B4
		O		COUT61_1	CCU61 output of capture/compare channel 1
P3.5	G15	O	PUC	OCDSB_5	OCDS L2 Debug Line B5
		I/O		CC61_2	CCU61 input/output of capture/ compare channel 2
P3.6	F15	O	PUC	OCDSB_6	OCDS L2 Debug Line B6
		O		COUT61_2	CCU61 output of capture/compare channel 2
P3.7	H14	O	PUC	OCDSB_7	OCDS L2 Debug Line B7
		I		CTRAP1	CCU61 trap input
		O		SLSO0_5	SSC0 Slave Select output 5
P3.8	C15	O	PUC	OCDSB_8	OCDS L2 Debug Line B8
		I		CCPOS1_0	CCU61 Hall input signal 0
		O		SLSO1_5	SSC1 Slave Select output 5
P3.9	H15	O	PUC	OCDSB_9	OCDS L2 Debug Line B9
		I		CCPOS1_1	CCU61 Hall input signal 1
		O		SLSO0_6	SSC0 Slave Select output 6
P3.10	B16	O	PUC	OCDSB_10	OCDS L2 Debug Line B10
		I		CCPOS1_2	CCU61 Hall input signal 2
		O		SLSO1_6	SSC1 Slave Select output 6
P3.11	C16	O	PUC	OCDSB_11	OCDS L2 Debug Line B11
		O		SLSO0_7	SSC0 Slave Select output 7
		I		CC61_T12HR	CCU61 Timer 12 hardware run

Table 2-1 Pin Definitions and Functions (cont’d)

Symbol	**Pin**	**In Out**	**PU/ PD**[1]	**Functions**	
P3.12	D16	O	PUC	OCDSB_12	OCDS L2 Debug Line B12
		O		SLSO1_7	SSC1 Slave Select output 7
		I		CC61_T13HR	CCU61 Timer 13 hardware run
P3.13	K13	O	PUC	OCDSB_13	OCDS L2 Debug Line B13
		I/O		MRST1B	SSC1 master receive/slave transmit input/output B
P3.14	J14	O	PUC	OCDSB_14	OCDS L2 Debug Line B14
		I/O		MTSR1B	SSC1 master transmit/slave receive input/output B
P3.15	J15	O	PUC	OCDSB_15	OCDS L2 Debug Line B15
		I/O		SCLK1B	SSC1 clock input/output line B
P4		I/O		**Port 4** Port 4 is an 8-bit bi-directional general purpose I/O port that can be alternatively used for MLI0 and SCU.	
P4.0	R8	O	PUC	TCLK0B	MLI0 transmit channel clock output B
P4.1	R9	I	PUC	TREADY0B	MLI0 transmit channel ready input B
P4.2	N7	O	PUC	TVALID0B	MLI0 transmit channel valid output B
P4.3	N6	O	PUC	TDATA0B	MLI0 transmit channel data output B
P4.4	P6	I	PUC	RCLK0B	MLI0 receive channel clock input B
P4.5	R7	O	PUC	RREADY0B	MLI0 receive channel ready output B
P4.6	R6	I	PUC	RVALID0B	MLI0 receive channel valid input B
P4.7	P5	I	PUC	RDATA0B	MLI0 receive channel data input B
		O		$\overline{\text{BRKOUT}}$_A	OCDS Break Out A
$\overline{\textbf{HDRST}}$	N5	I/O	PUA	**Hardware Reset Input/Reset Indication Output** Assertion of this bi-directional open-drain pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for a minimum 4 f_{CPU} clock cycles. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset for a specific period of time. For a software reset, activation of this pin is programmable.	
$\overline{\textbf{PORST}}$	R5	I	PUC	**Power-on Reset Input** A low level on $\overline{\text{PORST}}$ causes an asynchronous reset of the entire chip. $\overline{\text{PORST}}$ is a fully asynchronous level sensitive signal.	

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1]	Functions
$\overline{\text{NMI}}$	T7	I	PUC	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes a NMI-Trap request to the CPU.
$\overline{\text{TRST}}$	T11	I	PDC	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	T12	I	PUC	**JTAG Module Clock Input**
TDI	T13	I	PUC	**JTAG Module Serial Data Input**
TDO	T10	O	—	**JTAG Module Serial Data Output**
TMS	T9	I	PUC	**JTAG Module State Machine Control Input**
$\overline{\text{TRCLK}}$	T8	O	—	**Trace Clock for OCDS_L2 Lines**
HWCFG0 HWCFG1 HWCFG2	M14 L14 T6	I I I	PUC PUC PDC	**Hardware Configuration Inputs** The Configuration Inputs define the boot options of the TC1100 after a hardware invoked reset operation.
$\overline{\text{BRKIN}}$	T5	I	PUC	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{CS0}}$ $\overline{\text{CS1}}$ $\overline{\text{CS2}}$ $\overline{\text{CS3}}$	D9 D8 C9 B8	O O O O	PUC PUC PUC PUC	**EBU Chip Select Output Line 0** **EBU Chip Select Output Line 1** **EBU Chip Select Output Line 2** **EBU Chip Select Output Line 3** Each corresponds to a programmable region. Only one can be active at one time.
$\overline{\text{CSCOMB}}$	N3	O	PUC	**EBU Chip Select Output for Combination Function (Overlay Memory and Global)**
SDCLKI	J1	I	—	**SDRAM Clock Input (Clock Feedback)**
SDCLKO	H1	O	—	**SDRAM Clock Output** Accesses to SDRAM devices are synchronized to this clock.
$\overline{\text{RAS}}$	D6	O	PUC	**EBU SDRAM Row Address Strobe Output**
$\overline{\text{CAS}}$	D5	O	PUC	**EBU SDRAM Column Address Strobe Output**
CKE	L4	O	PUC	**EBU SDRAM Clock Enable Output**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1]	Functions
BFCLKI	D1	I	—	**Burst Flash Clock Input (Clock Feedback)**
BFCLKO	E1	O	—	**Burst Flash Clock Output** Accesses to Burst Flash devices are synchronized to this clock.
$\overline{\text{RD}}$	P2	O	PUC	**EBU Read Control Line** Output in master mode Input in slave mode
RD/$\overline{\text{WR}}$	T3	O	PUC	**EBU Write Control Line** Output in master mode Input in slave mode
$\overline{\text{WAIT}}$	B9	I	PUC	**EBU Wait Control Line**
ALE	R3	O	PDC	**EBU Address Latch Enable Output**
MR/$\overline{\text{W}}$	P3	O	PUC	**EBU Motorola-style Read/Write Output**
$\overline{\text{BAA}}$	A11	O	PUC	**EBU Burst Address Advance Output** For advancing address in a Burst Flash access
$\overline{\text{ADV}}$	B11	O	PUC	**EBU Burst Flash Address Valid Output**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	**Pin**	**In Out**	**PU/ PD$^{1)}$**	**Functions**
				EBU Address/Data Bus Input/Output Lines
AD0	C8	I/O	PUC	EBU Address/Data Bus Line 0
AD1	C7	I/O	PUC	EBU Address/Data Bus Line 1
AD2	B6	I/O	PUC	EBU Address/Data Bus Line 2
AD3	C6	I/O	PUC	EBU Address/Data Bus Line 3
AD4	C5	I/O	PUC	EBU Address/Data Bus Line 4
AD5	A3	I/O	PUC	EBU Address/Data Bus Line 5
AD6	A2	I/O	PUC	EBU Address/Data Bus Line 6
AD7	C3	I/O	PUC	EBU Address/Data Bus Line 7
AD8	C2	I/O	PUC	EBU Address/Data Bus Line 8
AD9	D2	I/O	PUC	EBU Address/Data Bus Line 9
AD10	F1	I/O	PUC	EBU Address/Data Bus Line 10
AD11	E3	I/O	PUC	EBU Address/Data Bus Line 11
AD12	F3	I/O	PUC	EBU Address/Data Bus Line 12
AD13	G1	I/O	PUC	EBU Address/Data Bus Line 13
AD14	H2	I/O	PUC	EBU Address/Data Bus Line 14
AD15	G3	I/O	PUC	EBU Address/Data Bus Line 15
AD16	D7	I/O	PUC	EBU Address/Data Bus Line 16
AD17	B5	I/O	PUC	EBU Address/Data Bus Line 17
AD18	A4	I/O	PUC	EBU Address/Data Bus Line 18
AD19	B4	I/O	PUC	EBU Address/Data Bus Line 19
AD20	C4	I/O	PUC	EBU Address/Data Bus Line 20
AD21	B3	I/O	PUC	EBU Address/Data Bus Line 21
AD22	B2	I/O	PUC	EBU Address/Data Bus Line 22
AD23	B1	I/O	PUC	EBU Address/Data Bus Line 23
AD24	C1	I/O	PUC	EBU Address/Data Bus Line 24
AD25	D3	I/O	PUC	EBU Address/Data Bus Line 25
AD26	E2	I/O	PUC	EBU Address/Data Bus Line 26
AD27	F2	I/O	PUC	EBU Address/Data Bus Line 27
AD28	F4	I/O	PUC	EBU Address/Data Bus Line 28
AD29	G4	I/O	PUC	EBU Address/Data Bus Line 29
AD30	H3	I/O	PUC	EBU Address/Data Bus Line 30
AD31	G2	I/O	PUC	EBU Address/Data Bus Line 31
$\overline{\mathbf{BC0}}$	A5	O	PUC	**EBU Byte Control Line 0**
$\overline{\mathbf{BC1}}$	A6	O	PUC	**EBU Byte Control Line 1**
$\overline{\mathbf{BC2}}$	B7	O	PUC	**EBU Byte Control Line 2**
$\overline{\mathbf{BC3}}$	A7	O	PUC	**EBU Byte Control Line 3**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	**Pin**	**In Out**	**PU/ PD**[1]	**Functions**
				EBU Address Bus Input/Output Lines
A0	K1	O	PUC	EBU Address Bus Line 0
A1	L1	O	PUC	EBU Address Bus Line 1
A2	M1	O	PUC	EBU Address Bus Line 2
A3	N1	O	PUC	EBU Address Bus Line 3
A4	P1	O	PUC	EBU Address Bus Line 4
A5	J2	O	PUC	EBU Address Bus Line 5
A6	K2	O	PUC	EBU Address Bus Line 6
A7	L2	O	PUC	EBU Address Bus Line 7
A8	M2	O	PUC	EBU Address Bus Line 8
A9	N2	O	PUC	EBU Address Bus Line 9
A10	J3	O	PUC	EBU Address Bus Line 10
A11	K3	O	PUC	EBU Address Bus Line 11
A12	L3	O	PUC	EBU Address Bus Line 12
A13	M3	O	PUC	EBU Address Bus Line 13
A14	K4	O	PUC	EBU Address Bus Line 14
A15	A8	O	PUC	EBU Address Bus Line 15
A16	A9	O	PUC	EBU Address Bus Line 16
A17	A10	O	PUC	EBU Address Bus Line 17
A18	B10	O	PUC	EBU Address Bus Line 18
A19	C10	O	PUC	EBU Address Bus Line 19
A20	D10	O	PUC	EBU Address Bus Line 20
A21	T4	O	PUC	EBU Address Bus Line 21
A22	R4	O	PUC	EBU Address Bus Line 22
A23	P4	O	PUC	EBU Address Bus Line 23
XTAL1	M16	I	—	**Oscillator/PLL/Clock Generator Input/Output Pins**
XTAL2	N16	O	—	XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking of the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation, XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC3}	P16	—	—	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC3}	R16	—	—	**Main Oscillator Ground**
V_{DDOSC}	L16	—	—	**Main Oscillator Power Supply (1.5 V)**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1]	Functions
V_{SSOSC}	L15	—	—	**Main Oscillator Ground**
V_{DD}	G7 G8 G9 G10 G13 K7,K8 K9 K10	—	—	**Core and Logic Power Supply (1.5 V)**
V_{DDP}	D4 D13 H4 J13 M4 N13	—	—	**Ports Power Supply (3.3 V)**
V_{SS}	E4 E13 H7 H8 H9 H10 H13 J4,J7 J8,J9 J10 M13 N4 R2,T2	—	—	**Ground**
N.C.	A1 A16 T1,R1 T14 T15 T16	—	—	**Not Connected** These pins must not be connected.

[1] Refers to internal pull-up or pull-down device connected and corresponding type. The notation '—' indicates that the internal pull-up or pull-down device is not enabled.

Note: P2.12 to P2.15 are always configured as open drain.

3 Functional Description

3.1 On-Chip Memories

The TC1100 provides the following on-chip memories:

- Program Memory Interface (PMI) with
  - 32-Kbyte Scratch-pad Code RAM (SPRAM)
  - 16-Kbyte Instruction Cache Memory (ICACHE)
- Data Memory Interface (DMI) with
  - 28-Kbyte Scratch-pad Data RAM (SPRAM)
  - 4-Kbyte Data Cache Memory (DCACHE)
- Data Memory Unit (DMU) with
  - 64-Kbyte SRAM
- 16-Kbyte Boot ROM (BROM)

3.2 Address Map

Table 3-1 defines the specific segment oriented address blocks of the TC1100 with its address range, size, and PMI/DMI access view. Table 3-2 shows the block address map of the Segment 15 which includes on-chip peripheral units and ports.

Table 3-1 TC1100 Block Address Map

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
0 – 7	0000 0000$_H$ – 7FFF FFFF$_H$	2 GB	MMU Space	via FPI	via FPI	cached
8	8000 0000$_H$ – 8FFF FFFF$_H$	256 MB	External Memory Space mapped from Segment 10	via LMB	via LMB	
9	9000 0000$_H$ – 9FDF FFFF$_H$	256 MB	Reserved	via FPI	via FPI	
10	A000 0000$_H$ – AFBF FFFF$_H$	252 MB	External Memory Space	via LMB	via LMB	non-cached
	AFC0 0000$_H$ – AFC0 FFFF$_H$	64 KB	DMU Space			
	AFC1 0000$_H$ – AFFF FFFF$_H$	~4 MB	Reserved			
11	B000 0000$_H$ – BFFF FFFF$_H$	256 MB	Reserved	via FPI	via FPI	
12	C000 0000$_H$ – C000 FFFF$_H$	64 KB	DMU	via LMB	via LMB	cached
	C001 0000$_H$ – CFFF FFFF$_H$	~ 256 MB	Reserved			

Table 3-1 TC1100 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
13	D000 0000$_H$ – D000 6FFF$_H$	28 KB	DMI Local Data RAM (LDRAM)	DMI local	via LMB	non-cached
	D000 7000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved			
	D400 0000$_H$ – D400 7FFF$_H$	32 KB	PMI Local Code Scratch Pad RAM (SPRAM)	via LMB	PMI local	
	D400 8000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved			
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via FPI	via FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	via LMB	
	E800 0000$_H$ – E83F FFFF$_H$	4 MB	Reserved for mapped space for lower 4 Mbytes of Local Memory in Segment 12 (Transformed by LFI bridge to C000 0000$_H$ – C03F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E840 0000$_H$ – E84F FFFF$_H$	1 MB	Reserved for mapped space for lower 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D000 0000$_H$ – D00F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E850 0000$_H$ – E85F FFFF$_H$	1 MB	Reserved for mapped space for 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D400 0000$_H$ – D40F FFFF$_H$)			

Table 3-1 TC1100 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
14	E860 0000$_H$ – EFFF FFFF$_H$	122 MB	Reserved	–	–	non-cached
15	F000 0000$_H$ - FFFF FFFF$_H$	256 MB	See **Table 3-2**	via LMB or via FPI	via LMB or via FPI	

Table 3-2 Block Address Map of Segment 15

Symbol	Description	Address Range	Size
System Peripheral Bus (SPB)			
SCU	System Control Unit (incl. WDT)	F000 0000$_H$ - F000 00FF$_H$	256 Bytes
SBCU	FPI Bus Control Unit	F000 0100$_H$ - F000 01FF$_H$	256 Bytes
STM	System Timer	F000 0200$_H$ - F000 02FF$_H$	256 Bytes
OCDS	On-Chip Debug Support (Cerberus)	F000 0300$_H$ - F000 03FF$_H$	256 Bytes
–	Reserved	F000 0400$_H$ - F000 04FF$_H$	256 Bytes
–	Reserved	F000 0500$_H$ - F000 05FF$_H$	256 Bytes
GPTU	General Purpose Timer Unit	F000 0600$_H$ - F000 06FF$_H$	256 Bytes
–	Reserved	F000 0700$_H$ - F000 07FF$_H$	256 Bytes
–	Reserved	F000 0800$_H$ - F000 08FF$_H$	256 Bytes
–	Reserved	F000 0900$_H$ - F000 09FF$_H$	256 Bytes
–	Reserved	F000 0A00$_H$ - F000 0AFF$_H$	256 Bytes
–	Reserved	F000 0B00$_H$ - F000 0BFF$_H$	256 Bytes
P0	Port 0	F000 0C00$_H$ - F000 0CFF$_H$	256 Bytes
P1	Port 1	F000 0D00$_H$ - F000 0DFF$_H$	256 Bytes
P2	Port 2	F000 0E00$_H$ - F000 0EFF$_H$	256 Bytes
P3	Port 3	F000 0F00$_H$ - F000 0FFF$_H$	256 Bytes
P4	Port 4	F000 1000$_H$ - F000 10FF$_H$	256 Bytes
–	Reserved	F000 1100$_H$ - F000 11FF$_H$	256 Bytes

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
–	Reserved	F000 1200_H - F000 $12FF_H$	256 Bytes
–	Reserved	F000 1300_H - F000 $13FF_H$	256 Bytes
–	Reserved	F000 1400_H - F000 $14FF_H$	256 Bytes
–	Reserved	F000 1500_H - F000 $15FF_H$	256 Bytes
–	Reserved	F000 1600_H - F000 $16FF_H$	256 Bytes
–	Reserved	F000 1700_H - F000 $17FF_H$	256 Bytes
–	Reserved	F000 1800_H - F000 $18FF_H$	256 Bytes
–	Reserved	F000 1900_H - F000 $19FF_H$	256 Bytes
–	Reserved; these locations should not be written.	F000 2000_H - F000 $20FF_H$	256 Bytes
CCU61	Capture/Compare Unit 1	F000 2100_H - F000 $21FF_H$	256 Bytes
–	Reserved	F000 2200_H - F000 $3BFF_H$	–
DMA	Direct Memory Access Controller	F000 $3C00_H$ - $F0003EFF_H$	3 × 256 Bytes
–	Reserved	F000 $3F00_H$ - F000 $3FFF_H$	–
–	Reserved; these locations should not be written.	F000 4000_H - F000 $5FFF_H$	8 Kbytes
–	Reserved	F000 6000_H - $F00E1FFF_H$	–
–	Reserved; these locations should not be written.	F00E 2000_H - F00E $219F_H$	416 Bytes
–	Reserved; these locations should not be written.	F00E $21A0_H$ - F00E $27FF_H$	1.6 Kbytes
–	Reserved; these locations should not be written.	F00E 2800_H - F00E $28FF_H$	256 Bytes
–	Reserved	F00E 2900_H - F00F $FFFF_H$	–
Units on SMIF Interface of DMA Controller			
–	Reserved	F010 0000_H - F010 $00FF_H$	256 Bytes
SSC0	Synchronous Serial Interface 0	F010 0100_H - F010 $01FF_H$	256 Bytes
SSC1	Synchronous Serial Interface 1	F010 0200_H - F010 $02FF_H$	256 Bytes
ASC0	Async./Sync. Serial Interface 0	F010 0300_H - F010 $03FF_H$	256 Bytes
ASC1	Async./Sync. Serial Interface 1	F010 0400_H - F010 $04FF_H$	256 Bytes

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	**Description**	**Address Range**	**Size**
–	Reserved; these locations should not be written.	F010 0500_H - F010 $05FF_H$	256 Bytes
I2C	Inter IC	F010 0600_H - F010 $06FF_H$	256 Bytes
–	Reserved	F010 0700_H - F010 $BFFF_H$	–
MLI0	Micro Link Interface 0	F010 $C000_H$ -F010 $C0FF_H$	256 Bytes
–	Reserved; these locations should not be written.	F010 $C100_H$ - F010 $C1FF_H$	256 Bytes
MCHK	Memory Checker	F010 $C200_H$ - F010 $C2FF_H$	256 Bytes
–	Reserved	F010 $C300_H$ - F01D $FFFF_H$	–
MLI0_ SP0	MLI0 Small Transfer Window 0	F01E 0000_H - F01E $1FFF_H$	8 Kbytes
MLI0_ SP1	MLI0 Small Transfer Window 1	F01E 2000_H - F01E $3FFF_H$	8 Kbytes
MLI0_ SP2	MLI0 Small Transfer Window 2	F01E 4000_H - F01E $5FFF_H$	8 Kbytes
MLI0_ SP3	MLI0 Small Transfer Window 3	F01E 6000_H - F01E $7FFF_H$	8 Kbytes
–	Reserved; these locations should not be written.	F01E 8000_H - F01E $9FFF_H$	8 Kbytes
–	Reserved; these locations should not be written.	F01E $A000_H$ - F01E $BFFF_H$	8 Kbytes
–	Reserved; these locations should not be written.	F01E $C000_H$- F01E $DFFF_H$	8 Kbytes
–	Reserved; these locations should not be written.	F01E $E000_H$ - F01E $FFFF_H$	8 Kbytes
–	Reserved	F01F 0000_H - F01F $FFFF_H$	–
MLI0_ LP0	MLI0 Large Transfer Window 0	F020 0000_H - F020 $FFFF_H$	64 Kbytes
MLI0_ LP1	MLI0 Large Transfer Window 1	F021 0000_H - F021 $FFFF_H$	64 Kbytes
MLI0_ LP2	MLI0 Large Transfer Window 2	F022 0000_H - F022 $FFFF_H$	64 Kbytes
MLI0_ LP3	MLI0 Large Transfer Window 3	F023 0000_H - F023 $FFFF_H$	64 Kbytes

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
–	Reserved; these locations should not be written.	F024 0000_H - F024 $FFFF_H$	64 Kbytes
–	Reserved; these locations should not be written.	F025 0000_H - F025 $FFFF_H$	64 Kbytes
–	Reserved; these locations should not be written.	F026 0000_H - F026 $FFFF_H$	64 Kbytes
–	Reserved; these locations should not be written.	F027 0000_H - F027 $FFFF_H$	64 Kbytes
–	Reserved	F028 0000_H - F200 $00FF_H$	–
–	Reserved; these locations should not be written.	F200 0100_H - F200 $05FF_H$	1280Bytes
–	Reserved	F200 0600_H - F7E0 $FEFF_H$	–
CPU (Part of System Peripheral Bus)			
CPU SFRs	CPU Slave Interface	F7E0 $FF00_H$ - F7E0 $FFFF_H$	256 Bytes
	Reserved	F7E1 0000_H - F7E1 $7FFF_H$	–
	MMU	F7E1 8000_H - F7E1 $80FF_H$	256 Bytes
	Reserved	F7E1 8100_H - F7E1 $BFFF_H$	–
	Memory Protection Registers	F7E1 $C000_H$- F7E1 $EFFF_H$	12 Kbytes
	Reserved	F7E1 $F000_H$ - F7E1 $FCFF_H$	–
	Core Debug Register (OCDS)	F7E1 $FD00_H$- F7E1 $FDFF_H$	256 Bytes
	Core Special Function Registers (CSFRs)	F7E1 $FE00_H$- F7E1 $FEFF_H$	256 Bytes
	General Purpose Register (GPRs)	F7E1 $FF00_H$ - F7E1 $FFFF_H$	256 Bytes
–	Reserved	F7E2 0000_H - F7FF $FFFF_H$	–
Local Memory Buses (LMB)			
EBU	External Bus Interface Unit	F800 0000_H - F800 $03FF_H$	1 Kbyte
DMU	Data Memory Unit	F800 0400_H - F800 $04FF_H$	256 Bytes
–	Reserved	F800 0500_H - F87F $FBFF_H$	–
DMI	Data Memory Interface Unit	F87F $FC00_H$ - F87F $FCFF_H$	256 Bytes
PMI	Program Memory Interface Unit	F87F $FD00_H$ - F87F $FDFF_H$	256 Bytes
LBCU	Local Memory Bus Control Unit	F87F $FE00_H$ - F87F $FEFF_H$	256 Bytes

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
LFI	LMB to FPI Bus Bridge	F87F FF00$_H$ - F87F FFFF$_H$	256 Bytes
–	Reserved	F880 0000$_H$ - FFFF FFFF$_H$	–

3.3 Memory Protection System

The TC1100 memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the kinds of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

In TC1100, TriCore™ supports two address spaces: the virtual address space and the physical address space. Both address space are 4 Gbytes in size and divided into 16 segments with each segment being 256 Mbytes. The upper 4 bits of the 32-bit address are used to identify the segment. Virtual segments are numbered 0 - 15. But a virtual address is always translated into a physical address before accessing memory. The virtual address is translated into a physical address using one of two translation mechanisms: (a) direct translation, and (b) Page Table Entry (PTE) based translation. If the virtual address belongs to the upper half of the virtual address space then the virtual address is directly used as the physical address (direct translation). If the virtual address belongs to the lower half of the address space, then the virtual address is used directly as the physical address if the processor is operating in physical mode (direct translation) or translated using a Page Table Entry if the processor is operating in virtual mode (PTE translation). These are managed by Memory Management Unit (MMU).

Memory protection is enforced using separate mechanisms for the two translation paths.

3.3.1 Protection for Direct translation

Memory protection for addresses that undergo direct translation is enforced using the range based protection that has been used in the previous generation of the TriCore™ architecture. The range based protection mechanism provides support for protecting memory ranges from unauthorized read, write, or instruction fetch accesses. The TriCore™ architecture provides up to four protection register sets with the PSW.PRS field controlling the selection of the protection register set. Because the TC1100 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection

Mode Register) which determines the memory access modes which apply to the specified range.

3.3.2 Protection for PTE based translation

Memory protection for addresses that undergo PTE based translation is enforced using the PTE used for the address translation. The PTE provides support for protecting a process from unauthorized read, write, or instruction fetches by other processes. The PTE has the following bits that are provided for the purpose of protection:

- Execute Enable (XE) enables instruction fetch to the page
- Write Enable (WE) enables data writes to the page
- Read Enable (RE) enables data reads from the page

Furthermore, User-0 accesses to virtual addresses in the upper half of the virtual address space are disallowed when operating in virtual mode. In physical mode, User-0 accesses are disallowed only to segments 14 and 15. Any User-0 access to a virtual address that is restricted to User-1 or supervisor mode will cause a Virtual Address Protection (VAP) Trap in both the physical and virtual modes.

3.3.3 Memory Checker

The Memory Checker module (MCHK) makes it possible to check the data consistency of memories. It uses DMA moves to read from the selected address area and to write the value read in a memory checker input register (the moves should be 32-bit moves). A polynomial checksum calculation is done with each write operation to the memory checker input register.

3.4 On-Chip Bus System

The TC1100 includes two bus systems:

- Local Memory Bus (LMB)
- Flexible Peripheral Interface Bus (FPI)

The LMB-to-FPI (LFI) bridge interconnects the FPI bus and LMB Bus.

3.4.1 Local Memory Bus (LMB)

The Local Memory Bus interconnects the memory units and functional units, such as CPU and DMU. The main objective of the LMB bus is to support devices with fast response time. This allows the DMI and PMI fast access to local memory and reduces load on the FPI bus. The TriCore™ system itself is located on the LMB bus. Via External Bus Unit, it interconnects TC1100 and external components.

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. It supports 8, 16, 32 and 64 bits single beat transactions and variable length 64 bits block transfers.

Features:

The LMB provides the following features:

- Synchronous, Pipelined, Multimaster, 64-bit high performance bus
- Optimized for high speed and high performance
- 32-bit address, 64-bit data buses
- Central, simple per cycle arbitration
- Slave controlled wait state insertion
- Address pipelining (max depth - 2)
- Supports Split transactions
- Supports Variable block size transfer
- Supports Locked transaction (read-modify-write)

3.4.2 Flexible Peripheral Interconnect Bus (FPI)

The FPI Bus is an on-chip bus that is used in modular and highly integrated microprocessors and microcontrollers (**systems-on-chips**). FPI Bus is designed for memory mapped data transfers between its bus agents. Bus agents are on-chip function blocks (modules), equipped with an FPI Bus interface and connected via FPI Bus signals. An FPI Bus agent acts as an FPI Bus master when it initiates data read or data write operations once bus ownership has been granted to the agent. An FPI Bus agent that is addressed by an FPI Bus operation acts as an FPI Bus slave when it performs the requested data read or write operation.

Features:

The FPI Bus is designed with the requirements of high-performance systems in mind. The features are:

- Core independent
- Multimaster capability (up to 16 masters)
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 800 Mbytes/sec (@ 100 MHz bus clock)
- Address and data bus scalable (address bus up to 32 bits, data bus up to 64 bits)
- 8-/16-/32- and 64-bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Split transaction support for agents with long response time
- Burst transfer capability
- EMI and power consumption minimized

3.4.3 LFI

The LMB-to-FPI Interface (LFI) block provides the circuitry to interface (bridge) the FPI bus and the Local Memory Bus (LMB).

LFI Features:

- Full support for bus transactions found within current TriCore™ 1.3 based systems:
  - Single 8/16/32-bit Write/Read transfers from FPI to LMB
  - Single 8/16/32/64-bit Write/Read transfers from LMB to FPI
  - Read-Modify-Write transfers of 8/16/32-bit in both directions
  - Burst transactions of 2, 4 or 8 data beats from the FPI to the LMB
  - Burst transactions of 2 or 4 data beats from the LMB to the FPI
- Address decoding and translation as required by TriCore™ 1.3 implementation
- FPI master interface supports full pipelining on FPI bus
- LMB master interface supports pipelining on LMB within the scope of the LMB specification
- FPI master interface can act as default master on FPI bus
- Programmable support for split LMB to FPI read transactions
- Retry generation on both FPI and LMB buses
- Full support for abort, retry, error and FPI timeout conditions
- Flexible LMB/FPI clock ratio support including dynamic clock switching support
- LFI core clock may be shut down when no transactions are being issued to LFI from either bus and the LFI has no transactions in progress, thus saving power.

3.5 LMB External Bus Unit

The LMB External Bus Control Unit (EBU) of the TC1100 is the interface between external resources, like memories and peripheral units, and the internal resources connected to on-chip buses if enabled. The basic structure and external interconnections of the EBU are shown in **Figure 3-1**.

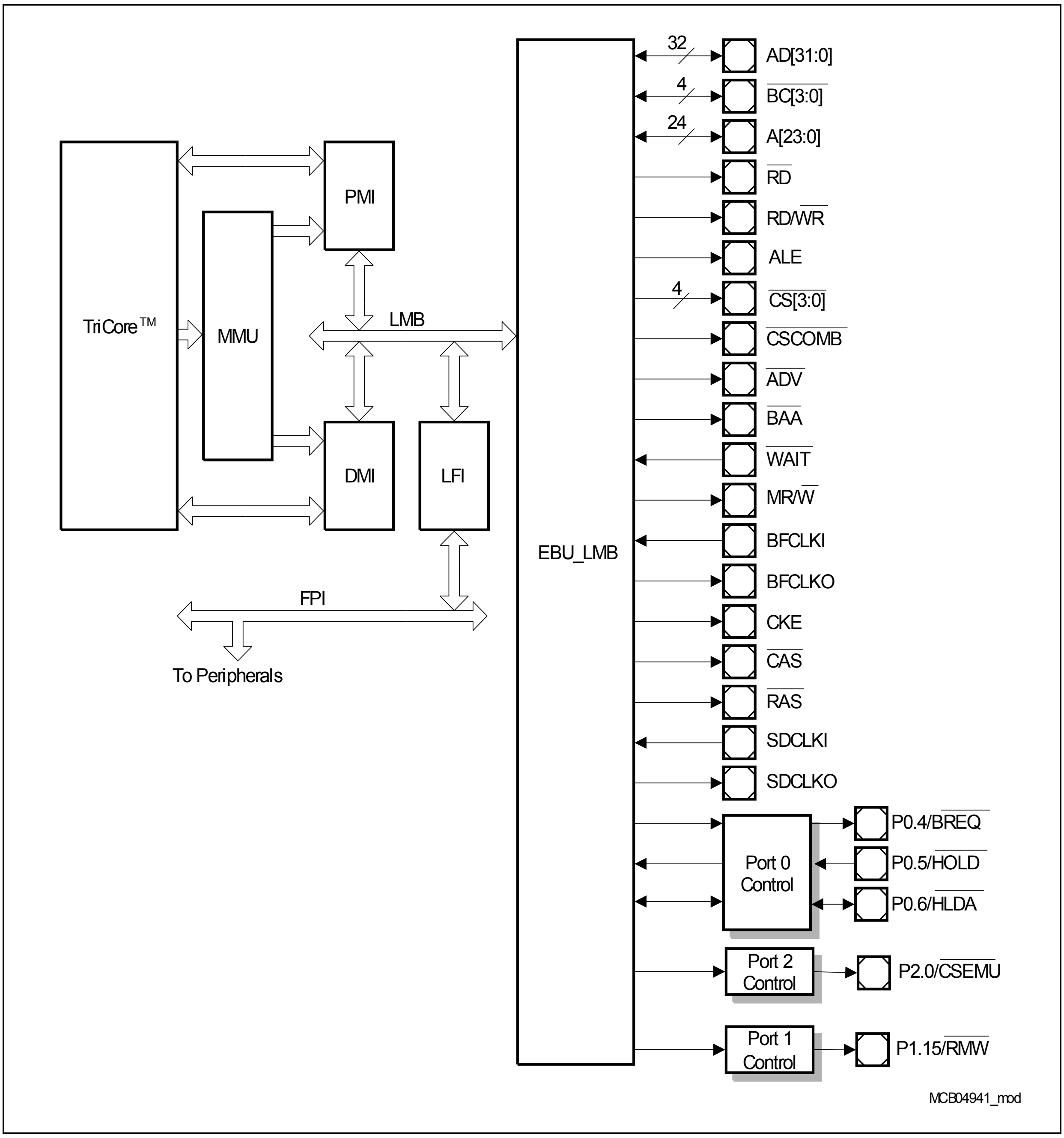


Figure 3-1 EBU Structure and Interface

The EBU is used primarily for any Local Memory Bus (LMB) master accessing external memories. The EBU controls all transactions required for this operation and in particular handles the arbitration between the internal EBU master and the external EBU master.

The types of external devices/bus modes controlled by the EBU are:

- Intel-style peripherals (separate $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals)
- ROMs, EPROMs
- Static RAMs
- PC100 and PC133 SDRAMs (Burst Read/Write Capacity/Multi-Bank/Page support)
- Specific types of Burst Mode Flash devices
- Special support for external emulator/debug hardware

Features:

- Supports 64-bit Local Memory Bus (LMB)
- Supports external bus frequency: internal LMB frequency = 1:1 or 1:2
- Provides highly programmable access parameters
- Supports Intel-style peripherals/devices
- Supports PC100 and PC133 (runs in maximum 120 MHz) SDRAM (burst access, multibanking, precharge, refresh)
- Supports 16- and 32-bit SDRAM data bus and 64-,128-, and 256-Mbit devices
- Supports Burst Flash devices
- Supports Multiplexed access (address and data on the same bus) when PC100 and PC133 SDRAM are not presented on the external bus
- Supports data buffering: Code Prefetch Buffer, Read/Write Buffer
- External master arbitration compatible to C166 and other TriCore™ devices
- Provides 4 programmable address regions (1 dedicated for emulator)
- Provides a $\overline{\text{CSGLB}}$ signal, bit programmable to combine one or more $\overline{\text{CS}}$ lines for buffer control
- Provides $\overline{\text{RMW}}$ signal reflecting read-modify-write action
- Supports Little Endian byte ordering
- Provides signal for controlling data flow of slow-memory buffer

3.6 Direct Memory Access (DMA)

The Direct Memory Access Controller executes DMA transactions from a source address location to a destination address location, without intervention of the CPU. One DMA transaction is controlled by one DMA channel. Each DMA channel has assigned its own channel register set. The total of 8 channels are provided by one DMA sub-block.

The DMA module is connected to 3 bus interfaces in TC1100, the Flexible Peripheral Interconnect Bus (FPI), the DMA Bus and the Micro Link Bus. It can do transfers on each of the buses as well as between the buses.

In addition, it bridges accesses from the Flexible Peripheral Interconnect Bus to the peripherals on the DMA Bus, allowing easy access to these peripherals by CPU. Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation specific and managed outside the DMA controller kernel.

Features:

- 8 independent DMA channels
  - Up to 8 selectable request inputs per DMA channel
  - Programmable priority of DMA channels within a DMA sub-block (2 levels)
  - Software and hardware DMA request generation
  - Hardware requests by selected peripherals and external inputs
- Programmable priority of the DMA sub-block on the bus interfaces
- Buffer capability for move actions on the buses (min. 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4-Gbyte address range
  - Support of circular buffer addressing mode
- Programmable data width of a DMA transaction: 8-bit, 16-bit, or 32-bit
- Micro Link supported
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- All buses/interfaces connected to the DMA module must work at the same frequency.
- Read/write requests of the FPI Bus Side to the Remote Peripherals are bridged to the DMA Bus (only the DMA is master on the DMA bus)

The basic structure and external interconnections of the DMA are shown in **Figure 3-2**.

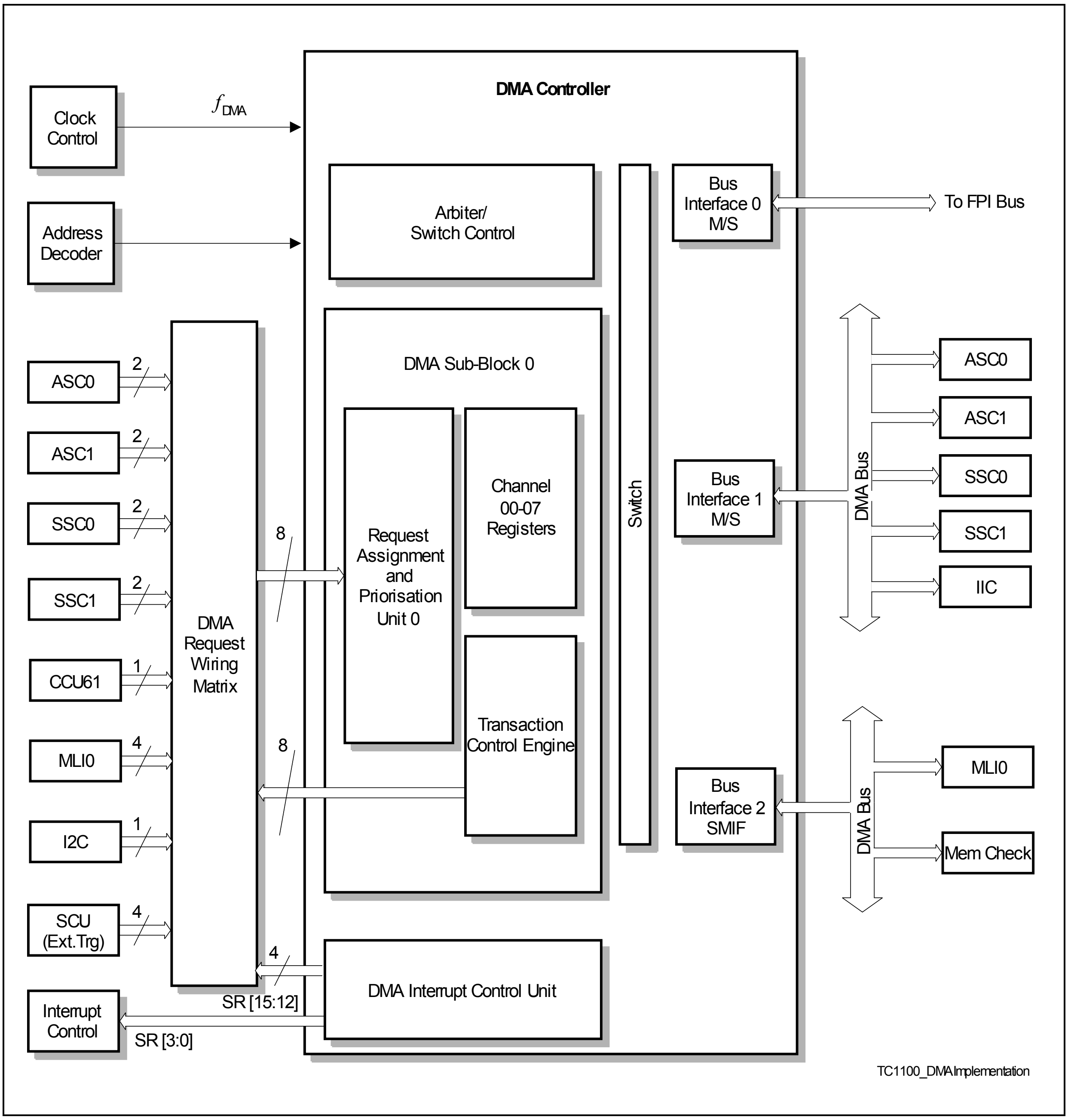


Figure 3-2 DMA Controller Structure and Interconnections

3.7 Interrupt System

An interrupt request can be serviced by the CPU, which is called “Service Provider”. Interrupt requests are referred to as “Service Requests” in this document.

Each peripheral in the TC1100 can generate service requests. Additionally, the Bus Control Unit, the Debug Unit, the DMA Controller and even the CPU itself can generate service requests to the Service Provider. As shown in **Figure 3-3**, each unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRC, where “mod” is the identifier of the unit requesting service. The SRNs are connected to the Interrupt Control Unit (ICU) via the CPU Interrupt Arbitration Bus. The ICU arbitrates service requests for the CPU and administers the Interrupt Arbitration Bus.

Units that can generate service requests are:

- Asynchronous/Synchronous Serial Interfaces (ASC0 and ASC1) with 4 SRNs each
- High-Speed Synchronous Serial Interfaces (SSC0 and SSC1) with 3 SRNs each
- Inter IC Interface (IIC) with 3 SRNs
- Micro Link Interface MLI0 with 4 SRNs
- General Purpose Timer Unit (GPTU) with 8 SRNs
- Capture/Compare Unit (CCU61) with 4 SRNs
- External Interrupts with 4 SRNs
- Direct Memory Access Controller (DMA) with 4 SRNs
- DMA Bus with 1 SRN
- System Timer (STM) with 2 SRNs
- Bus Control Units (SBCU and LBCU) with 1 SRN each
- Central Processing Unit (CPU) with 4 SRNs
- Floating Point Unit (FPU) with 1 SRN
- Debug Unit (OCDS) with 1 SRN

The CPU can make service requests directly to itself (via the ICU). The CPU Service Request Nodes are activated through software.

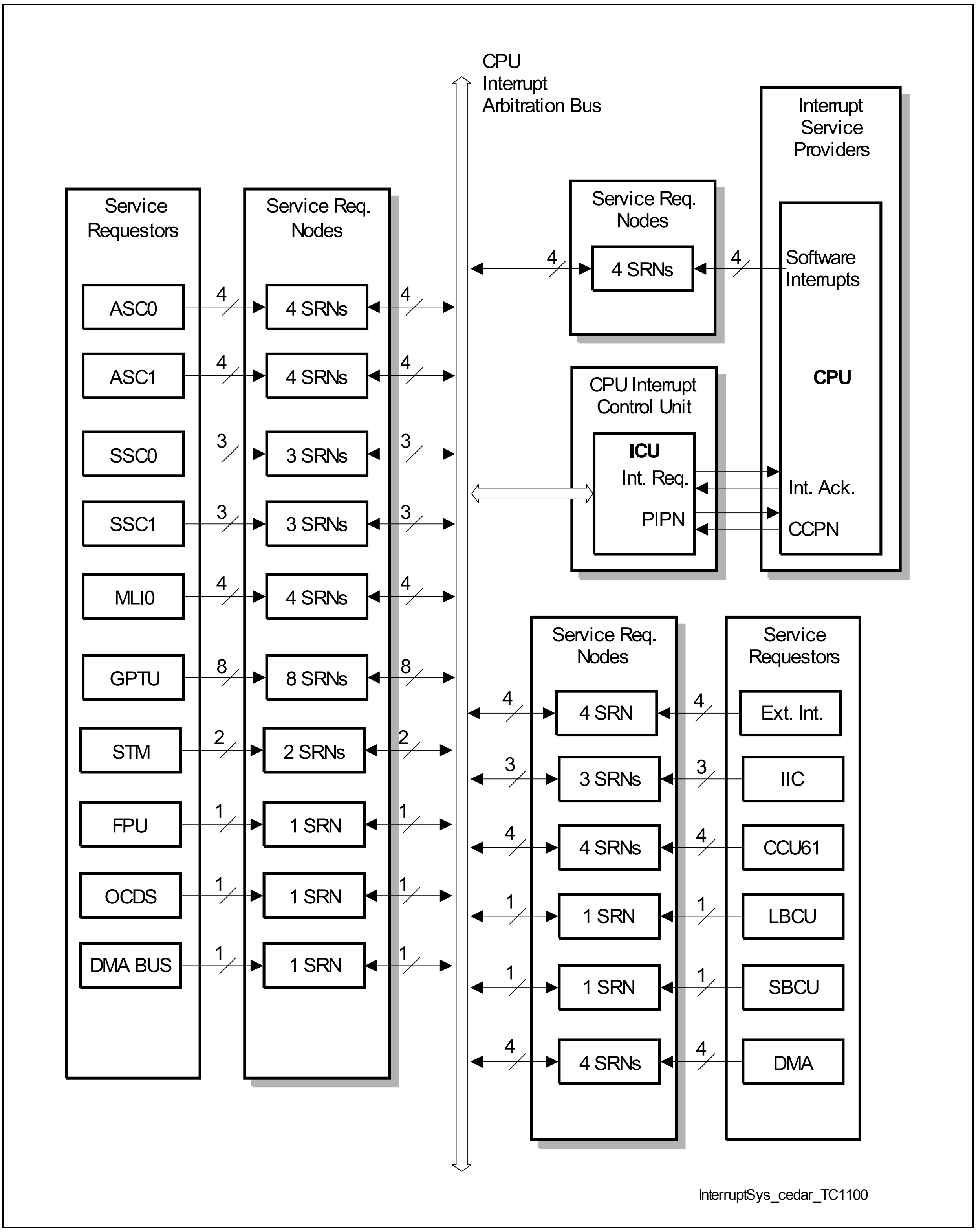


Figure 3-3 Block Diagram of the TC1100 Interrupt System

3.8 Parallel Ports

The TC1100 has 72 digital input/output port lines, which are organized into four parallel 16-bit ports and one parallel 8-bit port, Port P0 to Port P4 with 3.3 V nominal voltage.

The digital parallel ports can be used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units. An overview on the port-to-peripheral unit assignment is shown in **Figure 3-4**.

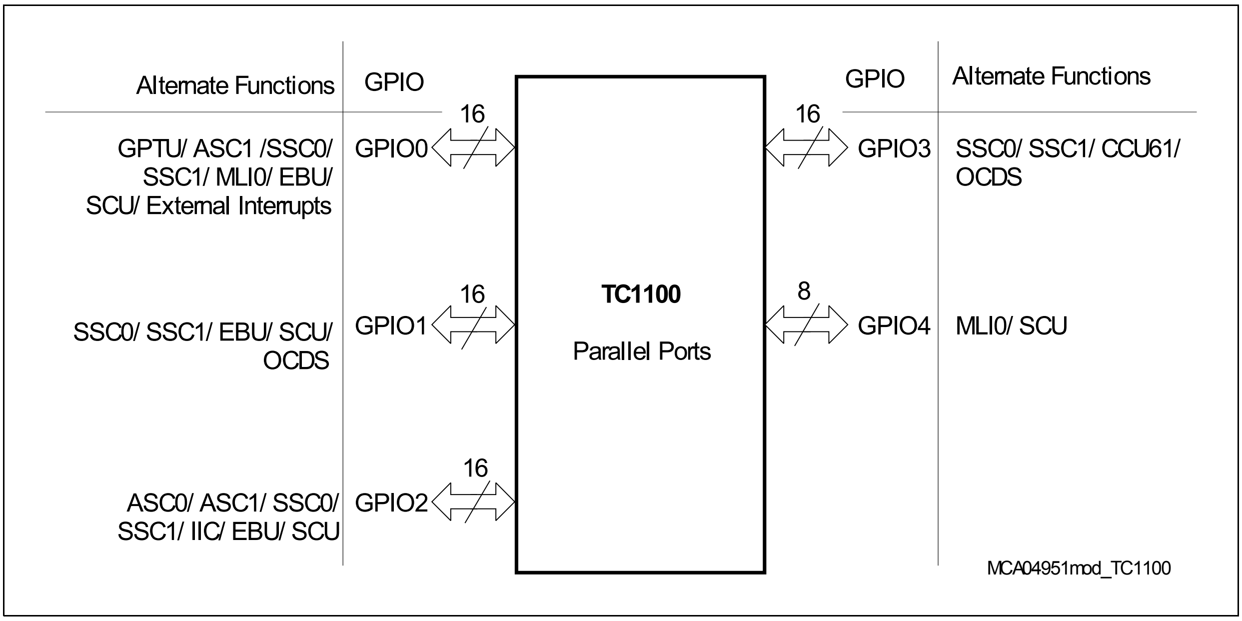


Figure 3-4 Parallel Ports of the TC1100

3.9 Asynchronous/Synchronous Serial Interface (ASC)

Figure 3-5 shows a global view of the functional blocks of two Asynchronous/ Synchronous Serial interfaces (ASC0 and ASC1).

Each ASC module (ASC0/ASC1) communicates with the external world via one pair of I/O lines. The RXD line is the receive data input signal (in synchronous mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

The Asynchronous/Synchronous Serial interfaces provide serial communication between the TC1100 and other microcontrollers, microprocessors or external peripherals.

Each ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In synchronous mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In asynchronous mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud-rate generator provides the ASC with a separate serial clock signal that can be accurately adjusted by a prescaler implemented as a fractional divider.

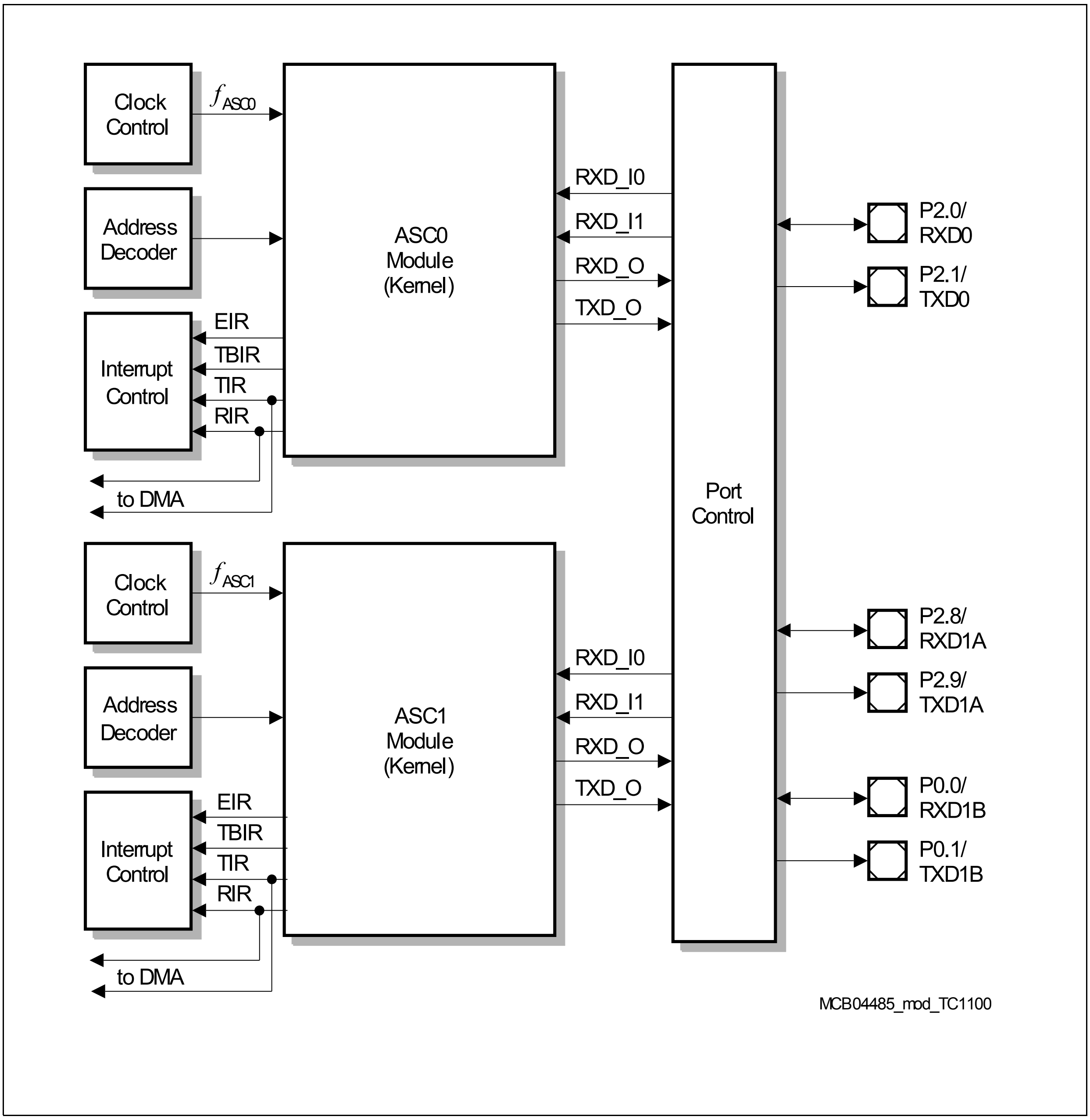


Figure 3-5 General Block Diagram of the ASC Interfaces

Features:

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 4.6875 MBaud to 1.1 Baud (@ 75 MHz clock)
- Multiprocessor mode for automatic address/data byte detection

- Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 9.375 MBaud to 762.9 Baud (@ 75 MHz clock)
- Support for IrDA data transmission up to 115.2 kBaud maximum
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error)
- FIFO
  - 8-byte receive FIFO (RXFIFO)
  - 8-byte transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 9-bit FIFO data width
  - Programmable Receive/Transmit Interrupt Trigger Level
  - Receive and Transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

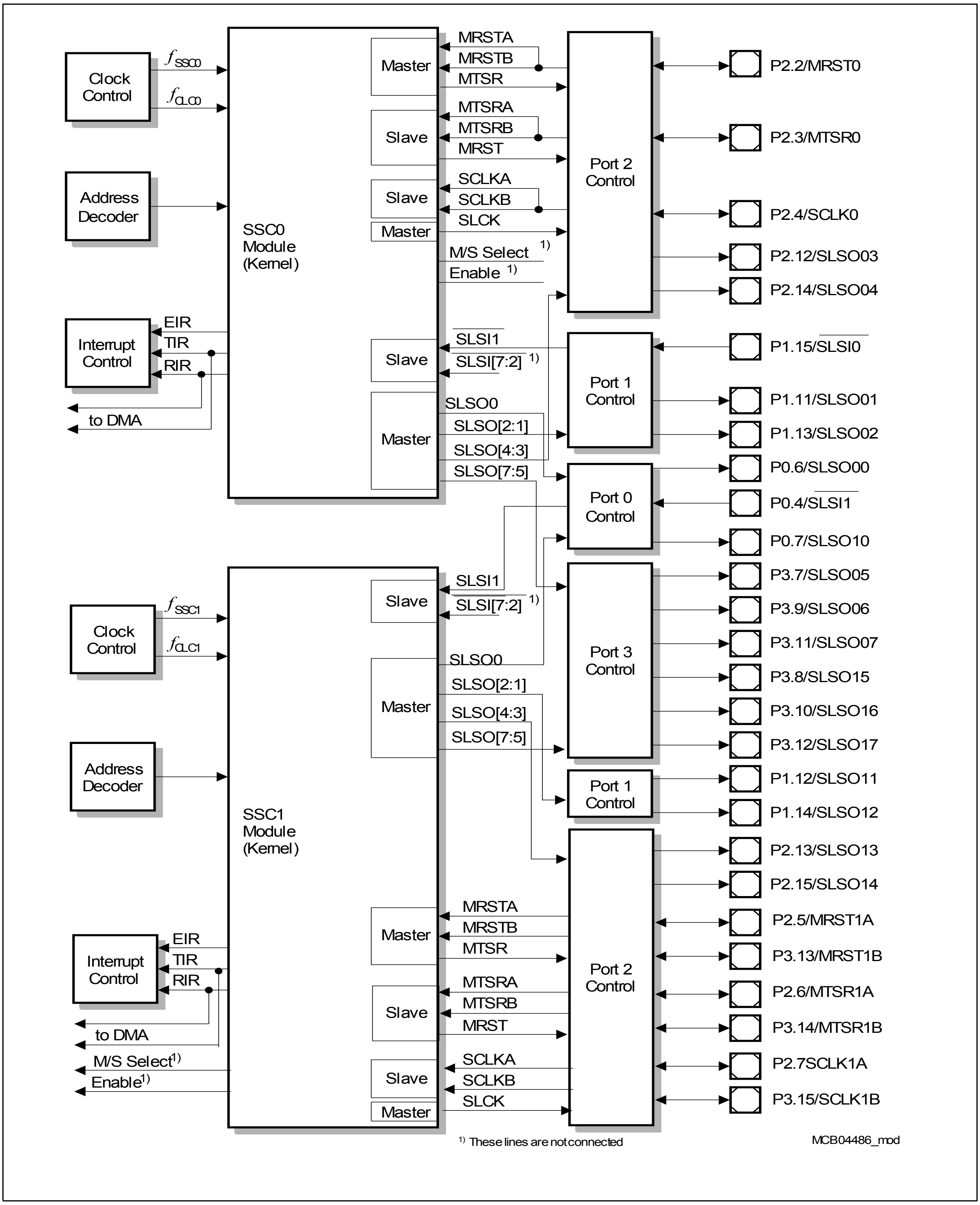
3.10 High-Speed Synchronous Serial Interface (SSC)

Figure 3-6 shows a global view of the functional blocks of two High-Speed Synchronous Serial interfaces (SSC0 and SSC1).

Each SSC supports full-duplex and half-duplex serial synchronous communication up to 37.5 MBaud (@ 75 MHz module clock) with receive and transmit FIFO support. The serial clock signal can be generated by the SSC itself (master mode) or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. Eight slave select inputs are available for slave mode operation. Eight programmable slave select outputs (chip selects) are supported in master mode.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation minimum at 572.2 Baud (@ 75 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Four-pin interface
- Flexible SSC pin configuration
- Up to eight slave select inputs in slave mode
- Up to eight programmable slave select outputs SLSO in master mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
- 4-stage receive FIFO (RXFIFO) and 4-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2- to 16-bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation



1) These lines are not connected

MCB04486_mod

Figure 3-6 General Block Diagram of the SSC Interfaces

3.11 Inter IC Serial Interface (IIC)

Figure 3-7 shows a global view of the functional blocks of the Inter IC Serial Interface (IIC).

The IIC module has four I/O lines, located at Port 2. The IIC module is further supplied with clock control, interrupt control and address decoding logic. One DMA request can be generated by IIC module.

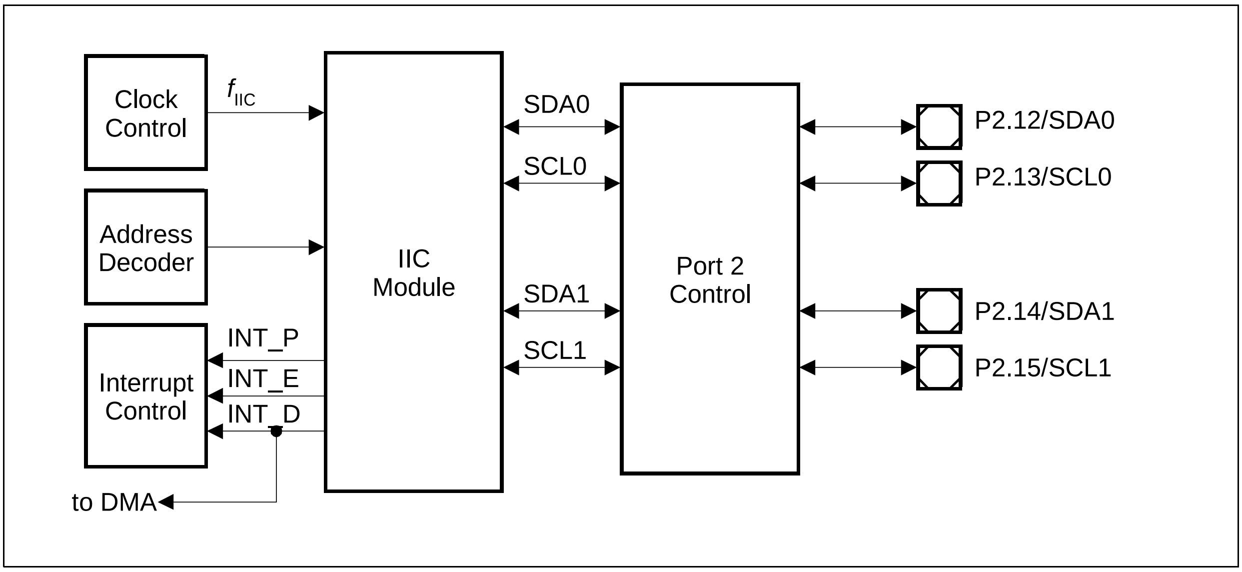


Figure 3-7 General Block Diagram of the IIC Interface

The on-chip IIC bus module connects the platform buses to other external controllers and/or peripherals via the two-line serial IIC interface. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA). The IIC bus module provides communication at data rates of up to 400 kbit/sec and features 7-bit addressing as well as 10-bit addressing. This module is fully compatible to the IIC bus protocol.

The module can operate in three different modes:

Master mode, where the IIC controls the bus transactions and provides the clock signal.

Slave mode, where an external master controls the bus transactions and provides the clock signal.

Multimaster mode, where several masters can be connected to the bus, i.e. the IIC can be master or slave.

The on-chip IIC bus module allows efficient communication via the common IIC bus. The module unloads the CPU of low level tasks such as:

- (De)Serialization of bus data
- Generation of start and stop conditions
- Monitoring the bus lines in slave mode

- Evaluation of the device address in slave mode
- Bus access arbitration in multimaster mode

Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored
- Selectable baud rate generation
- Support of standard 100 kBaud and extended 400 kBaud data rates
- Operation in 7-bit addressing mode or 10-bit addressing mode
- Flexible control via interrupt service routines or by polling
- Dynamic access to up to 2 physical IIC buses

3.12 Micro Link Serial Bus Interface (MLI)

Figure 3-8 shows a global view of the functional blocks of the Micro Link Serial Bus Interface (MLI0).

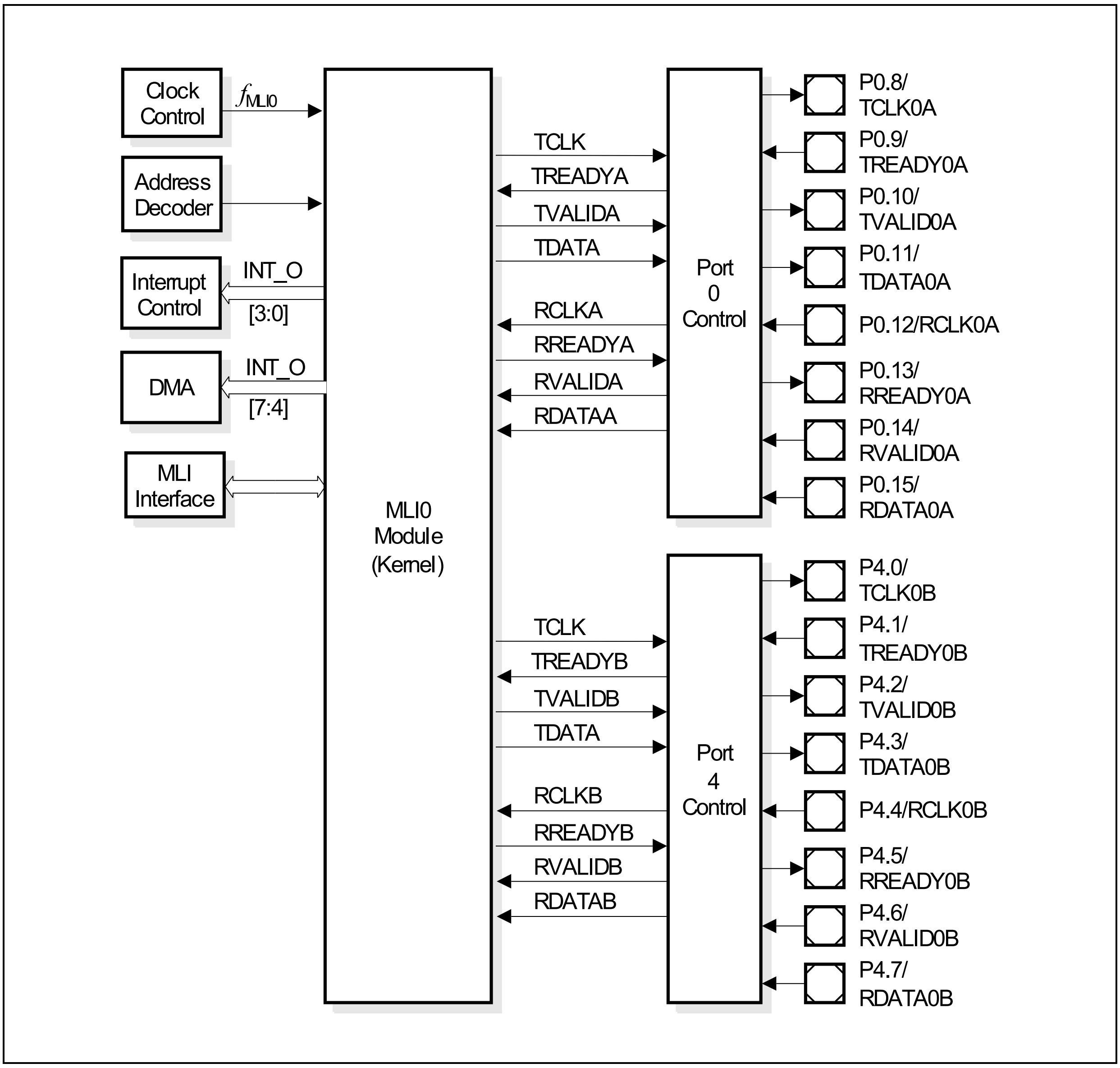


Figure 3-8 General Block Diagram of the MLI0 Interface

The Micro Link Serial Bus Interface is dedicated to the serial communication between the other Infineon 32-bit controllers with MLI. The communication is intended to be fast due to an address translation system, and it is not necessary to have any special program in the second controller.

Features:

- Serial communication from the MLI transmitter to MLI receiver of another controller
- Module supports connection of each MLI with up to four MLI from other controllers
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target controller available
- Special protocol to transfer data, address offset, or address offset and data
- Error control using a parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Address offset width: from 1- to 16-bit
- Baud rate: f_{MLI} / 2 (symmetric shift clock approach),
  baud rate definition by the corresponding fractional divider

3.13 General Purpose Timer Unit (GPTU)

Figure 3-9 shows a global view of the functional blocks of the General Purpose Timer Unit (GPTU).

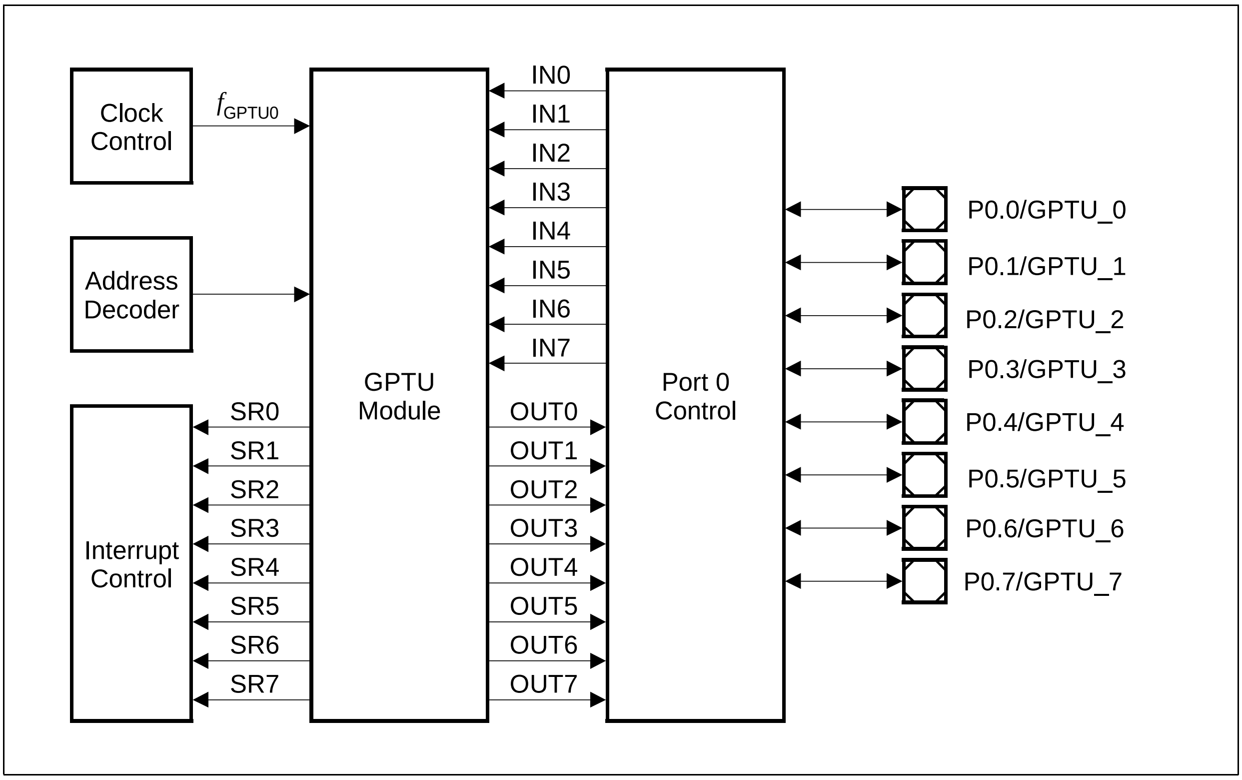


Figure 3-9 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight I/O lines located at Port 0.

The three timers of GPTU module, T0, T1 and T2, can operate independently of each other or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of f_{GPTU}
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers

- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can define a count option

Features of T2:

- Count up or down is selectable
- Operating modes:
  - Timer
  - Counter
  - Quadrature counter (incremental/phase encoded counter interface)
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes

3.14 Capture/Compare Unit 6 (CCU6)

Figure 3-10 shows a global view of the functional blocks of the Capture/Compare Unit (CCU61).

The CCU6 module is further supplied with clock control, interrupt control, address decoding, and port control logic. One DMA request can be generated by the CCU6 module.

The CCU6 provides two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features:

- Three capture/compare channels, each channel can be used either as capture or as compare channel.
- Generation of a three-phase PWM supported (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Features:

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported

Additional Features:

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

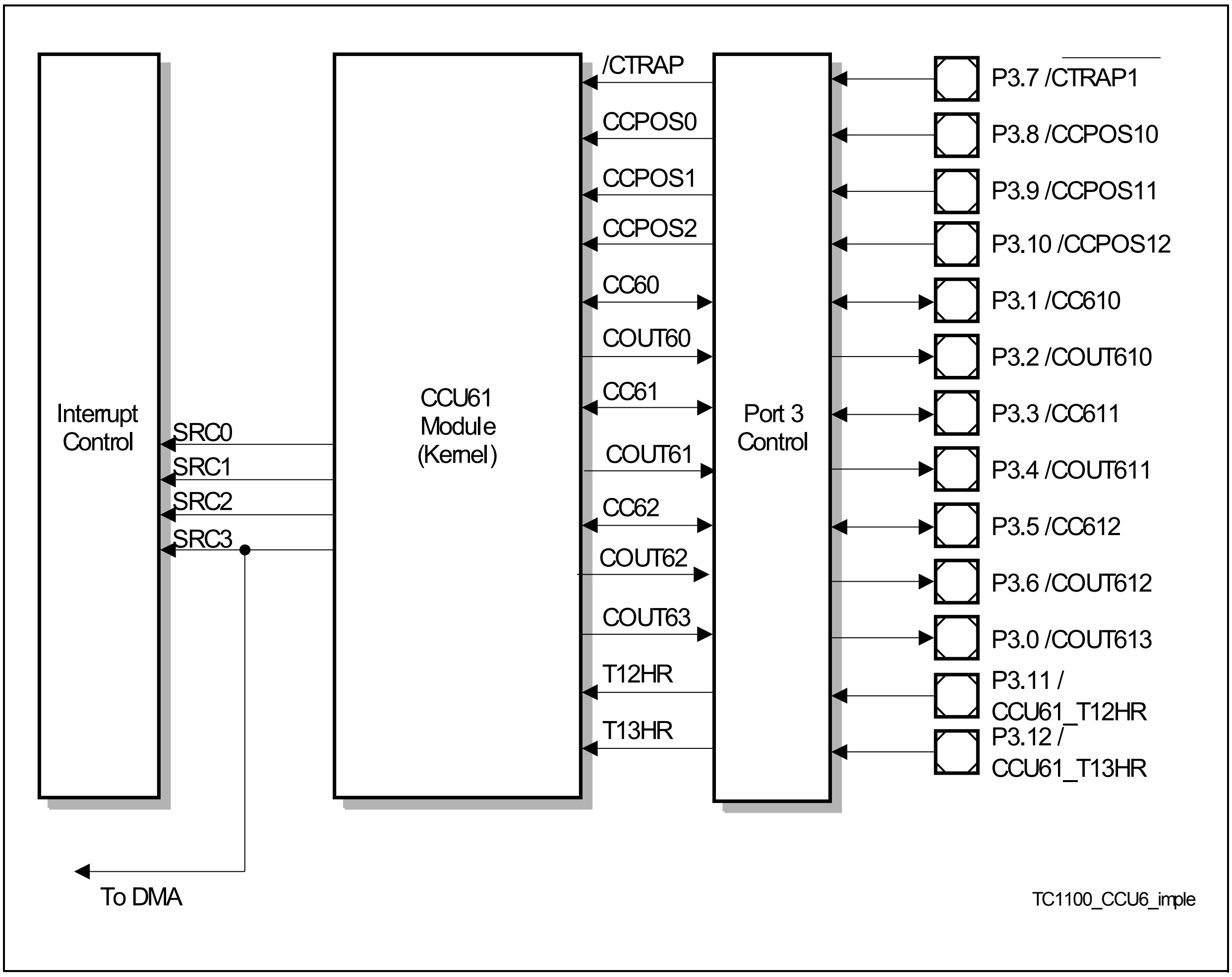


Figure 3-10 General Block Diagram of the CCU6 Interface

3.15 System Timer

The STM within the TC1100 is designed for global system timing applications requiring both high precision and long range. The STM provides the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation on partial STM content compare match
- Driven by clock f_{STM} after reset (default after reset is $f_{STM} = f_{SYS} = 150$ MHz)
- Counting starts automatically after a reset operation
- STM is reset under following reset causes:
  - Wake-up reset (PMG_CON.DSRW must be set)
  - Software reset (RST_REQ.RRSTM must be set)
  - Power-on reset
- STM (and the clock divider) is not reset at watchdog reset and hardware reset ($\overline{\text{HDRST}} = 0$)

The STM is an upward counter, running with the system clock frequency f_{SYS} (after reset $f_{STM} = f_{SYS}$). It is enabled per default after reset, and immediately starts counting up. Other than via reset, it is not possible to affect the contents of the timer during normal operation of the application; it can only be read, but not written to. Depending on the implementation of the clock control of the STM, the timer can optionally be disabled or suspended for power-saving and debugging purposes via a clock control register.

The maximum clock period is $2^{56}/f_{STM}$. At $f_{STM} = 150$ MHz (maximum), for example, the STM counts 15.2 years before overflowing. Thus, it is capable of continuously timing the entire expected product lifetime of a system without overflowing.

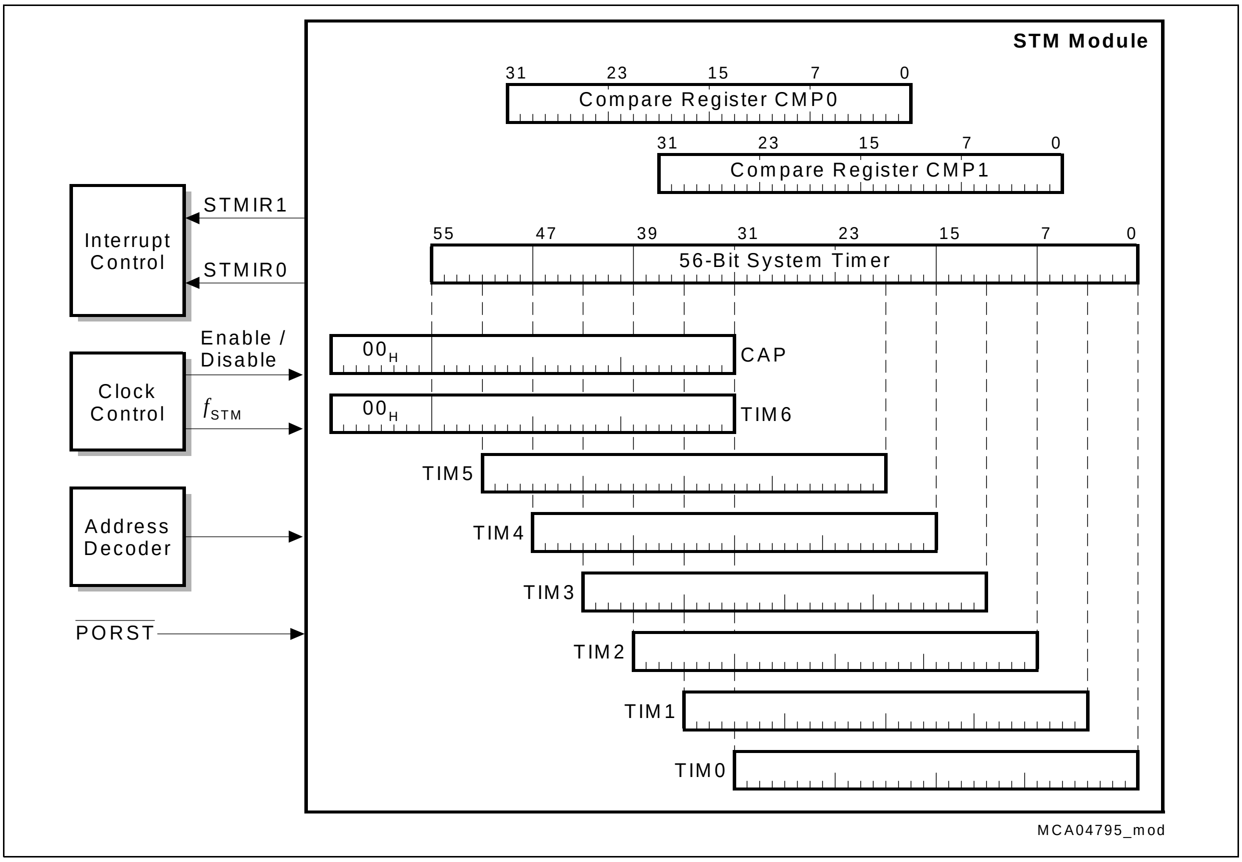


Figure 3-11 Block Diagram of the STM Module

3.16 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1100 in a user-specified time period. When enabled, the WDT will cause the TC1100 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1100 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard "Watchdog" function, the WDT incorporates the ENDINIT feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides supervisor mode protection). Registers protected via this line can be modified only when supervisor mode is active and bit ENDINIT = 0.

A further enhancement in the TC1100's Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device upon detection of an error, the WDT first issues a Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, thus providing an important aid in debugging.

Features:

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for time-out and prewarning modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection: If a Watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC1100 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

3.17 System Control Unit

The System Control Unit (SCU) of the TC1100 handles the system control tasks. All of these system functions are tightly coupled; thus, they are conveniently handled by one unit, the SCU. The system tasks of the SCU are:

- Clock Control
  - Clock generation
  - Oscillator and PLL control
- Reset and Boot Control
  - Generation of all internal reset signals
  - Generation of external hardware and software reset signal
- Power Management Control
  - Enabling of several power management modes
- Configuration input sampling
- FPU interrupts
- External Request Unit
- Parity Error Control
- Fault SRAM Fuse Box
- CSCOMB Control
- EBU Pull-Up Control
- NMI Control and Status
- DMA Request Signal Selection

3.18 Boot Options

The TC1100 booting schemes provides a number of different boot options for the start of code execution. **Table 3-3** shows the boot options available in the TC1100.

Table 3-3 Boot Selections

$\overline{\text{BRKIN}}$[1]	$\overline{\text{TM}}$[1]	HWCFG [2:0]	Type of Boot	PC Start Value (User Entry)
1	1	000	**Bootstrap Loader** Serial boot from ASC to PMI scratch pad, run loaded program	DFFF FFFC$_H$[2] (D400 0000$_H$)
		001	Reserved	----
		010	**Bootstrap Loader** Serial boot from SSC to PMI scratch pad, run loaded program	DFFF FFFC$_H$[2] (D400 0000$_H$)
		011	External memory, EBU as master	DFFF FFFC$_H$[2] (A000 0000$_H$)
		100	External memory, EBU as slave	DFFF FFFC$_H$[2] (A000 0000$_H$)
		101	Reserved (STOP)	----
		110	PMI scratch pad	D400 0000$_H$
		111	Reserved (STOP)	DFFF FFFC$_H$[2]
1	0	000-111	Reserved (STOP)	DFFF FFFC$_H$[2]
0	1	000	Tristate chip	----
		001	Go to external emulator space	DFFF FFFC$_H$[2] (DE00 0000$_H$)
		010	Reserved (STOP)	----
		011	OSC and PLL Bypass	----
		100-111	Reserved (STOP)	DFFFFFFC$_H$[2]
0	0	000-111	Reserved (STOP)	DFFFFFFC$_H$[2]

[1] This input signal is active low.

[2] This is the BootROM entry address; the start address of user program in parentheses.

3.19 Power Management System

The TC1100 power management system allows software to configure the various processing units to adjust automatically in order to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 3-4 describes the features of the power management modes.

Table 3-4 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to run mode. Idle mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the $\overline{\text{NMI}}$ pin, or any enabled interrupt event will return the system to run mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in sleep mode. The other peripheral modules will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the $\overline{\text{NMI}}$ pin, or a reset event will return the system to run mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

Besides these explicit software-controlled power-saving modes, special attention has been paid in the TC1100 to automatic power-saving in operating units that are currently not required or idle. In this case, they are shut off automatically until their operation is required again.

3.20 On-Chip Debug Support

The On-Chip Debug Support of the TC1100 consists of the following building blocks:

- OCDS L1 module of TriCore™
- OCDS L2 interface of TriCore™
- OCDS L1 module in the BCU of the FPI Bus
- OCDS L1 facilities within the DMA
- OCDS L2 interface of DMA
- OCDS System Control Unit (OSCU)
- Multi Core Break Switch (MCBS)
- JTAG based Debug Interface (Cerberus JDI)
- Suspend functionality of peripherals

Features:

- TriCore™ L1 OCDS:
  - Hardware event generation unit
  - Break by DEBUG instruction or break signal
  - Full Single-Step support in hardware, possible also with software break
  - Access to memory, SFRs, etc. on the fly
- DMA L1 OCDS:
  - Output break request on errors
  - Suspension of pre-selected channels
- Level 2 trace port with 16 pins that outputs either TriCore™, or DMA trace
- OCDS System Control Unit (Cerberus OSCU)
  - Minimum number of pins required (no OCDS enable pin)
  - Hardware allows hot attach of a debugger to a running system
  - System is secure (can be locked from internal)
- Multi Core Break Switch (Cerberus MCBS):
  - TriCore™, DMA, break pins, and BCUs as break sources
  - TriCore™ as break targets; other parts can in addition be suspended
  - Synchronous stop and restart of the system
  - Break to Suspend converter

Figure 3-12 shows a basic block diagram of the building blocks.

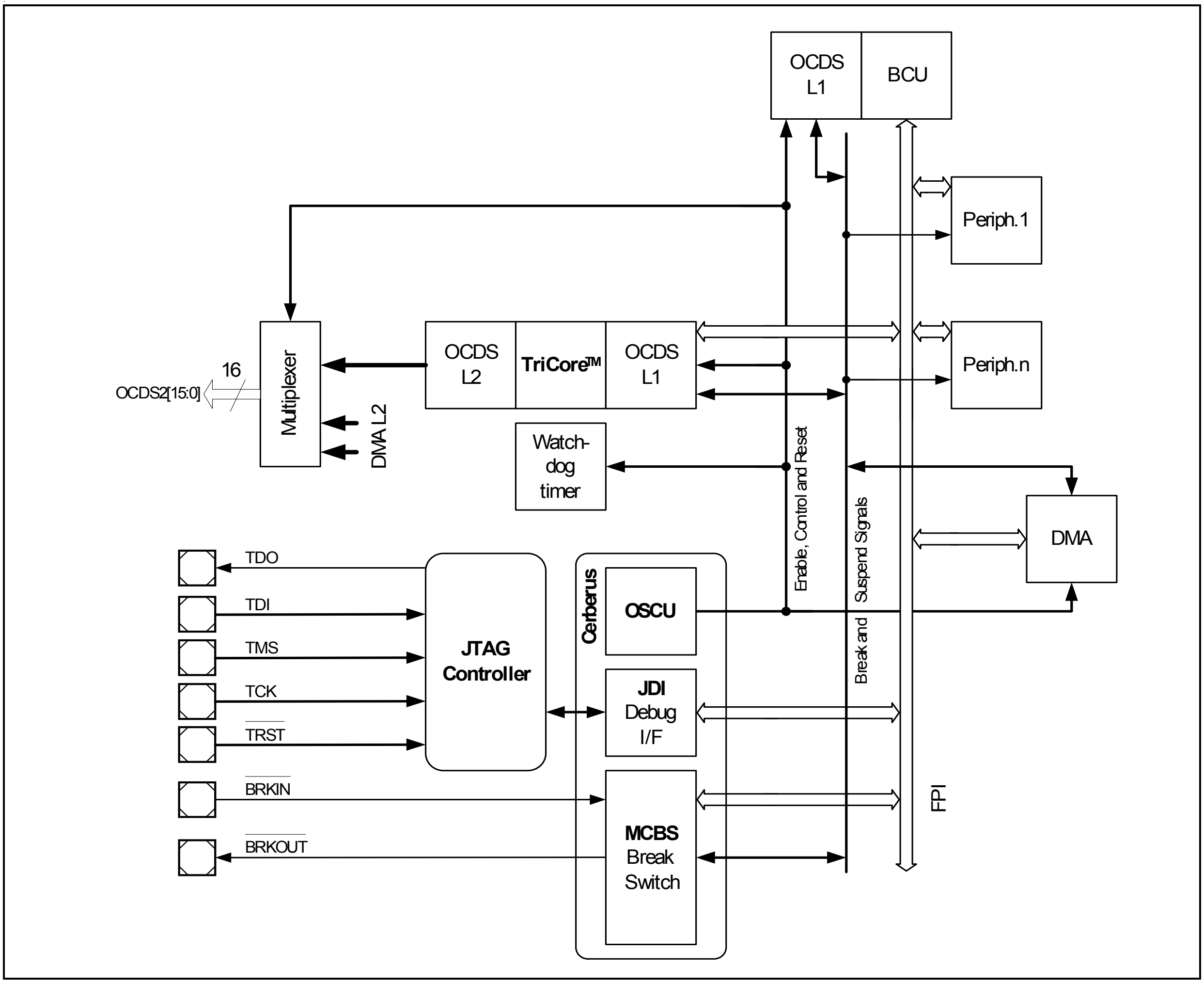


Figure 3-12 OCDS Support Basic Block Diagram

3.21 Clock Generation Unit

The Clock Generation Unit (CGU) allows a flexible clock generation for TC1100. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore, the power consumption can be adapted to the actual application state.

Features:

The Clock Generation Unit serves several purposes:

- PLL feature for multiplying clock source by different factors
- Direct Drive for direct clock input
- Comfortable state machine for secure switching between basic PLL, direct, or prescaler operation
- Sleep and power-down mode support

The Clock Generation Unit in the TC1100, shown in **Figure 3-13**, consists of an oscillator circuit and one Phase-Locked Loop (PLL). The PLL can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it looses the lock on the external clock.

In general, the Clock Generation Unit (CGU) is controlled through the System Control Unit (SCU) module of the TC1100.

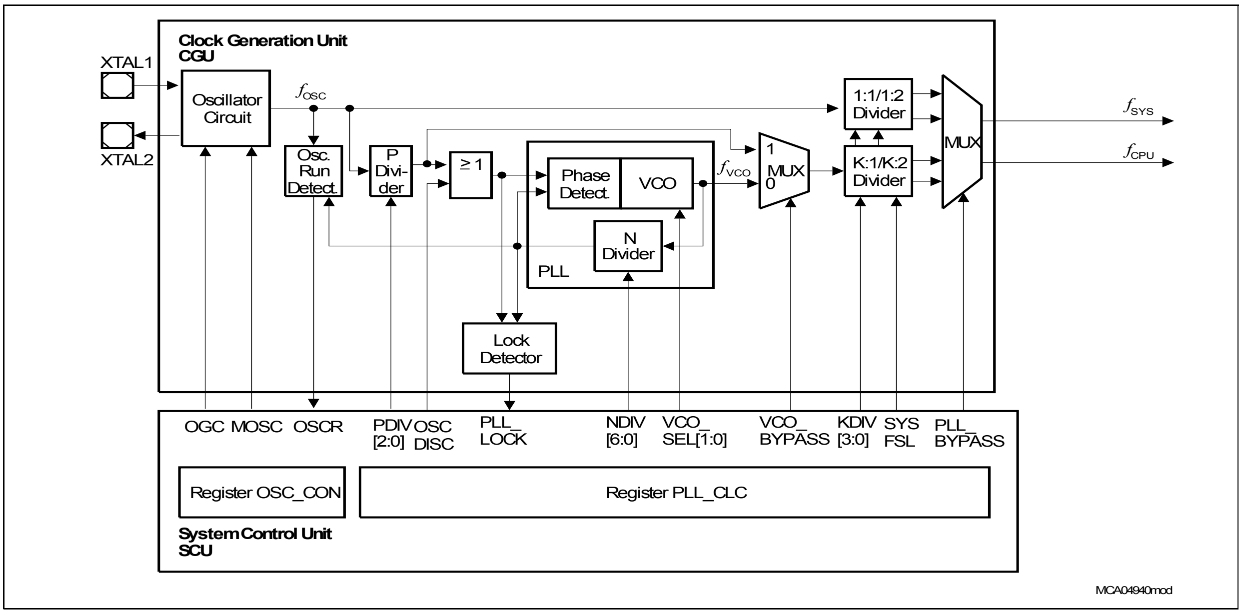


Figure 3-13 Clock Generation Unit Block Diagram

The oscillator circuit, which is designed to work with an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as input and XTAL2 as output.

Figure 3-14 shows the recommended external oscillator circuitries for both operating modes, i.e. external crystal mode and external input clock mode.

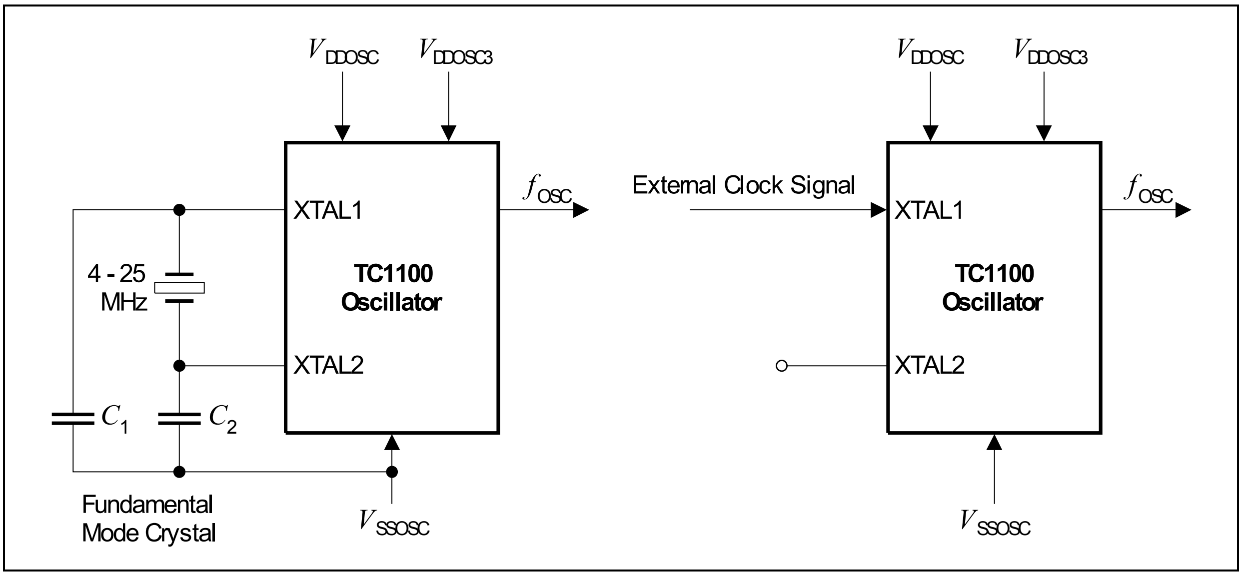


Figure 3-14 Oscillator Circuitries

When using an external clock signal, it must be connected to XTAL1 and XTAL2 is left open (unconnected). When supplying the clock signal directly, not using a crystal and the oscillator, the input frequency can be in the range of 0 - 40 MHz if the PLL is not used, 4 - 40 MHz in case the PLL is used.

When using a crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances, C1 and C2. For some crystals, a series damp resistor may be necessary. The exact values and related operating range are dependant on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method. As starting point for the evaluation and for non-productive systems, the following load capacitor values might be used.

Table 3-5 Load Capacitors Select

Fundamental Mode Crystal Frequency (approx., MHz)	Load Capacitors C1, C2 (pF)
4	33
8	18
12	12
16	10

Table 3-5 Load Capacitors Select (cont'd)

Fundamental Mode Crystal Frequency (approx., MHz)	**Load Capacitors C1, C2 (pF)**
20	10
24	10

A block capacitor between V_{DDOSC3} and V_{SSOSC}, V_{DDOSC} and V_{SSOSC} is recommended, too.

3.22 Power Supply

The TC1100 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 3-15 shows the TC1100’s power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

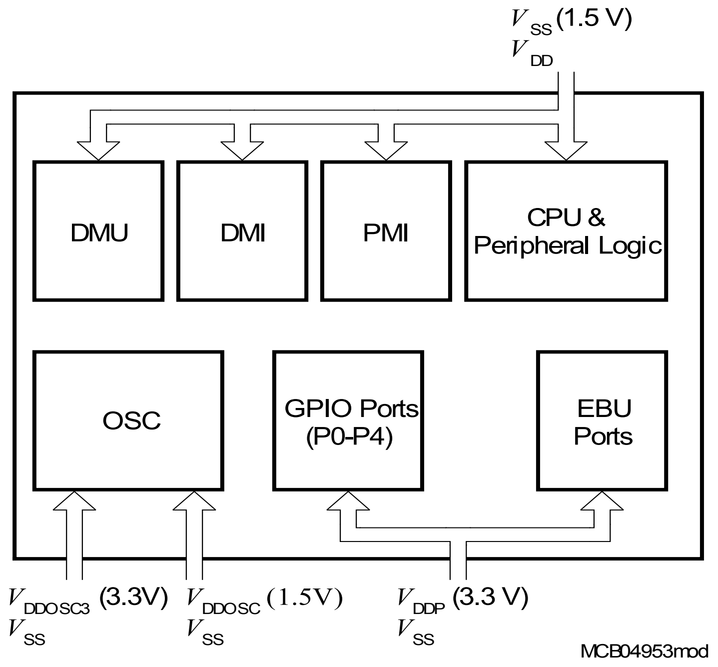


Figure 3-15 TC1100 Power Supply Concept

3.23 Power Sequencing

During power-up, reset pin $\overline{\text{PORST}}$ has to be held active until both power supply voltages have reached at least their minimum values.

During the power-up time (rising of the supply voltages from 0 to their regular operating values), it must be ensured, that the core V_{DD} power supply reaches its operating value first, and then followed by the GPIO V_{DDP} power supply. During the rising time of the core voltage, it must be ensured that $0< V_{DD}-V_{DDP} <0.5$ V.

During power-down, the core power supply V_{DD} and GPIO power supply V_{DDP} must be switched off completely until all capacitances are discharged to zero before the next power-up.

Note: The state of the pins are undefined when only the port voltage V_{DDP} is switched on.

3.24 Identification Register Values

Table 3-6 TC1100 Identification Registers

Short Name	Address	Value
SCU_ID	F000 0008$_H$	002C C001$_H$
MANID	F000 0070$_H$	0000 1820$_H$
CHIPID	F000 0074$_H$	0000 8C01$_H$
RTID	F000 0078$_H$	0000 0000$_H$
SBCU_ID	F000 0108$_H$	0000 6A0A$_H$
STM_ID	F000 0208$_H$	0000 C005$_H$
CBS_JDPID	F000 0308$_H$	0000 6307$_H$
GPTU_ID	F000 0608$_H$	0001 C002$_H$
CCU61_ID	F000 2108$_H$	0042 C004$_H$
DMA_ID	F000 3C08$_H$	001A C011$_H$
SSC0_ID	F010 0108$_H$	0000 4530$_H$
SSC1_ID	F010 0208$_H$	0000 4530$_H$
ASC0_ID	F010 0308$_H$	0000 44E2$_H$
ASC1_ID	F010 0408$_H$	0000 44E2$_H$
IIC_ID	F010 0608$_H$	0000 4604$_H$
MLI0_ID	F010 C008$_H$	0025 C004$_H$
MCHK_ID	F010 C208$_H$	001B C001$_H$
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$
MMU_ID	F7E1 8008$_H$	0009 C002$_H$
CPU_ID	F7E1 FE18$_H$	000A C005$_H$
EBU_ID	F800 0008$_H$	0014 C004$_H$
DMU_ID	F800 0408$_H$	002D C001$_H$
DMI_ID	F87F FC08$_H$	0008 C004$_H$
PMI_ID	F87F FD08$_H$	000B C004$_H$
LBCU_ID	F87F FE08$_H$	000F C005$_H$
LFI_ID	F87F FF08$_H$	000C C005$_H$

4 Electrical Parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the TC1100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for design purposes, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the TC1100 and must be considered for system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the TC1100 is included.

4.1.2 Absolute Maximum Rating

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_{A}	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_{J}	-40	125	°C	under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} 1)	V_{DD}	-0.5	1.7	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} 2)	V_{DDP}	-0.5	4.0	V	–
Voltage on any pin with respect to V_{SS} 2)	V_{IN}	-0.5	4.0	V	–
Input current on any pin during overload condition	I_{IN}	-10	10	mA	–
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	–
CPU & LMB Bus Frequency	f_{SYS}	–	150	MHz	–
FPI Bus Frequency	f_{FPI}	–	100	MHz	–

1) Applicable for V_{DD} and V_{DDOSC}.

2) Applicable for V_{DDP} and V_{DDOSC3}. The maximum voltage difference must not exceed 4.0 V in any case (i.e. Supply Voltage = 4.0 V and Input Voltage = -0.5 V is not allowed).

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.1.3 Operating Condition

The following operating conditions must be complied with in order to ensure correct operation of the TC1100. All parameters specified in the following table refer to these operating conditions, unless otherwise indicated.

Parameter	Symbol	Limit Values		Unit	Notes Conditions
		min.	max.		
Digital supply voltage	V_{DD}	1.43	1.58	V	–
	V_{DDP}	3.14	3.47	V	–
Digital ground voltage	V_{SS}	0		V	–
Digital core supply current	I_{DD}	–	525	mA	–
Ambient temperature under bias	T_A	-40	+85	°C	–
CPU clock	f_{SYS}	–[1]	150	MHz	–
Overload current	I_{OV}	-1	1	mA	[2][3]
		-3	3		duty cycle ≤ 25%
Short circuit current	I_{SC}	-1	1	mA	[4]
		-3	3		duty cycle ≤ 25%
Absolute sum of overload + short circuit currents	$\Sigma\lvert I_{OV}\rvert + \lvert I_{SC}\rvert$	–	|50|	mA	[3]
			|100|		duty cycle ≤ 25%
Inactive device pin current ($V_{DD} = V_{DDP} = 0$)	I_{ID}	-1	1	mA	–
External load capacitance	C_L	–	50	pF	–
ESD strength	–	2000	–	V	Human Body Model (HBM)

[1] The TC1100 uses a static design, so the minimum operation frequency is 0 MHz. However, due to test time restriction no lower frequency boundary is tested.

[2] Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DDP} + 0.5$ V or $V_{OV} < V_{SS} - 0.5$ V). The absolute sum of input overload currents on all digital I/O pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

[3] Not subject to production test, verified by design/characterization.

[4] Applicable for digital inputs.

4.2 DC Parameters

4.2.1 Input/Output Characteristics

V_{SS} = 0 V; T_A = -40°C to +125°C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
GPIO pins, Dedicated pins and EBU pins					
Input low voltage	V_{IL} SR	-0.3	0.8	V	LvTTL
Input high voltage	V_{IH} SR	2.0	V_{DDP} + 0.3	V	LvTTL
Output low voltage	V_{OL} CC	–	0.4	V	I_{OL} = 2mA
Output high voltage	V_{OH} CC	2.4	–	V	I_{OH} = -2mA
Pull-up current [1]	$\|I_{PUA}\|$ CC	–	149	µA	V_{IN} = 0V
	$\|I_{PUC}\|$ CC	–	7.2	µA	V_{IN} = 0V
Pull-down current [2]	$\|I_{PDA}\|$ CC	–	156	µA	V_{IN} = V_{DDP}
	$\|I_{PDC}\|$ CC	–	15.7	µA	V_{IN} = V_{DDP}
Input leakage current [3]	I_{OZ1} CC	–	±350	nA	$0 < V_{IN} < V_{DDP}$
Pin Capacitance [4]	C_{IO} CC	–	10	pF	*f* = 1 MHz T_A = 25 °C

---

[1] The current is applicable to the pins, for which a pull-up has been specified. Refer to **Table 2-1**. I_{PUx} refers to the pull-up current for type *x in absolute values*.

[2] The current is applicable to the pins, for which a pull-down has been specified. Refer to **Table 2-1**. I_{PDx} refers to the pull-down current for type *x in absolute values*.

[3] Excluded following pins: $\overline{\text{NMI}}$, $\overline{\text{TRST}}$, TCK, TDI, TMS, ALE, P2.1,HWCFG0, HWCFG1, HWCFG2, BRKIN, PORST, HDRST.

[4] Not subject to production test, verified by design/characterization

4.2.2 Oscillator Characteristics

V_{SS} = 0 V; T_A = -40°C to +125°C

Parameter	**Symbol**	**Limit Values**		**Unit**	**Test Condition**
		min.	**max.**		
Oscillator Pins					
Input low voltage at XTAL1	V_{ILX} SR	-0.3	–	V	[1]
Input high voltage at XTAL1	V_{IHX} SR	–	3	V	[1]
Quartz oscillation peak-peak amplitude at oscillator Input	V_{PPOSC} SR	0.6	–	V	[1]
Input low voltage at XTAL1	V_{ILX} SR	-0.3	0.1	V	[2]
Input high voltage at XTAL1	V_{IHX} SR	1.4	V_{DDC} + 0.3V	V	[2]
Oscillator input current	I_{OSCIN}	–	25	µA	

[1] Quartz mode: using a quartz crystal

[2] Bypass mode: using an external clock

4.2.3 IIC Characteristics

Each IIC Pin is an open drain output pin with different characteristics than other pins. The related characteristics are given in the following table.

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Output low voltage	V_{OL}	CC	–	0.4 0.6	V	3 mA sink current 6 mA sink current
Input high voltage[1]	V_{IH}	SR	$0.7V_{DDP}$	V_{DDP}+0.5	V	–
Input low voltage[1]	V_{IL}	SR	-0.5	$0.3V_{DDP}$	V	–

[1] Not subject to production test, verified by design/characterization.

Note: No 5 V IIC interface is supported with these pads. Only voltages lower than 3.63 V must be applied to these pads.

Note: IIC pins have no pull-up and pull-down devices.

4.2.4 Power Supply Current

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. [1]	max.		
Active mode supply current	I_{DD}	314	679	mA	Sum of I_{DDS} [2]
		153	345	mA	I_{DD} at V_{DD} [3]
		156	322	mA	I_{DD} at V_{DDP}
Idle mode supply current	I_{ID}	74	154	mA	Sum of I_{DDS}[2][4]
		66	130	mA	I_{DD} at V_{DD}[3][4]
		6	15	mA	I_{DD} at V_{DDP}[4]
Deep sleep mode supply current	I_{DS}	2	19	mA	Sum of I_{DDS}[2][5]
		2	19	mA	I_{DD} at V_{DD}[3][5]
		3.6	58	µA	I_{DD} at V_{DDP}[5]

[1] Typical values are measured at 25°C, CPU clock at 150 MHz, and nominal supply voltage that is 3.3 V for V_{DDP}, V_{DDOSC3} and 1.5 V for V_{DD}, V_{DDOSC}. These currents are measured using a typical application pattern. The power consumption of modules can increase or decrease using other application programs.

[2] These power supply currents are defined as the sum of all currents at the V_{DD} power supply lines: $V_{DD} + V_{DDP} + V_{DDOSC3} + V_{DDOSC}$

[3] This measurement includes the TriCore™ and Logic power supply lines.

[4] CPU is in idle state, input clocks to all peripherals are enabled.

[5] Clock generation is disabled at the source.

4.3 AC Parameters

4.3.1 Power, Pad and Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA} CC	0.6	–	V
Oscillator start-up time[2]	t_{OSCS} CC	–	30	ms
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA} CC	50	–	ms
$\overline{\text{HDRST}}$ pulse width	t_{HD} CC	1024 cycles[3]		f_{SYS}
Ports inactive after any reset active[2]	t_{PI} CC	–	30	ns

[1] This parameter is valid under assumption that PORST signal is constantly at low level during the power-up/power-down of the V_{DDP}.

[2] Not subject to production test, verified by design/characterization.

[3] Any $\overline{\text{HDRST}}$ activation is internally prolonged to 1024 FPI bus clock cycles.

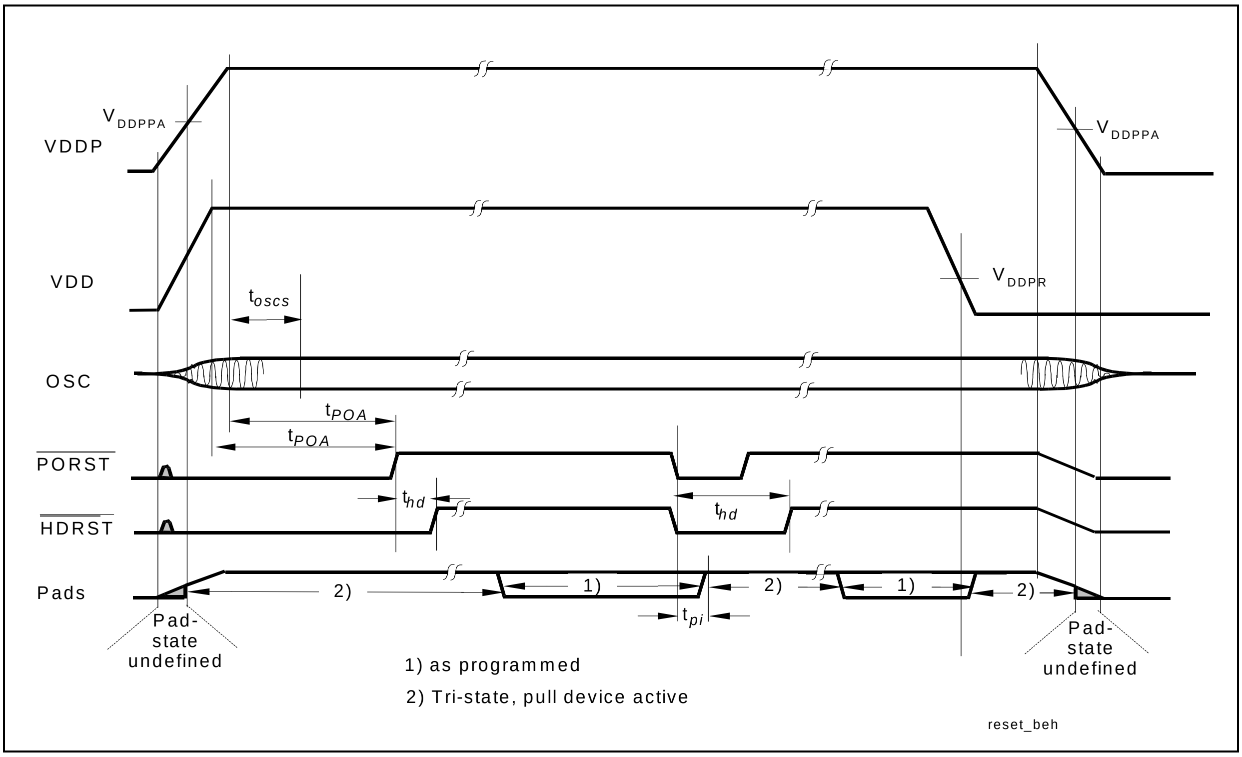


Figure 4-1 Power and Reset Timing

4.3.2 PLL Parameters

When PLL operation is configured (*PLL_CLC.LOCK* = *1*), the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor (N Factor), and the output divider (**F** = *NDIV+1 / (PDIV+1 × KDIV+1)*). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock, the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.

The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency in order to correspond to the applied input frequency (crystal or oscillator), the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 4-2**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baud rates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = *KDIV*+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as $K \times N$, where N is the number of consecutive f_{MC} cycles (TCM).

For a period of $N \times$ TCM, the accumulated PLL jitter is defined by the corresponding deviation D_N:

D_N [ns] = $\pm(1.5 + 6.32 \times N / f_{MC})$; f_{MC} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns.

This formula is applicable for $K \times N < 95$. For longer periods, the $K \times N = 95$ value can be used. This steady value can be approximated by: D_{Nmax} [ns] = $\pm(1.5 + 600 / (K \times f_{MC}))$.

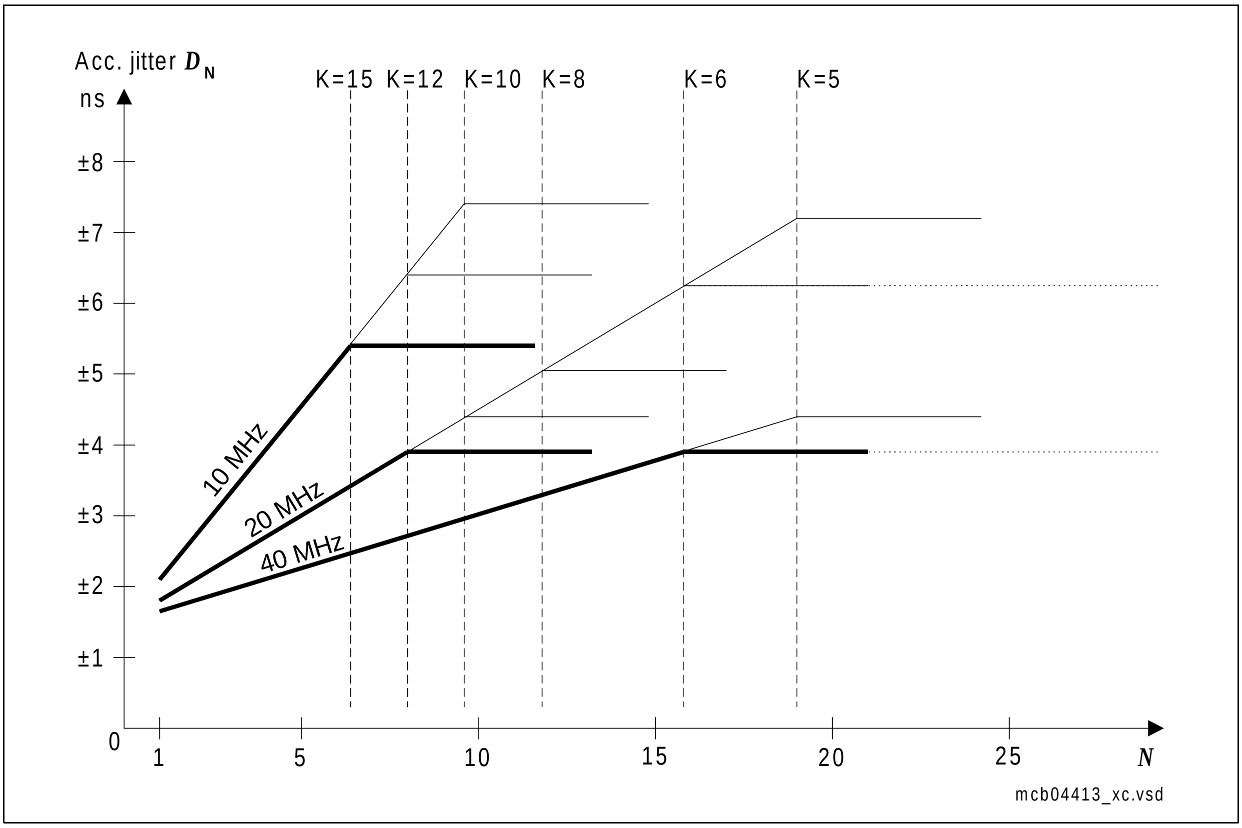


Figure 4-2 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 4-1 VCO Bands for PLL Operation

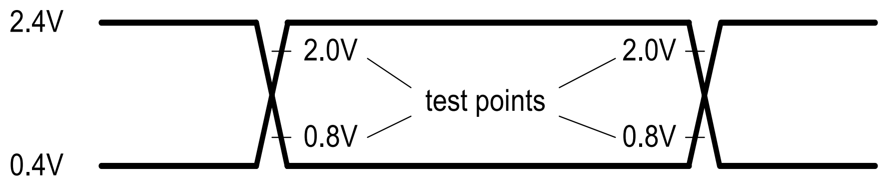
PLL_CLC.VCOSEL	VCO Frequency Range	Base Frequency Range [1]
00	400 ... 500 MHz	250 ... 320 MHz
01	500 ... 600 MHz	300 ... 400 MHz
10	600 ... 700 MHz	350 ... 480 MHz
11	Reserved [2]	

[1] Base Frequency Range is the free running operation frequency of the PLL, when no input clock is available.

[2] This option cannot be used.

4.3.3 AC Characteristics

(Operating Conditions apply)



AC inputs during testing are driven at 2.4V for a logic “1” and 0.4V for a logic “0”. Timing measurements are made at V_{IHmin} for a logic “1” and V_{ILmax} for a logic “0”.

Figure 4-3 Input/Output Waveforms for AC Tests - for GPIO, Dedicated and EBU pins

4.3.4 Input Clock Timing

(Operating Conditions apply)

Parameter		Symbol	Limits		Unit
			min	max	
Oscillator clock frequency	with PLL	f_{OSC} SR	4	25	MHz
Input clock frequency driving at XTAL1	with PLL	f_{OSCDD} SR	-	40	MHz
Input Clock Duty Cycle (t_1 /t_2)		SR	45	55	%

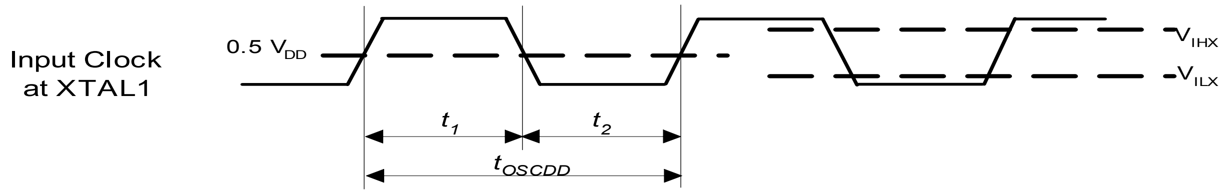


Figure 4-4 Input Clock Timing

4.3.5 Port Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
Port data valid from TRCLK [1] up to 120 MHz[2]	t_1	CC	–	13	ns

[1] Port data is output with respect to the FPI clock. The TRCLK is used as a reference here since the FPI clock is not available as an external pin and TRCLK is same frequency as CPU clock. Port lines maintain their states for at least 2 CPU clocks.

[2] 120 MHz is verified by design/characterization.

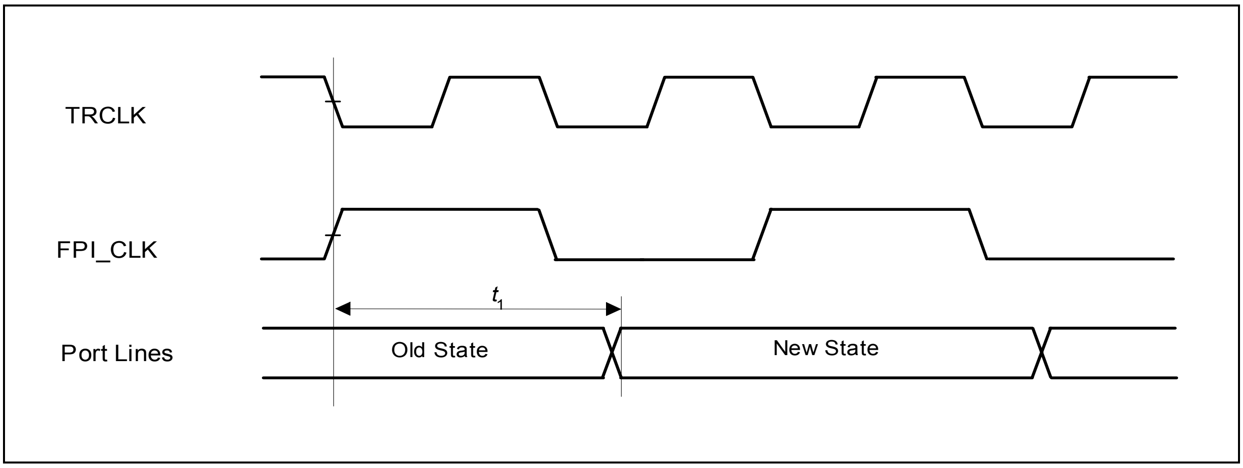


Figure 4-5 Port Timing

4.3.6 Timing for JTAG Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
TCK clock period	t_{TCK} SR	50	–	ns
TCK high time	t_1 SR	10	–	ns
TCK low time	t_2 SR	29	–	ns
TCK clock rise time	t_3 SR	–	0.4	ns
TCK clock fall time	t_4 SR	–	0.4	ns

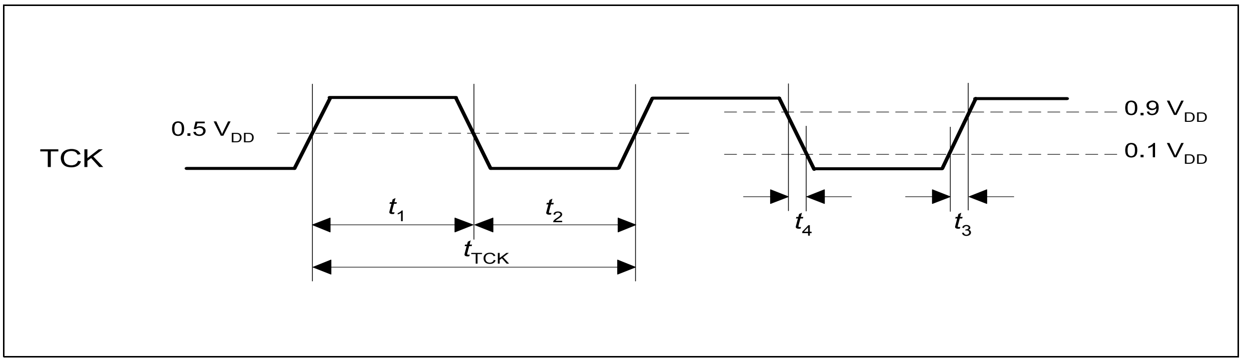


Figure 4-6 TCK Clock Timing

Parameter	Symbol	Limits		Unit
		min	max	
TMS setup to TCK ↑	t_1 SR	7.85	–	ns
TMS hold to TCK ↑	t_2 SR	3.0	–	ns
TDI setup to TCK ↑	t_1 SR	10.9	–	ns
TDI hold to TCK ↑	t_2 SR	3.0	–	ns
TDO valid output from TCK ↓	t_3 CC	–	10.7	ns
TDO high impedance to valid output from TCK ↓	t_4 CC	–	23.0	ns
TDO valid output to high impedance from TCK ↓	t_5 CC	–	26.0	ns

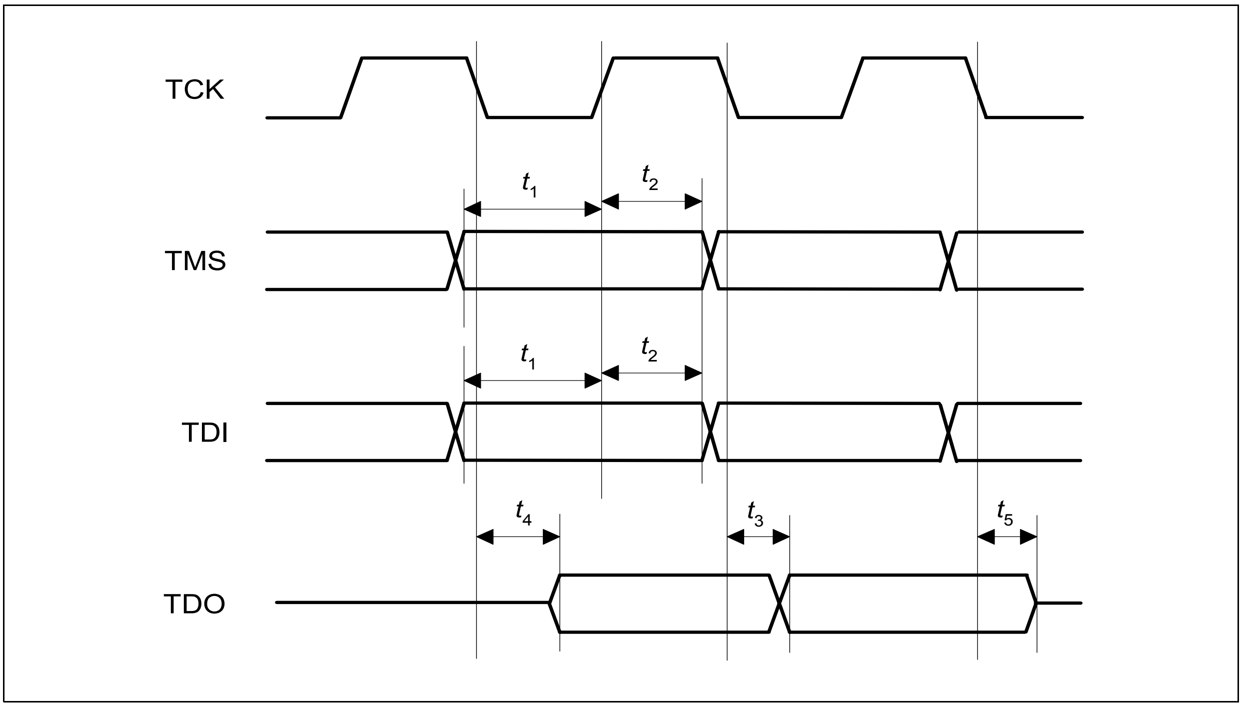
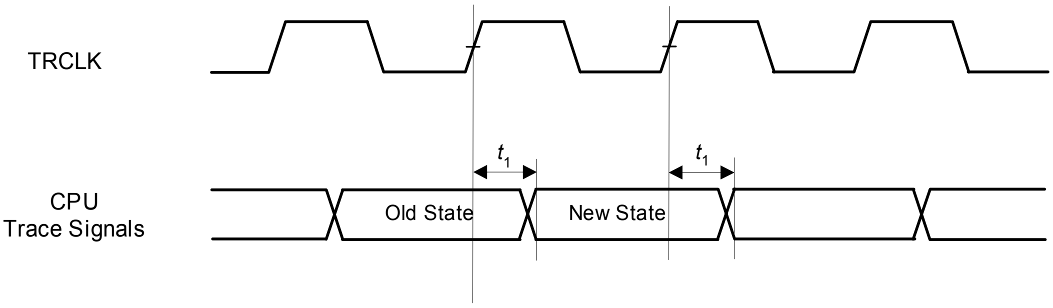


Figure 4-7 JTAG Timing

4.3.7 Timing for OCDS Trace and Breakpoint Signals

(Operating Conditions apply; C_L(TRCLK) = 25 pF, C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\text{BRK\_OUT}}$ valid from TRCLK ↑	t_1	CC	–	5.2	ns
$\overline{\text{OCDS2\_STATUS[4:0]}}$ valid from TRCLK ↑	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ valid from TRCLK ↑	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_BRKPT[2:0]}}$ valid from TRCLK ↑	t_1	CC	0	5	ns



Note: CPU Trace Signals include $\overline{\text{BRK\_IN}}$, $\overline{\text{BRK\_OUT}}$, $\overline{\text{OCDS2\_STATUS[4:0]}}$, OCDS2_INDIR_PC[7:0] and OCDS_BRKPT[2:0].

Figure 4-8 OCDS Trace Signals Timing

4.3.8 EBU Timings

4.3.8.1 SDCLKO Output Clock Timing

(Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits[1]		Limits[2]		Unit
			min	max	min	max	
SDCLKO period	t_1	CC	10	–	8.3	–	ns
SDCLKO high time	t_2	CC	3	–	2.5	–	ns
SDCLKO low time	t_3	CC	3	–	2.5	–	ns
SDCLKO rise time	t_4	CC	–	2.5	–	2.5	ns
SDCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

2) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

4.3.8.2 BFCLKO Output Clock Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit[1]		Limit[2]		Unit
			min	max	min	max	
Clock period	t_1	CC	20	–	16.7	–	ns
BFCLKO high time	t_2	CC	6.6	–	7.5	–	ns
BFCLKO low time	t_3	CC	6.6	–	7.5	–	ns
BFCLKO rise time	t_4	CC	–	3.5	–	3.5	ns
BFCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The CPU runs at 150 MHz and the Burst Flash runs at divided by 3 clock.

2) The CPU runs at 120 MHz and the Burst Flash runs at divided by 2 clock.

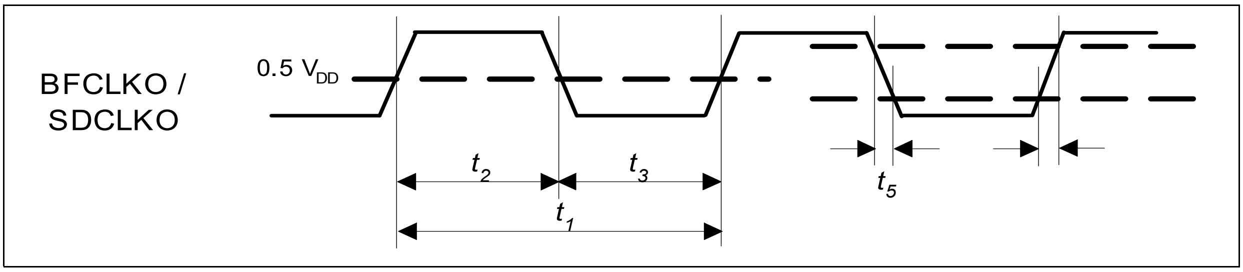


Figure 4-9 EBU Clock Output Timing

4.3.8.3 Timing for SDRAM Access Signals

(Operating Conditions apply; C_L = 50 pF[1])

Parameter	Symbol		Limits[2]		Limits[3]		Unit
			min	max	min	max	
SDCLKO period	t_1	CC	10	–	8.3	–	ns
CKE output valid time from SDCLKO ↗	t_1	CC	–	8.0	–	6.8	ns
CKE output hold time from SDCLKO ↗	t_2	CC	0	–	0.8	–	ns
Address output valid time from SDCLKO ↗	t_3	CC	–	8.0	–	6.8	ns
Address output hold time from SDCLKO ↗	t_4	CC	1.0	–	0.8	–	ns
$\overline{\text{CSx}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BC(3:0)}}$ output valid time from SDCLKO ↗	t_5	CC	–	8.0	–	6.8	ns
$\overline{\text{CSx}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BC(3:0)}}$ output hold time from SDCLKO ↗	t_6	CC	1.0	–	0.8	–	ns
AD(31:0) output valid time from SDCLKO ↗	t_7	CC	–	8.0	–	6.8	ns
AD(31:0) output hold time from SDCLKO ↗	t_8	CC	1.0	–	0.8	–	ns
AD(31:0) input setup time to SDCLKO ↗	t_9	SR	4.0	–	2.9	–	ns
AD(31:0) input hold time from SDCLKO ↗	t_{10}	SR	3.0	–	3.0	–	ns

1) If application conditions other than 50 pf capacitive load are used, then the proper correlation factor should be used for your specific application condition. For design team, the load should be set according to the system requirement.

2) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

3) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

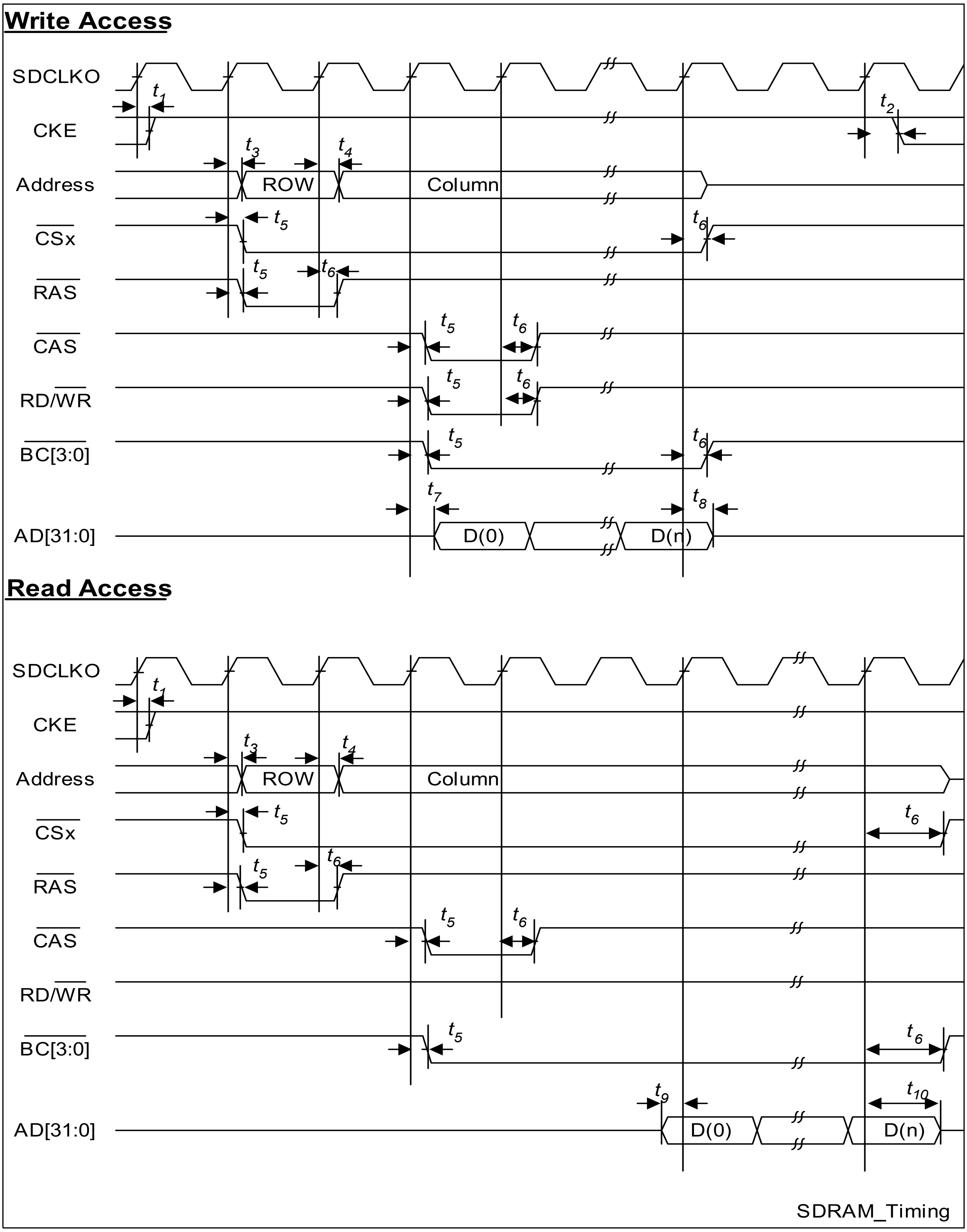


Figure 4-10 SDRAM Access Timing

4.3.8.4 Timing for Burst Flash Access Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
Address output valid time from BFCLKO ↑	t_1	CC	–	11.0	ns
Address output hold time from BFCLKO ↑	t_2	CC	10.0	–	ns
$\overline{\text{CSx}}$ output valid time from BFCLKO ↑	t_3	CC	–	9.0	ns
$\overline{\text{RD}}$ output valid time from BFCLKO ↑	t_4	CC	–	10.0	ns
$\overline{\text{ADV}}$ output valid time from BFCLKO ↑	t_5	CC	–	10.0	ns
$\overline{\text{ADV}}$ output hold time from BFCLKO ↑	t_6	CC	3.0	–	ns
$\overline{\text{BAA}}$ output valid time from BFCLKO ↑	t_7	CC	–	10.0	ns
$\overline{\text{BAA}}$ output hold time from BFCLKO ↑	t_8	CC	3.0	–	ns
AD(31:0) input setup time to BFCLKO ↑	t_9	SR	5.0	–	ns
AD(31:0) input hold time from BFCLKO ↑	t_{10}	SR	3.0	–	ns
$\overline{\text{WAIT}}$ input setup time to BFCLKO ↑	t_{11}	SR	5.0	–	ns
$\overline{\text{WAIT}}$ input hold time from BFCLKO ↑	t_{12}	SR	3.0	–	ns

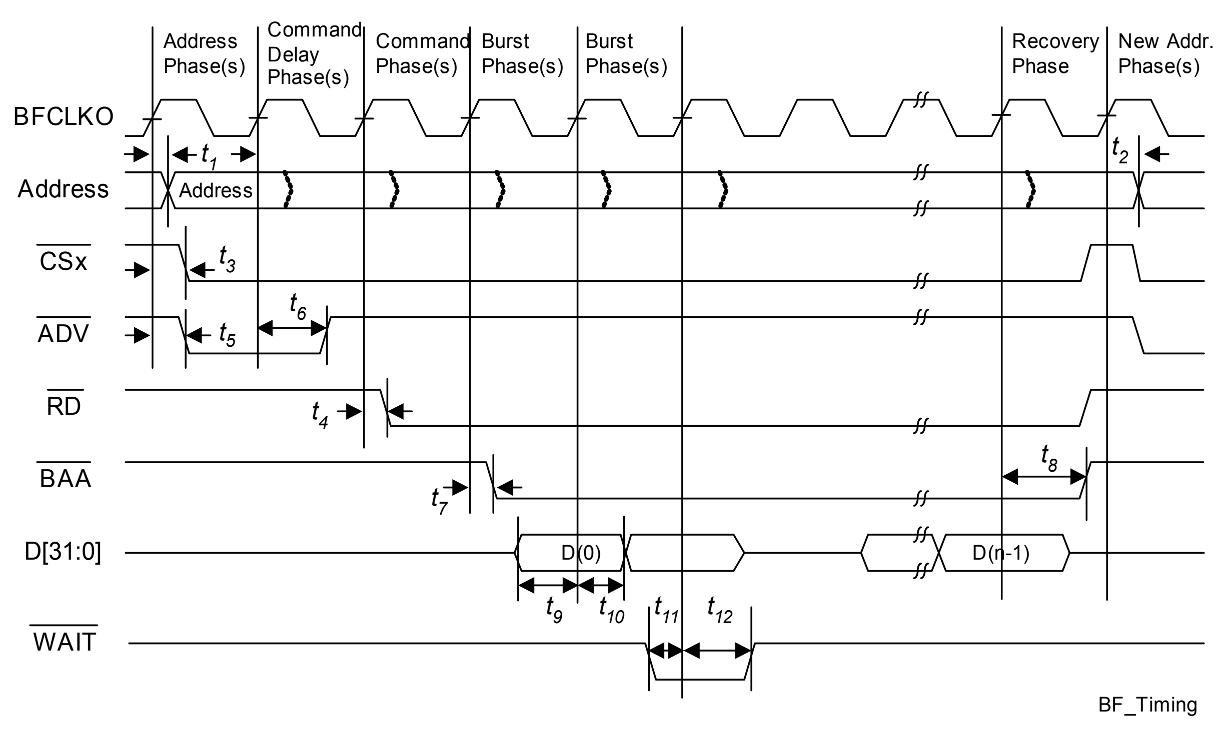


Figure 4-11 Burst Flash Access Timing

Note: Output delays are always referenced to BFCLKO. The reference clock for input characteristics depends on bit BFCON.FDBKEN.
BFCON.FDBKEN = 0: BFCLKO is the input reference clock.
BFCON.FDBKEN = 1: BFCLKI is the input reference clock (EBULMB clock feedback enabled).

4.3.8.5 Timing for Demultiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF) [1]

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\mathrm{CSx}}$, RD/$\overline{\mathrm{WR}}$, $\overline{\mathrm{RD}}$, MR/$\overline{\mathrm{W}}$, $\overline{\mathrm{BC(3:0)}}$ output valid time from output clock ↑	t_1	CC	–	9	ns
$\overline{\mathrm{CSx}}$, RD/$\overline{\mathrm{WR}}$, $\overline{\mathrm{RD}}$, MR/$\overline{\mathrm{W}}$, $\overline{\mathrm{BC(3:0)}}$ output hold time from output clock ↑	t_2	CC	0.0	–	ns
Address output valid time from output clock ↑	t_3	CC	–	9	ns
Address output hold time from output clock ↑	t_4	CC	0.0	–	ns
$\overline{\mathrm{WAIT}}$ input setup time to output clock ↑	t_7	SR	12	–	ns
$\overline{\mathrm{WAIT}}$ input hold time from output clock ↑	t_8	SR	3	–	ns
AD(31:0) output valid time from output clock ↑	t_9	CC	–	9	ns
AD(31:0) output hold time from output clock ↑	t_{10}	CC	0.0	–	ns
AD(31:0) input setup time to output clock ↑	t_{11}	SR	1.3	–	ns
AD(31:0) input hold time from output clock ↑	t_{12}	SR	3	–	ns
$\overline{\mathrm{RMW}}$ output valid time from output clock ↑	t_{13}	CC	–	8	ns
$\overline{\mathrm{RMW}}$ output hold time from output clock ↑	t_{14}	CC	1.3	–	ns
AD(31:0) output hold time from RD/$\overline{\mathrm{WR}}$ ↑	t_{16}	CC	0	–	ns

---

1) The purpose for characterization of Asynchronous access is to provide the performance of all of the signals to user. User can decide whether an extra cycle is needed or not based on above parameters to generate signals with correct timing sequence. It is user's responsibility to program the correct phase length according to the memory/peripheral device specification and EBU specification.

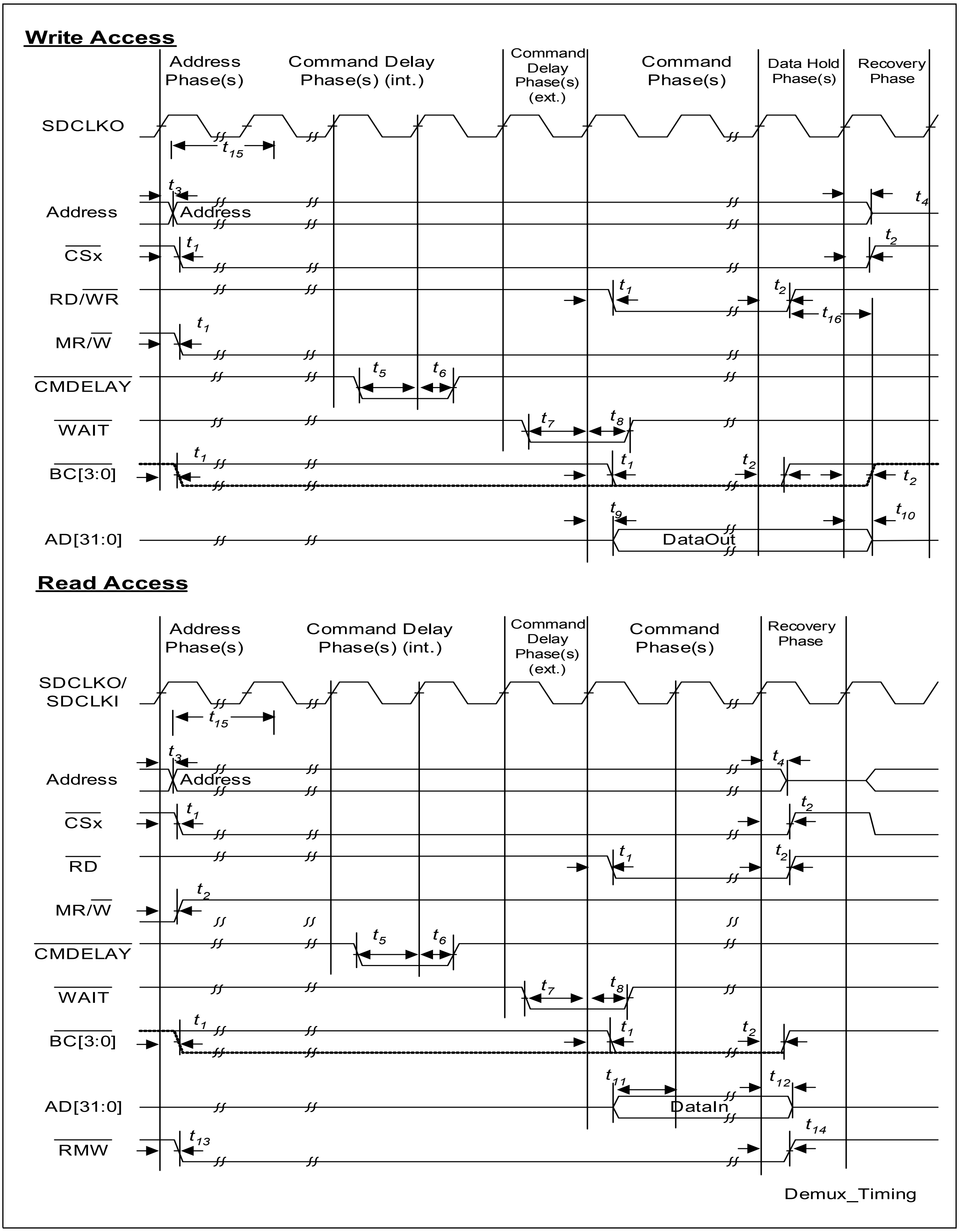


Figure 4-12 Demultiplexed Asynchronous Device Access Timing

4.3.8.6 Timing for Multiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF)[1]

Parameter	Symbol	Limits		Unit
		min	max	
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output valid time from output clock ↑	t_1 CC	–	9	ns
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output hold time from output clock ↑	t_2 CC	0.0	–	ns
AD(31:0) output valid time from output clock ↑	t_3 CC	–	9	ns
AD(31:0) output hold time from output clock ↑	t_4 CC	0.0	–	ns
AD(31:0) input setup time to output clock ↑	t_5 SR	1.4	–	ns
AD(31:0) input hold time from output clock ↑	t_6 SR	3	–	ns
$\overline{\text{WAIT}}$ input setup time to output clock ↑	t_9 SR	12	–	ns
$\overline{\text{WAIT}}$ input hold time from output clock ↑	t_{10} SR	3	–	ns
$\overline{\text{RMW}}$ output valid time from output clock ↑	t_{11} CC	–	8	ns
$\overline{\text{RMW}}$ output hold time from output clock ↑	t_{12} CC	1.3	–	ns
ALE width	t_{13} CC	8.5	–	ns
AD(31:0) output hold time from RD/$\overline{\text{WR}}$ ↑	t_{14} CC	0	–	ns

[1] The purpose for characterization of Asynchronous access is to provide the performance of all of the signals to user. User can decide whether an extra cycle is needed or not based on above parameters to generate signals with correct timing sequence. It is user's responsibility to program the correct phase length according to the memory/peripheral device specification and EBU Specification.

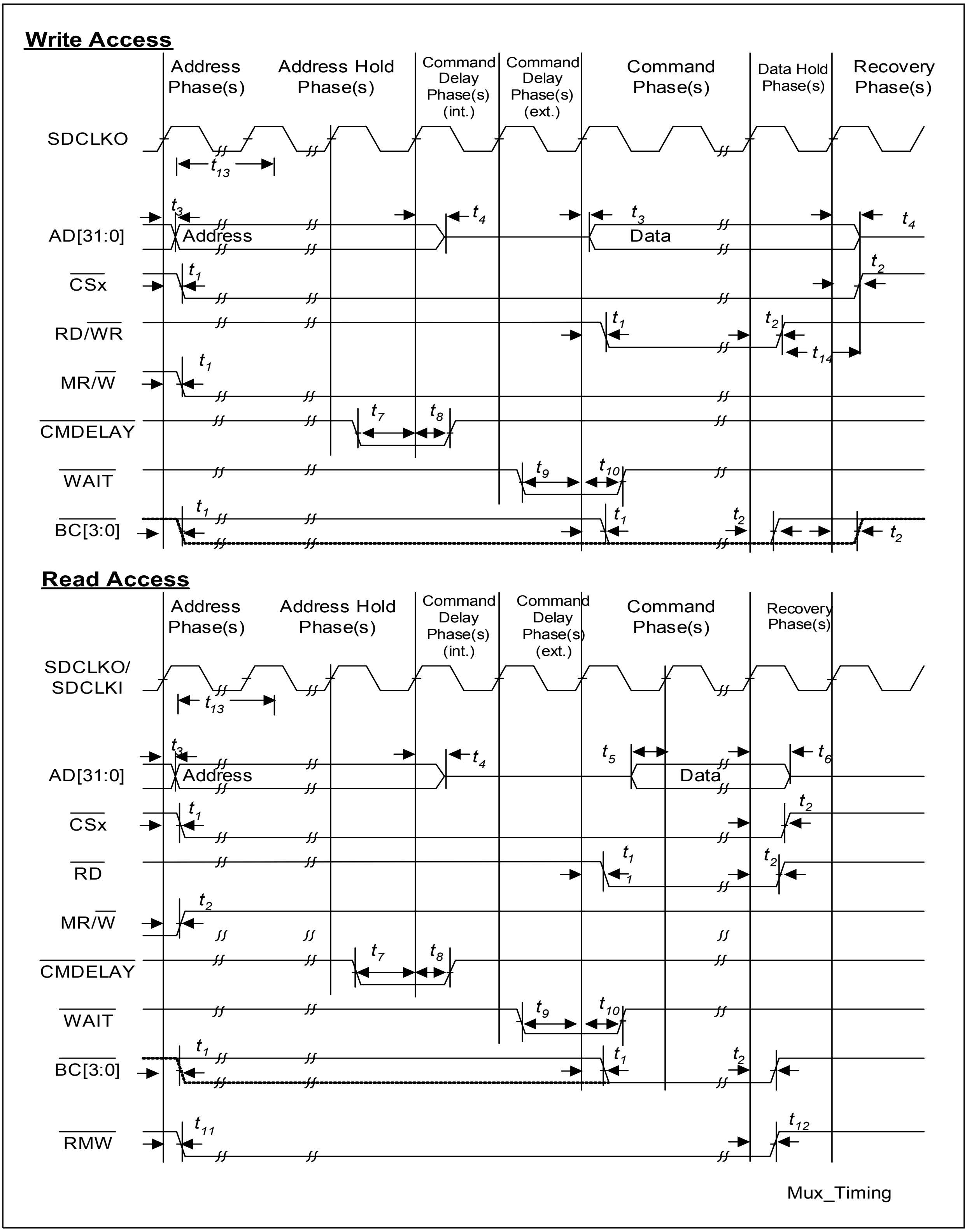


Figure 4-13 Write Access in Multiplexed Access

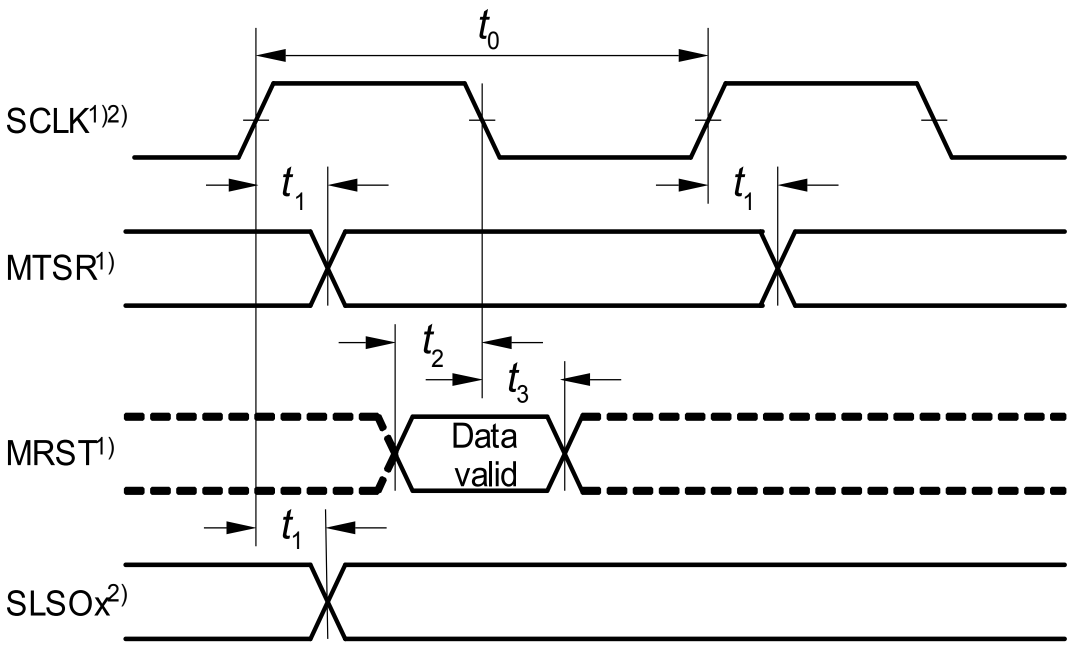
4.3.9 Peripheral Timings

4.3.9.1 SSC Master Mode Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK clock period	t_0	CC	2*T_{SSC} [1]	–	ns
MTSR/SLSOx delay from SCLK ↑	t_1	CC	0	8	ns
MRST setup to SCLK ↓	t_2	SR	10	–	ns
MRST hold from SCLK ↓	t_3	SR	5	–	ns

[1] $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 120MHz, t_0 = 16.7ns



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

Figure 4-14 SSC Master Mode Timing

4.3.9.2 MLI Interface Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
TCLK/RCLK clock period	t_0 CC/SR	$2*T_{MLI}$ [1]	–	ns
MLI outputs delay from TCLK ↑	t_5 CC	0	8	ns
MLI inputs setup to RCLK ↓	t_6 SR	4	–	ns
MLI inputs hold to RCLK ↓	t_7 SR	4	–	ns
RREADY output delay from TCLK ↓	t_8 CC	0	8	ns

[1] $T_{MLImin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 120MHz, t_0 = 16.7ns

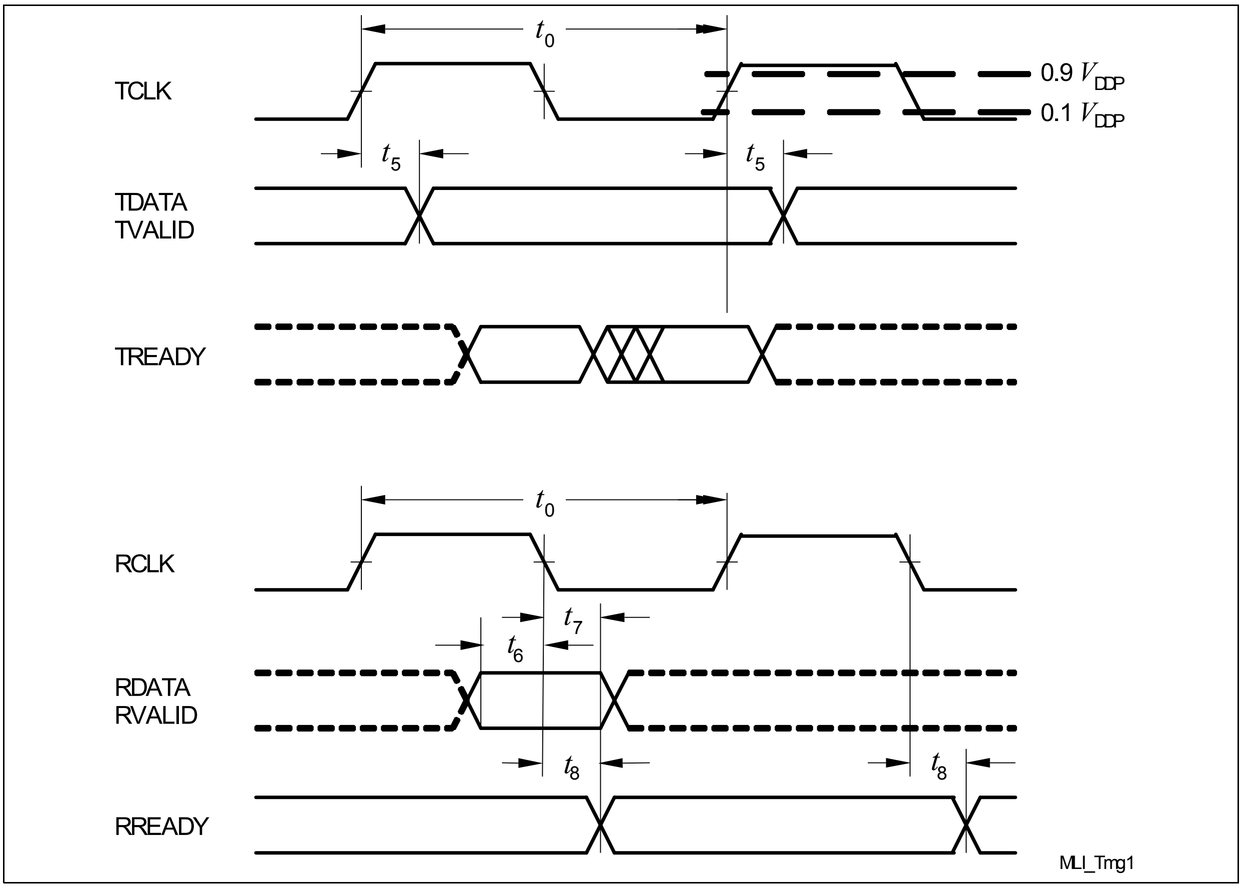


Figure 4-15 MLI Interface Timing

Note: The generation of RREADY is in the input clock domain of the receiver. The reception of TREADY is asynchronous to TCLK.

5 Package Outline

Plastic Package, P-LBGA-208-2 (SMD)
(Low Profile Ball

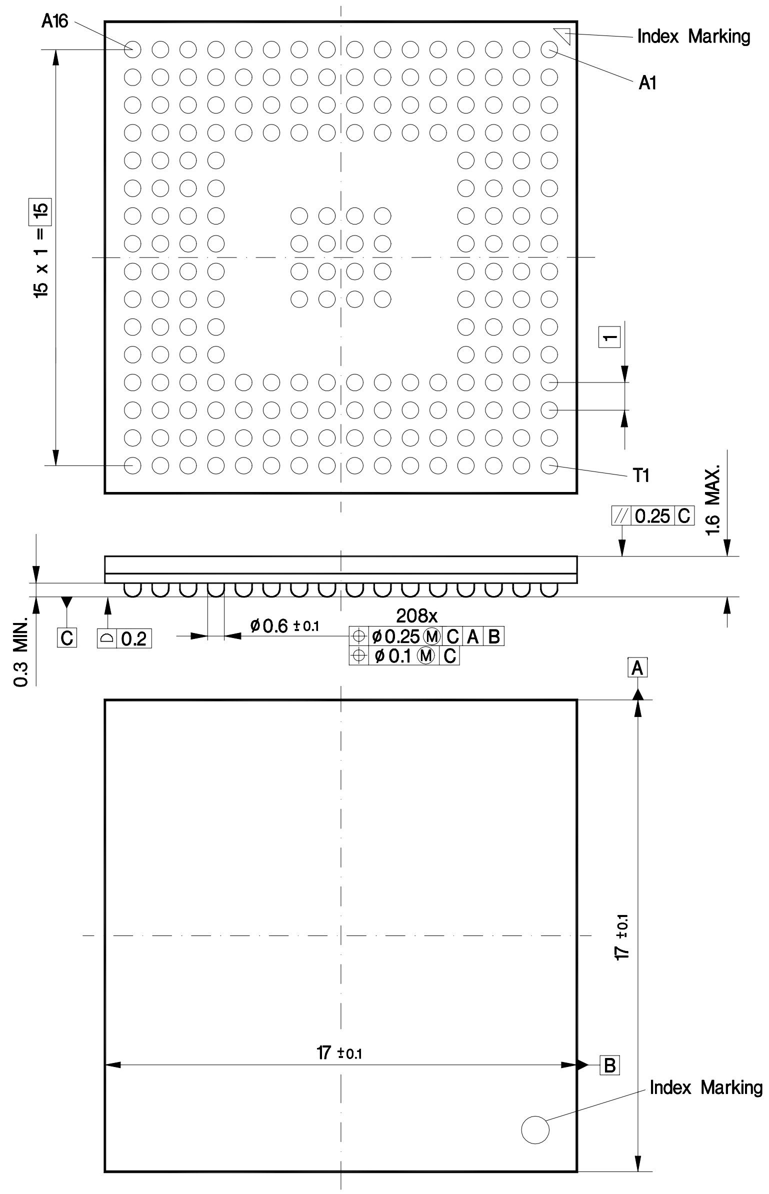


Figure 5-1 P-LBGA-208-2 Package

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

www.infineon.com

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