MOSFET – Single, N-Channel, Small Signal, SC-88

25 V, 1.2 A

Features

- Advance Planar Technology for Fast Switching, Low RDS(on)
- Higher Efficiency Extending Battery Life
- AEC-Q101 Qualified and PPAP Capable NVJS4405N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Boost and Buck Converter
- Load Switch
- Battery Protection

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit		
Drain-to-Source Voltage	V _{DSS}	25	V		
Gate-to-Source Voltage			V _{GS}	±8.0	V
Drain Current	t < 5 s	T _A = 25°C	I _D	1.2	Α
Continuous Drain Current	Steady	T _A = 25°C	I _D	1.0	Α
(Note 1)	State $T_A = 75^{\circ}C$			0.80	
Power Dissipation (Note 1)	Steady State		P_{D}	0.63	W
Power Dissipation (Note 1)	t≤	t ≤ 5 s		0.89	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	3.7	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to +150	°C
Source Current (Body Dioc	I _S	0.8	Α		
Lead Temperature for Sold (1/8" from case for 10 s		oses	T _L	260	°C
ESD Rating - Machine Mo	del			25	V

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Lead - Steady State (Note 1)	$R_{\theta JL}$	102	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	200	
Junction-to-Ambient - t ≤ 5 s (Note 1)	Reia	140	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1

 Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

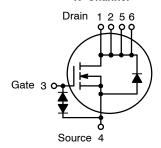


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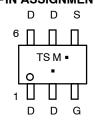
V _{(BR)DSS}	R _{DS(on)} Typ	I _D Max
25 V	249 mΩ @ 4.5 V	1.2 A
25 V	299 mΩ @ 2.7 V	1.27

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT





TS = Device Code

M = Date Code

Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTJS4405NT1G	SC-88 (Pb-Free)	3000 / Tape & Reel
NVJS4405NT1G	SC-88 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				30		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1.0	μΑ
		$V_{DS} = 20 \text{ V}$	T _J = 125°C			10	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{C}$	_S = 8.0 V			100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D}$	= 250 μΑ	0.65		1.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-2.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.6 A			249	350	mΩ
	-	V _{GS} = 2.7 V, I	_D = 0.2 A		299	400	1
	-	V _{GS} = 4.5 V, I _D = 1.2 A			260		
Forward Transconductance	9FS	$V_{DS} = 5.0 \text{ V}, I_D = 0.5 \text{ A}$			0.5		S
CHARGES AND CAPACITANCES							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 10 V			49	60	pF
Output Capacitance	C _{OSS}				22.4	30	
Reverse Transfer Capacitance	C _{RSS}				8.0	12	
Total Gate Charge	Q _{G(TOT)}				0.75	1.5	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, V _I	os = 5.0 V,		0.10		
Gate-to-Source Charge	Q_{GS}	I _D = 0.9	5 A		0.30	0.50	
Gate-to-Drain Charge	Q_{GD}				0.20	0.40	
SWITCHING CHARACTERISTICS (No	ote 3)						
Turn-On Delay Time	t _{d(ON)}				6.0	12	ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{I}$	os = 6.0 V,		4.7	8.0	7
Turn-Off Delay Time	t _{d(OFF)}	V_{GS} = 4.5 V, V_{DS} = 6.0 V, I_{D} = 0.5 A, R_{G} = 50 Ω			25	35	7
Fall Time	t _f				41	60	
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V, I _S = 0.6 A	T _J = 25°C		0.82	1.20	V

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

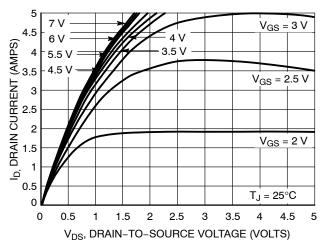


Figure 1. On-Region Characteristics

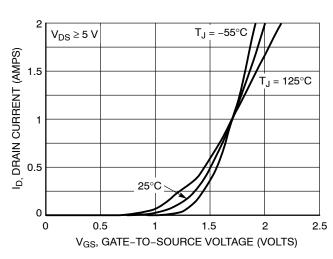


Figure 2. Transfer Characteristics

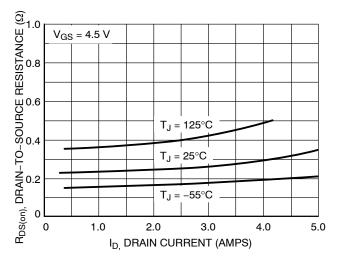


Figure 3. On-Resistance vs. Drain Current and Temperature

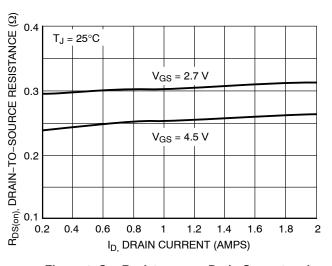


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

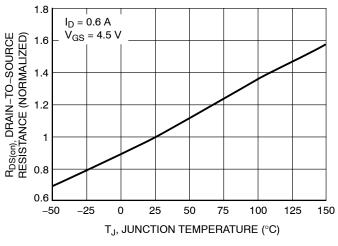


Figure 5. On–Resistance Variation with Temperature

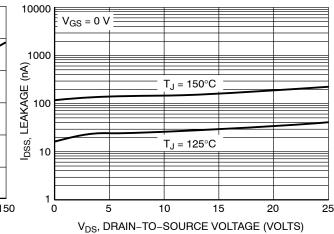


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

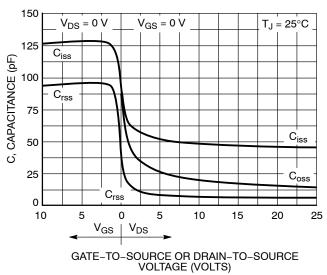


Figure 7. Capacitance Variation

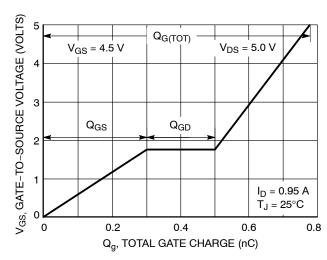


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

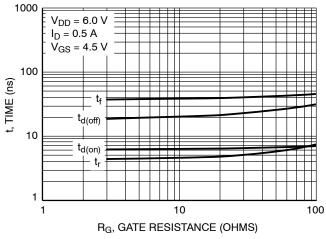


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

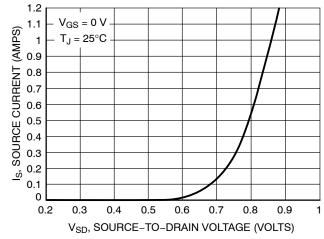
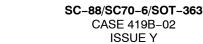
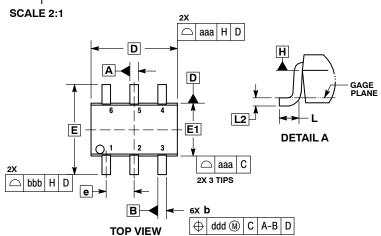


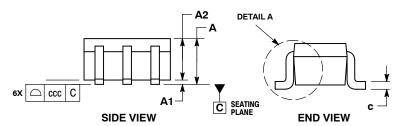
Figure 10. Diode Forward Voltage vs. Current





DATE 11 DEC 2012





NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M. 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRU-SIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.

- SIONS, OH GAILE BURHS SHALL NOT EXCEED 0.20 PEH END.
 DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF
 THE PLASTIC BODY AND DATUM H.
 DATUMS A AND B ARE DETERMINED AT DATUM H.
 DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE
 LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MIL	LIMETE	ERS		INCHES	;	
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α			1.10			0.043	
A1	0.00		0.10	0.000		0.004	
A2	0.70	0.90	1.00	0.027	0.035	0.039	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С	0.08	0.15	0.22	0.003	0.006	0.009	
D	1.80	2.00	2.20	0.070	0.078	0.086	
E	2.00	2.10	2.20	0.078	0.082	0.086	
E1	1.15	1.25	1.35	0.045	0.049	0.053	
е		0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018	
L2		0.15 BS	C	0.006 BSC			
aaa	0.15 0.006						
bbb	0.30				0.012		
ccc		0.10 0.004					
ddd		0.10			0.004		

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

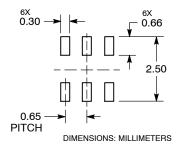
= Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

- *Date Code orientation and/or position may vary depending upon manufacturing location.
- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "=", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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