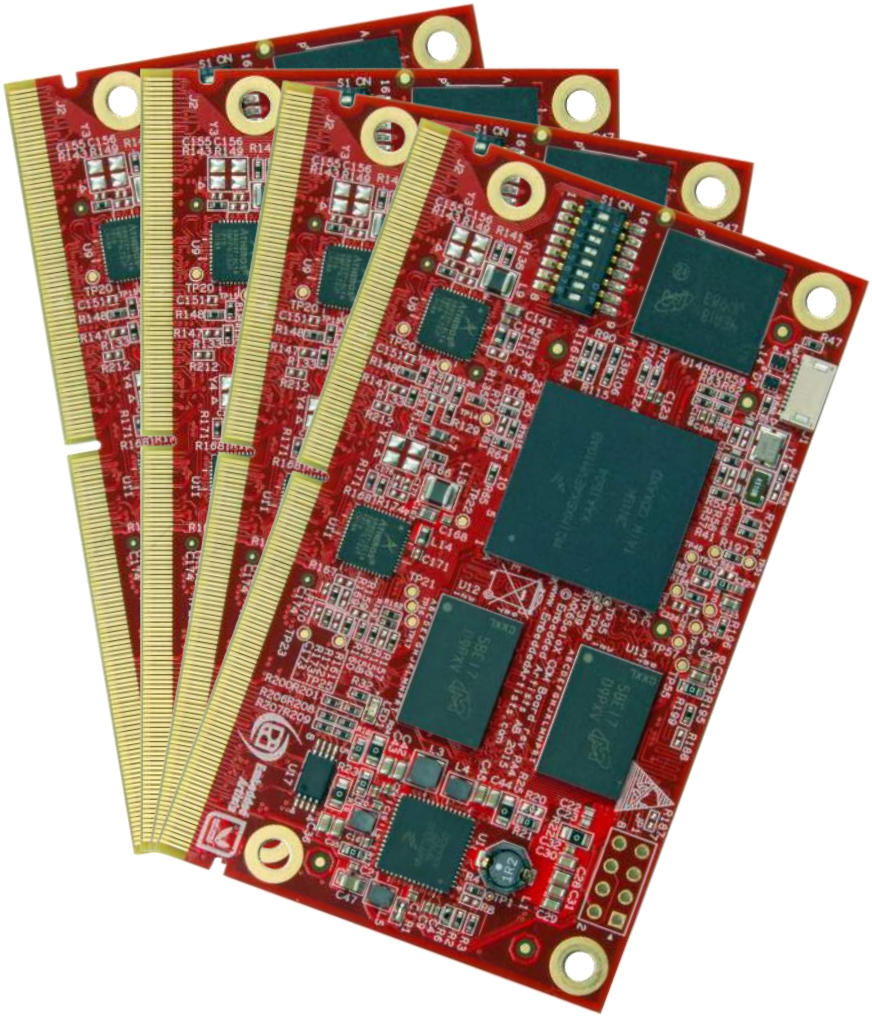
EACOM Board
Specification Version 1.0



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1 Document Revision History

Revision	*Date*	*Description*
PA1	2015-10-08	First version.
PA2	2015-11-02	Minor clarifications and corrections.
PA3	2016-05-16	Minor corrections. Changed UART, SPI and I2C channels to alphanumerical numbering.

2 Introduction

This document describes the specification of Embedded Artists' Computer-on-Modules (COM) Boards, hereafter referred to as ***EACOM***. Mechanical dimensions, interface groups, powering and pin assignments are defined.

The EACOM specification has been created to address a number of issues with embedded systems development . Some of the issues are generically addressed by COM boards, and some are specifically addressed by the EACOM specification:

- **Manage complexity** - modern high-performance and power efficient ARM cores with high-speed interfaces are complex to design. Much of the complexity is encapsulated in the COM boards, **reducing the design effort to integrate** advanced ARM application processors. The EACOM specification, together with the *Carrier Board Design Guide* document reduce the integration effort even further. EACOM pinning has been defined to simplify carrier board routing. In many cases, a standard **low-cost 4-layer PCB will be sufficient for the carrier board**.
- **Flexibility and upgrade path** - different EACOM boards gives different price/performance ratios and feature sets. Designers can select different EACOM boards based on needs, while still maintaining the same carrier board design. Designs tend to grow over the product lifetime and require more performance, memory and/or other features later on. Having higher-performing EACOM boards to select from makes upgrade a simpler process.
- **COM boards are proven designs**, allowing available engineering resources to focus on value adding features rather than spending time on infrastructure. The design effort saved is not only on hardware but also on software BSP design. All in all, EACOM boards **reduce development risk** and **shorten time to market**.
- The EACOM specification is based on a **proven, robust mechanical form factor** and associated (MXM3) connector. There are **ready-to-go thermal management solutions**, like heat spreader and heat sink.
- And last the obvious question; Why not the SMARC standard?
  Based on over 15 years in business and countless designs, Embedded Artists recommends another path for our customers. The SMARC standard has several great features and these have been preserved by the EACOM specification. Other features have changed.
    - SMARC pinning is not particularly well suited for the iMX6/7 family. Most SMARC boards either discard a lot of SoC pins (leave them unconnected) or has additional (non-standard) connectors on the boards to make all signals available - making the boards non-standard.
    - SMARC boards are only (reasonable) interchangeable if the SMARC-defined interfaces are used. In reality it is not a trivial task to switch SMARC boards from completely different suppliers and/or SoC families.
    - EACOM pinning focus on the iMX6/7 SoC family, where it is an ideal fit. All relevant pins are available on the main edge (MXM3) pads. The specification does not claim to be universally applicable.
    - EACOM has 3.3V preferred I/O voltage for most pins. SMARC has 1.8V as preferred I/O voltage, which can lead to several voltage translators on the carrier board.

3 Computer-on-Module Overview

This chapter give a general overview of the board architecture, interfaces and pinning.

An EACOM based system solution has the following overall physical structure:

- **EACOM board**, containing the core design that encapsulate a lot of the complexity of a modern, high-performance ARM SoC design.
- **Carrier board** that implements the needed interfaces in the specific solution. The carrier board also typically contains the powering solution and creates the mechanical entity that shall be mounted in box, or similar. The carrier board is typically a simpler design (i.e., less complex) than the EACOM board. Either the carrier board is a custom specific design or a standard, ready-to-go carrier board design. For custom specific designs, there is design support to minimize the design effort:
    - *EACOM Carrier Board Design Guide* document that contains many guidelines for implementing the many interfaces.
    - Pin assignment on the MXM3 connector has been defined to simplify routing on the carrier board as much as possible. In many cases, a standard low-cost 4-layer PCB will be sufficient for the carrier board.

  Standard, ready-to-go carrier boards are suitable for low volume applications since the cost for developing a custom specific carrier board shall be amortized over the number of boards needed. If the number of boards is low, the per-board cost can be quite high.

The combination of an EACOM board and accompanying Carrier board is very much like a Single Board Computer (SBC), but more flexible. The carrier board can be a much better fit for each specific application than a standard SBC. Normal design updates are more likely to be on the carrier board, which is simpler to update than a complete SBC would be. Upgrading a design for more execution power or more memory is as easy as changing EACOM board, as opposed to redesigning an SBC.

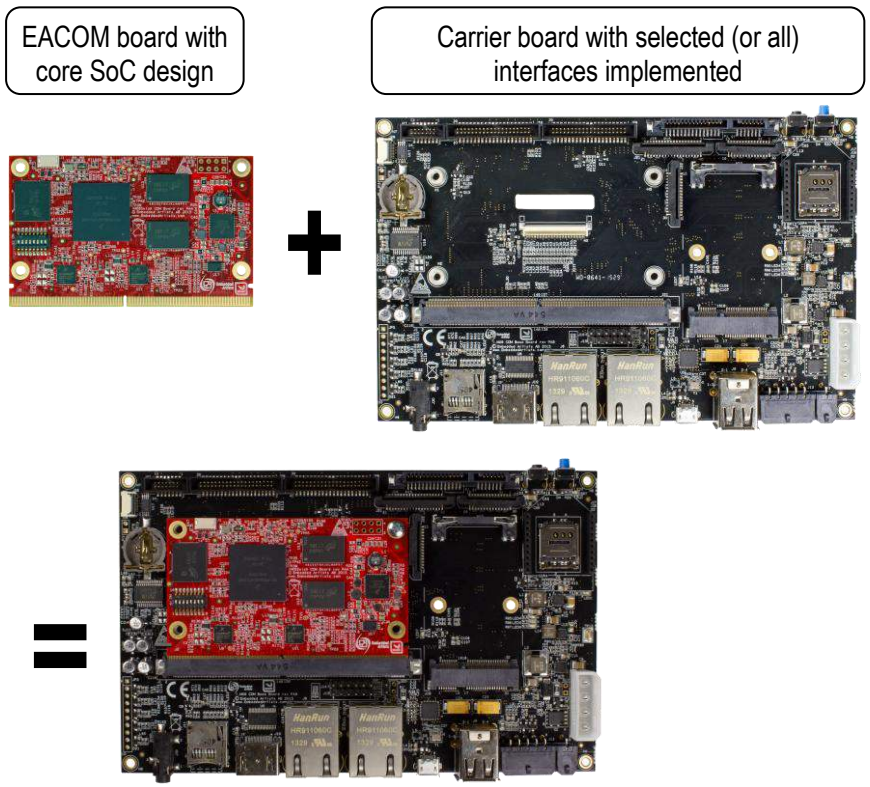


Figure 1 – COM Plus Carrier Board Equals SBC

3.1 EACOM Board Architecture

The block diagram in *Figure 2* below illustrates the typical components of an EACOM board:

- **SoC** - the main component , a member of the iMX6/7 family.
- **SDRAM** - a large memory array with 256 MByte - 4 GByte capacity. Typically DDR3L memories to get low power consumption, yet high density.
- **Parallel Flash** - for storing Operating System and boot loader images. Typically an eMMC memory but can also be an unmanaged FLASH memory.
- **Serial Flash** - for storing code for (possible) Cortex-M4 core or boot loader image.
- **Power Management** - typically in the form of a PMIC that supports low-power operation including DVFS (Dynamic Voltage and Frequency Scaling).
- **Debug interface** - for JTAG debugging.
- **Boot control** - for controlling the boot source.
- **Parameter storage** - for retrieving important parameters during boot, like memory bus calibration parameters and MAC address(es).
- **Edge connector** - edge pads conforming to the MXM3-standard with 314 positions.

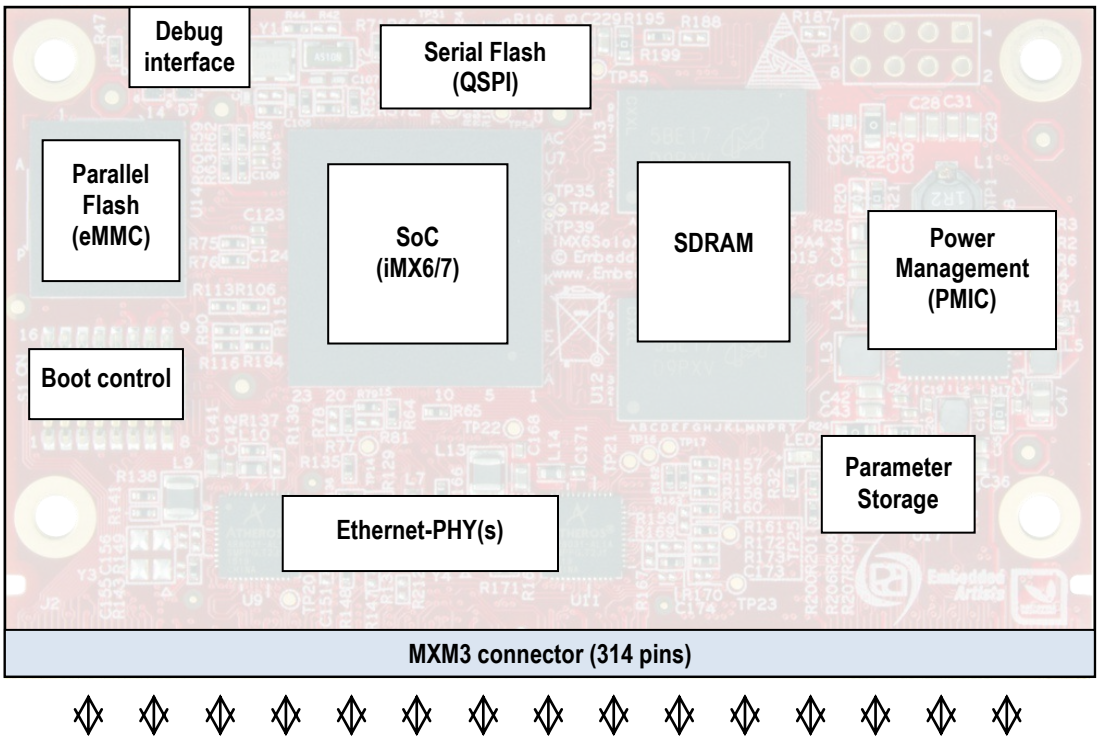


Figure 2 – COM Board Block Diagram

There are two types of interfaces to the EACOM boards:

- ***Standard Interfaces***
  The EACOM specification has defined a number of different interfaces and allocated positions for these interfaces on the MXM3 connector. These interfaces are reserved for their respective interface and will be the same on every EACOM board. Note that every EACOM board will assign signals to every interface whenever possible, but not necessarily all of them.

Some interfaces may for example not be present on some SoC, like PCIe, SATA and a second Ethernet interface. Some SoC's may not have enough pins to assign all interfaces. It is important to note that **to guarantee electrical compatibility between (carrier board) designs, only make use of the standard interfaces.**

- ***Type-specific Interfaces***
  A number of positions (39 to be specific) on the MXM3 connector have been left unassigned. Different EACOM boards can have different signals and interfaces assigned to these positions.
  Note that using these pins on a carrier board design may result in lost compatibility between EACOM boards, but not always. Details have to be checked in every specific case.

It can be limiting to only make use of the standard interfaces in the EACOM specification. If compatibility between EACOM boards is not a requirement then it is free to use every pin to whatever function the pin multiplexing allows.

3.2 Interface Overview

The table below lists the standard interfaces in the EACOM specification. Some interface are marked as *GPIO capable*. This means that the pins do not have any special voltage level or driver scheme, like for example the USB, Ethernet, PCIe, SATA and LVDS interfaces have. These interfaces have high-speed differential pin drivers that cannot function as a GPIO.

Interface	EACOM specification	Note
UART	3 ports	Two 4 wire and one 2 wire. GPIO capable.
SPI	2 ports	4 wire (SCLK, MOSI, MISO, SSEL). GPIO capable.
I2C	3 ports	GPIO capable.
SD/MMC	2 ports	One 4 databits and one 8 databits. GPIO capable.
Parallel LCD	24 databits, 4 ctrl	PIXCLK, HSYNC, VSYNC, DATA_ENABLE. GPIO capable.
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	1 PWM and 4 GPIO. GPIO capable.
LVDS LCD	2 ports	18/24 bit LVDS data.
HDMI (TDMS)		
Parallel Camera	8 databits, 4 ctrl	HSYNC, VSYNC, PCLK, MCLK. GPIO capable.
Serial Camera	CSI, 4 lane	
Gigabit Ethernet	2 ports	
PCIe	1 port, 1 lane	
SATA		
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	

SPDIF	1 TX/RX port	GPIO capable.
CAN	2 ports	GPIO capable.
I2S/SSI/AC97	1 port	4 wire synchronous plus MCLK. GPIO capable.
Analog audio	Stereo output	
GPIO	9 pins	
PWM	1 pin	GPIO capable.
ADC	8 inputs	
Power	10 VIN, VBAT and 47 GND	About 15% of the pins are ground pins.

There are also 39 pins that are not allocated to the standard interface, but rather left for the type-specific pins and interfaces.

3.3 Debug Interface / JTAG

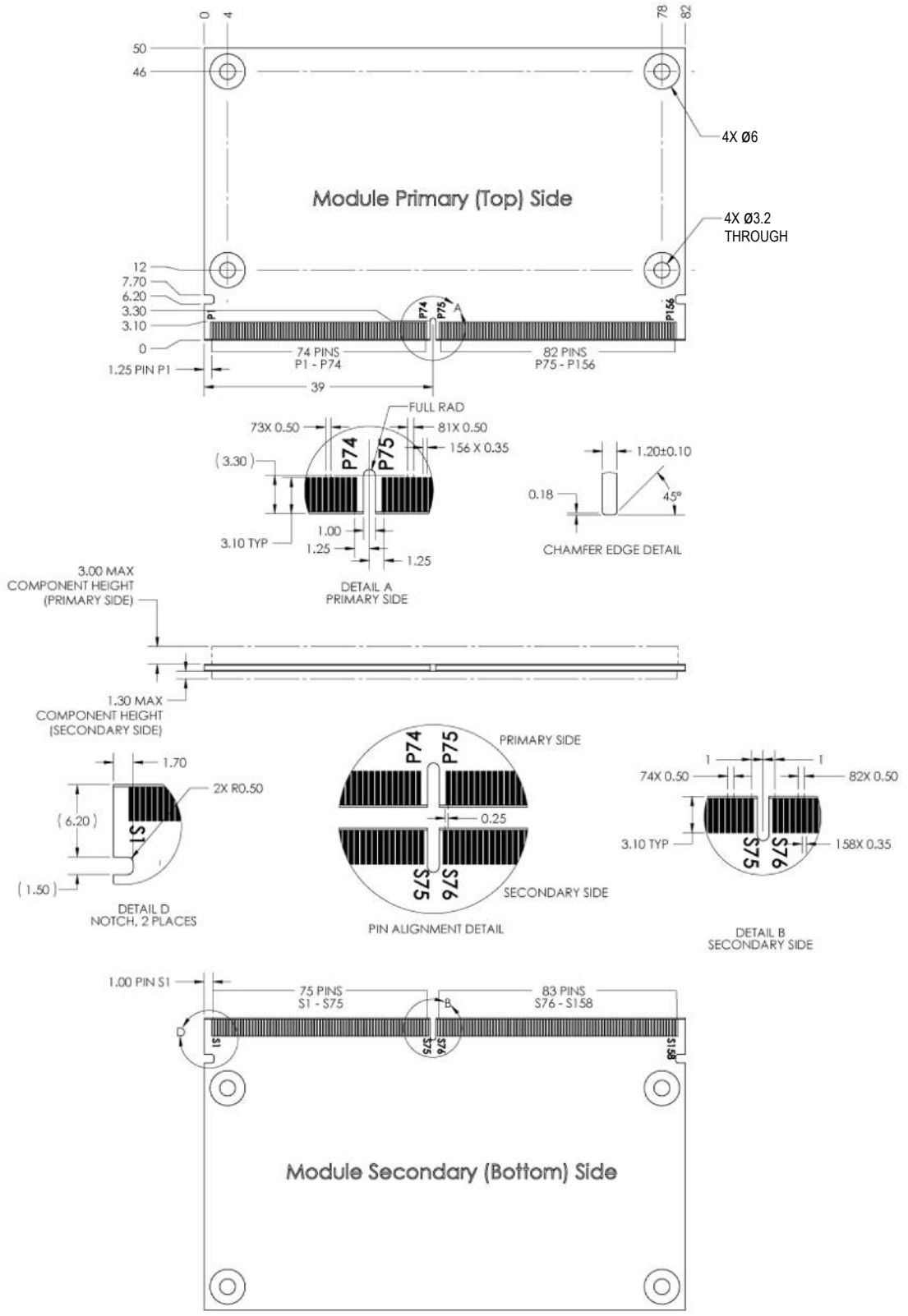
There is no debug interface (i.e., JTAG) signals allocated on the MXM3 edge connector. Instead such signals are available via an on-board connector (typically an FPC connector). The location of the debug connector and the exact type of connector are not dictated by EACOM specification.

4 Mechanical Specifications

The MXM3 connector dictates the mechanical form factor. The SMARC standard has also been an input. The EACOM boards are 82 mm wide and 50 mm high. Maximum component height on the top side is 3.0 mm and 1.3 mm on the bottom side. The MXM3 specification also dictated that pcb thickness is 1.2 mm. This results in a maximum thickness of the modules of 5.5 mm.

One single mechanical form factor is defined.

The picture below illustrates the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification. Note that the four mounting holes are 3.2 mm in diameter and this is not the same as the SMARC specification.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 3 – iMX6SoloX COM Board Mechanical Outline

4.1 EACOM Board Fixation

There are four 3.2 mm holes on the EACOM board, see mechanical drawing above.

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". It is recommended to select an MXM3 connector with 5 mm stacking height since there are standard SMTSO spacers with 5 mm height.

6-8 mm M3 screws are typically used.

Thermal management solutions, like heat spreaders, are also mounted and fixed via these four holes.

4.2 MXM3 Connector

EACOM boards have 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. The connector is originally defined for use with MXM3 graphics cards. The signal integrity is excellent and suitable for data rates up to 5 GHz. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE cannot be used since this specific connector lack some of the pins.

As an example, connector AS0B826-S78B from Foxconn has 5.0 mm board to board stacking height. This space allows some components to also be placed right under the EACOM board.

As a general rule, always check available component height before placing components on the carrier board under the EACOM board, see picture below.

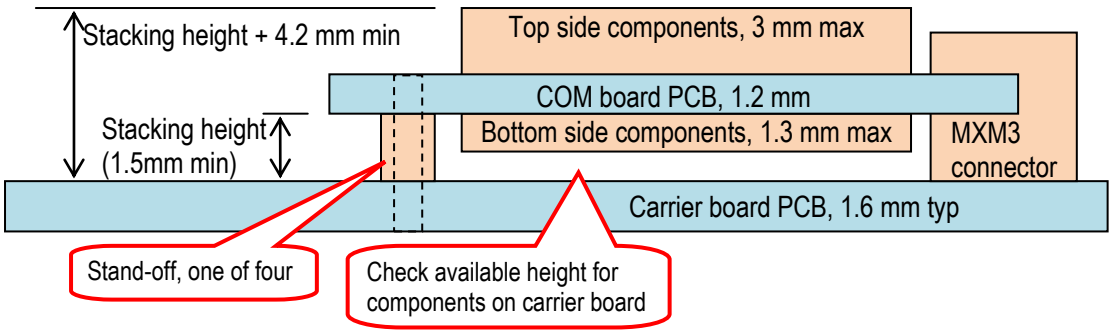


Figure 4 – EACOM Board Mounting in MXM3 Connector, Stacking Height

4.3 EACOM Pin Numbering

The figures below show the pin numbering for EACOM (the iMX6SoloX COM board is used as an example board in the pictures). Top (Primary) side edge fingers are numbered P1-P156. Bottom (Secondary) side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with odd numbers on the bottom and even numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying in the middle of the contact finger row.

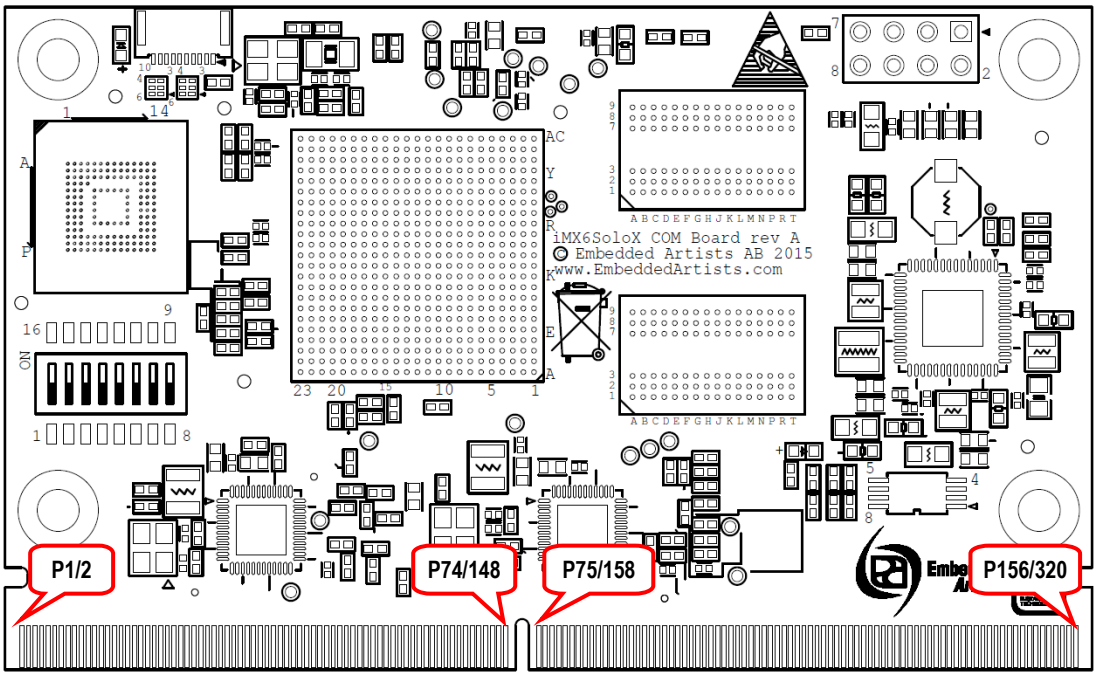


Figure 5 – EACOM Board Pin Numbering, Primary/Top Side

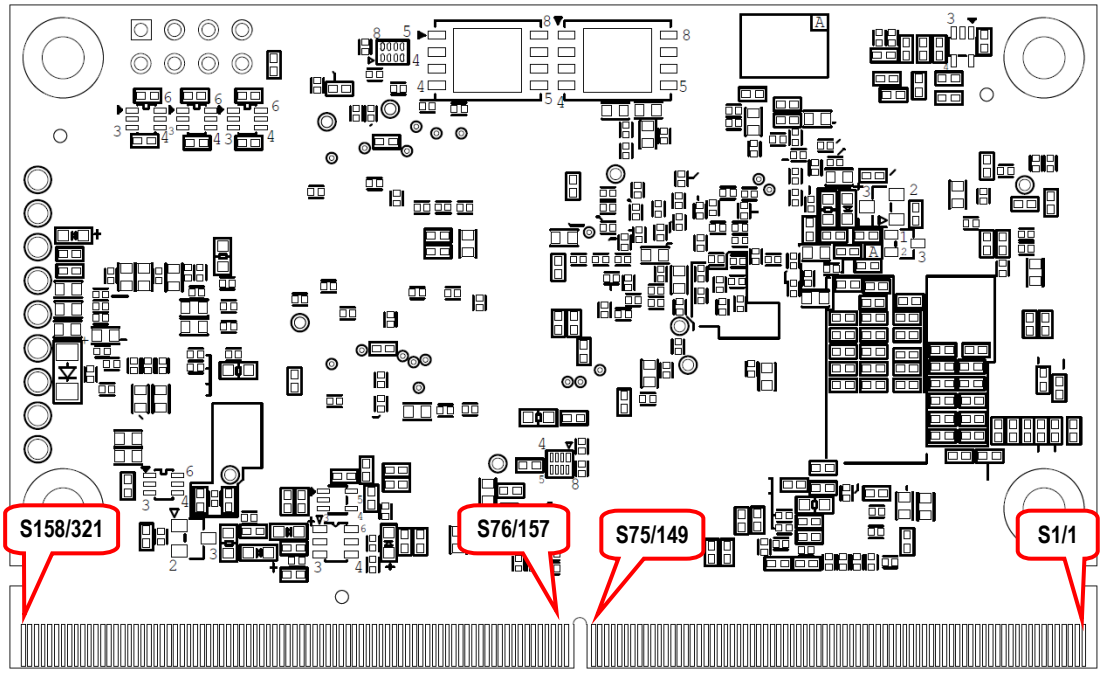


Figure 6 – EACOM Board Pin Numbering, Secondary/Bottom Side

5 Electrical Specification

5.1 Power Supplies

EACOM boards have a single main power supply input, VIN, with 3.3V nominal voltage. There is also an optional, low-current backup power supply input, VBAT, for Real Time Clock (RTC) support.

The EACOM board will power up and start normal operation once VIN is applied. VBAT is not needed for normal operation, but it is required for maintaining RTC operation. There can be other functions that rely on VBAT, like power on/off button control.

Each EACOM board will contain details about maximum current consumption and possible wider input voltage range but if the carrier board power supply is rated 3.3V +-5% / 3A it will be sufficient for all EACOM boards. Individual boards typically consumes considerable less than 3A in peak.

The *EACOM Carrier Board Design Guide* document gives recommendations about decoupling / bulk capacitance and ramp up times, etc.

5.2 Back Feed Protection

A typical SoC (and in particular the iMX6 family) requires back feed protection. No I/O pins should be externally driven before the EACOM board has powered up properly. If back feeding occurs it can prevent proper startup and also permanently damage the SoC.

EACOM board output signal PERI_PWR_EN is active high and signals when carrier board I/O signals are allowed to be driven. The signal typically controls carrier board power supplies but can also control transceivers and level shifters.

The *EACOM Carrier Board Design Guide* contains detailed information how to use the PERI_PWR_EN signal.

5.3 Voltage Domains

There are different voltage domains on the EACOM interfaces. VDD_IO is by far the most common and is the logic level that most interface signals use. VDD_IO is typically the same as VIN, but some EACOM boards allows VDD_IO to be lowered in order to save power.

Signal AIN_VREF is an output voltage level that reflect the upper range of the analog inputs (AINx) voltage range. The lower range is ground. Note that AIN_VREF voltage level can value. It is not a fixed voltage level. Converted analog values are relative to AIN_VREF.

5.4 VDD_SD

Signal VDD_SD is available to power the SD interface. Some EACOM boards supports dual voltage (1.8 / 3.3V) SD cards. The *EACOM Carrier Board Design Guide* contains detailed information how connect the signal.

Note that VDD_SD shall only be used to power the SD interface. Nothing else.

5.5 Reset Input / Output

EACOM boards have one RESET_IN signal and one RESET_OUT signal.

RESET_IN is active low. Pulling the signal low from the carrier board will trigger an internal reset on the EACOM board. There is no need to pull the signal high externally. The internal reset signal will generate an internal reset pulse that is active at least 100 ms, but it can be longer.

RESET_OUT is active low and reflect the EACOM board internal reset signal. It is an open drain output with a 1.5Kohm pull-up resistor to VIN.

5.6 Signal E2PROM_WP

Signal E2PROM_WP should be left unconnected or connected to GND. If signal is pulled low to ground, the parameter storage memory (I2C E2PROM) is write enabled and the iMX processor will power-up in USB OTG boot mode. This is normally only done during production.

Note that the content of the parameter storage memory (I2C E2PROM) should NEVER be altered. The parameters are written by Embedded Artists during production.

5.7 USB Interfaces

The EACOM interface specification contains two USB3.0 ports. Current iMX6/7 family members do not support USB3.0 but the interface feature has been included for future expansion.

USB3.0 interfaces are backward compatible with USB2.0 ports. The four new pins that have been added in USB3.0 (SSTXP/SSTXN and SSRXP/SSRXN) are just left unconnected.

Note that VBUS signals are inputs to EACOM boards, not outputs. Carrier boards must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces. It is not provided by the EACOM board.

6 Signal Allocation Specification

The table below present the signal allocation to the MXM3 edge connector on the primary/top side.

Top Side Pin Number	Pin Number MXM3	Signal Group	Signal Name	Signal Class	Voltage Domain
P1	2	GPIO	GPIO6	Bidirectional	VDD_IO
P2	4		GPIO5	Bidirectional	VDD_IO
P3	6		GPIO4	Bidirectional	VDD_IO
P4	8		GPIO3	Bidirectional	VDD_IO
P5	10	SD Interface	SD_D1	Bidirectional	VDD_SD
P6	12		SD_D0	Bidirectional	VDD_SD
P7	14		SD_CLK	Output	VDD_SD
P8	16		SD_CMD	Bidirectional	VDD_SD
P9	18		SD_D3	Bidirectional	VDD_SD
P10	20		SD_D2	Bidirectional	VDD_SD
P11	22		VCC_SD	Power	
P12	24	MMC Interface	MMC_D1	Bidirectional	VDD_IO
P13	26		MMC_D0	Bidirectional	VDD_IO
P14	28		MMC_D7	Bidirectional	VDD_IO
P15	30		MMC_D6	Bidirectional	VDD_IO
P16	32		MMC_CLK	Output	VDD_IO
P17	34		MMC_D5	Bidirectional	VDD_IO
P18	36		MMC_CMD	Bidirectional	VDD_IO
P19	38		MMC_D4	Bidirectional	VDD_IO
P20	40		MMC_D3	Bidirectional	VDD_IO
P21	42		MMC_D2	Bidirectional	VDD_IO
P22	44		GND	Power	
P23	46	HDMI	HDMI_TXC_N	Differential pair	
P24	48		HDMI_TXC_P	Differential pair	
P25	50		GND	Power	
P26	52		HDMI_TXD0_N	Differential pair	
P27	54		HDMI_TXD0_P	Differential pair	
P28	56		HDMI_HPD	Input	
P29	58		HDMI_TXD1_N	Differential pair	
P30	60		HDMI_TXD1_P	Differential pair	
P31	62		GND	Power	
P32	64		HDMI_TXD2_N	Differential pair	
P33	66		HDMI_TXD2_P	Differential pair	
P34	68		HDMI_CEC	Bidirectional	
P35	70		GND	Power	
P36	72	Gigabit Ethernet #1	ETH1_MD1_P	Differential pair	
P37	74		ETH1_MD1_N	Differential pair	
P38	76		GND	Power	
P39	78		ETH1_MD0_P	Differential pair	
P40	80		ETH1_MD0_N	Differential pair	
P41	82		ETH1_LINK1000	Output	VDD_IO
P42	84		ETH1_ACT	Output	VDD_IO
P43	86		ETH1_LINK	Output	VDD_IO
P44	88		ETH1_MD3_N	Differential pair	
P45	90		ETH1_MD3_P	Differential pair	
P46	92		GND	Power	
P47	94		ETH1_MD2_N	Differential pair	
P48	96		ETH1_MD2_P	Differential pair	
P49	98		GND	Power	
P50	100	Gigabit Ethernet #2	ETH2_MD1_P	Differential pair	
P51	102		ETH2_MD1_N	Differential pair	
P52	104		GND	Power	
P53	106		ETH2_MD0_P	Differential pair	
P54	108		ETH2_MD0_N	Differential pair	
P55	110		ETH2_LINK1000	Output	VDD_IO
P56	112		ETH2_ACT	Output	VDD_IO
P57	114		ETH2_LINK	Output	VDD_IO
P58	116		ETH2_MD3_N	Differential pair	
P59	118		ETH2_MD3_P	Differential pair	
P60	120		GND	Power	
P61	122		ETH2_MD2_N	Differential pair	
P62	124		ETH2_MD2_P	Differential pair	

P63	126		GND	Power	
P64	128	USB OTG #1	USB_O1_DN	Differential pair	
P65	130		USB_O1_DP	Differential pair	
P66	132		USB_O1_OTG_ID	Input	VDD_IO
P67	134		USB_O1_SSTXN	Differential pair	
P68	136		USB_O1_SSTXP	Differential pair	
P69	138		GND	Power	
P70	140		USB_O1_SSRXN	Differential pair	
P71	142		USB_O1_SSRXP	Differential pair	
P72	144		USB_O1_VBUS	Input	
P73	146		USB_O1_PWR_EN	Output	VDD_IO
P74	148		USB_O1_OC	Input	VDD_IO
	150	Key in MXM3 edge pads	Non existing pin		
	152		Non existing pin		
	154		Non existing pin		
	156		Non existing pin		
P75	158	USB Host #1	USB_H1_PWR_EN	Output	VDD_IO
P76	160		USB_H1_OC	Input	VDD_IO
P77	162		GND	Power	
P78	164		USB_H1_DN	Differential pair	
P79	166		USB_H1_DP	Differential pair	
P80	168		USB_H1_SSTXN	Differential pair	
P81	170		USB_H1_SSTXP	Differential pair	
P82	172		GND	Power	
P83	174		USB_H1_SSRXN	Differential pair	
P84	176		USB_H1_SSRXP	Differential pair	
P85	178		USB_H1_VBUS	Input	
P86	180	USB Host #2	USB_H2_PWR_EN	Output	VDD_IO
P87	182		USB_H2_OC	Input	VDD_IO
P88	184		GND	Power	
P89	186		USB_H2_DN	Differential pair	
P90	188		USB_H2_DP	Differential pair	
P91	190		GND	Power	
P92	192	COM board specific	COM board specific		
P93	194		COM board specific		
P94	196		COM board specific		
P95	198		COM board specific		
P96	200		COM board specific		
P97	202		COM board specific		
P98	204		COM board specific		
P99	206		COM board specific		
P100	208		COM board specific		
P101	210		COM board specific		
P102	212		COM board specific		
P103	214		COM board specific		
P104	216		COM board specific		
P105	218		COM board specific		
P106	220		COM board specific		
P107	222		COM board specific		
P108	224		COM board specific		
P109	226		COM board specific		
P110	228		COM board specific		
P111	230		COM board specific		
P112	232		COM board specific		
P113	234		COM board specific		
P114	236		COM board specific		
P115	238		COM board specific		
P116	240		COM board specific		
P117	242		COM board specific		
P118	244	SPI-B	GND	Power	
P119	246		SPI-B_SSEL	Output	VDD_IO
P120	248		SPI-B_MOSI	Output	VDD_IO
P121	250		SPI-B_MISO	Input	VDD_IO
P122	252		SPI-B_CLK	Output	VDD_IO
P123	254	SPI-A	SPI-A_SSEL	Output	VDD_IO
P124	256		SPI-A_MOSI	Output	VDD_IO
P125	258		SPI-A_MISO	Input	VDD_IO
P126	260		SPI-A_CLK	Output	VDD_IO
P127	262		GND	Power	
P128	264	UART-C	UART-C_RXD	Input	VDD_IO
P129	266		UART-C_TXD	Output	VDD_IO

P130	268	UART-B	UART-B_RXD	Input	VDD_IO
P131	270		UART-B_CTS	Input	VDD_IO
P132	272		UART-B_RTS	Output	VDD_IO
P133	274		UART-B_TXD	Output	VDD_IO
P134	276	UART-A	UART-A_RXD	Input	VDD_IO
P135	278		UART-A_CTS	Input	VDD_IO
P136	280		UART-A_RTS	Output	VDD_IO
P137	282		UART-A_TXD	Output	VDD_IO
P138	284	PWM	PWM	Output	VDD_IO
P139	286	GPIO	GPIO2	Bidirectional	VDD_IO
P140	288		GPIO1	Bidirectional	VDD_IO
P141	290	System Control	PERI_PWR_EN	Output	VDD_IO
P142	292		RESET_IN	Input	VDD_IO
P143	294		RESET_OUT	Output, open drain	VDD_IO
P144	96		GND	Power	
P145	298	Backup Power Supp.	VBAT	Power	
P146	300	System Control	E2PROM_WP	Input	VDD_IO
P147	302	Main Power Supply Input	VIN	Power	
P148	304		VIN	Power	
P149	306		VIN	Power	
P150	308		VIN	Power	
P151	310		VIN	Power	
P152	312		VIN	Power	
P153	314		VIN	Power	
P154	316		VIN	Power	
P155	318		VIN	Power	
P156	320		VIN	Power	

The table below present the signal allocation to the MXM3 edge connector on the secondary/bottom side.

Bottom Side Pin Number	Pin Number MXM3	Signal Group	Signal Name	Signal Class	Voltage Domain
S1	1	AUDIO MQS	MQS_RIGHT	Output	VDD_IO
S2	3		MQS_LEFT	Output	VDD_IO
S3	5		GND	Power	
S4	7	AUDIO I2S	AUDIO_TXFS	Output	VDD_IO
S5	9		AUDIO_RXD	Input	VDD_IO
S6	11		AUDIO_TXC	Output	VDD_IO
S7	13		AUDIO_TXD	Output	VDD_IO
S8	15		AUDIO_MCLK	Output	VDD_IO
S9	17		GND	Power	
S10	19	SPDIF	SPDIF_IN	Input	VDD_IO
S11	21		SPDIF_OUT	Output	VDD_IO
S12	23	CAN #2	CAN2_TX	Output	VDD_IO
S13	25		CAN2_RX	Input	VDD_IO
S14	27	CAN #1	CAN1_TX	Output	VDD_IO
S15	29		CAN1_RX	Input	VDD_IO
S16	31	LVDS #1	GND	Power	
S17	33		LVDS1_D3_P	Differential pair	
S18	35		LVDS1_D3_N	Differential pair	
S19	37		GPIO	Bidirectional	VDD_IO
S20	39		LVDS1_D2_P	Differential pair	
S21	41		LVDS1_D2_N	Differential pair	
S22	43		GND	Power	
S23	45		LVDS1_D1_P	Differential pair	
S24	47		LVDS1_D1_N	Differential pair	
S25	49		GND	Power	
S26	51		LVDS1_D0_P	Differential pair	
S27	53		LVDS1_D0_N	Differential pair	
S28	55		GND	Power	
S29	57		LVDS1_CLK_P	Differential pair	
S30	59		LVDS1_CLK_N	Differential pair	
S31	61	LVDS #0	GND	Power	
S32	63		LVDS0_D3_P	Differential pair	
S33	65		LVDS0_D3_N	Differential pair	
S34	67		GPIO	Bidirectional	VDD_IO
S35	69		LVDS0_D2_P	Differential pair	
S36	71		LVDS0_D2_N	Differential pair	
S37	73		GND	Power	
S38	75		LVDS0_D1_P	Differential pair	
S39	77		LVDS0_D1_N	Differential pair	
S40	79		GND	Power	
S41	81		LVDS0_D0_P	Differential pair	
S42	83		LVDS0_D0_N	Differential pair	
S43	85		GND	Power	
S44	87		LVDS0_CLK_P	Differential pair	
S45	89		LVDS0_CLK_N	Differential pair	
S46	91	I2C-A	I2C-A_SDA	Bidirectional	VDD_IO
S47	93		I2C-A_SCL	Output	VDD_IO
S48	95	I2C-B	I2C-B_SDA	Bidirectional	VDD_IO
S49	97		I2C-B_SCL	Output	VDD_IO
S50	99	HDMI / I2C-C	HDMI/I2C-C_SDA	Bidirectional	VDD_IO
S51	101		HDMI/I2C-C_SCL	Output	VDD_IO
S52	103	Display Control	TP_RST	Output	VDD_IO
S53	105		TP_IRQ	Input	VDD_IO
S54	107		DISP_PWR_EN	Output	VDD_IO
S55	109		BL_PWR_EN	Output	VDD_IO
S56	111		BL_PWM	Output	VDD_IO
S57	113	LCD	GND	Power	
S58	115		LCD_R0	Output	VDD_IO
S59	117		LCD_R1	Output	VDD_IO
S60	119		LCD_R2	Output	VDD_IO
S61	121		LCD_R3	Output	VDD_IO
S62	123		LCD_R4	Output	VDD_IO
S63	125		LCD_R5	Output	VDD_IO
S64	127		LCD_R6	Output	VDD_IO
S65	129		LCD_R7	Output	VDD_IO

S66	**131**		LCD_G0	Output	VDD_IO
S67	**133**		LCD_G1	Output	VDD_IO
S68	**135**		LCD_G2	Output	VDD_IO
S69	**137**		LCD_G3	Output	VDD_IO
S70	**139**		LCD_G4	Output	VDD_IO
S71	**141**		LCD_G5	Output	VDD_IO
S72	**143**		LCD_G6	Output	VDD_IO
S73	**145**		LCD_G7	Output	VDD_IO
S74	**147**		GND	Power	
S75	**149**		LCD_B0	Output	VDD_IO
	151	Key in MXM3 edge pads	Non existing pin		
	153		Non existing pin		
	155		Non existing pin		
S76	**157**	LCD cont.	LCD_B1	Output	VDD_IO
S77	**159**		LCD_B2	Output	VDD_IO
S78	**161**		LCD_B3	Output	VDD_IO
S79	**163**		LCD_B4	Output	VDD_IO
S80	**165**		LCD_B5	Output	VDD_IO
S81	**167**		LCD_B6	Output	VDD_IO
S82	**169**		LCD_B7	Output	VDD_IO
S83	**171**		LCD_CLK	Output	VDD_IO
S84	**173**		GPIO7	Bidirectional	VDD_IO
S85	**175**		LCD_HSYNC	Output	VDD_IO
S86	**177**		LCD_VSYNC	Output	VDD_IO
S87	**179**		LCD_ENABLE	Output	VDD_IO
S88	**181**	ADC	GND	Power	
S89	**183**		AIN_VREF	Analog output	
S90	**185**		AIN7	Analog input	AIN_VREF
S91	**187**		AIN6	Analog input	AIN_VREF
S92	**189**		AIN5	Analog input	AIN_VREF
S93	**191**		AIN4	Analog input	AIN_VREF
S94	**193**		AIN3	Analog input	AIN_VREF
S95	**195**		AIN2	Analog input	AIN_VREF
S96	**197**		AIN1	Analog input	AIN_VREF
S97	**199**		AIN0	Analog input	AIN_VREF
S98	**201**	COM board specific	GND	Power	
S99	**203**		COM board specific	Differential pair	
S100	**205**		COM board specific	Differential pair	
S101	**207**		GND	Power	
S102	**209**		COM board specific	Differential pair	
S103	**211**		COM board specific	Differential pair	
S104	**213**		GND	Power	
S105	**215**		COM board specific		
S106	**217**		COM board specific		
S107	**219**		COM board specific		
S108	**221**		COM board specific		
S109	**223**		COM board specific		
S110	**225**		COM board specific		
S111	**227**		COM board specific		
S112	**229**		COM board specific		
S113	**231**		COM board specific		
S114	**233**	Parallel Camera	CSI_HSYNC	Input	VDD_IO
S115	**235**		CSI_VSYNC	Input	VDD_IO
S116	**237**		CSI_MCLK	Output	VDD_IO
S117	**239**		CSI_PCLK	Input	VDD_IO
S118	**241**		GND	Power	
S119	**243**		CSI_D0	Input	VDD_IO
S120	**245**		CSI_D1	Input	VDD_IO
S121	**247**		CSI_D2	Input	VDD_IO
S122	**249**		CSI_D3	Input	VDD_IO
S123	**251**		CSI_D4	Input	VDD_IO
S124	**253**		CSI_D5	Input	VDD_IO
S125	**255**		CSI_D6	Input	VDD_IO
S126	**257**		CSI_D7	Input	VDD_IO
S127	**259**	Serial Camera (CSI/MIPI)	GND	Power	
S128	**261**		CSI_D3_M	Differential pair	
S129	**263**		CSI_D3_P	Differential pair	
S130	**265**		GND	Power	
S131	**267**		CSI_D2_M	Differential pair	
S132	**269**		CSI_D2_P	Differential pair	
S133	**271**		GND	Power	

S134	**273**		CSI_D1_M	Differential pair	
S135	**275**		CSI_D1_P	Differential pair	
S136	**277**		GND	Power	
S137	**279**		CSI_D0_M	Differential pair	
S138	**281**		CSI_D0_P	Differential pair	
S139	**283**		GND	Power	
S140	**285**		CSI_CLK_M	Differential pair	
S141	**287**		CSI_CLK_P	Differential pair	
S142	**289**	SATA	GND	Power	
S143	**291**		SATA_TX_P	Differential pair	
S144	**293**		SATA_TX_N	Differential pair	
S145	**295**		GND	Power	
S146	**297**		SATA_RX_N	Differential pair	
S147	**299**		SATA_RX_P	Differential pair	
S148	**301**		GND	Power	
S149	**303**	PCIe	GND	Power	
S150	**305**		PCIE_CLK_P	Differential pair	
S151	**307**		PCIE_CLK_N	Differential pair	
S152	**309**		GND	Power	
S153	**311**		PCIE_TX_P	Differential pair	
S154	**313**		PCIE_TX_N	Differential pair	
S155	**315**		GND	Power	
S156	**317**		PCIE_RX_P	Differential pair	
S157	**319**		PCIE_RX_N	Differential pair	
S158	**321**		GND	Power	

The table below lists the two board sides in the same table.

Signal Group	Signal Name	Top Side Pin Number	Pin Number MXM3		Bottom Side Pin Number	Signal Name	Signal Group
GPIO	GPIO6	P1	2	**1**	**S1**	MQS_RIGHT	AUDIO MQS
	GPIO5	P2	4	**3**	**S2**	MQS_LEFT	
	GPIO4	P3	6	**5**	**S3**	GND	
	GPIO3	P4	8	**7**	**S4**	AUDIO_TXFS	AUDIO I2S
SD Interface	SD_D1	P5	10	**9**	**S5**	AUDIO_RXD	
	SD_D0	P6	12	**11**	**S6**	AUDIO_TXC	
	SD_CLK	P7	14	**13**	**S7**	AUDIO_TXD	
	SD_CMD	P8	16	**15**	**S8**	AUDIO_MCLK	
	SD_D3	P9	18	**17**	**S9**	GND	
	SD_D2	P10	20	**19**	**S10**	SPDIF_IN	SPDIF
	SD_VCC	P11	22	**21**	**S11**	SPDIF_OUT	
MMC Interface	MMC_D1	P12	24	**23**	**S12**	CAN2_TX	CAN #2
	MMC_D0	P13	26	**25**	**S13**	CAN2_RX	
	MMC_D7	P14	28	**27**	**S14**	CAN1_TX	CAN #1
	MMC_D6	P15	30	**29**	**S15**	CAN1_RX	
	MMC_CLK	P16	32	**31**	**S16**	GND	LVDS #1
	MMC_D5	P17	34	**33**	**S17**	LVDS1_D3_P	
	MMC_CMD	P18	36	**35**	**S18**	LVDS1_D3_N	
	MMC_D4	P19	38	**37**	**S19**	GPIO	
	MMC_D3	P20	40	**39**	**S20**	LVDS1_D2_P	
	MMC_D2	P21	42	**41**	**S21**	LVDS1_D2_N	
	GND	P22	44	**43**	**S22**	GND	
HDMI	HDMI_TXC_N	P23	46	**45**	**S23**	LVDS1_D1_P	
	HDMI_TXC_P	P24	48	**47**	**S24**	LVDS1_D1_N	
	GND	P25	50	**49**	**S25**	GND	
	HDMI_TXD0_N	P26	52	**51**	**S26**	LVDS1_D0_P	
	HDMI_TXD0_P	P27	54	**53**	**S27**	LVDS1_D0_N	
	HDMI_HPD	P28	56	**55**	**S28**	GND	
	HDMI_TXD1_N	P29	58	**57**	**S29**	LVDS1_CLK_P	
	HDMI_TXD1_P	P30	60	**59**	**S30**	LVDS1_CLK_N	
	GND	P31	62	**61**	**S31**	GND	LVDS #0
	HDMI_TXD2_N	P32	64	**63**	**S32**	LVDS0_D3_P	
	HDMI_TXD2_P	P33	66	**65**	**S33**	LVDS0_D3_N	
	HDMI_CEC	P34	68	**67**	**S34**	GPIO	
	GND	P35	70	**69**	**S35**	LVDS0_D2_P	
Gigabit Ethernet #1	ETH1_MD1_P	P36	72	**71**	**S36**	LVDS0_D2_N	
	ETH1_MD1_N	P37	74	**73**	**S37**	GND	
	GND	P38	76	**75**	**S38**	LVDS0_D1_P	
	ETH1_MD0_P	P39	78	**77**	**S39**	LVDS0_D1_N	
	ETH1_MD0_N	P40	80	**79**	**S40**	GND	
	ETH1_LINK1000	P41	82	**81**	**S41**	LVDS0_D0_P	
	ETH1_ACT	P42	84	**83**	**S42**	LVDS0_D0_N	
	ETH1_LINK	P43	86	**85**	**S43**	GND	
	ETH1_MD3_N	P44	88	**87**	**S44**	LVDS0_CLK_P	
	ETH1_MD3_P	P45	90	**89**	**S45**	LVDS0_CLK_N	
	GND	P46	92	**91**	**S46**	I2C-A_SDA	I2C-A
	ETH1_MD2_N	P47	94	**93**	**S47**	I2C-A_SCL	
	ETH1_MD2_P	P48	96	**95**	**S48**	I2C-B_SDA	I2C-B
	GND	P49	98	**97**	**S49**	I2C-B_SCL	
Gigabit Ethernet #2	ETH2_MD1_P	P50	100	**99**	**S50**	HDMI/I2C-C_SDA	HDMI / I2C-C
	ETH2_MD1_N	P51	102	**101**	**S51**	HDMI/I2C-C_SCL	
	GND	P52	104	**103**	**S52**	TP_RST	Display Control
	ETH2_MD0_P	P53	106	**105**	**S53**	TP_IRQ	
	ETH2_MD0_N	P54	108	**107**	**S54**	DISP_PWR_EN	
	ETH2_LINK1000	P55	110	**109**	**S55**	BL_PWR_EN	
	ETH2_ACT	P56	112	**111**	**S56**	BL_PWM	
	ETH2_LINK	P57	114	**113**	**S57**	GND	LCD
	ETH2_MD3_N	P58	116	**115**	**S58**	LCD_R0	
	ETH2_MD3_P	P59	118	**117**	**S59**	LCD_R1	
	GND	P60	120	**119**	**S60**	LCD_R2	
	ETH2_MD2_N	P61	122	**121**	**S61**	LCD_R3	
	ETH2_MD2_P	P62	124	**123**	**S62**	LCD_R4	
	GND	P63	126	**125**	**S63**	LCD_R5	
USB OTG #1	USB_O1_DN	P64	128	**127**	**S64**	LCD_R6	
	USB_O1_DP	P65	130	**129**	**S65**	LCD_R7	
	USB_O1_OTG_ID	P66	132	**131**	**S66**	LCD_G0	

	USB_O1_SSTXN	P67	134	**133**	**S67**	LCD_G1	
	USB_O1_SSTXP	P68	136	**135**	**S68**	LCD_G2	
	GND	P69	138	**137**	**S69**	LCD_G3	
	USB_O1_SSRXN	P70	140	**139**	**S70**	LCD_G4	
	USB_O1_SSRXP	P71	142	**141**	**S71**	LCD_G5	
	USB_O1_VBUS	P72	144	**143**	**S72**	LCD_G6	
	USB_O1_PWR_EN	P73	146	**145**	**S73**	LCD_G7	
	USB_O1_OC	P74	148	**147**	**S74**	GND	
	Non existing pin		150	**149**	**S75**	LCD_B0	
	Non existing pin		152	**151**		Non existing pin	
	Non existing pin		154	**153**		Non existing pin	
	Non existing pin		156	**155**		Non existing pin	
USB Host #1	USB_H1_PWR_EN	P75	158	**157**	**S76**	LCD_B1	
	USB_H1_OC	P76	160	**159**	**S77**	LCD_B2	
	GND	P77	162	**161**	**S78**	LCD_B3	
	USB_H1_DN	P78	164	**163**	**S79**	LCD_B4	
	USB_H1_DP	P79	166	**165**	**S80**	LCD_B5	
	USB_H1_SSTXN	P80	168	**167**	**S81**	LCD_B6	
	USB_H1_SSTXP	P81	170	**169**	**S82**	LCD_B7	
	GND	P82	172	**171**	**S83**	LCD_CLK	
	USB_H1_SSRXN	P83	174	**173**	**S84**	GPIO7	
	USB_H1_SSRXP	P84	176	**175**	**S85**	LCD_HSYNC	
	USB_H1_VBUS	P85	178	**177**	**S86**	LCD_VSYNC	
USB Host #2	USB_H2_PWR_EN	P86	180	**179**	**S87**	LCD_ENABLE	
	USB_H2_OC	P87	182	**181**	**S88**	GND	ADC
	GND	P88	184	**183**	**S89**	AIN_VREF	
	USB_H2_DN	P89	186	**185**	**S90**	AIN7	
	USB_H2_DP	P90	188	**187**	**S91**	AIN6	
	GND	P91	190	**189**	**S92**	AIN5	
COM board specific	COM board specific	P92	192	**191**	**S93**	AIN4	
	COM board specific	P93	194	**193**	**S94**	AIN3	
	COM board specific	P94	196	**195**	**S95**	AIN2	
	COM board specific	P95	198	**197**	**S96**	AIN1	
	COM board specific	P96	200	**199**	**S97**	AIN0	
	COM board specific	P97	202	**201**	**S98**	GND	COM board specific
	COM board specific	P98	204	**203**	**S99**	COM board specific	
	COM board specific	P99	206	**205**	**S100**	COM board specific	
	COM board specific	P100	208	**207**	**S101**	GND	
	COM board specific	P101	210	**209**	**S102**	COM board specific	
	COM board specific	P102	212	**211**	**S103**	COM board specific	
	COM board specific	P103	214	**213**	**S104**	GND	
	COM board specific	P104	216	**215**	**S105**	COM board specific	
	COM board specific	P105	218	**217**	**S106**	COM board specific	
	COM board specific	P106	220	**219**	**S107**	COM board specific	
	COM board specific	P107	222	**221**	**S108**	COM board specific	
	COM board specific	P108	224	**223**	**S109**	COM board specific	
	COM board specific	P109	226	**225**	**S110**	COM board specific	
	COM board specific	P110	228	**227**	**S111**	COM board specific	
	COM board specific	P111	230	**229**	**S112**	COM board specific	
	COM board specific	P112	232	**231**	**S113**	COM board specific	
	COM board specific	P113	234	**233**	**S114**	CSI_HSYNC	Parallel Camera
	COM board specific	P114	236	**235**	**S115**	CSI_VSYNC	
	COM board specific	P115	238	**237**	**S116**	CSI_MCLK	
	COM board specific	P116	240	**239**	**S117**	CSI_PCLK	
	COM board specific	P117	242	**241**	**S118**	GND	
SPI-B	GND	P118	244	**243**	**S119**	CSI_D0	
	SPI-B_SSEL	P119	246	**245**	**S120**	CSI_D1	
	SPI-B_MOSI	P120	248	**247**	**S121**	CSI_D2	
	SPI-B_MISO	P121	250	**249**	**S122**	CSI_D3	
	SPI-B_CLK	P122	252	**251**	**S123**	CSI_D4	
SPI-A	SPI-A_SSEL	P123	254	**253**	**S124**	CSI_D5	
	SPI-A_MOSI	P124	256	**255**	**S125**	CSI_D6	
	SPI-A_MISO	P125	258	**257**	**S126**	CSI_D7	
	SPI-A_CLK	P126	260	**259**	**S127**	GND	Serial Camera (CSI/MIPI)
	GND	P127	262	**261**	**S128**	CSI_D3_M	
UART-C	UART-C_RXD	P128	264	**263**	**S129**	CSI_D3_P	
	UART-C_TXD	P129	266	**265**	**S130**	GND	
UART-B	UART-B_RXD	P130	268	**267**	**S131**	CSI_D2_M	
	UART-B_CTS	P131	270	**269**	**S132**	CSI_D2_P	
	UART-B_RTS	P132	272	**271**	**S133**	GND	
	UART-B_TXD	P133	274	**273**	**S134**	CSI_D1_M	

UART-A	UART-A_RXD	P134	276	**275**	**S135**	CSI_D1_P	
	UART-A_CTS	P135	278	**277**	**S136**	GND	
	UART-A_RTS	P136	280	**279**	**S137**	CSI_D0_M	
	UART-A_TXD	P137	282	**281**	**S138**	CSI_D0_P	
PWM	PWM	P138	284	**283**	**S139**	GND	
GPIO	GPIO2	P139	286	**285**	**S140**	CSI_CLK_M	
	GPIO1	P140	288	**287**	**S141**	CSI_CLK_P	
System Control	PERI_PWR_EN	P141	290	**289**	**S142**	GND	
	RESET_IN	P142	292	**291**	**S143**	SATA_TX_P	
	RESET_OUT	P143	294	**293**	**S144**	SATA_TX_N	
	GND	P144	96	**295**	**S145**	GND	SATA
	VBAT	P145	298	**297**	**S146**	SATA_RX_N	
	E2PROM_WP	P146	300	**299**	**S147**	SATA_RX_P	
Power Supply Input	VIN	P147	302	**301**	**S148**	GND	
	VIN	P148	304	**303**	**S149**	GND	
	VIN	P149	306	**305**	**S150**	PCIE_CLK_P	
	VIN	P150	308	**307**	**S151**	PCIE_CLK_N	
	VIN	P151	310	**309**	**S152**	GND	
	VIN	P152	312	**311**	**S153**	PCIE_TX_P	PCIe
	VIN	P153	314	**313**	**S154**	PCIE_TX_N	
	VIN	P154	316	**315**	**S155**	GND	
	VIN	P155	318	**317**	**S156**	PCIE_RX_P	
	VIN	P156	320	**319**	**S157**	PCIE_RX_N	
				321	**S158**	GND	

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