EACOM Board - Specification

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EACOM Board Specification Version 1.0





Embedded Artists AB

Davidshallsgatan 16 211 45 Malmö Sweden

http://www.EmbeddedArtists.com

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Revision	Date	Description
PA1	2015-10-08	First version.
PA2	2015-11-02	Minor clarifications and corrections.
PA3	2016-05-16	Minor corrections. Changed UART, SPI and I2C channels to alphanumerical numbering.

This document describes the specification of Embedded Artists' Computer-on-Modules (COM) Boards, hereafter referred to as *EACOM*. Mechanical dimensions, interface groups, powering and pin assignments are defined.

The EACOM specification has been created to address a number of issues with embedded systems development. Some of the issues are generically addressed by COM boards, and some are specifically addressed by the EACOM specification:

- Manage complexity modern high-performance and power efficient ARM cores with highspeed interfaces are complex to design. Much of the complexity is encapsulated in the COM boards, reducing the design effort to integrate advanced ARM application processors. The EACOM specification, together with the *Carrier Board Design Guide* document reduce the integration effort even further. EACOM pinning has been defined to simplify carrier board routing. In many cases, a standard low-cost 4-layer PCB will be sufficient for the carrier board.
- Flexibility and upgrade path different EACOM boards gives different price/performance ratios and feature sets. Designers can select different EACOM boards based on needs, while still maintaining the same carrier board design. Designs tend to grow over the product lifetime and require more performance, memory and/or other features later on. Having higher-performing EACOM boards to select from makes upgrade a simpler process.
- COM boards are proven designs, allowing available engineering resources to focus on value adding features rather than spending time on infrastructure. The design effort saved is not only on hardware but also on software BSP design. All in all, EACOM boards reduce development risk and shorten time to market.
- The EACOM specification is based on a **proven**, **robust mechanical form factor** and associated (MXM3) connector. There are **ready-to-go thermal management solutions**, like heat spreader and heat sink.
- And last the obvious question; Why not the SMARC standard? Based on over 15 years in business and countless designs, Embedded Artists recommends another path for our customers. The SMARC standard has several great features and these have been preserved by the EACOM specification. Other features have changed.
 - SMARC pinning is not particularly well suited for the iMX6/7 family. Most SMARC boards either discard a lot of SoC pins (leave them unconnected) or has additional (non-standard) connectors on the boards to make all signals available - making the boards non-standard.
 - SMARC boards are only (reasonable) interchangeable if the SMARC-defined interfaces are used. In reality it is not a trivial task to switch SMARC boards from completely different suppliers and/or SoC families.
 - EACOM pinning focus on the iMX6/7 SoC family, where it is an ideal fit. All relevant pins are available on the main edge (MXM3) pads. The specification does not claim to be universally applicable.
 - EACOM has 3.3V preferred I/O voltage for most pins. SMARC has 1.8V as preferred I/O voltage, which can lead to several voltage translators on the carrier board.

3 Computer-on-Module Overview

This chapter give a general overview of the board architecture, interfaces and pinning.

An EACOM based system solution has the following overall physical structure:

- **EACOM board**, containing the core design that encapsulate a lot of the complexity of a modern, high-performance ARM SoC design.
- Carrier board that implements the needed interfaces in the specific solution. The carrier board also typically contains the powering solution and creates the mechanical entity that shall be mounted in box, or similar. The carrier board is typically a simpler design (i.e., less complex) than the EACOM board. Either the carrier board is a custom specific design or a standard, ready-to-go carrier board design. For custom specific designs, there is design support to minimize the design effort:
 - EACOM Carrier Board Design Guide document that contains many guidelines for implementing the many interfaces.
 - Pin assignment on the MXM3 connector has been defined to simplify routing on the carrier board as much as possible. In many cases, a standard low-cost 4-layer PCB will be sufficient for the carrier board.

Standard, ready-to-go carrier boards are suitable for low volume applications since the cost for developing a custom specific carrier board shall be amortized over the number of boards needed. If the number of boards is low, the per-board cost can be quite high.

The combination of an EACOM board and accompanying Carrier board is very much like a Single Board Computer (SBC), but more flexible. The carrier board can be a much better fit for each specific application than a standard SBC. Normal design updates are more likely to be on the carrier board, which is simpler to update than a complete SBC would be. Upgrading a design for more execution power or more memory is as easy as changing EACOM board, as opposed to redesigning an SBC.

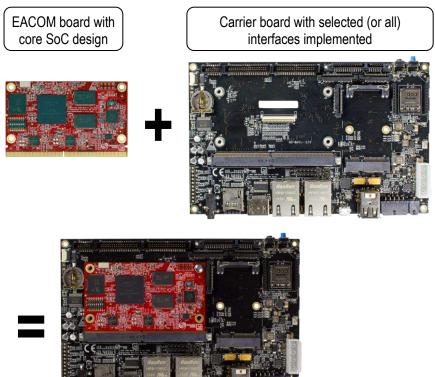
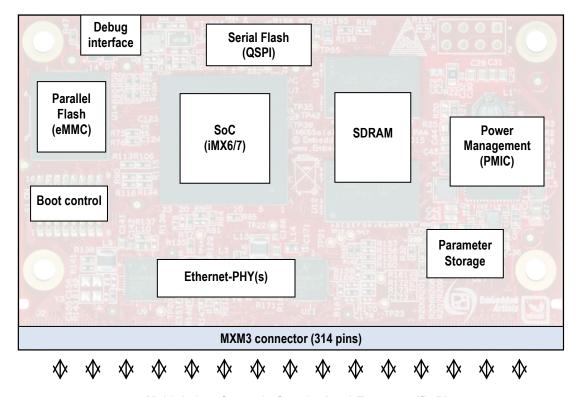


Figure 1 – COM Plus Carrier Board Equals SBC

3.1 EACOM Board Architecture

The block diagram in *Figure 2* below illustrates the typical components of an EACOM board:

- **SoC** the main component , a member of the iMX6/7 family.
- SDRAM a large memory array with 256 MByte 4 GByte capacity. Typically DDR3L memories to get low power consumption, yet high density.
- Parallel Flash for storing Operating System and boot loader images. Typically an eMMC memory but can also be an unmanaged FLASH memory.
- Serial Flash for storing code for (possible) Cortex-M4 core or boot loader image.
- Power Management typically in the form of a PMIC that supports low-power operation including DVFS (Dynamic Voltage and Frequency Scaling).
- Debug interface for JTAG debugging.
- Boot control for controlling the boot source.
- Parameter storage for retrieving important parameters during boot, like memory bus calibration parameters and MAC address(es).



Edge connector - edge pads conforming to the MXM3-standard with 314 positions.

Multiple Interfaces via Standard and Type-specific Pins

Figure 2 – COM Board Block Diagram

There are two types of interfaces to the EACOM boards:

Standard Interfaces

The EACOM specification has defined a number of different interfaces and allocated positions for these interfaces on the MXM3 connector. These interfaces are reserved for their respective interface and will be the same on every EACOM board. Note that every EACOM board will assign signals to every interface whenever possible, but not necessarily all of them.

Some interfaces may for example not be present on some SoC, like PCIe, SATA and a second Ethernet interface. Some SoC's may not have enough pins to assign all interfaces. It is important to note that to guarantee electrical compatibility between (carrier board) designs, only make use of the standard interfaces.

• Type-specific Interfaces

A number of positions (39 to be specific) on the MXM3 connector have been left unassigned. Different EACOM boards can have different signals and interfaces assigned to these positions.

Note that using these pins on a carrier board design may result in lost compatibility between EACOM boards, but not always. Details have to be checked in every specific case.

It can be limiting to only make use of the standard interfaces in the EACOM specification. If compatibility between EACOM boards is not a requirement then it is free to use every pin to whatever function the pin multiplexing allows.

3.2 Interface Overview

The table below lists the standard interfaces in the EACOM specification. Some interface are marked as *GPIO capable*. This means that the pins do not have any special voltage level or driver scheme, like for example the USB, Ethernet, PCIe, SATA and LVDS interfaces have. These interfaces have high-speed differential pin drivers that cannot function as a GPIO.

Interface	EACOM specification	Note
UART	3 ports	Two 4 wire and one 2 wire. GPIO capable.
SPI	2 ports	4 wire (SCLK, MOSI, MISO, SSEL). GPIO capable.
12C	3 ports	GPIO capable.
SD/MMC	2 ports	One 4 databits and one 8 databits. GPIO capable.
Parallel LCD	24 databits, 4 ctrl	PIXCLK, HSYNC, VSYNC, DATA_ENABLE. GPIO capable.
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	1 PWM and 4 GPIO. GPIO capable.
LVDS LCD	2 ports	18/24 bit LVDS data.
HDMI (TDMS)		
Parallel Camera	8 databits, 4 ctrl	HSYNC, VSYNC, PCLK, MCLK. GPIO capable.
Serial Camera	CSI, 4 lane	
Gigabit Ethernet	2 ports	
PCle	1 port, 1 lane	
SATA		
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	

SPDIF	1 TX/RX port	GPIO capable.
CAN	2 ports	GPIO capable.
I2S/SSI/AC97	1 port	4 wire synchronous plus MCLK. GPIO capable.
Analog audio	Stereo output	
GPIO	9 pins	
PWM	1 pin	GPIO capable.
ADC	8 inputs	
Power	10 VIN, VBAT and 47 GND	About 15% of the pins are ground pins.

There are also 39 pins that are not allocated to the standard interface, but rather left for the typespecific pins and interfaces.

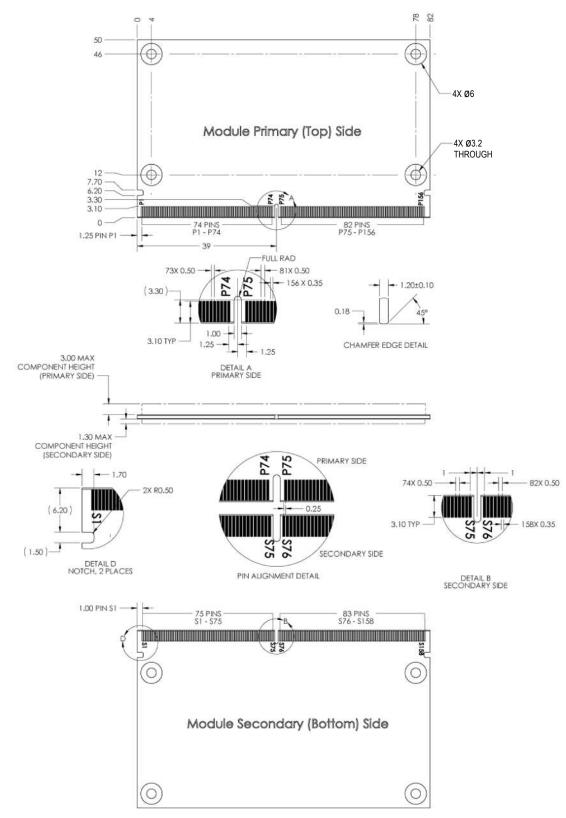
3.3 Debug Interface / JTAG

There is no debug interface (i.e., JTAG) signals allocated on the MXM3 edge connector. Instead such signals are available via an on-board connector (typically an FPC connector). The location of the debug connector and the exact type of connector are not dictated by EACOM specification.

The MXM3 connector dictates the mechanical form factor. The SMARC standard has also been an input. The EACOM boards are 82 mm wide and 50 mm high. Maximum component height on the top side is 3.0 mm and 1.3 mm on the bottom side. The MXM3 specification also dictated that pcb thickness is 1.2 mm. This results in a maximum thickness of the modules of 5.5 mm.

One single mechanical form factor is defined.

The picture below illustrates the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification. Note that the four mounting holes are 3.2 mm in diameter and this is not the same as the SMARC specification.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 3 - iMX6SoloX COM Board Mechanical Outline

There are four 3.2 mm holes on the EACOM board, see mechanical drawing above.

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". It is recommended to select an MXM3 connector with 5 mm stacking height since there are standard SMTSO spacers with 5 mm height.

6-8 mm M3 screws are typically used.

Thermal management solutions, like heat spreaders, are also mounted and fixed via these four holes.

4.2 MXM3 Connector

EACOM boards have 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. The connector is originally defined for use with MXM3 graphics cards. The signal integrity is excellent and suitable for data rates up to 5 GHz. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE cannot be used since this specific connector lack some of the pins.

As an example, connector AS0B826-S78B from Foxconn has 5.0 mm board to board stacking height. This space allows some components to also be placed right under the EACOM board.

As a general rule, always check available component height before placing components on the carrier board under the EACOM board, see picture below.

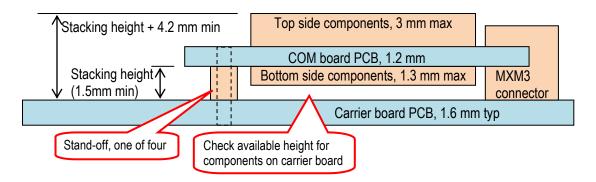


Figure 4 – EACOM Board Mounting in MXM3 Connector, Stacking Height

4.3 EACOM Pin Numbering

The figures below show the pin numbering for EACOM (the iMX6SoloX COM board is used as an example board in the pictures). Top (Primary) side edge fingers are numbered P1-P156. Bottom (Secondary) side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with odd numbers on the bottom and even numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying in the middle of the contact finger row.

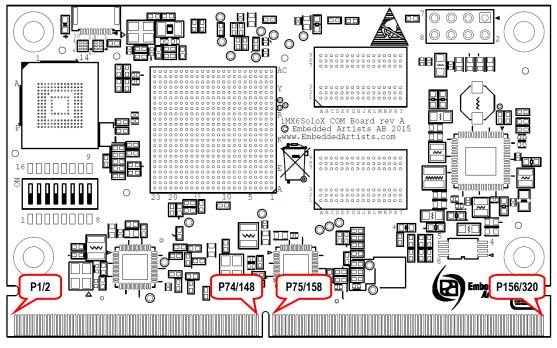


Figure 5 – EACOM Board Pin Numbering, Primary/Top Side

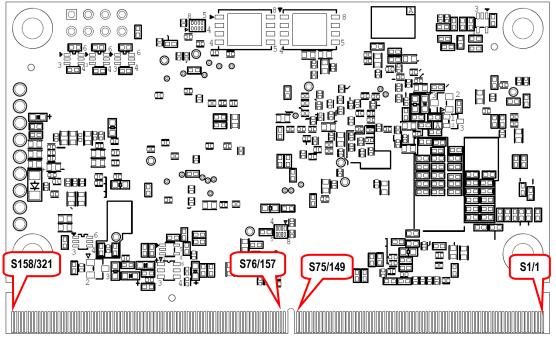


Figure 6 - EACOM Board Pin Numbering, Secondary/Bottom Side

5 Electrical Specification

5.1 **Power Supplies**

EACOM boards have a single main power supply input, VIN, with 3.3V nominal voltage. There is also an optional, low-current backup power supply input, VBAT, for Real Time Clock (RTC) support.

The EACOM board will power up and start normal operation once VIN is applied. VBAT is not needed for normal operation, but it is required for maintaining RTC operation. There can be other functions that rely on VBAT, like power on/off button control.

Each EACOM board will contain details about maximum current consumption and possible wider input voltage range but if the carrier board power supply is rated 3.3V +-5% / 3A it will be sufficient for all EACOM boards. Individual boards typically consumes considerable less than 3A in peak.

The EACOM Carrier Board Design Guide document gives recommendations about decoupling / bulk capacitance and ramp up times, etc.

5.2 Back Feed Protection

A typical SoC (and in particular the iMX6 family) requires back feed protection. No I/O pins should be externally driven before the EACOM board has powered up properly. If back feeding occurs it can prevent proper startup and also permanently damage the SoC.

EACOM board output signal PERI_PWR_EN is active high and signals when carrier board I/O signals are allowed to be driven. The signal typically controls carrier board power supplies but can also control transceivers and level shifters.

The EACOM Carrier Board Design Guide contains detailed information how to use the PERI_PWR_EN signal.

5.3 Voltage Domains

There are different voltage domains on the EACOM interfaces. VDD_IO is by far the most common and is the logic level that most interface signals use. VDD_IO is typically the same as VIN, but some EACOM boards allows VDD_IO to be lowered in order to save power.

Signal AIN_VREF is an output voltage level that reflect the upper range of the analog inputs (AINx) voltage range. The lower range is ground. Note that AIN_VREF voltage level can value. It is not a fixed voltage level. Converted analog values are relative to AIN_VREF.

5.4 VDD_SD

Signal VDD_SD is available to power the SD interface. Some EACOM boards supports dual voltage (1.8 / 3.3V) SD cards. The EACOM Carrier Board Design Guide contains detailed information how connect the signal.

Note that VDD_SD shall only be used to power the SD interface. Nothing else.

5.5 Reset Input / Output

EACOM boards have one RESET_IN signal and one RESET_OUT signal.

RESET_IN is active low. Pulling the signal low from the carrier board will trigger an internal reset on the EACOM board. There is no need to pull the signal high externally. The internal reset signal will generate an internal reset pulse that is active at least 100 ms, but it can be longer.

RESET_OUT is active low and reflect the EACOM board internal reset signal. It is an open drain output with a 1.5Kohm pull-up resistor to VIN.

5.6 Signal E2PROM_WP

Signal E2PROM_WP should be left unconnected or connected to GND. If signal is pulled low to ground, the parameter storage memory (I2C E2PROM) is write enabled and the iMX processor will power-up in USB OTG boot mode. This is normally only done during production.

Note that the content of the parameter storage memory (I2C E2PROM) should NEVER be altered. The parameters are written by Embedded Artists during production.

5.7 USB Interfaces

The EACOM interface specification contains two USB3.0 ports. Current iMX6/7 family members do not support USB3.0 but the interface feature has been included for future expansion.

USB3.0 interfaces are backward compatible with USB2.0 ports. The four new pins that have been added in USB3.0 (SSTXP/SSTXN and SSRXP/SSRXN) are just left unconnected.

Note that VBUS signals are inputs to EACOM boards, not outputs. Carrier boards must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces. It is not provided by the EACOM board.

6 Signal Allocation Specification

The table below present the signal allocation to the MXM3 edge connector on the primary/top side.

			5			
Top Side	Pin	Signal Group	Signal Name	Signal Class	Voltage Domain	
Pin Number	Number					
	МХМЗ					
P1	2	-	GPI06	Bidirectional	VDD_IO	
P2	4	GPIO	GPI05	Bidirectional	VDD_IO	
P3	6		GPIO4	Bidirectional	VDD_IO	
P4	8		GPIO3	Bidirectional	VDD_IO	
P5	10		SD_D1	Bidirectional	VDD_SD	
P6	12		SD_D0	Bidirectional	VDD_SD	
P7	14		SD_CLK	Output	VDD_SD	
P8	16	SD Interface	SD_CMD	Bidirectional	VDD_SD	
P9	18		SD_D3	Bidirectional	VDD_SD	
P10	20		SD_D2	Bidirectional	VDD_SD	
P11	22		VCC_SD	Power		
P12	24		MMC_D1	Bidirectional	VDD_IO	
P13	26		MMC_D0	Bidirectional	VDD_IO	
P14	28		MMC_D7	Bidirectional	VDD_IO	
P15	30		MMC_D6	Bidirectional	VDD_IO	
P16	32		MMC_CLK	Output	VDD IO	
P17	34	MMC Interface	MMC D5	Bidirectional	VDD IO	
P18	36		MMC CMD	Bidirectional	VDD IO	
P19	38		MMC D4	Bidirectional	VDD IO	
P20	40		MMC D3	Bidirectional	VDD IO	
P21	40		MMC_D3	Bidirectional	VDD IO	
P22	44		GND	Power	VDD_10	
P23	46		HDMI_TXC_N	Differential pair		
P23	40	-	HDMI_TXC_N			
P24 P25	40 50	-	GND	Differential pair		
		-		Power Differential agin		
P26	52		HDMI_TXD0_N	Differential pair		
P27	54		HDMI_TXD0_P	Differential pair		
P28	56		HDMI_HPD	Input		
P29	58	HDMI	HDMI_TXD1_N	Differential pair		
P30	60		HDMI_TXD1_P	Differential pair		
P31	62		GND	Power		
P32	64		HDMI_TXD2_N	Differential pair		
P33	66		HDMI_TXD2_P	Differential pair		
P34	68		HDMI_CEC	Bidirectional		
P35	70		GND	Power		
P36	72		ETH1_MD1_P	Differential pair		
P37	74		ETH1_MD1_N	Differential pair		
P38	76		GND	Power		
P39	78		ETH1_MD0_P	Differential pair		
P40	80		ETH1 MD0 N	Differential pair		
P41	82		ETH1 LINK1000	Output	VDD IO	
P42	84		ETH1_ACT	Output	VDD IO	
P43	86	Gigabit Ethernet #1	ETH1_LINK	Output	VDD_IO	
P44	88		ETH1 MD3 N	Differential pair		
P45	90		ETH1_MD3_P	Differential pair		
P46	92		GND	Power		
P47	94	-	ETH1_MD2_N	Differential pair		
P48	94 96		ETH1_MD2_N ETH1_MD2_P	Differential pair		
P48 P49	96 98	-	GND	Power	1	
P49 P50	100		ETH2_MD1_P	Differential pair		
	100	-				
P51	-		ETH2_MD1_N	Differential pair		
P52	104		GND	Power		
P53	106	-	ETH2_MD0_P	Differential pair		
P54	108	-	ETH2_MD0_N	Differential pair		
P55	110		ETH2_LINK1000	Output	VDD_IO	
P56	112	Gigabit Ethernet #2	ETH2_ACT	Output	VDD_IO	
P57	114		ETH2_LINK	Output	VDD_IO	
P58	116		ETH2_MD3_N	Differential pair		
P59	118		ETH2_MD3_P	Differential pair		
P60	120		GND	Power		
P61	122		ETH2_MD2_N	Differential pair		
P62	124		ETH2_MD2_P	Differential pair		
·				· · · · · ·		

P63	126		GND	Power	
P64	120		USB_01_DN	Differential pair	
P65	120	-	USB_01_DR	Differential pair	
P66	130	-	USB_01_0TG_ID		
	-	-		Input Differential pair	VDD_IO
P67	134		USB_01_SSTXN	Differential pair	
P68	136		USB_01_SSTXP	Differential pair	
P69	138	USB OTG #1	GND	Power Differential pair	
P70	140		USB_01_SSRXN	Differential pair	
P71	142	-	USB_01_SSRXP	Differential pair	
P72	144		USB_01_VBUS	Input	
P73	146		USB_01_PWR_EN	Output	VDD_IO
P74	148		USB_01_0C	Input	VDD_IO
	150		Non existing pin		
	152	Key in MXM3 edge	Non existing pin		
	154	pads	Non existing pin		
	156		Non existing pin		
P75	158		USB_H1_PWR_EN	Output	VDD_IO
P76	160		USB_H1_OC	Input	VDD_IO
P77	162		GND	Power	
P78	164		USB_H1_DN	Differential pair	
P79	166		USB_H1_DP	Differential pair	
P80	168	USB Host #1	USB_H1_SSTXN	Differential pair	
P81	170		USB_H1_SSTXP	Differential pair	
P82	172		GND	Power	
P83	174	1	USB_H1_SSRXN	Differential pair	1
P84	176		USB_H1_SSRXP	Differential pair	<u> </u>
P85	178		USB_H1_VBUS	Input	
P86	180		USB H2 PWR EN	Output	VDD IO
P87	182		USB_H2_OC	Input	VDD_IO
P88	184		GND	Power	
P89	186	USB Host #2	USB_H2_DN	Differential pair	
P90	188		USB_H2_DP	Differential pair	
P91	190		GND	Power	
P92	190		COM board specific	FOWEI	
P92	192	-	COM board specific		
P93	194	-	COM board specific		
P94 P95					
	198		COM board specific		
P96	200		COM board specific		
P97	202	-	COM board specific		
P98	204	-	COM board specific		
P99	206		COM board specific		
P100	208		COM board specific		
P101	210		COM board specific		
P102	212		COM board specific		
P103	214		COM board specific		
P104	216	COM board specific	COM board specific		
P105	218		COM board specific		
P106	220		COM board specific		
P107	222		COM board specific		
P108	224		COM board specific		
P109	226		COM board specific		
P110	228		COM board specific		
P111	230		COM board specific		
P112	232		COM board specific		
P113	234		COM board specific		
P114	236		COM board specific		
P115	238		COM board specific		
P116	240		COM board specific		
P117	242		COM board specific		1
P118	244		GND	Power	1
P119	246		SPI-B_SSEL	Output	VDD IO
P120	248	SPI-B	SPI-B MOSI	Output	VDD IO
P121	250		SPI-B_MISO	Input	VDD_IO
P122	252		SPI-B_CLK	Output	VDD_IO
P123	252		SPI-A_SSEL	Output	VDD_IO
P123	256		SPI-A_SSEL	Output	VDD_IO VDD_IO
P124	258	SPI-A	SPI-A_MISO		VDD_IO VDD_IO
		SFI-A		Input Output	
P126 P127	260 262		SPI-A_CLK GND	Output	VDD_IO
	262			Power	
	1 / 04		UART-C_RXD	Input	VDD_IO
P128 P129	266	UART-C	UART-C_TXD	Output	VDD_IO

P130 268 UART-B UART-B_RXD Input VDD_IO P132 272 UART-B_CTS Input VDD_IO P133 274 UART-B_RTS Output VDD_IO P134 276 UART-B_TS Output VDD_IO P135 278 UART-A UART-A_CTS Input VDD_IO P136 280 UART-A_CTS Input VDD_IO P137 282 UART-A_TS Output VDD_IO P138 284 PWM PWM Output VDD_IO P139 286 GPIO GPIO2 Bidirectional VDD_IO P140 288 GPIO GPIO2 Bidirectional VDD_IO P141 290 System Control RESET_IN Input VDD_IO P143 294 System Control RESET_OUT Output, open drain VDD_IO P144 96 GND Power POWer VIN POwer P146 <						
P132 272 UART-B UART-B_RTS Output VDD_IO P133 274 UART-B_TXD Output VDD_IO P134 276 UART-A_RXD Input VDD_IO P135 278 UART-A_RXD Input VDD_IO P136 280 UART-A_RXD Input VDD_IO P137 282 PWM VMRT-A_TS Output VDD_IO P138 284 PWM PWM Output VDD_IO P139 286 GPIO GPIO2 Bidirectional VDD_IO P140 288 GPIO GPIO2 Bidirectional VDD_IO P141 290 PERI_PWR_EN Output VDD_IO P143 294 System Control RESET_IN Input VDD_IO P144 96 GND Power VIN Power VIN P144 96 VIN Power VD_IO VIN VD_IO P144 96	P130	268		UART-B_RXD	Input	VDD_IO
P132 2/2 UART-B_TXD Output VDD_IO P133 274 UART-B_TXD Output VDD_IO P134 276 UART-A_RXD Input VDD_IO P135 278 UART-A_CTS Input VDD_IO P136 280 UART-A_CTS Input VDD_IO P137 282 UART-A_TXD Output VDD_IO P138 284 PWM PWM Output VDD_IO P139 286 GPIO GPIO1 Bidirectional VDD_IO P141 290 PERI_PWR_EN Output VDD_IO P142 292 System Control RESET_IN Input VDD_IO P143 294 PCRI_PWR_EN Output VDD_IO PCRI_PWR_EN Output VDD_IO P144 96 GND Power	P131	270		UART-B_CTS	Input	VDD_IO
P134 276 P135 278 P136 280 P137 282 P138 284 P139 286 P130 286 P131 286 P132 GPIO GPIO GPIO GPIO GPIO GPIO GPIO P141 290 P142 292 System Control RESET_IN RESET_OUT Output VDD_IO P143 294 P144 96 P145 298 Backup Power Supp. VBAT P144 96 P145 298 Backup Power Supp. VBAT Power Power P144 96 P145 298 Backup Power Supp. VBAT Power VIN P144 96 P145 306 P144 96 VIN <td>P132</td> <td>272</td> <td>UART-B</td> <td>UART-B_RTS</td> <td>Output</td> <td>VDD_IO</td>	P132	272	UART-B	UART-B_RTS	Output	VDD_IO
P135 278 UART-A UART-A_CTS Input VDD_IO P137 282 PWM PWM Output VDD_IO P138 284 PWM PWM Output VDD_IO P139 286 GPIO GPIO2 Bidirectional VDD_IO P140 288 GPIO GPIO1 Bidirectional VDD_IO P141 290 PERLPWR_EN Output VDD_IO P142 292 System Control RESET_IN Input VDD_IO P143 294 PERLPWR_EN Output VDD_IO P143 294 System Control RESET_OUT Output, open drain VDD_IO P144 96 GND Power VID_IO POWER VIN POWER P144 96 GND Power VID_IO VID_IO POWER VID_IO POWER VID_IO POWER VIN POWER VIN POWER VIN POWER VIN VIN	P133	274		UART-B_TXD	Output	VDD_IO
P136 280 UAR1-A UART-A_RTS Output VDD_IO P137 282 PWM PWM Output VDD_IO P138 284 PWM PWM Output VDD_IO P139 286 GPIO GPIO2 Bidirectional VDD_IO P140 288 GPIO GPIO1 Bidirectional VDD_IO P141 290 System Control RESET_IN Input VDD_IO P143 294 System Control RESET_OUT Output, open drain VDD_IO P144 96 GND Power Power POWer POWer P145 298 Backup Power Supp. VBAT Power VIN VDD_IO P146 300 System Control E2PROM_WP Input VDD_IO P148 304 P149 306 VIN Power VIN P150 308 VIN Power VIN VIN Power VIN	P134	276		UART-A_RXD	Input	VDD_IO
P136 280 UAR1-A_R1S Output VDD_1O P137 282 UAR1-A_R1S Output VDD_1O P138 284 PWM PWM Output VDD_1O P139 286 GPIO GPIO2 Bidirectional VDD_1O P140 288 GPIO GPIO1 Bidirectional VDD_1O P141 290 PER_PWR_EN Output VDD_1O P142 292 System Control RESET_IN Input VDD_1O P143 294 PER_PWR_EN Output VDD_1O P144 96 GND Power Power P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VD_1O P147 302 VIN Power VIN VIN VIN P148 304 VIN Power VIN VIN VIN VIN P150 308	P135	278		UART-A_CTS	Input	VDD_IO
P138 284 PWM PWM Output VDD_IO P139 286 GPIO GPIO2 Bidirectional VDD_IO P140 288 GPIO GPIO1 Bidirectional VDD_IO P141 290 System Control FERLPWR_EN Output VDD_IO P142 292 System Control RESET_IN Input VDD_IO P143 294 GND Power VDD_IO P144 96 GND Power VDD_IO P144 96 GND Power Power P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN Power P148 304 Pisi Nain Power Supply VIN Power P150 308 Pisit Nain Power Supply VIN Power VIN Power	P136	280	UART-A	UART-A_RTS	Output	VDD_IO
P139 286 GPIO GPIO2 Bidirectional VDD_IO P140 288 GPIO GPIO1 Bidirectional VDD_IO P141 290 System Control PERI_PWR_EN Output VDD_IO P142 292 System Control RESET_IN Input VDD_IO P143 294 GND Power VDD_IO P144 96 GND Power VDD_IO P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN VIN Power P148 304 Pit49 306 VIN Power VIN VIN VIN Power VIN VIN Power VIN VI	P137	282		UART-A_TXD	Output	VDD_IO
P140 288 GPIO GPIO1 Bidirectional VDD_IO P141 290	P138	284	PWM	PWM	Output	VDD_IO
P140 228 GPI01 Bidirectional VDD_IO P141 290 PERI_PWR_EN Output VDD_IO P142 292 System Control RESET_IN Input VDD_IO P143 294 PERI_PWR_EN Output VDD_IO P144 96 GND Power P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P148 304 P149 306 VIN Power VIN P150 308 Main Power Supply VIN Power VIN Power P152 312 Input VIN Power VIN Power P153 314 P155 318 VIN Power VIN Power	P139	286	CDIO	GPIO2	Bidirectional	VDD_IO
P142 292 System Control RESET_IN Input VDD_IO P143 294 RESET_OUT Output, open drain VDD_IO P144 96 GND Power Power P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN Power P148 304 VIN Power VIN Power P149 306 VIN Power VIN Power P150 308 VIN Power VIN Power P152 312 Input VIN Power VIN Power VIN Power VIN Power VIN VIN Power P153 314 VIN Power VIN VIN Power VIN Power VIN Power VIN VIN Power <	P140	288	GPIO	GPI01	Bidirectional	VDD_IO
P143 294 RESET_OUT Output, open drain VDD_IO P144 96 GND Power Power P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN Power P148 304 VIN Power VIN Power P149 306 VIN Power VIN Power P150 308 VIN Power VIN Power V1N Power VIN Power VIN VIN P152 312 Input VIN Power VIN VIN Power V1N Power VIN Power VIN VIN </td <td>P141</td> <td>290</td> <td></td> <td>PERI_PWR_EN</td> <td>Output</td> <td>VDD_IO</td>	P141	290		PERI_PWR_EN	Output	VDD_IO
P144 96 GND Power P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN Power P148 304 VIN Power VIN Power P149 306 VIN Power VIN Power P150 308 VIN Power VIN Power V152 312 Input VIN Power VIN Power V153 314 VIN Power VIN Power VIN Power V1N Power VIN Power VIN VIN <td>P142</td> <td>292</td> <td>System Control</td> <td>RESET_IN</td> <td>Input</td> <td>VDD_IO</td>	P142	292	System Control	RESET_IN	Input	VDD_IO
P145 298 Backup Power Supp. VBAT Power P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN Power P148 304 VIN Power VIN Power P149 306 VIN Power VIN Power P150 308 VIN Power VIN Power P151 310 Input VIN Power VIN Power P152 312 Input VIN Power VIN Power P153 316 VIN Power VIN Power VIN P155 318 VIN Power VIN Power VIN Power	P143	294		RESET_OUT	Output, open drain	VDD_IO
P146 300 System Control E2PROM_WP Input VDD_IO P147 302 VIN Power VIN Power P148 304 VIN Power VIN Power P149 306 VIN Power VIN Power P150 308 VIN Power VIN Power P151 310 Input VIN Power VIN Power P152 312 Input VIN Power VIN Power VIN Power VIN Power VIN Power P153 314 VIN Power VIN Power VIN Power VIN Power VIN VIN Power P155 318 VIN Power VIN VIN <td< td=""><td>P144</td><td>96</td><td></td><td>GND</td><td>Power</td><td></td></td<>	P144	96		GND	Power	
P147 302 VIN Power P148 304 VIN Power P149 306 VIN Power P150 308 VIN Power P151 310 Input VIN Power VIN Power VIN Power VIN Power VIN VIN P152 312 Input VIN Power VIN Power VIN VIN VIN Power VIN VIN VIN Power VIN VIN	P145	298	Backup Power Supp.	VBAT	Power	
P148 304 P149 306 P150 308 P151 310 P152 312 P153 314 P154 316 P155 318	P146	300	System Control	E2PROM_WP	Input	VDD_IO
P149 306 P150 308 P151 310 P152 312 P153 314 P154 316 P155 318	P147	302		VIN	Power	
P150 308 P151 310 P152 312 P153 314 P154 316 P155 318	P148	304		VIN	Power	
P151 310 Main Power Supply VIN Power P152 312 Input VIN Power VIN P153 314 VIN Power VIN VIN Power P154 316 VIN Power VIN Power VIN P155 318 VIN Power VIN Power	P149	306		VIN	Power	
P152 312 Input VIN Power P153 314 VIN Power VIN P154 316 VIN Power VIN P155 318 VIN Power VIN	P150	308		VIN	Power	
P153 314 P154 316 P155 318	P151	310	Main Power Supply	VIN	Power	
P154 316 VIN Power P155 318 VIN Power	P152	312	Input	VIN	Power	
P155 318 VIN Power	P153	314		VIN	Power	
	P154	316	1	VIN	Power	
P156 320 VIN Power	P155	318	1	VIN	Power	
	P156	320		VIN	Power	

The table below present the signal allocation to the MXM3 edge connector on the secondary/bottom side.

Bottom Pin Side Pin Number		Signal Group	Signal Name	Signal Class	Voltage Domain
Number	MXM3				
S1 S2	3	AUDIO MQS	MQS_RIGHT MQS_LEFT	Output	VDD_IO VDD_IO
S2 S3	5		GND	Output Power	VDD_IO
S4	7		AUDIO_TXFS	Output	VDD_IO
S5	9	-	AUDIO_RXD	Input	VDD_IO
S6	11		AUDIO TXC	Output	VDD IO
\$7	13	AUDIO I2S	AUDIO_TXD	Output	VDD_IO
S8	15	-	AUDIO_MCLK	Output	VDD_IO
S9	17		GND	Power	
S10	19	SPDIF	SPDIF_IN	Input	VDD_IO
S11	21	SEDI	SPDIF_OUT	Output	VDD_IO
S12	23	CAN #2	CAN2_TX	Output	VDD_IO
S13	25	0/11/12	CAN2_RX	Input	VDD_IO
S14	27	CAN #1	CAN1_TX	Output	VDD_IO
S15	29	0	CAN1_RX	Input	VDD_IO
S16	31	-	GND	Power	
S17	33	-	LVDS1_D3_P	Differential pair	
S18	35	-	LVDS1_D3_N	Differential pair	
S19 S20	37 39	-	GPIO LVDS1 D2 P	Bidirectional Differential pair	VDD_IO
S20 S21	39 41	-	LVDS1_D2_P LVDS1_D2_N	Differential pair	+
S22	41	-	GND	Power	
S23	45	LVDS #1	LVDS1_D1_P	Differential pair	
S24	47	LVD0#1	LVDS1_D1_N	Differential pair	
S25	49	-	GND	Power	
S26	51	-	LVDS1_D0_P	Differential pair	
S27	53	-	LVDS1 D0 N	Differential pair	
S28	55	-	GND	Power	
S29	57		LVDS1_CLK_P	Differential pair	
S30	59		LVDS1_CLK_N	Differential pair	
S31	61		GND	Power	
S32	63		LVDS0_D3_P	Differential pair	
S33	65	_	LVDS0_D3_N	Differential pair	
S34	67	_	GPIO	Bidirectional	VDD_IO
S35	69	_	LVDS0_D2_P	Differential pair	
S36	71	-	LVDS0_D2_N	Differential pair	
S37	73		GND	Power Differential pair	
S38 S39	75 77	LVDS #0	LVDS0_D1_P	Differential pair	
S40	79	-	LVDS0_D1_N GND	Differential pair Power	
S41	81	-	LVDS0_D0_P	Differential pair	
S42	83	-	LVDS0 D0 N	Differential pair	
S43	85	-	GND	Power	
S44	87	-	LVDS0_CLK_P	Differential pair	
S45	89		LVDS0_CLK_N	Differential pair	
S46	91		I2C-A_SDA	Bidirectional	VDD_IO
S47	93	I2C-A	I2C-A_SCL	Output	VDD_IO
S48	95	I2C-B	I2C-B_SDA	Bidirectional	VDD_IO
S49	97	120-0	I2C-B_SCL	Output	VDD_IO
S50	99	HDMI / I2C-C	HDMI/I2C-C_SDA	Bidirectional	VDD_IO
S51	101		HDMI/I2C-C_SCL	Output	VDD_IO
S52	103	-	TP_RST	Output	VDD_IO
S53	105	Disclose Control	TP_IRQ	Input	VDD_IO
S54	107	Display Control	DISP_PWR_EN	Output	VDD_IO
S55	109	-	BL_PWR_EN	Output	VDD_IO
S56 S57	111 113		BL_PWM GND	Output Power	VDD_IO
S58	113	-	LCD_R0	Output	VDD_IO
S59	115	-	LCD_R0	Output	VDD_IO VDD_IO
S60	119		LCD_R1	Output	VDD_IO VDD IO
S61	121	LCD	LCD_R3	Output	VDD_IO
S62	123	200	LCD_R4	Output	VDD_IO
S63	125		LCD_R5	Output	VDD IO
S64	127		LCD_R6	Output	VDD_IO
S65	129		LCD_R7	Output	VDD_IO

Se6 131 LCD 60 Odput YOD 10 S88 133 S						
S86 137 589 137 570 141 572 143 573 145 574 141 573 145 574 147 573 145 574 147 575 149 151 CD 63 Output VOD 10 153 Non existing pin VOD 10 VOD 10 576 157 159 Non existing pin VOD 10 577 159 Non existing pin VOD 10 VOD 10 578 161 CD 81 Output VOD 10 VOD 10 581 173 Stating pin VOD 10 VOD 10 VOD 10 582 169 CD 81 Output VOD 10 VOD 10 583 171 Stating pin VOD 10 CD 85 Output VOD 10 584 173 Stating pin VOD 10 CD 97 Output VOD 10 CD 97	S66	131		LCD_G0	Output	VDD_IO
Seg 137 Second	S67	133		LCD_G1	Output	VDD_IO
370 141 571 141 572 143 573 145 574 147 574 147 574 149 575 149 151 CO G Output VOD IO 153 Participant State Non existing pin VOD IO 157 159 Non existing pin VOD IO 576 157 Non existing pin VOD IO 577 159 Non existing pin VOD IO 578 161 Non existing pin VOD IO 578 161 CD B1 Output VOD IO 580 165 CD B1 Output VOD IO 581 173 CD B2 Output VOD IO 582 169 CD B1 Output VOD IO 584 173 S S S S 584 183 S S S 584 183	S68	135		LCD_G2	Output	VDD_IO
S74 141 S73 143 S73 143 S74 147 S75 149 S75 149 S75 149 S75 149 S75 149 S76 151 S77 159 S78 161 S79 163 S81 167 S82 169 S83 171 S84 173 S85 175 S86 177 S87 179 S88 181 S89 183 S89 183 S89 183 S89 183 S89 183 S89 183 S89	S69			LCD_G3	Output	_
S72 143 LCD 66 Output VOD 10 S74 147 VOD 10 VOD 10 VOD 10 S74 149 VOD 10 VOD 10 VOD 10 151 For 151 VOD 10 VOD 10 VOD 10 153 Partial CD 80 Output VOD 10 VOD 10 157 159 Non existing pin VOD 10 VOD 10 157 159 Non existing pin VOD 10 VOD 10 157 159 VOD 10 VOD 10 VOD 10 158 161 VOD 10 VOD 10 VOD 10 158 161 VOD 10 VOD 10 VOD 10 158 161 VOD 10 VOD 10 VOD 10 158 171 VOD 10 VOD 10 VOD 10 158 171 VOD 10 VOD 10 VOD 10 158 171 VOD 10 VOD 10 VOD 10 158 181 181 VOD 10 VOD 10 VOD 10					Output	
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375 149 CD_B 0 Output VDD_O 153 Mey in MXM3 edg pads Men existing pin Non existing pin Non existing pin 156 157 159 Non existing pin Non existing pin Non existing pin 157 159 161 Non existing pin Non existing pin Non existing pin 157 163 Non existing pin Non existing pin Non existing pin Non existing pin 158 161 Non existing pin Non existing pin Non existing pin Non existing pin 158 161 Non existing pin						VDD_IO
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S92 189 ADC AIN5 Analog input AIN_VREF S93 193 AIN4 Analog input AIN_VREF S95 195 AIN3 Analog input AIN_VREF S96 197 Sime AIN1 Analog input AIN_VREF S98 201 Sime AIN0 Analog input AIN_VREF AIN0 Analog input AIN_VREF AIN1 Analog input AIN_VREF S98 203 Simo COM board specific Differential pair COM board specific COM board specific Differential pair COM board specific						—
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S97199AINOAnalog inputAIN_VREFS98201PowerPowerImage: Second Seco					Analog input	
S98 201 S99 203 S100 205 S100 205 S101 207 S102 209 S103 211 S104 213 S105 215 S106 217 S108 221 S108 221 S109 223 S111 227 S112 229 S111 227 S112 229 S113 231 S114 233 S112 229 S113 231 S114 233 S114 233 S112 229 S113 231 S114 233 S115 235 S116 237 S118 241 S119 243 Parallel Camera CSL_DO GND Power GSL_DO In		-	-			—
S99 203 S100 205 S101 207 S102 209 S103 211 S104 213 S105 215 S106 217 S106 217 S106 217 S107 219 S108 221 S109 223 S110 225 S111 227 S112 229 S112 229 S111 227 S112 229 S111 221 S112 229 S113 231 S114 233 S115 235 S118 231 S118 231 S119 243 S111 239 S112 249 S112 241 S120 245 S121 247 S122 255					U 1	AIN_VREF
S100 205 S101 207 S102 209 S103 211 S104 213 S105 215 S106 217 S107 219 S108 221 S109 223 S110 225 S110 225 S111 227 S112 229 S113 231 S114 233 S115 235 S114 233 S115 235 S116 237 S118 241 S119 243 S120 245 S121 247 S122 249 S124 253 S125 255 <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>						
St01 207 St02 209 St03 211 St04 213 St05 215 St06 217 St08 221 St09 223 St10 225 St11 225 St11 227 St12 229 St12 229 St13 231 St14 233 St12 229 St13 231 St14 233 St15 235 St18 241 St19 243 St19 243 St20 245 St21 251 St22 249 <th></th> <th></th> <th>-</th> <th></th> <th></th> <th></th>			-			
S102 209 S103 211 S104 213 S105 215 S106 217 S107 219 S108 221 S109 223 S109 223 S109 223 S100 225 S110 225 S111 227 S112 229 S113 231 S114 233 S115 235 S116 237 S118 241 S119 243 S118 241 S119 243 S118 241 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S128 251 S129 263 <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>						
S103 211 S104 213 S105 215 S106 217 S107 219 S108 221 S109 223 S110 225 S111 227 S112 229 S113 231 S114 233 S115 235 S114 233 S115 235 S114 233 S115 235 S116 237 S117 239 S118 241 S119 243 S112 247 S118 241 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S128 251 S129 263 S121 267 <th></th> <th>-</th> <th></th> <th>-</th> <th></th> <th></th>		-		-		
S104 213 S105 215 S106 217 S107 219 S108 221 S109 223 S110 225 S111 227 S112 229 S113 231 S114 233 S115 235 S114 233 S115 235 S116 237 S118 241 S119 243 S112 229 Parallel Camera CSI_HSYNC S118 241 S118 241 S118 241 S118 241 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129						
S106 217 COM board specific COM board specific <thc< th=""><th></th><th></th><th></th><th>GND</th><th></th><th></th></thc<>				GND		
Silo Zili COM board specific Image: Com board specific Silo Z21 COM board specific Image: Com board specific	S105	215		COM board specific		
Si108 221 Si109 223 Si10 225 Si11 227 Si11 229 Si11 229 Si11 231 Si114 233 Si115 235 Si116 237 Si118 241 Si118 241 Si120 245 Si121 247 Si121 247 Si122 249 Si123 251 Si124 253 Si125 255 Si26 257 Si126 257 Si26 257 Si26 257 Si26 257 Si27 259 Si31 267 Si31 26		217	COM board specific	COM board specific		
S109 223 S110 225 S111 227 S112 229 S113 231 S114 233 S115 235 S116 237 S118 241 S118 241 S118 241 S118 241 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129 263 S121 247 S126 257 S126 257 S126 255 S126 257 S126 257 S127 259 S128 261 S130 265 S131 267 <th></th> <th>219</th> <th></th> <th></th> <th></th> <th></th>		219				
S110 225 S111 227 S112 229 S113 231 S113 231 S114 233 S115 235 S116 237 S117 239 S118 241 S119 243 S119 243 S112 247 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129 263 S130 265 S131 267 S132 269 Cold board specific Col						
S111 227 S112 229 S113 231 COM board specific COM board specific S113 231 S114 233 S115 235 S116 237 S117 239 S118 241 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S128 261 S129 263 S120 265 S121 2747 S122 249 S124 253 S125 255 S126 257 S126 257 S128 261 S129 263 Serial Camera GND GND Power CSI_D7 Input VDD_IO						
S112 229 S113 231 S114 233 S114 233 S115 235 S116 237 S116 237 S117 239 S118 241 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S128 261 S129 263 S121 261 S128 261 S129 263 S131 267 S131 267 S132 269						
S113 231 COM board specific Input VDD_IO S114 233 CSI_HSYNC Input VDD_IO S115 235 CSI_VSYNC Input VDD_IO S116 237 CSI_MCLK Output VDD_IO S117 239 CSI_PCLK Input VDD_IO S118 241 CSI_DO Input VDD_IO S119 243 Parallel Camera CSI_DO Input VDD_IO S120 245 SI21 247 CSI_D1 Input VDD_IO S121 247 CSI_D2 Input VDD_IO CSI_D3 Input VDD_IO S122 249 CSI_D3 Input VDD_IO CSI_D3 Input VDD_IO S123 251 CSI_D5 Input VDD_IO CSI_D3 CSI_D1 CSI_D3 CS			-			
S114 233 CSI_HSYNC Input VDD_IO S115 235 CSI_MSYNC Input VDD_IO S116 237 CSI_MCLK Output VDD_IO S117 239 CSI_MCLK Output VDD_IO S118 241 CSI_PCLK Input VDD_IO S119 243 Parallel Camera CSI_DO Input VDD_IO S120 245 Parallel Camera CSI_D1 Input VDD_IO S121 247 CSI_D2 Input VDD_IO S122 249 CSI_D3 Input VDD_IO S123 251 CSI_D4 Input VDD_IO S124 253 CSI_D5 Input VDD_IO S125 255 CSI_D6 Input VDD_IO S126 257 Serial Camera CSI_D7 Input VDD_IO S128 261 St29 CSI_D3_M Differential pair CSI_D3_P CSI_D3_P CSI_D						
S115 235 S116 237 S116 237 S117 239 S118 241 S119 243 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129 263 S130 265 S131 267 S132 269					Input	
S116 237 S117 239 S118 241 S119 243 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S127 259 S128 261 S129 263 S130 265 S131 267 S132 269			-			—
S117 239 S118 241 S119 243 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S126 257 S127 259 S128 261 S129 263 S131 267 S131 267 S132 269						
S118 241 S119 243 S120 245 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S128 261 S129 263 S131 267 S132 269			-			
S119 243 S120 245 S121 247 S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129 263 S129 263 S130 265 S131 267 S132 269						
S120 245 Parallel Camera CSI_D1 Input VDD_IO S121 247 CSI_D2 Input VDD_IO S122 249 CSI_D3 Input VDD_IO S123 251 CSI_D4 Input VDD_IO S124 253 CSI_D4 Input VDD_IO S125 255 Input VDD_IO CSI_D4 Input VDD_IO S126 257 CSI_D6 Input VDD_IO CSI_D2 CSI_D7 Input VDD_IO S127 259 Serial Camera GND Power CSI_D3_M Differential pair S128 261 Serial Camera CSI_D3_P Differential pair CSI_D3_P CSI_D3_P Differential pair CSI_D2_M CSI_D2_M CSI_D2_P Differential pair CSI_D2_P CSI_D2_P Differential pair CSI_D2_P CSI_D2_P Differential pair CSI_D2_P CSI_D2_P Differential pair CSI_D3_P CSI_D3_P CSI_D3_P CSI_D3_P CSI_D3_P	S119					VDD_IO
S121 247 S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129 263 S130 265 S131 267 S132 269			Parallel Camera		- · ·	—
S122 249 S123 251 S124 253 S125 255 S126 257 S127 259 S128 261 S129 263 S130 265 S131 267 S132 269						—
S124 253 CSI_D5 Input VDD_IO S125 255 CSI_D6 Input VDD_IO S126 257 CSI_D7 Input VDD_IO S127 259 CSI_D7 Input VDD_IO S128 261 CSI_D3_M Differential pair CSI_D3_P S129 263 Serial Camera (CSI/MIPI) CSI_D3_P Differential pair S131 267 CSI_D2_M Differential pair CSI_D2_P CSI_D2_P S132 269 CSI_D2_P Differential pair CSI_D2_P Differential pair		249		CSI_D3	- · ·	VDD_IO
S125 255 CS_D6 Input VDD_IO S126 257 Input VDD_IO S127 259 CS_D7 Input VDD_IO S128 261 CSI_D3_M Differential pair CSI_D3_P Oifferential pair S130 265 CSI/MIPI) GND Power CSI_D3_P Differential pair S131 267 CSI_D2_M Differential pair CSI_D2_M Differential pair S132 269 CSI_D2_P Differential pair CSI_D2_P Differential pair						
S126 257 CS_D7 Input VDD_IO S127 259						
S127 259 GND Power S128 261 CSI_D3_M Differential pair S129 263 Serial Camera (CSI/MIPI) CSI_D3_P Differential pair S130 265 CSI/MIPI) GND Power S131 267 CSI_D2_M Differential pair S132 269 CSI_D2_P Differential pair				_		
S128 261 S129 263 S130 265 S131 267 S132 269 CSI_D3_M Differential pair CSI_D3_P Differential pair CSI_D1 Power CSI_D2_M Differential pair						VDD_IO
S129 263 Serial Camera CSI_D3_P Differential pair S130 265 (CSI/MIPI) Power CSI_D2_M Differential pair S132 269 CSI_D2_P Differential pair CSI_D2_P Differential pair						
S130265Serial Carliera (CSI/MIPI)GNDPowerS131267CSI/D2_MDifferential pairS132269CSI_D2_PDifferential pair						
S130 265 CSI/MIPI) GND Power S131 267 CSI_D2_M Differential pair S132 269 CSI_D2_P Differential pair			Serial Camera			
S131 267 CST_D2_M Differential pair S132 269 CST_D2_P Differential pair						
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S134	273		CSI_D1_M	Differential pair	
S135	275		CSI_D1_P	Differential pair	
S136	277		GND	Power	
S137	279		CSI_D0_M	Differential pair	
S138	281		CSI_D0_P	Differential pair	
S139	283		GND	Power	
S140	285		CSI_CLK_M	Differential pair	
S141	287		CSI_CLK_P	Differential pair	
S142	289		GND	Power	
S143	291		SATA_TX_P	Differential pair	
S144	293		SATA_TX_N	Differential pair	
S145	295	SATA	GND	Power	
S146	297		SATA_RX_N	Differential pair	
S147	299		SATA_RX_P	Differential pair	
S148	301		GND	Power	
S149	303		GND	Power	
S150	305		PCIE_CLK_P	Differential pair	
S151	307		PCIE_CLK_N	Differential pair	
S152	309		GND	Power	
S153	311	PCle	PCIE_TX_P	Differential pair	
S154	313	FOIE	PCIE_TX_N	Differential pair	
S155	315		GND	Power	
S156	317		PCIE_RX_P	Differential pair	
S157	319		PCIE_RX_N	Differential pair	
S158	321		GND	Power	

Signal Group	Signal Name	Top Side Pin Number	Pin Nur MXM3	nber	Bottom Side Pin Number	Signal Name	Signal Group
	GPI06	P1	2	1	S1	MQS_RIGHT	
GPIO	GPIO5	P2	4	3	S2	MQS_LEFT	AUDIO MQS
GFIO	GPIO4	P3	6	5	S3	GND	
	GPIO3	P4	8	7	S4	AUDIO_TXFS	_
	SD_D1	P5	10	9	S5	AUDIO_RXD	-
	SD_D0 SD_CLK	P6 P7	12 14	11 13	S6 S7	AUDIO_TXC AUDIO_TXD	AUDIO I2S
SD Interface	SD_CMD	P8	16	15	S8	AUDIO_TXD	-
	SD D3	P9	18	17	S9	GND	
	SD_D2	P10	20	19	S10	SPDIF_IN	SPDIF
	SD_VCC	P11	22	21	S11	SPDIF_OUT	SPDIF
	MMC_D1	P12	24	23	S12	CAN2_TX	CAN #2
	MMC_D0	P13	26	25	S13	CAN2_RX	0/11/12
	MMC_D7 MMC D6	P14 P15	28 30	27 29	S14 S15	CAN1_TX CAN1 RX	CAN #1
	MMC_D0	P16	30	31	S16	GND	
MMC Interface	MMC D5	P17	34	33	S17	LVDS1 D3 P	-
	MMC_CMD	P18	36	35	S18	LVDS1_D3_N	-
	MMC_D4	P19	38	37	S19	GPIO]
	MMC_D3	P20	40	39	S20	LVDS1_D2_P	
	MMC_D2	P21	42	41	S21	LVDS1_D2_N	_
	GND	P22	44	43	S22	GND	
	HDMI_TXC_N HDMI_TXC_P	P23 P24	46 48	45 47	S23 S24	LVDS1_D1_P LVDS1_D1_N	LVDS #1
	GND	P24 P25	40 50	47	S25	GND	
	HDMI TXD0 N	P26	52	-+ <i>3</i> 51	S26	LVDS1_D0_P	-
	HDMI_TXD0_P	P27	54	53	S27	LVDS1 D0 N	-
	HDMI_HPD	P28	56	55	S28	GND	
HDMI	HDMI_TXD1_N	P29	58	57	S29	LVDS1_CLK_P	
	HDMI_TXD1_P	P30	60	59	S30	LVDS1_CLK_N	
	GND	P31	62	61	S31	GND	_
	HDMI_TXD2_N HDMI_TXD2_P	P32 P33	64 66	63 65	S32 S33	LVDS0_D3_P LVDS0_D3_N	-
	HDMI_TXD2_F	P34	68	67	S34	GPIO	-
	GND	P35	70	69	S35	LVDS0_D2_P	-
	ETH1_MD1_P	P36	72	71	S36	LVDS0_D2_N	
	ETH1_MD1_N	P37	74	73	S37	GND	
	GND	P38	76	75	S38	LVDS0_D1_P	LVDS #0
	ETH1_MD0_P	P39	78	77	S39	LVDS0_D1_N	
	ETH1_MD0_N	P40	80	79	S40	GND	-
Gigabit	ETH1_LINK1000 ETH1_ACT	P41 P42	82 84	81 83	S41 S42	LVDS0_D0_P LVDS0_D0_N	-
Ethernet #1	ETH1 LINK	P43	86	85	S43	GND	
Eulomotari	ETH1_MD3_N	P44	88	87	S44	LVDS0_CLK_P	
	ETH1_MD3_P	P45	90	89	S45	LVDS0_CLK_N	-
	GND	P46	92	91	S46	I2C-A_SDA	I2C-A
	ETH1_MD2_N	P47	94	93	S47	I2C-A_SCL	120-74
	ETH1_MD2_P	P48	96	95	S48	I2C-B_SDA	I2C-B
	GND	P49	98	97	S49	I2C-B_SCL	
	ETH2_MD1_P ETH2_MD1_N	P50 P51	100 102	99 101	S50 S51	HDMI/I2C-C_SDA HDMI/I2C-C_SCL	HDMI / I2C-C
	GND	P52	102	103	S52	TP_RST	
	ETH2_MD0_P	P53	106	105	S53	TP_IRQ	1
	ETH2_MD0_N	P54	108	107	S54	DISP_PWR_EN	Display Control
	ETH2_LINK1000	P55	110	109	S55	BL_PWR_EN	4
Gigabit	ETH2_ACT	P56	112	111	S56	BL_PWM	
Ethernet #2	ETH2_LINK	P57	114	113	\$57	GND	-
	ETH2_MD3_N ETH2 MD3 P	P58 P59	116 118	115 117	S58 S59	LCD_R0 LCD R1	-
	GND	P59 P60	120	117	S60	LCD_R1	1
	ETH2_MD2_N	P61	120	121	S61	LCD_R3	1.00
	ETH2_MD2_P	P62	124	123	S62	LCD_R4	LCD
	GND	P63	126	125	S63	LCD_R5	
	USB_01_DN	P64	128	127	S64	LCD_R6	
USB OTG #1	USB_01_DP	P65	130	129	S65	LCD_R7	-
	USB_01_0TG_ID	P66	132	131	S66	LCD_G0	

The table below lists the two board sides in the same table.

-	USB_O1_SSTXN USB_O1_SSTXP GND USB_O1_SSRXN	P67 P68 P69	134 136	133 135	S67 S68	LCD_G1 LCD G2	
	GND		136	135	568	1(1)(42	
			400	407		_	
			138	137	S69	LCD_G3	
		P70	140 142	139	S70	LCD_G4	
	USB_01_SSRXP USB_01_VBUS	P71 P72	142	141 143	\$71 \$72	LCD_G5 LCD G6	
	USB O1 PWR EN	P73	146	145	\$73	LCD G7	
	USB 01 OC	P74	148	147	S74	GND	
	Non existing pin		150	149	\$75	LCD B0	
	Non existing pin		152	151		Non existing pin	
	Non existing pin		154	153		Non existing pin	
	Non existing pin		156	155		Non existing pin	
	USB_H1_PWR_EN	P75	158	157	S76	LCD_B1	
	USB_H1_OC	P76	160	159	S77	LCD_B2	
	GND	P77	162	161	S78	LCD_B3	
_	USB_H1_DN	P78	164	163	S79	LCD_B4	
	USB_H1_DP	P79	166	165	S80	LCD_B5	
USB Host #1	USB_H1_SSTXN	P80	168	167	S81	LCD_B6	
_	USB_H1_SSTXP	P81	170	169	S82	LCD_B7	
-	GND	P82	172	171	S83	LCD_CLK	
-	USB_H1_SSRXN USB_H1_SSRXP	P83 P84	174 176	173 175	S84 S85	GPIO7 LCD HSYNC	
	USB_H1_SSRAP	P64 P85	176	175	S86	LCD_HSTNC LCD_VSYNC	
	USB H2 PWR EN	P86	180	179	S87	LCD_V3TRC	
	USB H2 OC	P87	182	181	S88	GND	
	GND	P88	184	183	S89	AIN VREF	
USB Host #2	USB H2 DN	P89	186	185	S90	AIN7	
	USB_H2_DP	P90	188	187	S91	AIN6	
	GND	P91	190	189	S92	AIN5	ADC
	COM board specific	P92	192	191	S93	AIN4	ADC
	COM board specific	P93	194	193	S94	AIN3	
	COM board specific	P94	196	195	S95	AIN2	
	COM board specific	P95	198	197	S96	AIN1	
_	COM board specific	P96	200	199	S97	AINO	
_	COM board specific	P97	202	201	S98	GND	
	COM board specific COM board specific	P98 P99	204 206	203 205	S99 S100	COM board specific COM board specific	
	COM board specific	P100	200	203	S100	GND	
-	COM board specific	P101	210	209	S102	COM board specific	
	COM board specific	P102	212	211	S103	COM board specific	
	COM board specific	P103	214	213	S104	GND	
	COM board specific	P104	216	215	S105	COM board specific	
specific	COM board specific	P105	218	217	S106	COM board specific	COM board specific
	COM board specific	P106	220	219	S107	COM board specific	
	COM board specific	P107	222	221	S108	COM board specific	
_	COM board specific	P108	224	223	S109	COM board specific	
_	COM board specific	P109	226	225	S110	COM board specific	
-	COM board specific	P110	228	227	S111	COM board specific	
	COM board specific	P111	230	229	S112	COM board specific	
	COM board specific COM board specific	P112 P113	232 234	231 233	S113 S114	COM board specific CSI_HSYNC	
	COM board specific	P113 P114	234	235	S114 S115	CSI_VSYNC	
	COM board specific	P115	230	233	S115	CSI_V3TNC	
-	COM board specific	P116	240	239	\$110 \$117	CSI_PCLK	
-	COM board specific	P117	242	241	S118	GND	
	GND	P118	244	243	S119	CSI_D0	
	SPI-B_SSEL	P119	246	245	S120	CSI_D1	Parallel Camera
SPI-B	SPI-B_MOSI	P120	248	247	S121	CSI_D2	
	SPI-B_MISO	P121	250	249	S122	CSI_D3	
	SPI-B_CLK	P122	252	251	S123	CSI_D4	
	SPI-A_SSEL	P123	254	253	S124	CSI_D5	
	SPI-A_MOSI	P124	256	255	S125	CSI_D6	
SPI-A	SPI-A_MISO	P125	258	257	S126	CSI_D7	
_	SPI-A_CLK	P126	260	259	S127	GND	
	GND	P127	262	261	S128	CSI_D3_M	
	UART-C_RXD	P128	264	263	S129	CSI_D3_P	Sorial Comoro
	UART-C_TXD UART-B RXD	P129 P130	266 268	265 267	S130 S131	GND CSI_D2_M	Serial Camera (CSI/MIPI)
_	UART-B_CTS	P130 P131	208	267	\$131 \$132	CSI_D2_M CSI D2 P	(00///////1)
UART-B	UART-B_CTS	P132	270	209	\$132 \$133	GND	
U-III-D	5. att D_110	P133	272	273	S133	CSI_D1_M	

UART-A	UART-A_RXD	P134	276	275	S135	CSI_D1_P	
	UART-A_CTS	P135	278	277	S136	GND	
	UART-A_RTS	P136	280	279	S137	CSI_D0_M	
	UART-A_TXD	P137	282	281	S138	CSI_D0_P	
PWM	PWM	P138	284	283	S139	GND	
GPIO	GPIO2	P139	286	285	S140	CSI_CLK_M	
GPIO	GPI01	P140	288	287	S141	CSI_CLK_P	
System	PERI_PWR_EN	P141	290	289	S142	GND	SATA
	RESET_IN	P142	292	291	S143	SATA_TX_P	
Control	RESET_OUT	P143	294	293	S144	SATA_TX_N	
	GND	P144	96	295	S145	GND	
	VBAT	P145	298	297	S146	SATA_RX_N	
	E2PROM_WP	P146	300	299	S147	SATA_RX_P	
Power Supply Input	VIN	P147	302	301	S148	GND	PCle
	VIN	P148	304	303	S149	GND	
	VIN	P149	306	305	S150	PCIE_CLK_P	
	VIN	P150	308	307	S151	PCIE_CLK_N	
	VIN	P151	310	309	S152	GND	
	VIN	P152	312	311	S153	PCIE_TX_P	
	VIN	P153	314	313	S154	PCIE_TX_N	
	VIN	P154	316	315	S155	GND	
	VIN	P155	318	317	S156	PCIE_RX_P	
	VIN	P156	320	319	S157	PCIE_RX_N	
				321	S158	GND	

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