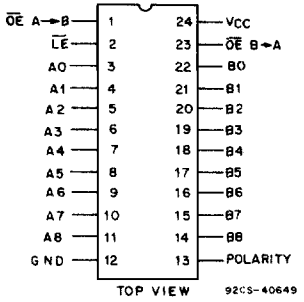
CD54/74HC7038
CD54/74HCT7038

File Number **1872**

High-Speed CMOS Logic



TERMINAL ASSIGNMENT

9-Bit Bus Transceiver With Latch

Type Features:

- *48 mA sink current*
- *Inverting and non-inverting data paths*
- *Open drain outputs*
- *Interface compatible with SCSI, multibus, and VME bus specifications*

The RCA-CD54/74HC7038 and the CD54/74HCT7038 are high-speed CMOS 9-bit bidirectional transceivers with input data latch and data polarity selection capability. These data-bus interface products are intended for two-way asynchronous communications between data buses. The 48 mA output sink current meets the drive requirements for the SCSI/Q-02, multibus, and VME bus specifications. The HC/HCT7038 devices feature the low power consumption of standard CMOS circuits and the speed and drive capabilities of LSTTL and TTL circuits.

The CD54/74HC7038 and CD54/74HCT7038 allow transmission and internal latch storage of 9 bits of positive or negative logic data from the "A" bus to the "B" bus. A low level on the Latch Enable input ($\overline{LE}$) stores "A" bus data in a 9 bit latch. When $\overline{LE}$ is a high level, the latch is transparent and data flows from "A" to "B". The "B" bus output data drivers are open drain N-MOS transistors that allow the "B" bus high logic state level to be set by the B bus termination network which may be the SCSI/Q-02 (220/330 ohm) or multibus/VME (dual 330/470 ohm) terminations. B-bus data may be transferred to the A-bus via appropriate $\overline{OE}$ control levels as shown in the Function Table.

Data polarity may be reversed in either direction as shown in the Function Table.

For the HC types, A-bus ports and control are compatible with CMOS logic levels. For the HCT types, the A-bus ports and control are compatible with CMOS or TTL logic levels. For both types, the B-bus ports are compatible with only TTL levels; the TTL high-logic-level must be set by the external bus termination network.

The CD54HC7038 and CD54HCT7038 are supplied in 24-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC7038 and CD74HCT7038 are supplied in 24-lead dual-in-line narrow body plastic packages (EN suffix) and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

FUNCTION TABLE

CONTROL INPUTS			OPERATION
$\overline{OE}$ A → B	$\overline{OE}$ B → A	POLARITY	
L	H	H	A_n to $\overline{B}_n$
L	H	L	A_n to B_n
H	L	H	B Data to A
H	L	L	B Data to $\overline{A}$
H	H	X	Isolation

When $\overline{LE}$ = L "A" data is latched
When $\overline{LE}$ = H latch is transparent
H = High Level; L = Low Level; X = Irrelevant

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < 0$ V or $V_I > V_{CC}$ + 0.5 V) ..... ±20 mA
DC INPUT VOLTAGE, V_I ..... -0.5 to V_{CC} +0.5 V
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < 0$ V or $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT VOLTAGE, V_O ..... -0.5 to V_{CC} +0.5 V
DC DRAIN CURRENT, PER OUTPUT, I_O, A SIDE ..... ±35 mA
B SIDE ..... ±50 mA
DC VCC CURRENT, I_{CC} ..... +200 mA
DC GROUND CURRENT, I_{GND} ..... -450 mA
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

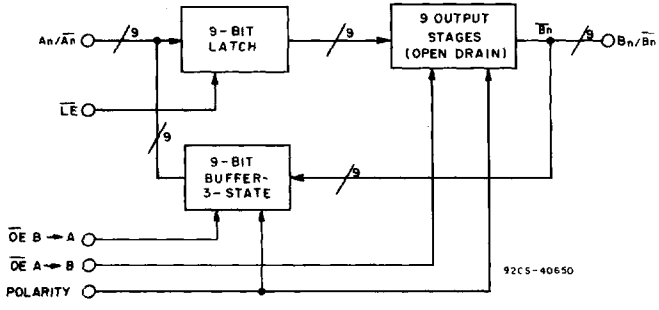

Fig. 1 - Logic block diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}: *	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f:	0	500	ns

* Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC7038/CD54HC7038									CD74HCT7038/CD54HCT7038								UNITS
	TEST CONDITIONS			74HC/54HC TYPE		74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/ 54HCT TYPE			74HCT TYPE		54HCT TYPE	
				+25°C		-40/+85°C		-55/+125°C				+25°C			-40/+85°C		-55/+125°C	
	V_I V	I_O mA	V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	V_I V	V_{CC} V	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	0.7 V_{CC}	—	0.7 V_{CC}	—	0.7 V_{CC}	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.3 V_{CC}	—	0.3 V_{CC}	—	0.3 V_{CC}	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage "A" Side V_{OH}	V_{IL} or V_{IH}	-0.02	4.5	4.4	—	4.4	—	4.4	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
		-6	4.5	3.98	—	3.84	—	3.7	—		4.5	3.98	—	—	3.84	—	3.7	—	
Low-Level Output Voltage "A" Side V_{OL}	V_{IL} or V_{IH}	0.02	4.5	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
		6	4.5	—	0.26	—	0.33	—	0.4		4.5	—	—	0.26	—	0.33	—	0.4	
"B" Side	V_{IL} or V_{IH}	0.02	4.5	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
		48	4.5	—	0.31	—	0.4	—	0.46		4.5	—	—	0.31	—	0.4	—	0.46	
Input Leakage Current I_I	$V_{I/O}$= V_{CC} or Gnd		5.5	—	±0.5	—	±5	—	±10	$V_{I/O}$= V_{CC} or Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	5.5	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}										V_I=2.4V Other Inputs: at V_{CC} or Gnd I_O = 0	5.5	—	100	390	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}		5.5	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

HCT Input Loading Table

Input	Unit Loads
All	1

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r,t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay A → B	t_{PLZ}, t_{PZL}	15	18	18	ns
A → $\overline{B}$	t_{PLZ}	15	17	17	ns
A → $\overline{B}$	t_{PZL}	15	15	15	ns
B → A	t_{PLH}, t_{PHL}	15	11	14	ns
B → $\overline{A}$	t_{PLH}, t_{PHL}	15	9	10	ns

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS +25° C HC Min.	+25° C HC Max.	+25° C HCT Min.	+25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
$\overline{LE}$ Pulse Width	t_W	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	ns
		6	10	—	—	—	13	—	—	—	15	—	—	—	ns
Set-up Time Data to $\overline{LE}$	t_{SU}	2	35	—	—	—	45	—	—	—	55	—	—	—	ns
		4.5	7	—	7	—	9	—	9	—	11	—	11	—	ns
		6	6	—	—	—	8	—	—	—	9	—	—	—	ns
Hold Time Data to $\overline{LE}$	t_H	2	35	—	—	—	45	—	—	—	55	—	—	—	ns
		4.5	7	—	7	—	9	—	9	—	11	—	11	—	ns
		6	6	—	—	—	8	—	—	—	9	—	—	—	ns

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SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS	LIMITS												UNITS
			+25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay A to B	t_{PLZ}, t_{PZL}	2	—	220	—	—	—	275	—	—	—	330	—	—	ns
		4.5	—	44	—	44	—	55	—	55	—	66	—	66	
		6	—	37	—	—	—	47	—	—	—	56	—	—	
	t_{PLZ}	2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	40	—	50	—	50	—	60	—	60	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
A to $\overline{B}$	t_{PZL}	2	—	180	—	—	—	225	—	—	—	270	—	—	
		4.5	—	36	—	36	—	45	—	45	—	54	—	54	
		6	—	31	—	—	—	38	—	—	—	46	—	—	
$\overline{LE}$ to $\overline{B}$n	t_{PLZ}	2	—	260	—	—	—	325	—	—	—	390	—	—	
		4.5	—	52	—	52	—	65	—	65	—	78	—	78	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
Polarity Low	t_{PZL}	2	—	230	—	—	—	290	—	—	—	345	—	—	
		4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
Polarity High	t_{PLZ}, t_{PZL}	2	—	230	—	—	—	290	—	—	—	345	—	—	
		4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
$\overline{OE}$ A → B Disable	t_{PLZ}	2	—	170	—	—	—	215	—	—	—	255	—	—	
		4.5	—	34	—	34	—	43	—	43	—	51	—	51	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
Enable	t_{PZL}	2	—	170	—	—	—	215	—	—	—	255	—	—	
		4.5	—	34	—	34	—	43	—	43	—	51	—	51	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
B to A	t_{PLH}, t_{PHL}	2	—	140	—	—	—	175	—	—	—	210	—	—	
		4.5	—	28	—	28	—	35	—	35	—	42	—	42	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
B to $\overline{A}$	t_{PLH}, t_{PHL}	2	—	120	—	—	—	150	—	—	—	180	—	—	
		4.5	—	24	—	26	—	30	—	33	—	36	—	39	
		6	—	20	—	—	—	26	—	—	—	31	—	—	
$\overline{OE}$ B → A Disable	t_{PLZ}, t_{PHZ}	2	—	185	—	—	—	230	—	—	—	280	—	—	
		4.5	—	37	—	37	—	46	—	46	—	56	—	56	
		6	—	31	—	—	—	39	—	—	—	48	—	—	
Enable	t_{PZL}	2	—	175	—	—	—	220	—	—	—	265	—	—	
	t_{PZH}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	39	—	—	—	45	—	—	

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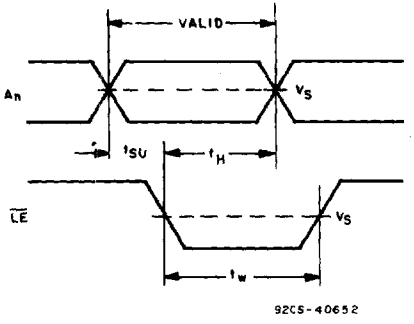


Fig. 2 - Latch enable pulse width, setup and hold times.

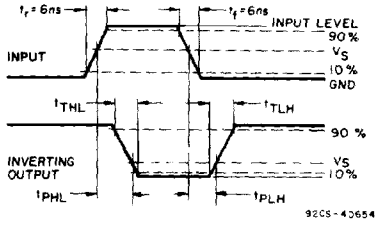
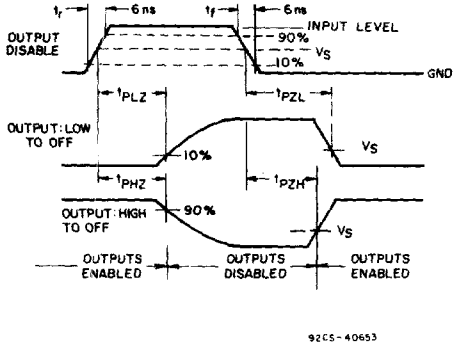
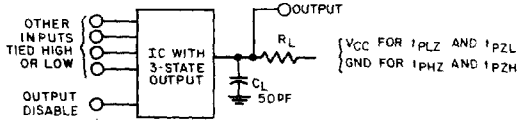


Fig. 3 - Transition times and propagation delay times, combination logic.





	V_{CC}	R_L
Side A	**4.5 V**	**1k Ω**
Side B	**3 V**	**133 Ω**

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Fig. 4 - Three-state propagation delay wave shapes and test circuit.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

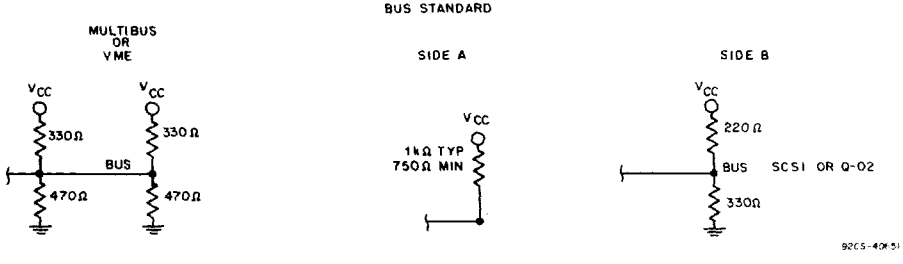

Fig. 5 - Recommended bus terminations.