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20855

MARKING (example only)



Bar = cathode marking

X = date code

Y = type code (see table below)

DESIGN SUPPORT TOOLS



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Ultra compact LLP1006-2L package Low package height < 0.4 mm 1-line ESD protection

FEATURES

- Low leakage current < 0.2 μA
- Low load capacitance C_D = 38 pF $(V_R = 2.5 V; f = 1 MHz)$
- ESD immunity acc. IEC 61000-4-2 ± 30 kV contact discharge ± 30 kV air discharge



- Soldering can be checked by standard vision inspection. No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- PATENT(S): www.vishay.com/patents
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

ORDERING INFORMATION				
DEVICE NAME ORDERING CODE		TAPED UNITS PER REEL (8 mm TAPE on 7" REEL)	MINIMUM ORDER QUANTITY	
VESD05A1C-HD1	VESD05A1C-HD1-GS08	8000	8000	

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD05A1C-HD1	LLP1006-2L	F	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS VESD05A1C-HD1						
PARAMETER	TEST CONDITIONS	TEST CONDITIONS SYMBOL		UNIT		
Peak pulse current	Acc. IEC 61000-4-5; $t_P = 8/20 \ \mu s$; single shot	I _{PPM}	8	A		
Peak pulse power	Acc. IEC 61000-4-5; $t_P = 8/20 \ \mu s$; single shot	P _{PP}	80	W		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	N/	± 30	kV		
	Air discharge acc. IEC 61000-4-2; 10 pulses	V _{ESD}	± 30	kV		
Operating temperature	Junction temperature	TJ	-40 to +125	°C		
Storage temperature		T _{stg}	-55 to +150	°C		

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

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BIAs-MODE (bidirectional asymmetrical protection mode)

With the VESD05A1C-HD1 one signal- or data-lines (L1) can be protected against voltage transients. With pin 1 connected to ground and pin 2 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage (V_{RWM}) the protection diode between data line and ground offers a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage (V_C) is defined by the breakthrough Voltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device. Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the VESD05A1C-HD1 clamping behaviour is bidirectional and asymmetrical (BiAs).

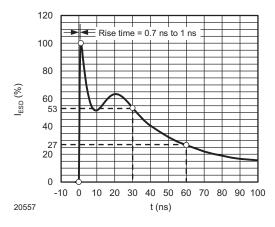


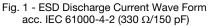
(T _{amb} = 25 °C, unless otherwise specified)								
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Protection paths	Number of lines which can be protected	N _{channel}	-	-	1	lines		
Reverse stand-off voltage	Max. reverse working voltage	V _{RWM}	-	-	5	V		
Reverse voltage	At I _R = 0.2 μA	V _R	5	-	-	V		
Reverse current	At V _R = 5 V	I _R	-	0.03	0.2	μA		
Reverse breakdown voltage	At I _R = 1 mA	V _{BR}	6	6.7	8	V		
Reverse clamping voltage	At I _{PP} = 1 A	V _C	-	7.1	8.	V		
	At I _{PP} = I _{PPM} = 8 A	V _C	-	9.3	10	V		
Forward clamping voltage	At I _{PP} = 0.2 A	V _F	-	0.95	1.2	V		
	At I _{PP} = 1 A	V _F	-	1.1	1.5	V		
	At I _{PP} = I _{PPM} = 8 A	V _F	-	1.9	-	V		
Capacitance	At $V_R = 0 V$; f = 1 MHz	CD	-	63	75	pF		
	At V _B = 2.5 V; f = 1 MHz	CD	-	38	-	pF		





TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)





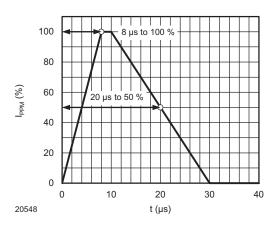


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form (acc. IEC 61000-4-5)

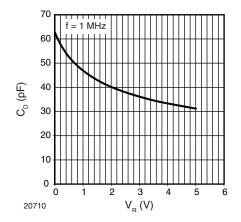


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

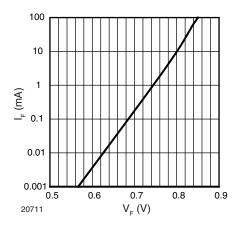


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

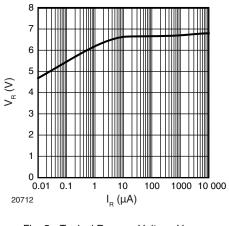


Fig. 5 - Typical Reverse Voltage $V_{\rm R}$ vs. Reverse Current $I_{\rm R}$

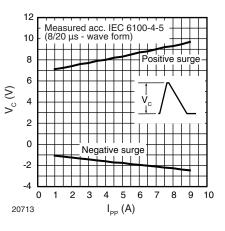


Fig. 6 - Typical Clamping Voltage vs. Peak Pulse Current I_{PP}

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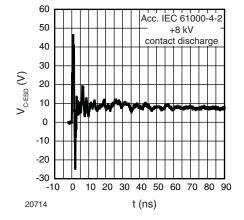
3 For technical questions, contact: <u>ESDprotection@vishay.com</u> Document Number: 81798

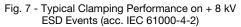
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VESD05A1C-HD1

Vishay Semiconductors





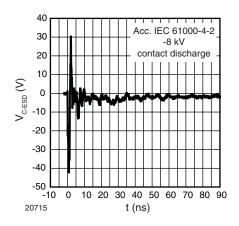
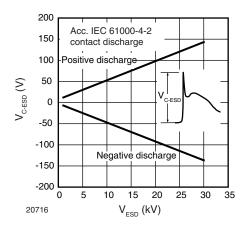
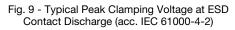


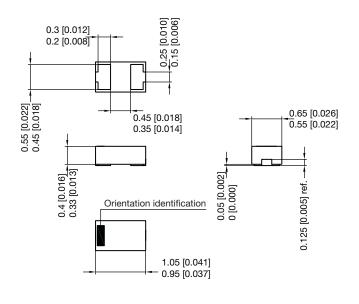
Fig. 8 - Typical Clamping Performance on - 8 kV ESD Events (acc. IEC 61000-4-2)



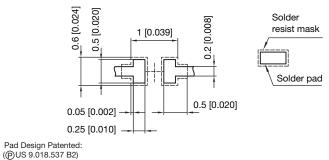




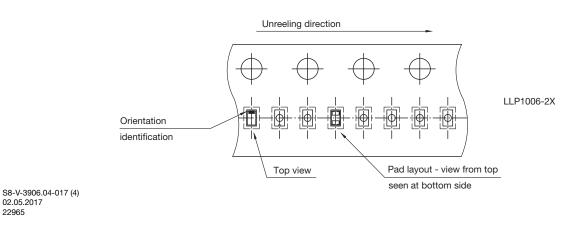
PACKAGE DIMENSIONS in millimeters (inches): LLP1006-2L



Foot print recommendation:



Document no.: S8-V-3906.04-005 (4) Rev. 7 - Date: 11.May 2016 20812



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