EAPP Hybrid Digital 4-Phase Green PWM Controller for Digital Power Management of Core and Memory With AUTO Phase Shedding

ISL6381

The ISL6381 is an EAPP Hybrid Digital 4-Phase PWM controller and is designed to be compliant to Intel VR12.5/VR12 specifications and control the microprocessor core or memory voltage regulator. It includes programmable functions and telemetries for easy use, high system flexibility and overclocking applications using SMBus, PMBus, or I^2C interface, which is designed to be conflict free with CPU's SVID bus. This hybrid digital approach eliminates the need of NVM and Firmware often seen in a full digital solution and significantly reduces design complexity, inventory and manufacturing costs.

The ISL6381 utilizes Intersil's proprietary Enhanced Active Pulse Positioning (EAPP) modulation scheme to achieve the extremely fast transient response with fewer output capacitors. The ISL6381 accurately monitors the load current via the IMON pin and reports this information via the I_{OUT} register to the microprocessor, which sends a PSI# signal to the controller at low power mode via SVID bus. The controller enters 1- or 2-phase operation in low power mode (PSI1); in the ultra low power mode (PSI2, PSI3), it operates in single phase with diode emulation option. In low power modes, the magnetic core and switching losses are significantly reduced, yielding high efficiency at light load. After the PSI# signal is deasserted, the dropped phase(s) are added back to sustain heavy load transient response and efficiency. In addition, the ISL6381 features auto-phase shedding to optimize the efficiency from light to full load for Green Environment without sacrificing the transient performance.

Today's microprocessors require a tightly regulated output voltage position versus load current (droop). The ISL6381 senses the output current continuously by measuring the voltage across a dedicated current sense resistor or the DCR of the output inductor. The sensed current flows out of the FB pin to develop the precision voltage drop across the feedback resistor for droop control. Current sensing circuits also provide the needed signals for channel-current balancing, average overcurrent protection and individual phase current limiting. The TM pin senses an NTC thermistor's temperature, which is internally digitized for thermal monitoring and for integrated thermal compensation of the current sense elements of the regulator.

The ISL6381 features remote voltage sensing and completely eliminates any potential difference between remote and local grounds. This improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start-up of the ISL6381 with other voltage rails.

Features

- Intel VR12.5/VR12 compliant
  - SerialVID with programmable IMAX, TMAX, BOOT, ADDRESS OFFSET registers
  - VR12.5 core and VR12/VR12.5 memory
- Intersil's proprietary EAPP Hybrid Digital Enhanced Active Pulse Positioning (EAPP) Modulation Scheme (Patented)
  - SMBus/PMBus/I^2C interface with SVID conflict free
  - NVM and firmware free for low cost and easy use
  - Auto phase shedding option for greener environment
  - Variable frequency control during load transients to reduce beat frequency oscillation
  - Linear control with evenly distributed PWM pulses for better phase current balance during load transients
  - Voltage feed-forward and ramp adjustable options
  - High frequency and PSI compensation options
  - Proprietary active phase adding and dropping with diode emulation scheme for enhanced light load efficiency
- 1 to 4-Phase with phase doubler compatibility
- Differential remote voltage sensing
- ±0.5% closed-loop system accuracy over load, line and temperature
- Programmable 1 or 2-phase operation in PSI1 mode
- Programmable slew rate of fast dynamic VID with Dynamic VID Compensation (DVC)
- Droop and diode emulation options
- Precision resistor or DCR differential current sensing
  - Integrated programmable current sense resistors
  - Accurate load-line (droop) programming
  - Accurate current monitoring and channel-current balancing
- True Catastrophic Failure Protection (CFP)
- Average overcurrent protection and channel current limit with internal current comparators
- Precision overcurrent protection on IMON pin
- Output voltage open sensing protection
- Protection disable option
- Accurate load-line (droop) programming
- Up to 2MHz per phase
- Thermal monitoring and integrated compensation
- Start-up into precharged load
- Pb-free (RoHS compliant)
- 40 Ld 5x5 TQFN

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Ordering Information

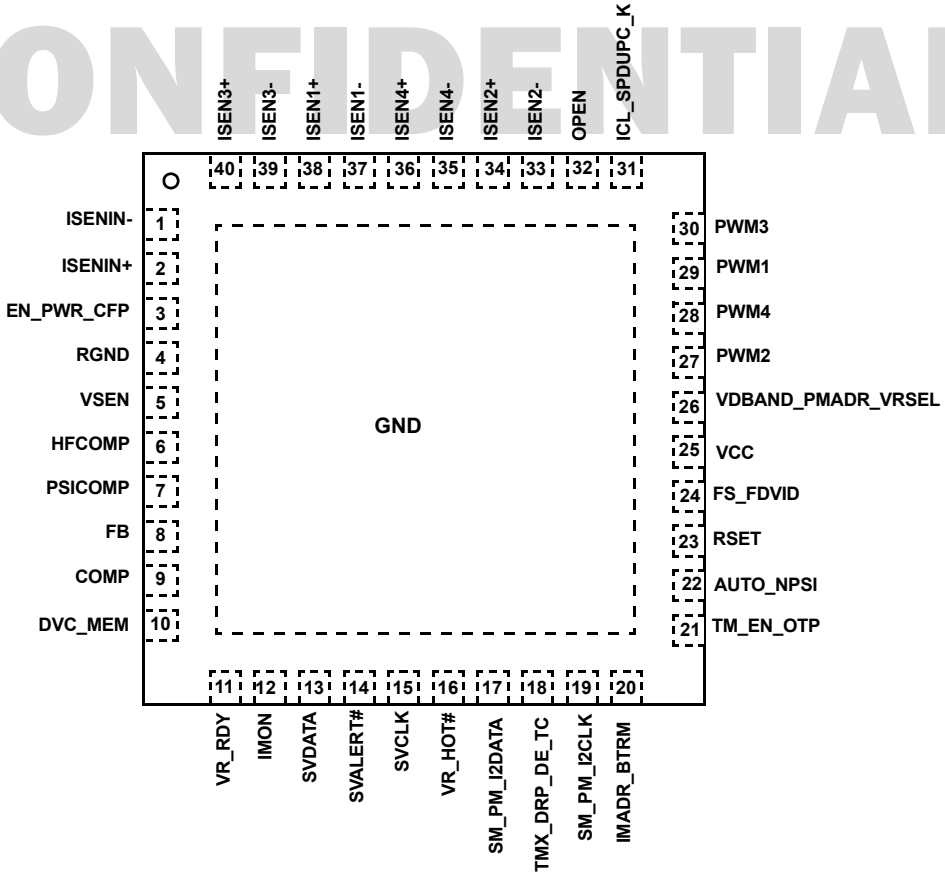
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6381CRTZ	ISL6381 CRTZ	0 to +70	40 Ld 5x5 TQFN	L40.5x5

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on MSL, please see tech brief TB363.

Pin Configuration

ISL6381
(40 LD 5X5 TQFN)
TOP VIEW

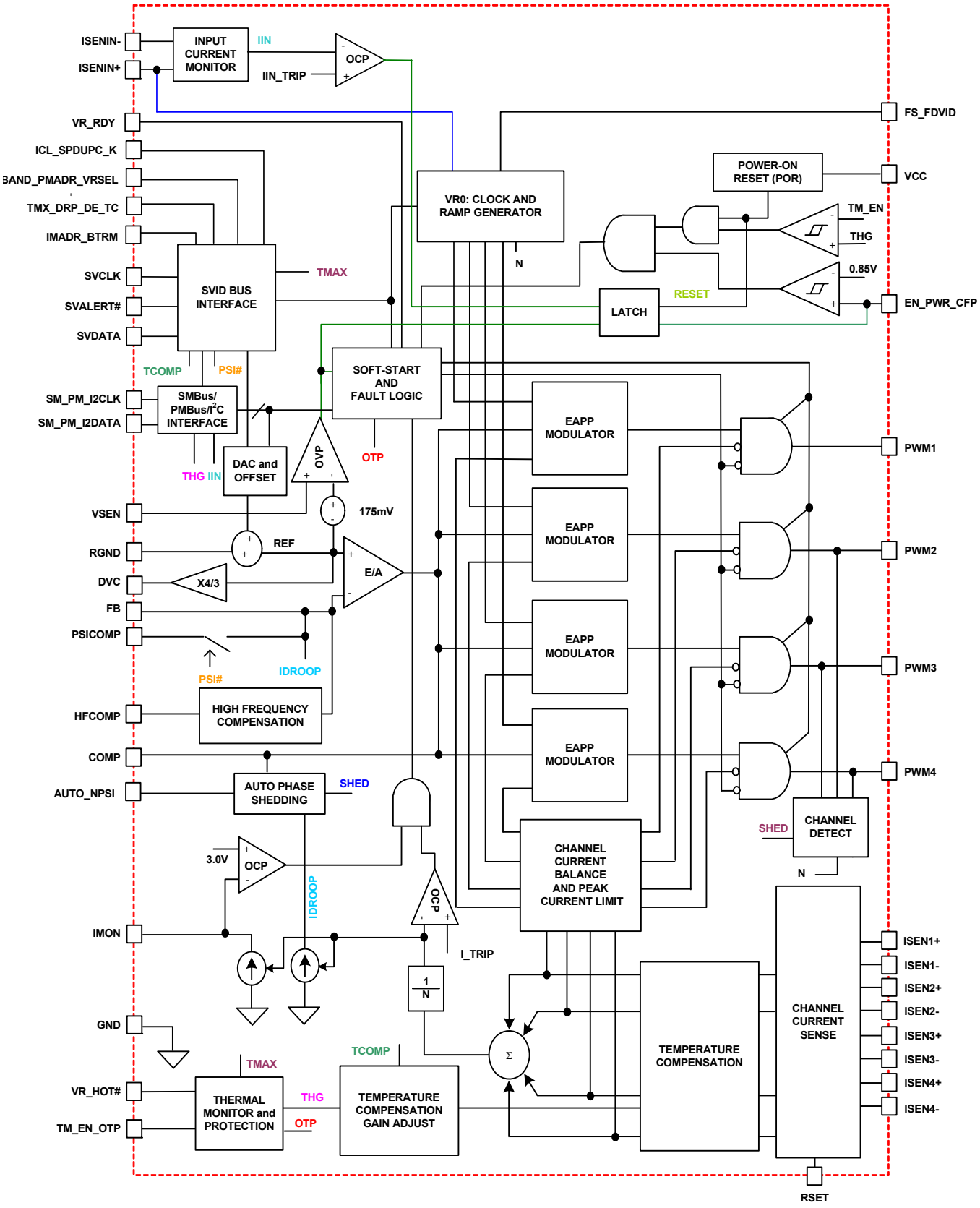


Driver Recommendation

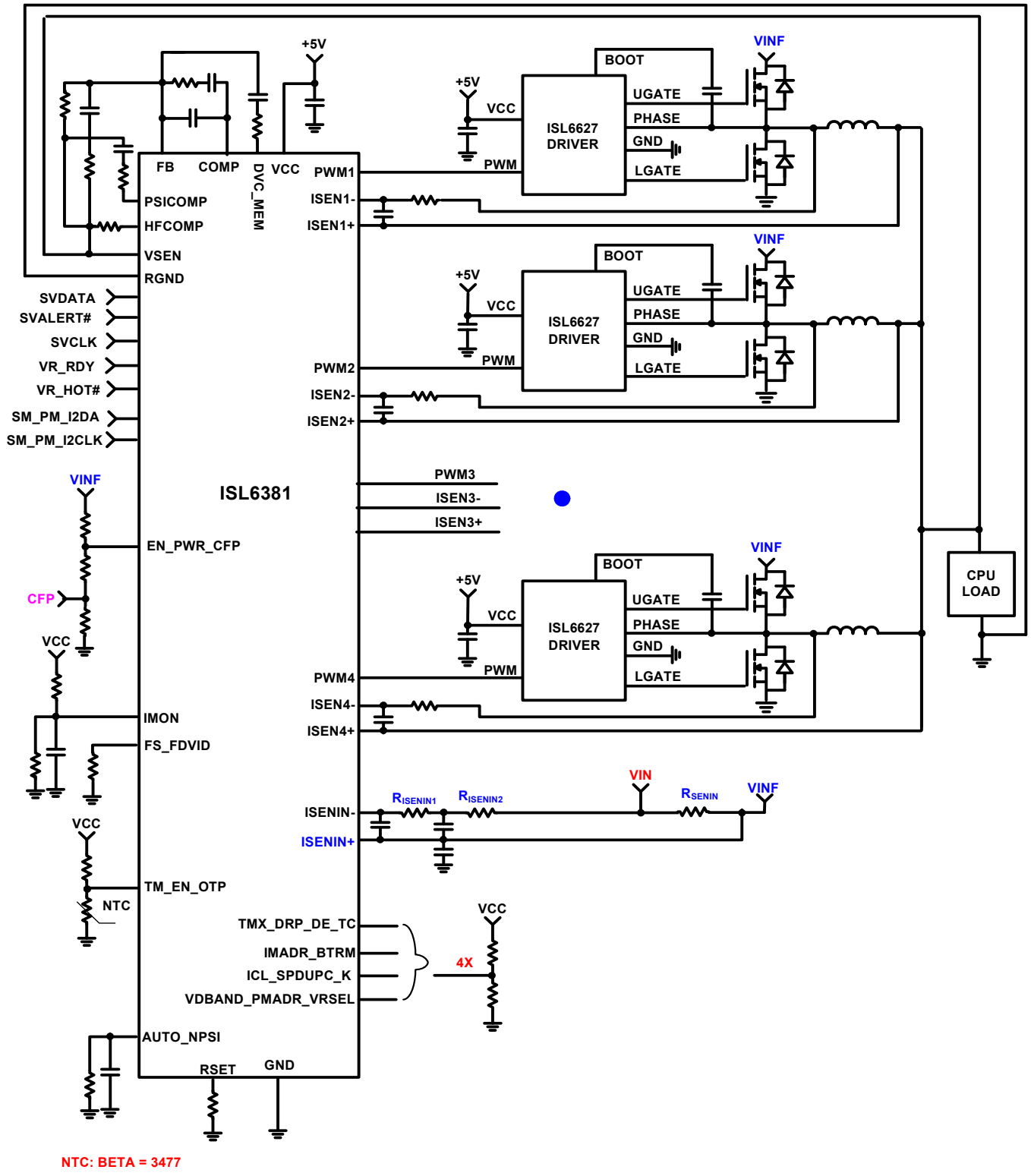
DRIVER	QUIESCENT CURRENT (mA)	GATE DRIVE VOLTAGE	# OF DRIVERS	DIODE EMULATION (DE)	GATE DRIVE DROP (GVOT)	COMMENTS
ISL6627	1.0	5V	Single	Yes	No	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels.
ISL6620 ISL6620A	1.2	5V	Single	Yes	No	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels. Shorter body diode conduction time when entering PSI2 mode at a fixed voltage.
ISL6596	0.19	5V	Single	No	No	For dropped phases or all channels without DE.
ISL6610 ISL6610A	0.24	5V	Dual	No	No	For dropped phases or all channels without DE.
ISL6611A	1.25	5V	Dual	No	No	Phase Doubler with Integrated Drivers, up to 12-Phase. For all channels with DE Disabled.
ISL6617	5.0	N/A	N/A	No	No	PWM Doubler for DrMOS, up to 12- or 24-Phase. For all channels with DE Disabled.
ISL6622	5.5	12V	Single	Yes	Yes	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels. Shorter body diode conduction time when entering PSI2 mode at a fixed voltage.
ISL6622A ISL6622B	5.5	12V	Single	Yes	No Yes	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels. Shorter body diode conduction time when entering PSI2 mode at a fixed voltage.

NOTE: Intersil 5V and 12V drivers are mostly pin-to-pin compatible and allow for dual footprint layout implementation to optimize MOSFET selection and efficiency. The 5V Drivers are more suitable for high frequency and high power density applications.

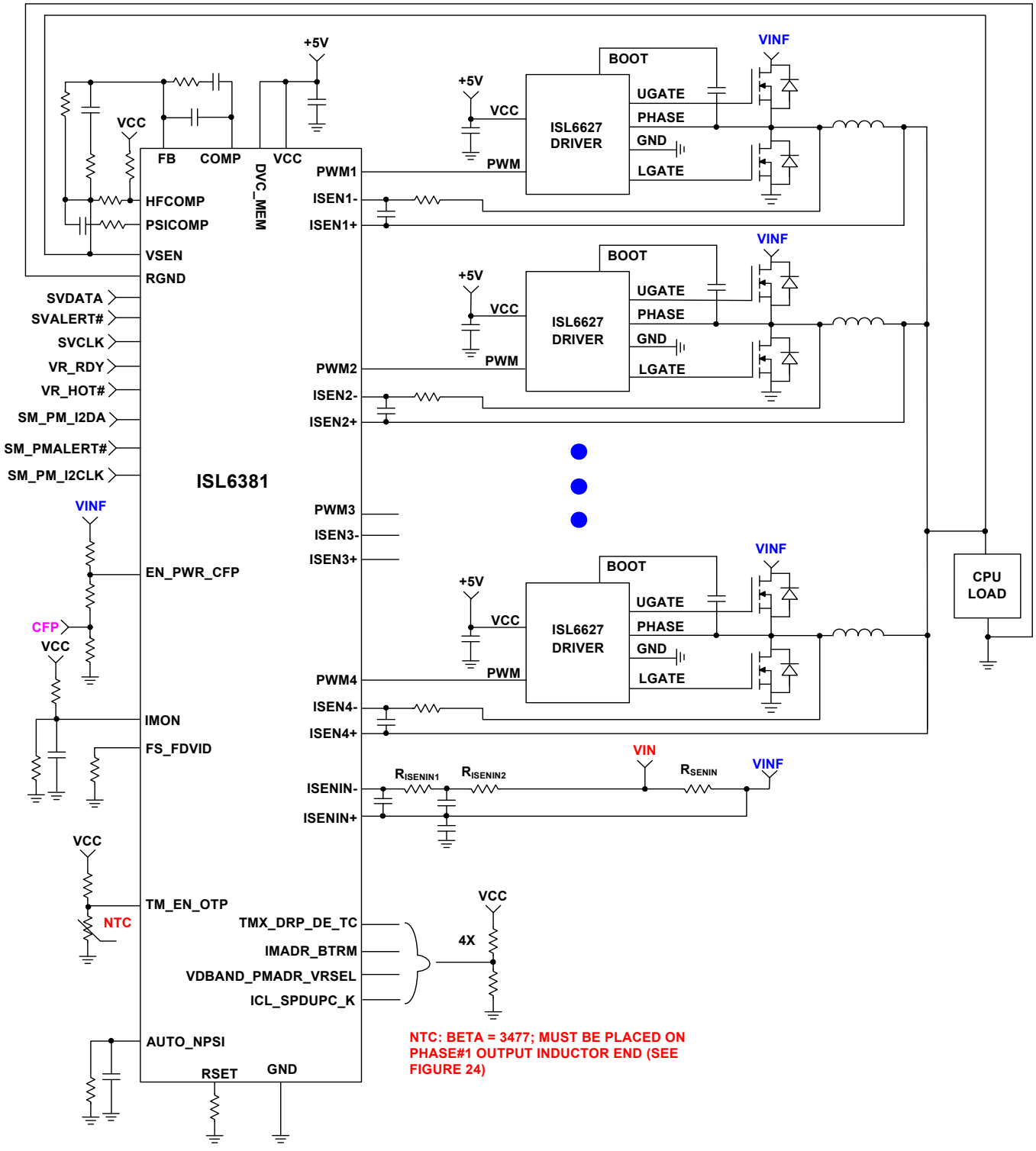
ISL6381 Internal Block Diagram



Typical Application: 4-Phase Core VR



Typical Application: 4-Phase Memory VR



Absolute Maximum Ratings

VCC, VR_RDY . . . . . +6V
ISENIN± . . . . . .GND -0.3V to 27V
All Other Pins . . . . . .GND -0.3V to V_{CC} + 0.3V
ESD Rating
Human Body Model 2.5kV
Charged Device Model 1kV
Machine Model 250V

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld 5x5 TQFN Package	31	2.5

Maximum Junction Temperature . . . . . .+150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Pb-Free Reflow Profile TB493

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . .+5V ±5%
Ambient Temperature
ISL6381CRTZ . . . . . 0°C to +70°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply over the operating temperature range.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	V_{CC} = 5VDC; EN_PWR = 5VDC; R_T = 125kΩ, ISEN1-4 = 0µA	**18**	22	**24**	mA
Shutdown Supply	V_{CC} = 5VDC; EN_PWR = 0VDC; R_T = 125kΩ	**14**	18	**21**	mA
POWER-ON RESET AND ENABLE					
V_{CC} Rising POR Threshold		**4.30**	4.40	**4.50**	V
V_{CC} Falling POR Threshold		**4.00**	4.11	**4.20**	V
EN_PWR_CFP High Level Turn-OFF Threshold	Externally Driven	**3.55**	3.63	**3.70**	V
EN_PWR_CFP High Level Turn-ON Threshold	Externally Driven	**3.33**	3.47	**3.53**	V
EN_PWR_CFP Latch-OFF Level	Internally Driven, 5mA Load	**4.80**			V
EN_PWR_CFP Internal Pull-Up Impedance			12	**34**	Ω
EN_PWR_CFP Rising Threshold		**0.830**	0.850	**0.870**	V
EN_PWR_CFP Falling Threshold		**0.730**	0.750	**0.770**	V
DAC (VID+OFFSET)					
System Accuracy of ISL6381CRTZ (DAC = 1.5V to 3.04 V, T_J = 0°C to +70°C)	(Note 6, Closed-Loop)	**-0.5**	-	**0.5**	%VID
System Accuracy of ISL6381CRTZ (DAC = 0.8V to 1.49V, T_J = 0°C to +70°C)	(Note 6, Closed-Loop)	**-5**	-	**5**	mV
System Accuracy of ISL6381CRTZ (DAC = 0.25V to 0.795V, T_J = 0°C to +70°C)	(Note 6, Closed-Loop)	**-8**	-	**8**	mV
OSCILLATORS					
Accuracy of Switching Frequency Setting	R_{FS} = 125kΩ	**360**	400	**440**	kHz
Maximum Switching Frequency		**2.0**			MHz
Minimum Switching Frequency				**0.08**	MHz

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Soft-start Ramp Rate	FDVID = 10mV/µs	**2.5**	2.75	**3.2**	mV/µs
	FDVID = 20mV/µs	**5.0**	5.5	**6.0**	mV/µs
Fast Dynamic VID Slew Rate Range	Programmable via PMBus	**10**		**53**	mV/µs
Maximum Duty Cycle Per PWM	400kHz	**95**	98	**99**	%
PWM GENERATOR (Note 7)					
Sawtooth Amplitude	VR_{RAMP_ADJ} = 1.2V; ISENIN+ = 12V		1.2		V
	VR_{RAMP_ADJ} = 1.5V; ISENIN+ = 12V		1.5		V
Maximum Adjustable Ramp	Via PMBus or Pin		1.5		V
Minimum Adjustable Ramp	Via PMBUs		0.75		V
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground		96		dB
Open-Loop Bandwidth			80		MHz
Slew Rate			25		V/µs
Maximum Output Voltage	No Load	**4.1**	4.4		V
Output High Voltage	1mA Load	**3.8**	4.1		V
Output Low Voltage	1mA Load	**0.85**	1.00	**1.50**	V
PWM OUTPUT (PWM[4:1]					
PWM[4:1] Sink Impedance	PWM = Low with 1mA, Load for Fast Transition		80		Ω
	PWM = Low with 1mA Load	**190**	285	**410**	Ω
PWM[4:1] Source Impedance	PWM = High, Forced to 3.7V	**95**	125	**175**	Ω
PWM PSI1/2/3/Decay Mid-Level	0.4mA Load	**36**	40	**44**	%VCC
CURRENT SENSE AND OVERCURRENT PROTECTION					
Sensed Current Tolerance	ISEN1-4 = 40µA; CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	**37**	40	**43.5**	µA
	ISEN1-4 = 80µA; CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	**76**	80	**84**	µA
Average Overcurrent Trip Level at Normal CCM PWM Mode	CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	**94**	100	**106**	µA
Average Overcurrent Trip Level at PSI1/2/3 Mode	N = 4 Drop to 1-Phase	**96**	108	**121**	µA
Average Overcurrent Trip Level at PSI1 Mode	N = 4 Drop to 2-Phase	**91**	103	**113**	µA
Peak Current Limit for Individual Channel			125		µA
IMON OCP Trip Level		**2.9**	3.0	**3.1**	V
IMON Voltage IMAX (FF) Trip Point	Higher than this will be “FF”	**2.45**	2.5	**2.56**	V
READ_IIN (1F) Maximum Threshold			10		µA
Input Peak Current Trip Level		**14**	15	**16**	µA
Maximum Common Mode Input			VCC-1.5V		
THERMAL MONITORING					
VR_HOT# Pull-down Impedance			7	**13**	Ω
TM Voltage at Thermal Trip (Programmable via TMAX)	TMAX = +100°C, (see Table 7)		39.12		%VCC

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VR_HOT# and Thermal Alert# Hysteresis			3		°C
Leakage Current of VR_HOT#	With external pull-up resistor connected to V_{CC}			**1**	µA
TM_EN_OTP Shutdown Threshold		**0.85**	0.95	**1.05**	V
TM_EN_OTP Turn-ON Threshold		**0.98**	1.08	**1.18**	V
VR READY AND PROTECTION MONITORS					
Leakage Current of VR_RDY	With pull-up resistor externally connected to V_{CC}			**1**	µA
VR READY Low Voltage	4mA Load			**0.3**	V
Overvoltage Protection Threshold	Prior to the End of Soft-start		2.15		V
	After the End of Soft-start, the voltage above VID		175		mV
	After the End of Soft-start, the voltage above VID		350		mV
Overvoltage Protection Reset Hysteresis			100		mV
SVID BUS					
ALERT# Pull-down Impedance			7	**13**	Ω
SVDATA			7	**13**	Ω
SVCLK Maximum Speed at Room Temperature	T_J = +25°C		60		MHz
SVCLK Maximum Speed			43		MHz
SVCLK Minimum Speed			13		MHz
SMBus/PMBus/I^2C					
DATA Pull-down Impedance			28	**40**	Ω
CLOCK Maximum Speed			1.5		MHz
CLOCK Minimum Speed			0.05		MHz
Timeout		**25**	32	**35**	ms

NOTES:

6. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Functional Pin Descriptions

Refer to Table 25 on page 48, for Design and Layout Considerations.

VCC - Supplies the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply with a high quality ceramic bypass capacitor.

GND - The bottom metal base of ISL6381 is the GND, bias and reference ground for the IC. It is also the return for all PWM output drivers.

EN_PWR_CFP - This pin is a threshold-sensitive enable input and a catastrophic failure protection (CFP) output for controller. Connecting the power train input supply to this through an appropriate resistor divider provides a means to synchronize the power sequencing of the controller and the MOSFET driver ICs. When EN_PWR_CFP is driven above 0.85V but below 3.3V, the controller is actively depending on status of the TM_EN_OTP, the internal POR, and pending fault states. Driving EN_PWR_CFP below 0.75V will turn off the controller, clear all fault states (except for CFP latch up) and prepare the ISL6381 to soft-start when re-enabled. In addition, this pin will be latched high (VCC) by the input overcurrent event (monitored by ISENIN±) or VR overvoltage event. The latch resets by cycling VCC and cannot reset by TM_EN_OTP or EN_PWR_CFP since when the catastrophic failure (CFP) is triggered, the power is removed from VR so is the VTT voltage rail and its PGOOD signal. This feature means to provide protection to the case that the shorted high-side MOSFET VR draws insufficient current to trigger the input supply's over current trip level, this pin will send an active high signal (CFP) to disconnect the input supply before catching fire. When this pin is driven above 3.7V externally, the controller turns off.

VSEN - This pin monitors the regulator output for overvoltage protection. Connect this pin to the positive rail remote sensing point of the microprocessor or load. This pin tracks with the FB pin. If a resistive divider is placed on the FB pin, a resistive divider with the same ratio should be placed on the VSEN pin. Tie to GND if not used.

RGND - This pin compensates the offset between the remote ground of the load and the local ground of this device. Connect this pin to the negative rail remote sensing point of the microprocessor or load. Tie to GND if not used.

COMP and FB - The COMP and FB are the output and inverting input of the precision error amplifier, respectively. A type III loop compensation network should be connected to these pins, while the FB's R-C network should connect to the positive rail remote sensing point of the microprocessor or load. Combined with RGND, the potential difference between remote and local rails is completely compensated for and it improves regulation accuracy. A properly chosen resistor between FB and remote sensing point can set the load-line (droop, if enabled). The droop scale factor is set by the ratio of the effective ISEN resistors (set by RSET) and the inductor DCR or the dedicated current sense resistor. The COMP is tied back to FB through an external R-C network to compensate the regulator. An RC from the FB pin to ground is needed if the output is lagging from the DAC, typical of applications with many output capacitors and droop enabled.

VR_RDY_ VR_RDY indicates that soft-start has completed and the output remains in normal operation. It is an open-drain logic output. When OCP or OVP occurs, VR_RDY is pulled low.

TM_EN_OTP - The input pin for the temperature measurement. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is inversely proportional to the VR temperature. The device monitors the VR temperature based on the voltage at the TM pin. Combined with the "TCOMP" setting, the sensed current is thermally compensated. The VR_HOT# asserts low if the sensed temperature at this pin is higher than the maximum desired temperature, "TMAX". The NTC should be placed close to the current sensing element, the output inductor or dedicated sense resistor on Phase 1. A decoupling capacitor (0.1µF) is typically needed in close proximity to the controller. In addition, the controller is disabled when this pin's voltage drops below 0.95 (typically) and is active when it is above 1.08V (typically); it can serve as enable and over-temperature functions, however, when it is used as an enable toggle input, bit2 of STATUS_BYTE (78h) will flag OT; CLEAR_FAULTS (03h) command must be sent to clear the fault after VR start-up. If not used, connect a 1MΩ/2MΩ resistor divider or tie to VCC.

VR_HOT# - Indicator of high VR temperature. It is an open-drain logic output. Normally open if the measured VR temperature is less than a certain level, and pulled low when the measured VR temperature reaches a certain level.

PWM[4:1] - Pulse width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver IC(s). The number of active channels is determined by the state of PWM[4:2]. Tie PWM(N+1) to VCC to configure for N-phase operation. The PWM firing order is sequential from 1 to N with N being the number of active phases. If PWM1 is tied high, the respective address is released for use, i.e, the VR is disabled and does not respond to the SVID commands.

ISEN[4:1]+, ISEN[4:1] - The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers of VR. The sensed current is used for channel current balancing, overcurrent protection, and droop regulation. Inactive channels should have their respective current sense inputs, ISEN[4:#]- grounded, and ISEN[4:#]+ open. For example, ground ISEN[4:3]- and open ISEN[4:3]+ for 2-phase operation. DO NOT ground ISEN[4:1]+. For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor (typically output rail). The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sensed current is proportional to the inductor current and scaled by the DCR of the inductor and R_{SET}.

RSET- A resistor connected from this pin to ground sets the current gain of the current sensing amplifier. The R_{SET} resistor value can be set from 3.84kΩ to 60.4kΩ and is 64x of the equivalent R_{ISEN} resistor value. Therefore, the effective current sense resistor value can be set between 60Ω and 943Ω.

IMON - MON is the output pin of sensed, thermally compensated (if internal thermal compensation is used) average current of VR. The voltage at the IMON pin is proportional to the load current and the

resistor value. When it reaches to 3.0V, it initiates an overcurrent shutdown, while 2.5V IMON voltage corresponds to I_{OUT} (15h) of FFh reading. By choosing the proper value for the resistor at IMON pin, the overcurrent trip level can be set lower than the fixed internal overcurrent threshold. During dynamic VID, the OCP function of this pin is disabled to avoid false triggering. Tie it to GND if not used. See "Current Sense Output" on page 25 for more details.

AUTO_NPSI - A paralleling resistor and capacitor from the pin to ground sets the current threshold and hysteresis of phase dropping. The AUTO mode can be disabled by pulling this pin to ground or VCC. This pin also sets the operating phase number option (NPSI) in low power mode. See Table 3 on page 16 on and Table 14 on page 35 for more details.

FS_FDVID - A resistor placed from this pin to GND/VCC will set the switching frequency. The relationship between the resistor value of the resistor and the switching frequency is approximated by Equation 4 on page 16. When the resistor is connected to GND, it sets the fast Dynamic VID rate 20mV/µs for V_{CORE} Mode (DVC_MEM = RC or Open); 10mV/µs for Memory Mode (DVC_MEM = V_{CC}); when the resistor is connected to V_{CC}, it sets the fast Dynamic VID rate 10mV/µs, typically used for desktop applications.

HFCOMP - Connect a resistor of the same or slightly higher (~ 150%) value as the feedback impedance (R_{FB}) to the VR output to compensate the level-shifted output voltage during high-frequency load transient events. Connecting more than 3x of R_{FB} to this pin virtually disables this feature. When the droop disabled, an additional 499kΩ (typically) from this pin to VCC, as shown in Figure 29, to ensure proper VR operation when the integrator capacitance from COMP to FB is too low (typically less than 68pF).

PSICOMP - Connect a series RC across the type III compensation network of the VR output voltage. This improves loop gain and load transient response in PSI1/2/3/Decay mode. An open pin disables this feature.

DVC_MEM - A series resistor and capacitor can be connected from this pin to the FB pin to compensate and smooth dynamic VID transitions. When this pin tied to VCC, the DVID rate will be default at 10mV/µs independent of FS_DVID pin, while boot voltages (see BT) are set for memory applications and VDBAND_PMADR_VRSEL becomes a programming pin for VDBAND, PMBus address offset and VR12/VR12.5 mode selection. When this pin is NOT tied to VCC (Open or RC), it can program VDBAND, but not PMADR or VRSEL (see Table 10 for more details).

SVCLK - Synchronous clock signal input of SerialVID bus from CPU.

SVDATA - I/O pin for transferring data signals between CPU and VR controller.

SVALERT# - Output pin for transferring the active low signal driven asynchronously from the VR controller to CPU.

ISENIN+, ISENIN - These pins are current sense inputs to the differential amplifier of the input supply. The sensed current is used for input power monitoring and power management of the system. The resistor sensing is typically recommended. For DCR sensing, connect each ISENIN pin to the node between the RC sense elements. Tie the ISENIN- pin to the other end of the sense capacitor through a resistor, R_{ISENIN}. The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sense current is proportional to the inductor current and scaled by the DCR of the inductor and R_{ISENIN}. In addition, if the 15µA comparator is triggered, it will see it as the catastrophic failure and pull the EN_PWR_CFP pin VCC to signal the system for protection. When not used, connect ISENIN+ to VIN and a resistor divider with a ratio of 1/3 on ISENIN± pins (for instance, 499kΩ in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 34). Refer to "Input Current Sensing" on page 34 for proper configuration details. Furthermore, ISENIN+ should be connected to the input voltage (VIN) for feed-forward compensation to maintain a constant loop gain over the input line variation. Do not leave the ISENIN+ pin OPEN.

SM_PM_I2CLK - Synchronous clock signal input of SMBus/PMBus/I^2C.

SM_PM_I2DATA - I/O pin for transferring data signals SMBus/PMBus/I^2C and VR controller.

OPEN - Keep this pin floating.

IMADR_BTRM, TMX_DRP_DE_TC, VDBAND_PMADR_VRSEL, ICL_SPDUPC_K - Register pins used to program system parameters. They can be read back via 0C, 0D, 0E, 0F in SVID or DC, DD, DE, B0 via SMBus/PMBus/I^2C, respectively. Their functionalities are described in the following; refer to Table 10, "SYSTEM PARAMETER DESCRIPTION" on page 31 on for summary.

IMADR_BTRM (IMAX_ADDR_BT_RAMP, Reg. 0C/DC) - IMAX
Maximum current, I_{CCMAX}, register of the voltage regulator. It has a range of 0A to 255A with 1A/step on independent register DA while programmed by the PMBus/SMBus/I^2C, otherwise, it has limited choices based upon operating phase number listed in Table 11. This register represents the maximum allowed load current for VR and corresponds to a 2.5V (typically set) at IMON.

ADDR - SVID and SMBus/PMBus/I^2C Address offset register of VR: 0/80, 0/82, 0/84, 0/86 (SVID/PMBus) when DVC_MEM is OPEN or an RC to FB pin; 2, 4, 6, 8 (SVID) when DVC_MEM tied to VCC. E/F is an ALL call address for SVID.

BT - Start-up boot voltage register of VR. When the DVC_MEM pin is open or connects an RC to FB pin, the boot voltages are: 0V, 1.65V, 1.70V, and 1.75V for core applications where SVID is compliant with VR12.5. When the DVC_MEM pin is tied to VCC, the boot levels are changed to 0V, 1.2V, 1.35V, and 1.5V for memory applications and where SVID protocol is compliant with VR12 or VR12.5 selectable via the VDBAND_PMADR_VRSEL pin.

RAMP - Get feed-forward Ramp (1.2V or 1.5V).

TMX_DRP_DE_TC (TMAX_DRP_DE_TCOMP, Reg. 0D/DD) - TMAX

Maximum temperature register (TMAX) of the VR and the thermal trip point of VR_HOT#. It covers +85°C to +120°C with +5°C/step. The register represents the maximum allowed temperature of VR, and programs the over-temperature trip point at VR_HOT#. The typical application should use a setting of +100°C or lower, since the NTC thermistor temperature represents the PCB, not the hottest component on the board. In addition, the NTC thermistor typically

picks up a temperature lower than the PCB due to the thermal impedance between PCB and NTC.

DRP - Select the droop enable or disable of VR.

DE - Diode emulation (DE) operation register of VR in PSI2, PSI3, and Decay modes. In PSI1 mode, the VR always operates in CCM mode. When diode emulation is disabled, the output decays at the rate of setVID Slow; however, the SVID bus still acknowledges execution of the command.

TCOMP - Temperature differential (-2.5°C to +29.7°C) between the actual sensed inductor of the VR regulator and the NTC thermistor at the TM pin. The voltage sensed on the TM pin is utilized as the temperature input to adjust the droop current and the overcurrent protection limit to effectively compensate for the temperature coefficient of the current sense element of VR. To implement the integrated temperature compensation, select a proper temperature offset "TCOMP," other than the "OFF" value, which disables the integrated temperature compensation function.

VDBAND_PADR_VRSEL (AVAILABLE DVC_MEM = VCC, 0E/DE)
VDBAND - Select COMP ripple voltage band, to control speed up.

PADR (PMADDR) - It sets SMBus/PMBus/I^2C 16 independent address offset (E0 to EE, C8 to CE, 88 to 8E) when DVC_MEM is tied to VCC for memory applications.

VRSEL - When DVC_MEM is tied to VCC, this pin allows selection of VR12 or VR12.5 VID code for memory applications.

ICL_SPDUPC_K (Reg 0F/B0) ICL - It sets the cycle-by-cycle overcurrent limit, independently for each channel. It also adds on top of the level programmed by F4h. This current will be used as reference and compared with the sensed peak current to detect over current condition. It ranges from 70µA to 125µA.

SPDUPC - Select the sensitivity of speed up control. It has selection values ranging from 2pF to 16pF (2pF/step, no 14pF selection), and ORIGINAL.

K - Select's COMP voltage clamp control threshold, which will determine how close it should be to the targeted COMP voltage before starting PWM pulse.

Operation

The ISL6381 is a 4-Phase PWM controller for microprocessor VR12.5 core and up to 4-Phase for VR12/VR12.5 memory voltage regulator. The ISL6381 is designed to be compliant to Intel VR12.5/VR12 specifications with SerialVID Features. The SMBus/PMBus/I^2C can be programmed with Embedded Controller. The system parameters and SVID required registers are programmable with two dedicated pins in ISL6381. This greatly simplifies the system design for various platforms and lowers inventory complexity and cost by using a single device.

In addition, this controller is compatible with phase doublers (ISL6611A and ISL6617), which can double or quadruple the phase count. For instance, the multi-phase PWM can realize up to 16-phase count system. A higher phase count system can improve thermal distribution and power conversion efficiency at heavy load.

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter (which are both cost-effective and thermally viable), have forced a change to the cost-saving approach of multiphase. The ISL6381 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The typical application circuit diagrams on page 7 and page 8 provide the top level views of multiphase power conversion using the ISL6381 controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase, as illustrated in Figure 1. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and F_{SW} is the switching frequency.

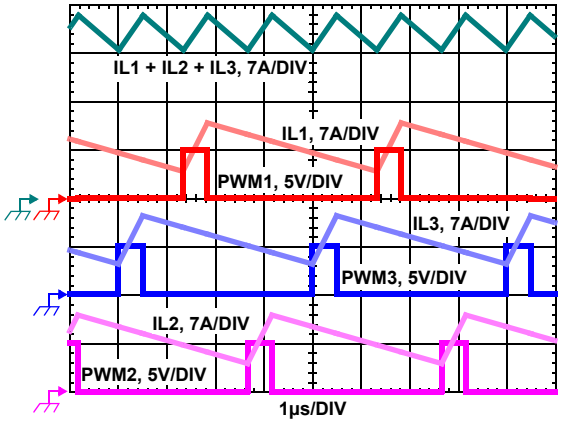


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2, the peak-to-peak overall ripple current ($I_{C,PP}$) decreases with the increase in the number of

channels, as shown in Figure 2.

Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and the summed inductor ripple current. Increased ripple frequency and lower ripple amplitude mean that the designer can use less per channel inductance and few or less costly output capacitors for any performance specification.

$$I_{C,PP} = \frac{V_{OUT}}{L \cdot F_{SW}} K_{RCM}$$

$$K_{RCM} = \frac{(N \cdot D - m + 1) \cdot (m - (N \cdot D))}{N \cdot D} \quad \text{(EQ. 2)}$$

for

$$m - 1 \le N \cdot D \le m$$

$$m = \text{ROUNDUP}(N \cdot D, 0)$$

Another benefit of interleaving is to reduce the input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitors. The example in Figure 3 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

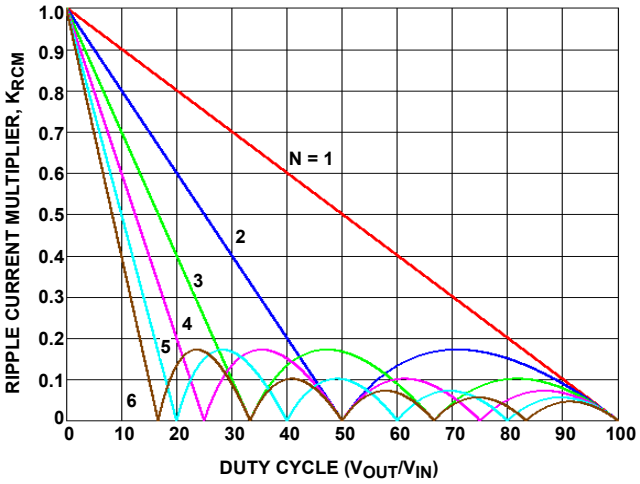


FIGURE 2. RIPPLE CURRENT MULTIPLIER vs. DUTY CYCLE

The converter depicted in Figure 3 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

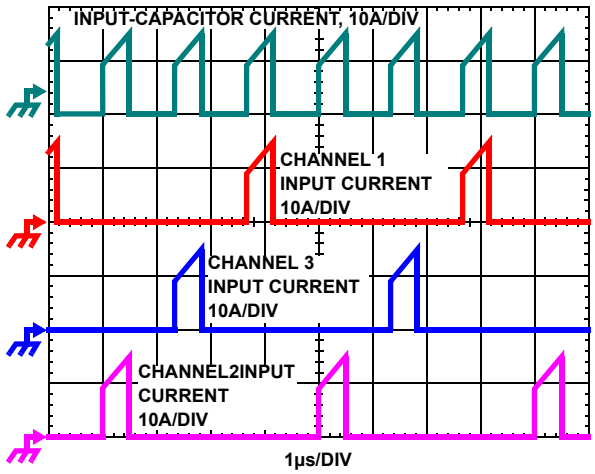


FIGURE 3. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 42, 43 and 44, as described in the "Input Capacitor Selection" on page 47, can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 45 shows the single phase input-capacitor RMS current for comparison.

PWM Modulation Scheme

The ISL6381 adopts Intersil's proprietary Enhanced Active Pulse Positioning (EAPP) modulation scheme to improve transient performance. The EAPP is a unique dual-edge PWM modulation scheme with both PWM leading and trailing edges being independently moved to give the best response to transient loads. The EAPP has an inherited function, similar to Intersil's proprietary Adaptive Phase Alignment (APA) technique, to turn on all phases together to further improve the transient response, when there are sufficiently large load step currents. The EAPP is a variable frequency architecture, providing linear control over transient events and evenly distributing the pulses among all phases to achieve very good current balance and eliminate beat frequency oscillation over a wide range of load transient frequencies.

To further improve the line and load transient responses, the multi-phase PWM features feed-forward function to change the up ramp with the input line (ISENIN+ input) to maintain a constant overall loop gain over a wide range input voltage. The up ramp of the internal Sawtooth is defined in Equation 3, where V_{UPRAMP} is programmable by "RM" register pin and SMBus/PMBus/I^2C.

$$V_{RAMP} = \frac{V_{IN} \cdot V_{UPRAMP}}{12V} \quad \text{(EQ. 3)}$$

With EAPP control and feed-forward function, the ISL6381 can achieve excellent transient performance over wide frequency range of load step, resulting in lower demand on the output capacitors.

At DC load conditions, the PWM frequency is constant and set by the external resistor between the FS pin and GND during normal mode (PSI0) and low power mode (PSI1). However, when PSI2 or PSI3 is asserted in ultra low power conditions, if the VR is

configured for diode emulation operation, the EAPP reduces the switching frequency as the load decreases. Thus, the VR can enter burst mode at extreme light load conditions and improve power conversion efficiency significantly.

Under steady state conditions, the operation of the ISL6381 PWM modulator is similar to a conventional trailing edge modulator. Conventional analysis and design methods can therefore be used for steady state and small signal analysis.

PWM and PSI# Operation

The timing of each channel is set by the number of active channels. The default channel setting for the ISL6381 is four. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

The ISL6381 can work in a 0 to 4-Phase configuration. Tie PWM(N+1) to VCC to configure for N-phase operation, and leave other higher order PWM (>N+1) open. PWM firing order is sequential from 1 to N with N being the number of active phases, as summarized in Table 1. For 4-Phase operation, the channel firing sequence is 1-2-3-4, and they are evenly spaced over 1/4 of a cycle. Connecting PWM4 to VCC configures 3-phase operation; the channel firing order is 1-2-3 and the phase spacing is 1/3 of a cycle. If PWM2 is connected to VCC, only Channel 1 operation is selected. If PWM1 is connected to VCC, the VR operation is turned off. For memory applications, the DVC_MEM pin should be tied to VCC, the VDBAND_PMADR_VRSEL pin becomes a register pin to program VR12 or VR12.5 mode and SMBus/PMBus/I^2C addresses.

TABLE 1. PHASE NUMBER AND PWM FIRING SEQUENCE

N	PHASE SEQUENCE PSI# = PSI0	PWM# TIED TO V_{CC} (VCORE)	PWM# TIED TO V_{CC} (MEMORY)	ACTIVE PHASE PSI# = PSI1
4	1-2-3-4		x_MEM = V_{CC}	PWM1/3
3	1-2-3	PWM4	PWM4	PWM1/2
2	1-2	PWM3	PWM3	PWM1/2
1	1	PWM2	PWM2	PWM1

The CPU can enter four distinct power states, as shown in Table 2. The ISL6381 supports all states, but it treats PSI2 and PSI3 the same. In addition, the setDecay mode will automatically enter PSI2 State while the output voltage decaying. However, prior to the end of soft-start (i.e: VR_RDY goes high), the lower power modes (PSI1/2/3/Decay) are NOT enabled.

TABLE 2. POWER STATE COMMAND FROM CPU

STATE	DESCRIPTION
PSI0	High Power Mode; all Phases are running
PSI1	Low Power Mode
PSI2	Very Low Power Mode
PSI3	Ultra Low Power Mode, Treated as PSI2
Decay	Automatically enter PSI2 and ramp down the output voltage reference to the target voltage

When the SVID bus sends PSI1/2/3 or Set VID Decay command, it indicates the low power mode operation of the processor. The controller starts phase shedding the next switching cycle. The controller reduces the number of active phases according to the logic on Table 3. “NPSI” register programs the controller number of phases operation in PSI1 mode.

When PSI1 is asserted, VR is in single-phase CCM operation with PWM1, or 2-phase CCM operation with PWM1 and 2, 3 or 4, as shown in Table 1. The number of operational phases is configured by “NPSI” register, as shown in Table 3. In PSI2/3/Decay State, only PWM1 is in DCM/CCM operation, which is programmed by the “DE” register.

TABLE 3. PHASE DROPPING CONFIGURATION AT PSI1 AND PSI2/3/DECAY

NPSI CODE	PSI1 MODE	PSI2/3 AND DECAY
SI1	1-Phase	1-Phase
SI2	2-Phase	1-Phase

While the controller is operational (V_{CC} above POR, TM_EN_OTP and EN_PWR are both high, valid VID inputs), it can pull the PWM pins to ~40% of V_{CC} (~2V for 5V VCC bias) during various stages, such as soft-start delay, phase shedding operation, or fault conditions (OC or OV events). The matching driver's internal PWM resistor divider can further raise the PWM potential, but not lower it below the level set by the controller IC. Therefore, the controller's PWM outputs are directly compatible with Intersil drivers that require 5V PWM signal amplitudes. Drivers requiring 3.3V PWM signal amplitudes are generally incompatible.

Diode Emulation Operation

To improve light efficiency, the ISL6381 can enter diode emulation operation in PSI2/3 or Decay mode. Users should select Intersil VR12/VR12.5 compatible drivers: The ISL6627 or ISL6622 for PSI# channel(s). The diode emulation should be disabled when non-compatible power stages or drivers are used.

Switching Frequency

The VR’s switching frequency is determined by the selection of the frequency-setting resistor, R_T, which is connected from FS_FDVID pin to GND or VCC. Equation 4 and Figure 4 are provided to assist in selecting the correct resistor value.

$$R_T = \frac{5 \cdot 10^{10}}{F_{SW}} \quad \text{(EQ. 4)}$$

where F_{SW} is the switching frequency of each phase.

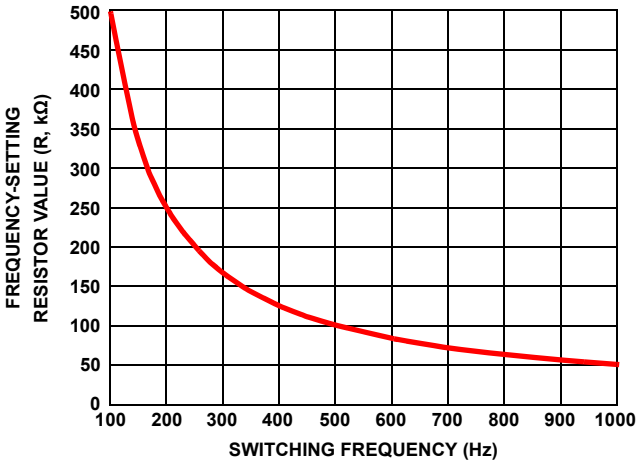


FIGURE 4. SWITCHING FREQUENCY vs R_T

Current Sensing

The ISL6381 senses current continuously for fast response. The ISL6381 supports inductor DCR sensing, or resistive sensing techniques. The associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance, load-line regulation, and overcurrent protection.

The internal circuitry, shown in Figures 5 and 6, represents one channel of the VR output, respectively. The ISEN± circuitry is repeated for each channel, but may not be active depending on the status of the PWM[4:2] pins, as described in "PWM and PSI# Operation" on page 16. The input bias current of the current sensing amplifier is typically 20nA; less than 10kΩ input impedance is preferred to minimize the offset error, i.e., a larger C value as needed.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 5. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 5 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 5.

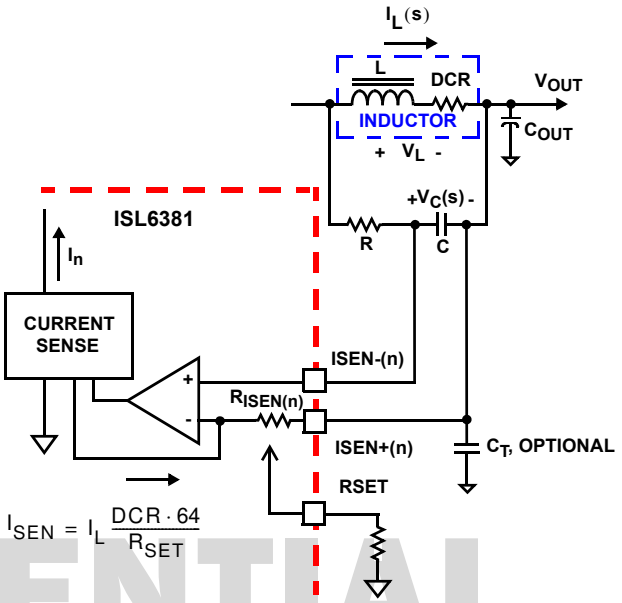


FIGURE 5. DCR SENSING CONFIGURATION

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L (See Equation 6).

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the RC time constant matches the inductor time constant (R*C = L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of the ISEN+ pin, I_{SEN}, is proportional to the inductor current.

Equation 7 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} = I_L \frac{DCR \cdot 64}{R_{SET}} \quad \text{(EQ. 7)}$$

RESISTIVE SENSING

For more accurate current sensing, a dedicated current-sense resistor R_{SENSE} in series with each output inductor can serve as the current sense element (see Figure 6). This technique however reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.

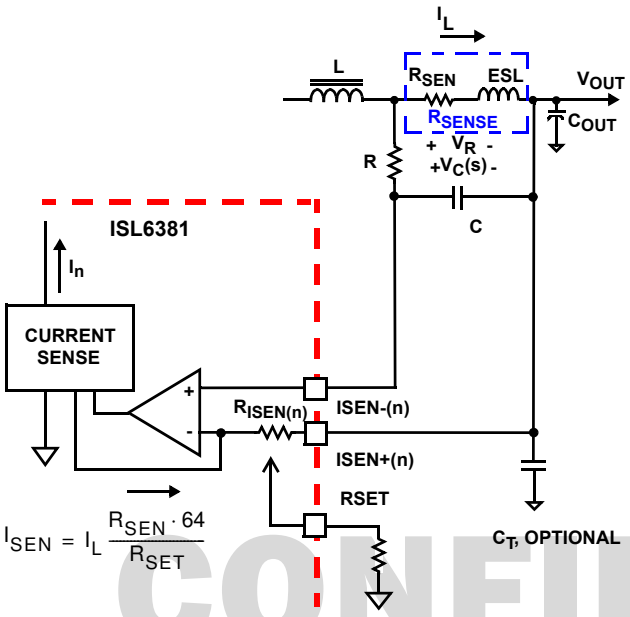


FIGURE 6. SENSE RESISTOR IN SERIES WITH INDUCTORS

A current sensing resistor has a distributed parasitic inductance, known as ESL (equivalent series inductance, typically less than 1nH) parameter. Consider the ESL as a separate lumped quantity, as shown in Figure 6. The channel current I_L, flowing through the inductor, will also pass through the ESL. Equation 8 shows the s-domain equivalent voltage across the resistor V_R.

$$V_R(s) = I_L \cdot (s \cdot ESL + R_{SEN}) \quad \text{(EQ. 8)}$$

A simple R-C network across the current sense resistor extracts the R_{SEN} voltage, as shown in Figure 7.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L (see Equation 9).

$$V_C(s) = \frac{\left(s \cdot \frac{ESL}{R_{SEN}} + 1\right) \cdot (R_{SEN} \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 9)}$$

If the R-C network components are selected such that the RC time constant matches the ESL-R_{SEN} time constant ($R*C = ESL/R_{SEN}$), the voltage across the capacitor V_C is equal to the voltage drop across the R_{SEN}, i.e., proportional to the channel current. As an example, a typical 1mΩ sense resistor can use R = 348Ω and C = 820pF for the matching. Figures 7 and 8 show the sensed waveforms without and with matching RC when using resistive sense.

FIGURE 7. VOLTAGE ACROSS R WITHOUT RC

FIGURE 8. VOLTAGE ACROSS C WITH MATCHING RC

Equation 10 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the R_{ISEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISEN}} = I_L \frac{R_{SEN} \cdot 64}{R_{SET}} \quad \text{(EQ. 10)}$$

However, the R_{ISEN} resistor of each channel is integrated, while its value is determined by the R_{SET} resistor. The R_{SET} resistor value can be from 3.84kΩ to 60.4kΩ and is 64x the required I_{SEN} resistor value. Therefore, the current sense gain resistor (Integrated R_{ISEN}) value can be effectively set at 60Ω to 943Ω.

The inductor DCR value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Negative Temperature Coefficient (NTC) resistor can be used for thermal compensation, or the integrated temperature compensation function of the ISL6381 should be utilized. The integrated temperature compensation function is described in "Temperature Compensation" on page 28.

Decoupling capacitor (C_T) on ISEN[4:1]- pins are optional and might be required for long sense traces and a poor layout.

L/DCR OR ESL/R_{SEN} MATCHING

Assuming the compensator design is correct, Figure 9 shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant. When the load current I_{OUT} has a square change, the output voltage V_{OUT} also has a square response, except for the overshoot at load release. However, there is always some PCB contact impedance of current sensing components between the two current sensing points; it hardly accounts into the L/DCR or ESL/R_{SEN} matching calculation. Fine tuning the matching is necessarily done in the board level to improve overall transient performance and system reliability.

If the R-C timing constant is too large or too small, $V_C(s)$ will not accurately represent real-time $I_{OUT}(s)$ and will worsen the transient response. Figure 10 shows the load transient response when the R-C timing constant is too small. The V_{OUT} will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 11 shows the transient response when the R-C timing constant is too large. V_{OUT} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.

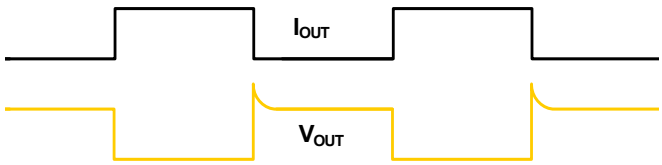


FIGURE 9. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

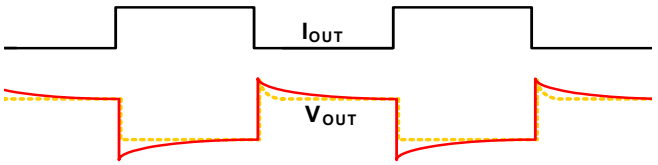


FIGURE 10. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

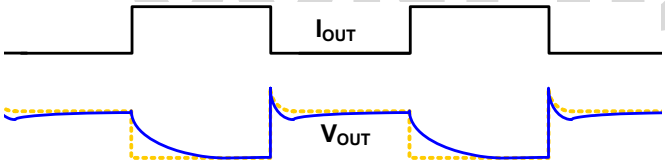


FIGURE 11. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

Channel-Current Balance

The sensed current I_n from each active channel is summed together and divided by the number of active channels. The resulting average current I_{AVG} provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current to make an appropriate adjustment to the PWM duty cycle of each channel with Intersil's patented current-balance method.

In addition, the channel current or thermal balance can be adjusted via PMBus (F7-FA). Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

Voltage Regulation

The compensation network shown in Figure 12 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (DAC and OFFSET) and droop current source, remote sense, and error amplifier.

The sensed average current I_{DROOP} is tied to FB internally and will develop voltage drop across the resistor between FB and V_{OUT} for droop control. This current can be disconnected from the FB node by tying R_{FS_DRP} high to V_{CC} for non-droop applications.

The output of the error amplifier, V_{COMP}, is compared to the internal sawtooth waveforms to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage.

The ISL6381 does not have a unity gain amplifier in between the feedback path and error amplifier. For remote sensing, connect the microprocessor sensing pins to the non-inverting input, FB, via the feedback resistor (R_{FB}), and inverting input, RGND, of the error amplifier. This configuration effectively removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point. VSEN should connect to remote sensing's positive rail as well for overvoltage protection.

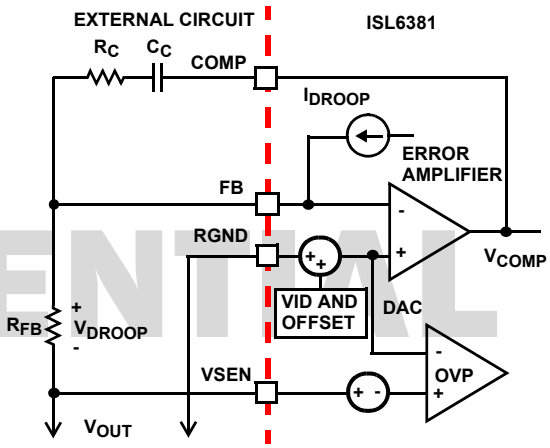
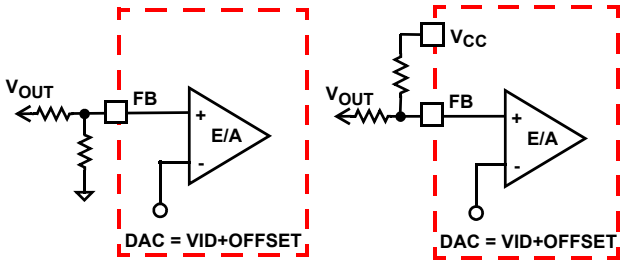


FIGURE 12. OUTPUT VOLTAGE AND LOAD-LINE REGULATION

A digital-to-analog converter (DAC) generates a reference voltage, which is programmable via SVID bus or PMBus. The DAC decodes the SVID or PMBus set command into one of the discrete voltages shown in Table 4. In addition, the output voltage can be margined in ±5mV step between -640mV and 635mV for VR12 mode, ±10mV step between -1280mV and 1270mV for VR12.5 mode, as shown in Table 4, via SVID set OFFSET command (33h). For a finer than 5mV or 10mV offset, a large ratio resistor divider can be placed on the FB pin between the output and GND for positive offset or VCC for negative offset, as in Figure 13.



A. V_{OUT} HIGHER THAN DAC B. V_{OUT} LOWER THAN DAC

FIGURE 13. EXTERNAL PROGRAMMABLE REGULATION

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
00000000	0	OFF	OFF	0	0
00000001	1	0.250	0.500	5	10
00000010	2	0.255	0.510	10	20
00000011	3	0.260	0.520	15	30
00000100	4	0.265	0.530	20	40
00000101	5	0.270	0.540	25	50
00000110	6	0.275	0.550	30	60
00000111	7	0.280	0.560	35	70
00001000	8	0.285	0.570	40	80
00001001	9	0.290	0.580	45	90
00001010	A	0.295	0.590	50	100
00001011	B	0.300	0.600	55	110
00001100	C	0.305	0.610	60	120
00001101	D	0.310	0.620	65	130
00001110	E	0.315	0.630	70	140
00001111	F	0.320	0.640	75	150
00010000	10	0.325	0.650	80	160
00010001	11	0.330	0.660	85	170
00010010	12	0.335	0.670	90	180
00010011	13	0.340	0.680	95	190
00010100	14	0.345	0.690	100	200
00010101	15	0.350	0.700	105	210
00010110	16	0.355	0.710	110	220
00010111	17	0.360	0.720	115	230
00011000	18	0.365	0.730	120	240
00011001	19	0.370	0.740	125	250
00011010	1A	0.375	0.750	130	260
00011011	1B	0.380	0.760	135	270
00011100	1C	0.385	0.770	140	280
00011101	1D	0.390	0.780	145	290
00011110	1E	0.395	0.790	150	300
00011111	1F	0.400	0.800	155	310
00100000	20	0.405	0.810	160	320
00100001	21	0.410	0.820	165	330
00100010	22	0.415	0.830	170	340
00100011	23	0.420	0.840	175	350
00100100	24	0.425	0.850	180	360
00100101	25	0.430	0.860	185	370

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
00100110	26	0.435	0.870	190	380
00100111	27	0.440	0.880	195	390
00101000	28	0.445	0.890	200	400
00101001	29	0.450	0.900	205	410
00101010	2A	0.455	0.910	210	420
00101011	2B	0.460	0.920	215	430
00101100	2C	0.465	0.930	220	440
00101101	2D	0.470	0.940	225	450
00101110	2E	0.475	0.950	230	460
00101111	2F	0.480	0.960	235	470
00110000	30	0.485	0.970	240	480
00110001	31	0.490	0.980	245	490
00110010	32	0.495	0.990	250	500
00110011	33	0.500	1.000	255	510
00110100	34	0.505	1.010	260	520
00110101	35	0.510	1.020	265	530
00110110	36	0.515	1.030	270	540
00110111	37	0.520	1.040	275	550
00111000	38	0.525	1.050	280	560
00111001	39	0.530	1.060	285	570
00111010	3A	0.535	1.070	290	580
00111011	3B	0.540	1.080	295	590
00111100	3C	0.545	1.090	300	600
00111101	3D	0.550	1.100	305	610
00111110	3E	0.555	1.110	310	620
00111111	3F	0.560	1.120	315	630
01000000	40	0.565	1.130	320	640
01000001	41	0.570	1.140	325	650
01000010	42	0.575	1.150	330	660
01000011	43	0.580	1.160	335	670
01000100	44	0.585	1.170	340	680
01000101	45	0.590	1.180	345	690
01000110	46	0.595	1.190	350	700
01000111	47	0.600	1.200	355	710
01001000	48	0.605	1.210	360	720
01001001	49	0.610	1.220	365	730
01001010	4A	0.615	1.230	370	740
01001011	4B	0.620	1.240	375	750

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
01001100	4C	0.625	1.250	380	760
01001101	4D	0.630	1.260	385	770
01001110	4E	0.635	1.270	390	780
01001111	4F	0.640	1.280	395	790
01010000	50	0.645	1.290	400	800
01010001	51	0.650	1.300	405	810
01010010	52	0.655	1.310	410	820
01010011	53	0.660	1.320	415	830
01010100	54	0.665	1.330	420	840
01010101	55	0.670	1.340	425	850
01010110	56	0.675	1.350	430	860
01010111	57	0.680	1.360	435	870
01011000	58	0.685	1.370	440	880
01011001	59	0.690	1.380	445	890
01011010	5A	0.695	1.390	450	900
01011011	5B	0.700	1.400	455	910
01011100	5C	0.705	1.410	460	920
01011101	5D	0.710	1.420	465	930
01011110	5E	0.715	1.430	470	940
01011111	5F	0.720	1.440	475	950
01100000	60	0.725	1.450	480	960
01100001	61	0.730	1.460	485	970
01100010	62	0.735	1.470	490	980
01100011	63	0.740	1.480	495	990
01100100	64	0.745	1.490	500	1000
01100101	65	0.750	1.500	505	1010
01100110	66	0.755	1.510	510	1020
01100111	67	0.760	1.520	515	1030
01101000	68	0.765	1.530	520	1040
01101001	69	0.770	1.540	525	1050
01101010	6A	0.775	1.550	530	1060
01101011	6B	0.780	1.560	535	1070
01101100	6C	0.785	1.570	540	1080
01101101	6D	0.790	1.580	545	1090
01101110	6E	0.795	1.590	550	1100
01101111	6F	0.800	1.600	555	1110
01110000	70	0.805	1.610	560	1120
01110001	71	0.810	1.620	565	1130

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
01110010	72	0.815	1.630	570	1140
01110011	73	0.820	1.640	575	1150
01110100	74	0.825	1.650	580	1160
01110101	75	0.830	1.660	585	1170
01110110	76	0.835	1.670	590	1180
01110111	77	0.840	1.680	595	1190
01111000	78	0.845	1.690	600	1200
01111001	79	0.850	1.700	605	1210
01111010	7A	0.855	1.710	610	1220
01111011	7B	0.860	1.720	615	1230
01111100	7C	0.865	1.730	620	1240
01111101	7D	0.870	1.740	625	1250
01111110	7E	0.875	1.750	630	1260
01111111	7F	0.880	1.760	635	1270
10000000	80	0.885	1.770	-640	-1280
10000001	81	0.890	1.780	-635	-1270
10000010	82	0.895	1.790	-630	-1260
10000011	83	0.900	1.800	-625	-1250
10000100	84	0.905	1.810	-620	-1240
10000101	85	0.910	1.820	-615	-1230
10000110	86	0.915	1.830	-610	-1220
10000111	87	0.920	1.840	-605	-1210
10001000	88	0.925	1.850	-600	-1200
10001001	89	0.930	1.860	-595	-1190
10001010	8A	0.935	1.870	-590	-1180
10001011	8B	0.940	1.880	-585	-1170
10001100	8C	0.945	1.890	-580	-1160
10001101	8D	0.950	1.900	-575	-1150
10001110	8E	0.955	1.910	-570	-1140
10001111	8F	0.960	1.920	-565	-1130
10010000	90	0.965	1.930	-560	-1120
10010001	91	0.970	1.940	-555	-1110
10010010	92	0.975	1.950	-550	-1100
10010011	93	0.980	1.960	-545	-1090
10010100	94	0.985	1.970	-540	-1080
10010101	95	0.990	1.980	-535	-1070
10010110	96	0.995	1.990	-530	-1060
10010111	97	1.000	2.000	-525	-1050

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
10011000	98	1.005	2.010	-520	-1040
10011001	99	1.010	2.020	-515	-1030
10011010	9A	1.015	2.030	-510	-1020
10011011	9B	1.020	2.040	-505	-1010
10011100	9C	1.025	2.050	-500	-1000
10011101	9D	1.030	2.060	-495	-990
10011110	9E	1.035	2.070	-490	-980
10011111	9F	1.040	2.080	-485	-970
10100000	A0	1.045	2.090	-480	-960
10100001	A1	1.050	2.100	-475	-950
10100010	A2	1.055	2.110	-470	-940
10100011	A3	1.060	2.120	-465	-930
10100100	A4	1.065	2.130	-460	-920
10100101	A5	1.070	2.140	-455	-910
10100110	A6	1.075	2.150	-450	-900
10100111	A7	1.080	2.160	-445	-890
10101000	A8	1.085	2.170	-440	-880
10101001	A9	1.090	2.180	-435	-870
10101010	AA	1.095	2.190	-430	-860
10101011	AB	1.100	2.200	-425	-850
10101100	AC	1.105	2.210	-420	-840
10101101	AD	1.110	2.220	-415	-830
10101110	AE	1.115	2.230	-410	-820
10101111	AF	1.120	2.240	-405	-810
10110000	B0	1.125	2.250	-400	-800
10110001	B1	1.130	2.260	-395	-790
10110010	B2	1.135	2.270	-390	-780
10110011	B3	1.140	2.280	-385	-770
10110100	B4	1.145	2.290	-380	-760
10110101	B5	1.150	2.300	-375	-750
10110110	B6	1.155	2.310	-370	-740
10110111	B7	1.160	2.320	-365	-730
10111000	B8	1.165	2.330	-360	-720
10111001	B9	1.170	2.340	-355	-710
10111010	BA	1.175	2.350	-350	-700
10111011	BB	1.180	2.360	-345	-690
10111100	BC	1.185	2.370	-340	-680
10111101	BD	1.190	2.380	-335	-670

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
10111110	BE	1.195	2.390	-330	-660
10111111	BF	1.200	2.400	-325	-650
11000000	C0	1.205	2.410	-320	-640
11000001	C1	1.210	2.420	-315	-630
11000010	C2	1.215	2.430	-310	-620
11000011	C3	1.220	2.440	-305	-610
11000100	C4	1.225	2.450	-300	-600
11000101	C5	1.230	2.460	-295	-590
11000110	C6	1.235	2.470	-290	-580
11000111	C7	1.240	2.480	-285	-570
11001000	C8	1.245	2.490	-280	-560
11001001	C9	1.250	2.500	-275	-550
11001010	CA	1.255	2.510	-270	-540
11001011	CB	1.260	2.520	-265	-530
11001100	CC	1.265	2.530	-260	-520
11001101	CD	1.270	2.540	-255	-510
11001110	CE	1.275	2.550	-250	-500
11001111	CF	1.280	2.560	-245	-490
11010000	D0	1.285	2.570	-240	-480
11010001	D1	1.290	2.580	-235	-470
11010010	D2	1.295	2.590	-230	-460
11010011	D3	1.300	2.600	-225	-450
11010100	D4	1.305	2.610	-220	-440
11010101	D5	1.310	2.620	-215	-430
11010110	D6	1.315	2.630	-210	-420
11010111	D7	1.320	2.640	-205	-410
11011000	D8	1.325	2.650	-200	-400
11011001	D9	1.330	2.660	-195	-390
11011010	DA	1.335	2.670	-190	-380
11011011	DB	1.340	2.680	-185	-370
11011100	DC	1.345	2.690	-180	-360
11011101	DD	1.350	2.700	-175	-350
11011110	DE	1.355	2.710	-170	-340
11011111	DF	1.360	2.720	-165	-330
11100000	E0	1.365	2.730	-160	-320
11100001	E1	1.370	2.740	-155	-310
11100010	E2	1.375	2.750	-150	-300
11100011	E3	1.380	2.760	-145	-290

TABLE 4. VR12.5/VR12/IMVP7 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
11100100	E4	1.385	2.770	-140	-280
11100101	E5	1.390	2.780	-135	-270
11100110	E6	1.395	2.790	-130	-260
11100111	E7	1.400	2.800	-125	-250
11101000	E8	1.405	2.810	-120	-240
11101001	E9	1.410	2.820	-115	-230
11101010	EA	1.415	2.830	-110	-220
11101011	EB	1.420	2.840	-105	-210
11101100	EC	1.425	2.850	-100	-200
11101101	ED	1.430	2.860	-95	-190
11101110	EE	1.435	2.870	-90	-180
11101111	EF	1.440	2.880	-85	-170
11110000	F0	1.445	2.890	-80	-160
11110001	F1	1.450	2.900	-75	-150
11110010	F2	1.455	2.910	-70	-140
11110011	F3	1.460	2.920	-65	-130
11110100	F4	1.465	2.930	-60	-120
11110101	F5	1.470	2.940	-55	-110
11110110	F6	1.475	2.950	-50	-100
11110111	F7	1.480	2.960	-45	-90
11111000	F8	1.485	2.970	-40	-80
11111001	F9	1.490	2.980	-35	-70
11111010	FA	1.495	2.990	-30	-60
11111011	FB	1.500	3.000	-25	-50
11111100	FC	1.505	3.010	-20	-40
11111101	FD	1.510	3.020	-15	-30
11111110	FE	1.515	3.030	-10	-20
11111111	FF	1.520	3.040	-5	-10

Load-Line Regulation

Some microprocessor manufacturers require a precisely controlled output resistance. This dependence of the output voltage on load current is often termed “droop” or “load-line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction that works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 12, a current proportional to the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined, as shown in Equation 11:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 11)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 11 with the appropriate sample current expression defined by the current sense method employed, as shown in Equation 12:

$$V_{OUT} = V_{REF} - \left(\frac{I_{LOAD}}{N} \frac{R_X}{R_{ISEN}} R_{FB} \right) \quad \text{(EQ. 12)}$$

where V_{REF} is the reference voltage (DAC), I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback resistor, N is the active channel number, and R_X is the DCR, or R_{SENSE} depending on the sensing method.

Therefore, the equivalent loadline impedance, i.e. Droop impedance, is equal to Equation 13:

$$R_{LL} = \frac{R_{FB}}{N} \frac{R_X}{R_{ISEN}} \quad \text{(EQ. 13)}$$

The major regulation error comes from the current sensing elements. To improve load-line regulation accuracy, a tight DCR tolerance of inductor or a precision sensing resistor should be considered.

In addition to adjusting R_{FB} for the droop impedance, the droop impedance can be programmed as a percentage of R_{LL} or disabled via PMBus (D3h, D4h).

Dynamic VID

Modern microprocessors need to make changes to their voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID during regulator operation. The power management solution is required to monitor the DAC and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption is a necessary function of the core-voltage regulator.

Three different kinds of DVID operation (Fast, Slow, Decay) can be selected during Dynamic VID (DVID) transition for VR, but during VR soft-start, the setVID SLOW rate is defaulted. The SetVID rate is programmable via FS_DVID pin, as in Table 5, and SMBus/PMBus/I^2C, as in Table 6. In memory mode

(DVC_MEM = V_{CC}), Fast DVID rate is defaulted at 10mV/µs, unless programmed by SMBus/PMBus/I^2C. SetVID SLOW rate is always 1/4 of setVID Fast Rate.

TABLE 5. SLEW RATE OPTIONS VIA FS_DVID PIN

DVC_MEM	FS_DVID	SetVID FAST (MINIMUM RATE) mV/µs	SetVID SLOW (MINIMUM RATE) mV/µs
RC/ OPEN	V_{CC}	10	2.5
	GND	20	5.0
V_{CC}	V_{CC}	10	2.5
	GND	10	2.5

TABLE 6. SLEW RATE OPTIONS VIA PMBUS (F6h)

PMBus F6h[2:0]	FS_DVID (DVC_MEM = OPEN, RC)	SetVID FAST (MINIMUM RATE) mV/µs	SetVID SLOW (MINIMUM RATE) mV/µs
0h	V_{CC}	10	2.5
1h	GND	20	5.0
2h	N/A	14	3.5
3h	N/A	17	4.3
4h	N/A	26	6.5
5h	N/A	32	8.0
6h	N/A	40	10
7h	N/A	53	13.3

During dynamic VID transition and VID step up, the overcurrent trip point increases by 140% to avoid falsely triggering OCP circuits, while the overvoltage trip point will follow DAC+OVP (350mV or 175mV), which programmable via PMBus (D8[0]).

If the dynamic VID occurs at PSI1/2/3/Decay (lower power state) asserted, the system should exit to PSI0 (full power state) and complete the transition, and will not resume the lowe power state operation unless the low power mode command is asserted again.

In addition to ramping down the output voltage with a controlled rate as previously described, VR can be programmed into decay mode via SVID's setDecay command. Whenever the Decay command is received, the VR will enter PSI2 mode. The VR will be in single-phase operation. If the DE register is selected to be "Enabled", the VR will operate in diode emulation mode and drop to the target voltage at a decay rate determined by the load impedance and output capacitive bank. The decay rate will be limited to 2.5mV/µs rate setting. If the "DE" register is selected to be "Disabled", then the VR will drop at 2.5mV/µs rate setting.

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and V_{CC}. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, VR_RDY asserts logic high.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state (or pulled to 40% of V_{CC}) to assure the drivers remain off. The following input conditions must be met before the ISL6381 is released from shutdown mode.

1. The bias voltage applied at V_{CC} must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6381 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6381 will not inadvertently turn off unless the bias voltage drops substantially (see "Electrical Specifications" table beginning on page 9).
2. The ISL6381 features an enable input (EN_PWR_CFP) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6381 in shutdown until the voltage at EN_PWR rises above 0.85V. The enable comparator has about 100mV of hysteresis to prevent bounce. It is important that the drivers reach their POR level before the ISL6381 becomes enabled. The schematic in Figure 14 demonstrates sequencing the ISL6381 with the ISL66xx family of Intersil MOSFET drivers.
3. The voltage on TM_EN_OTP must be higher than 1.08V (typically) to enable the controller. This pin is typically connected to the output of VTT VR. However, since the TM_EN_OTP pin is also used for thermal monitoring, it will flag STATUS_BYTE due to thermal alert prior to start-up, therefore, it needs to use CLEAR_FAULT (03h) command to clear STATUS_BYTE (78h).

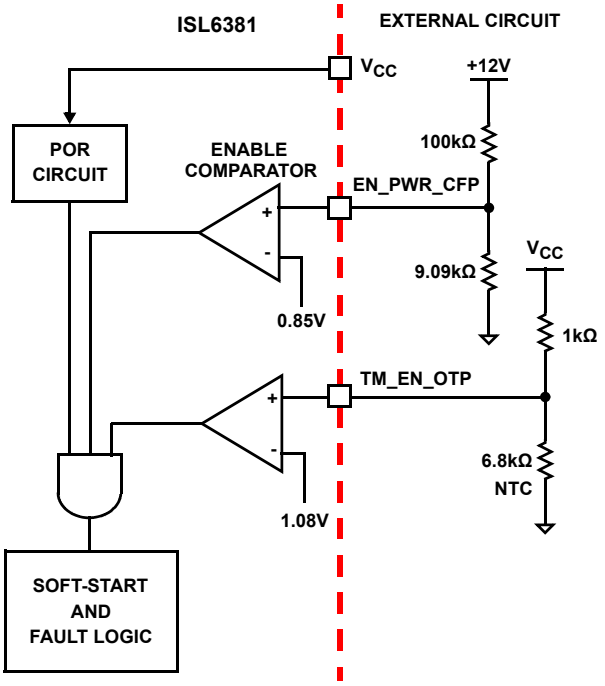


FIGURE 14. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

When all conditions previously mentioned are satisfied, the ISL6381 begins the soft-start and ramps the output voltage to the boot voltage set by hard-wired "BT" register, E6h of PMBus, or first setVID command if boot voltage set to zero volts. After

remaining at the boot voltage for some time, the ISL6381 reads the VID code via SVID bus. If the VID code is valid, ISL6381 will regulate the output to the final VID setting. If the VID code is "OFF" code, ISL6381 will remain shutdown.

Soft-Start

The ISL6381 based VR has 4 periods during soft-start, as shown in Figure 15. After V_{CC}, TM_EN_OTP and EN_PWR reach their POR/enable thresholds, the controller will have a fixed delay period t_{D1}. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches V_{BOOT} voltage at a fixed slew rate, one-quarter of setVID FAST rate as in Table 5. Then, the controller will regulate the VR voltage at V_{BOOT} for another period t_{D3} until SVID sends a new VID command. If the VID code is valid, ISL6381 will initiate the second soft-start ramp at a slew rate, set by SetDVID FAST or SLOW command in Table 5, until the voltage reaches the new VID voltage.

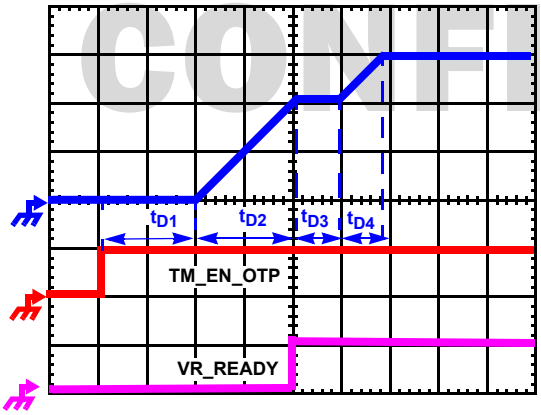


FIGURE 15. SOFT-START WAVEFORMS

The soft-start time is the sum of the 4 periods, as shown in Equation 14.

$$t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4} \quad \text{(EQ. 14)}$$

The t_{D1} is a fixed delay with the typical value as 4.6ms, which becomes 0ms delay when a successful PMBus command is recognized during ENABLE (EN_PWR_CFP or TM_EN_OTP) low shown in Figure 38. The t_{D3} is determined by the time to obtain a new valid VID voltage from SVID bus. If the VID is valid before the output reaches the boot voltage, the output will turn around to respond to the new VID code.

During t_{D2} and t_{D4}, the ISL6381 digitally controls the DAC voltage change at 5mV per step. The soft-start ramp time t_{D2} and t_{D4} can be calculated based on Equations 15 and 16:

$$t_{D2} = \frac{V_{BOOT}}{\text{SetVID SLOW RATE}}(\mu s) \quad \text{(EQ. 15)}$$

$$t_{D4} = \frac{V_{VID} - V_{BOOT}}{\text{SetVID RATE}}(\mu s) \quad \text{(EQ. 16)}$$

For example, when the V_{BOOT} is set at 1.1V and setVID rate is set at 10mV/µs, the first soft-start ramp time t_{D2} will be around 440µs and the second soft-start ramp time t_{D4} will be at maximum of 40µs if an setVID command for 1.5V is received after t_{D3}. However, if V_{BOOT} is set at 0V, the first setVID command is for 1.5V, then t_{D2} will be around 150µs. Note that the initial 0 to 250mV DAC is typically at a slower rate to minimize the in-rush current, the response time could be dictated by the compensation network and the output filter.

Current Sense Output

The current flowing out of the IMON pin is equal to the sensed average current inside the ISL6381. In typical applications, a resistor is placed from the IMON pin to GND to generate a voltage, which is proportional to the load current and the resistor value, as shown in Equation 17:

$$V_{IMON} = \frac{R_{IMON}}{N}\frac{R_X}{R_{ISEN}}I_{LOAD} \quad \text{(EQ. 17)}$$

where V_{IMON} is the voltage at the IMON pin, R_{IMON} is the resistor between the IMON pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, and R_X is the DC resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

The resistor from the IMON pin to GND should be chosen to ensure that the voltage at the IMON pin is typically 2.5V at the maximum load current, typically corresponding to I_{CCMAX} register. The IMON voltage is linearly digitized every 88µs and stored in the IOUT register (15h). When the IMON voltage reaches 2.5V or higher, the digitized IOUT will be FFh and the SVALERT# pin is pulled low to alarm the CPU. If the desired CPU maximum load current alert is not listed in Table 11 (SVID 21h register programmed by IMAX pin, not PMBus), a higher ICCMAX should be selected from Table 11, while the IMON resistor should be scaled accordingly to make sure that it reaches 2.5V at the selected ICCMAX output load, as in the following. In Intel CPU applications, the CPU itself scales the ICC_MAX register (21h in Table 14) to meet the CPU desired ICCMAX alert.

$$R_{IMON} = \frac{2.5V\,R_{ISEN}}{R_X}\frac{N}{I_{CC\_MAX\_21h}} \quad \text{(EQ. 18)}$$

A small capacitor can be placed between the IMON pin and GND to reduce the noise impact and provide averaging. The typical time constant is <200µs for VR12.5 Server Core (i.e., 5.6nF for a 30kΩ R_{IMON}) and 1-2ms for Desktop Core applications. If this pin is not used, tie it to GND.

To deal with layout and design variation of different platforms, the ISL6381 is intentionally trimmed to negative range at no load, thus, an offset can easily be added to calibrate the digitized IMON reading (15h in SVID and 8Ch in PMBus) whenever needed by PMBus (BFh) or the external pull-up resistor in Figure 16. Hence, the slope on the IMON pin is set by the equivalent impedance of $R_{MON1}//R_{MON2} = R_{IMON}$.

$$R_{MON2} = \frac{V_{CC}\,R_{IMON}}{V_{IMON\_OFFSET\_DESIRED}} \quad \text{(EQ. 19)}$$

$$R_{MON1} = \frac{R_{IMON2}\,R_{IMON}}{R_{IMON2} - R_{IMON}}$$

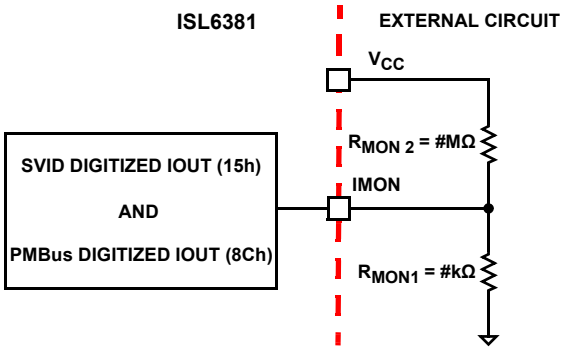


FIGURE 16. IMON NO LOAD OFFSET CALIBRATION

In addition, if the IMON pin voltage is higher than 3.0V, overcurrent shutdown will be triggered, as described in "Overcurrent Protection" on page 26.

Fault Monitoring and Protection

The ISL6381 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power-good indicator VR_RDY is provided for linking to external system monitors. The schematic in Figure 17 outlines the interaction between the fault monitors and the VR_RDY signals.

VR_Ready Signal

The VR_RDY pin is an open-drain logic output that indicates when the soft-start period is complete and the output voltage is within the regulated range. The VR_RDY is pulled low during shutdown and releases high after a successful soft-start. The VR_RDY will be pulled low when an fault (OCP or OVP) condition is detected, or the controller is disabled by a reset from EN_PWR_CFP, TM_EN_OTP, POR, or VID OFF-code. If the Multi_VR_config register is set to 01h, then the VR_Ready line will stay high when receiving a 00h VID code after the first soft-start. The defaulted Multi_VR_config is 00h.

Overvoltage Protection

Regardless of the VR being enabled or not, the ISL6381 overvoltage protection (OVP) circuit will be active after its POR. The OVP thresholds are different under different operation conditions. Prior to the end of the soft-start, the OVP threshold is 2.15V, which is also programmable via D8[2:1]. Once the VR completes the soft-start, the OVP trip point will change to a tracking level of DAC+ OVP (350mV or 175mV), which is programmable via PMBus (D8[0]).

Two actions are taken by the ISL6381 to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low instantly. This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level to avoid damaging the load. When the output voltage falls below the DAC plus 100mV, PWM signals enter a high-impedance state. The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, ISL6381 will again command the lower MOSFETs to turn on. The ISL6381 will continue to protect the load in this fashion as long as the overvoltage condition occurs.

Once an overvoltage condition is detected, the VR ceases the normal PWM operation and pulls its VR_Ready low until the ISL6381 is reset. Cycling the voltage V_{CC} below the POR-falling threshold will reset the controller. Cycling EN_PWR or TM_EN_OTP will NOT reset the controller.

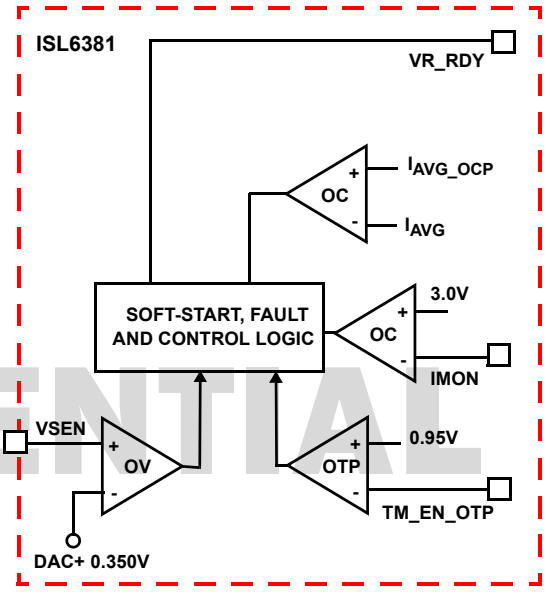
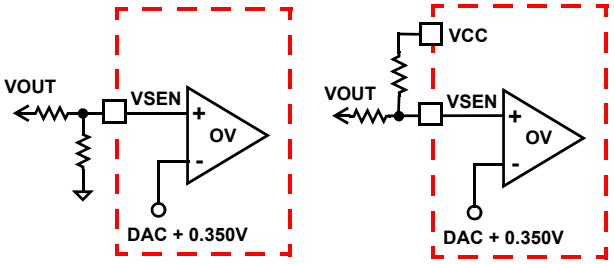


FIGURE 17. VR_RDY AND PROTECTION CIRCUITRY

In addition, the ISL6381 features open sensing protection to detect an open of the output voltage sensing as an OVP event, which suspends the controller operation. Without this protection, the VR can regulate up to maximum duty cycle and damage the load and power trains when the output sensing is broken open. Furthermore, since the regulation loop is sensed via the FB pin and the OVP is sensed via the VSEN pin, they are independent paths to keep output within target and below OVP level, respectively. Thus, the ISL6381 protects against a single point of failure.

Furthermore, since the regulation loop (FB pin) and the OVP sense (VSEN) are separated paths, the OVP level can be programmed higher or lower than the target, as in Figure 18; the OVP level however cannot be scaled too close to DAC to ensure that the OVP is not triggered during transient response and start-up.



A. INCREASED OVP B. REDUCED OVP

FIGURE 18. EXTERNAL PROGRAMMABLE OVP

Overcurrent Protection

The ISL6381 has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition by limiting its

peak current, while the combined phase currents are protected on an instantaneous basis.

For the individual channel overcurrent protection, the ISL6381 continuously compares the sensed peak current (~50ns filter) signal of each channel with a reference current programmed by ICL_SPDUP_K pin or PMBus (F4h, defaulted 125µA). If one channel current exceeds the reference current, ISL6381 will pull the PWM signal of this channel to low for the rest of the switching cycle. This PWM signal can be turned on next cycle if the sensed channel current is less than the reference current. The peak current limit of individual channels will only use cycle-by-cycle current limiting and will not trigger the converter to shutdown.

In instantaneous protection mode, the ISL6381 utilizes the sensed average current I_{AVG} to detect an overcurrent condition. See "Current Sensing" on page 17 for more details on how the average current is measured. The average current is continually compared with a reference current (I_{AVG_OCP}) programmed by PMBus (F4h, defaulted 100µA), as shown in Figure 17. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown. In addition, the current out of the IMON pin is equal to the sensed average current I_{AVG}. With a resistor from IMON to GND, the voltage at IMON will be proportional to the sensed average current and the resistor value. The ISL6381 continuously monitors the voltage at the IMON pin. If the voltage at the IMON pin is higher than 3.0V, a precision comparator triggers the overcurrent shutdown. Since the internal current comparator has wider tolerance than the voltage comparator, the IMON voltage comparator is the preferred one for OCP trip. Therefore, the resistor between IMON and GND can be scaled such that the overcurrent protection threshold is tripping lower than I_{AVG_OCP}. For example, the overcurrent threshold for the sensed average current I_{AVG} can be set to 95µA by using a 31.6kΩ resistor from IMON to GND. Thus, the internal overcurrent comparator (say defaulted 100µA) might only be triggered at its lower corner. However, IMON OCP trip should NOT be too far away from cycle-by-cycle reference current, which is used for cycle-by-cycle protection and inductor saturation.

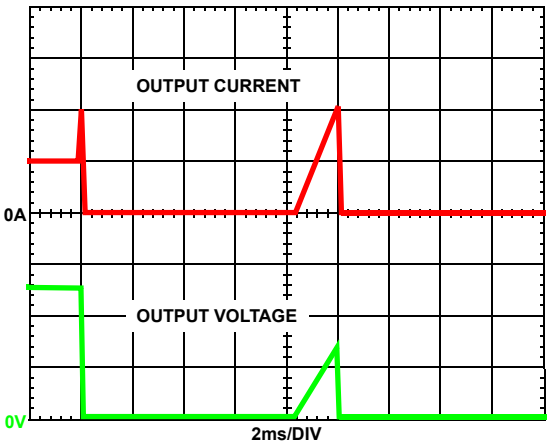


FIGURE 19. OVERCURRENT BEHAVIOR IN HICCUP MODE F_{SW} = 500kHz

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state, commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 8ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will continue indefinitely (as shown in Figure 19) until either controller is disabled or the fault is cleared.

NOTE: That the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard during this kind of operation.

Thermal Monitoring (VR_HOT#) and Protection

The VR_HOT# indicates the temperature status of the voltage regulator. VR_HOT# is an open-drain output, and an external pull-up resistor is required. This signal is valid only after the controller is enabled.

The VR_HOT# signal can be used to inform the system that the temperature of the voltage regulator is too high and the CPU should reduce its power consumption. The VR_HOT# signal may be tied to the CPU's PROC_HOT signal.

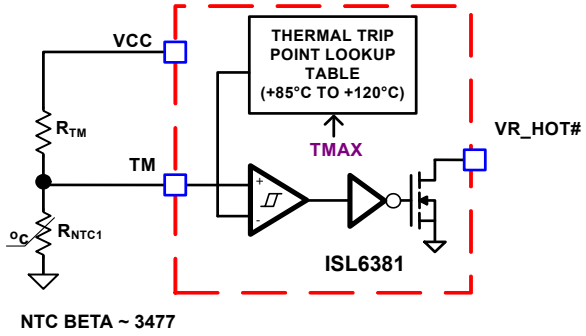


FIGURE 20. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

The thermal monitoring function block diagram is shown in Figure 20. One NTC resistor should be placed close to the respective power stage of the voltage regulator VR to sense the operational temperature, and pull-up resistors are needed to form the voltage dividers for the TM pin. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at the TM pin. Figure 21 shows the TM voltage over the temperature for a typical design with a recommended 6.8kΩ NTC (P/N: NTHS0805N02N6801 from Vishay, b = 3477) and 1kΩ resistor R_{TM}. It is recommended to use those resistors for the accurate temperature compensation since the internal thermal digital code is developed based upon these two components. If a different value is used, the temperature coefficient must be close to 3477 and R_{TM} must be scaled accordingly. For instance, NTC = 10kΩ (b = 3477), then R_{TM} should be 10kΩ/6.8kΩ*1kΩ = 1.47kΩ.

There is a comparator with hysteresis to compare the TM pin voltage to the threshold set by the TMAX register for VR_HOT# signal. With TMAX is set at +100°C, the VR_HOT# signal is pulled to GND when the TM pin voltage is lower than 39.12% of the V_{CC} voltage, and is open (pulled high through TM) when the TM voltage increase to above 40.98% of the V_{CC} voltage. The comparator trip point will be programmable by TMAX values.

Figure 22 shows the operation of those signals.

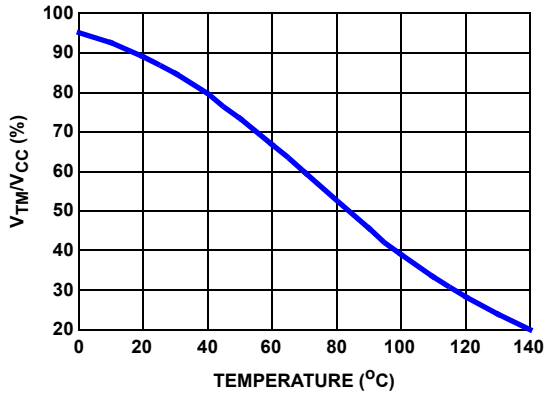


FIGURE 21. THE RATIO OF TM VOLTAGE TO NTC TEMPERATURE WITH RECOMMENDED PARTS

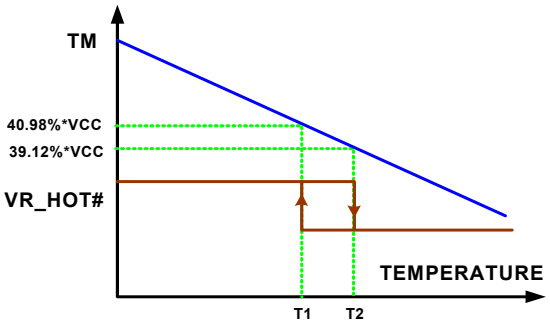


FIGURE 22. VR_HOT# SIGNAL (TMAX = +100°C) vs TM VOLTAGE

Based on the NTC temperature characteristics and the desired threshold of the VR_HOT# signal, the pull-up resistor R_{TM} of TM pin is given by Equation 20:

$$R_{TM} = 1.557 \times R_{NTC(T2)} \quad \text{(EQ. 20)}$$

$R_{NTC(T2)}$ is the NTC resistance at the VR_HOT# threshold temperature T2. The VR_HOT# is deasserted at temperature T1, as shown in Table 7. The NTC directly senses the temperature of the PCB and not the exact temperature of the hottest component on the board due to airflow and varied thermal impedance. Therefore, the user should select a lower TMAX number, depending upon the mismatch between NTC and the hottest components, than such component to guarantee a safe operation.

TABLE 7. VR_HOT# TYPICAL TRIP POINT AND HYSTERESIS

TMAX (°C)	VR_HOT# LOW (°C, T2, %V_{CC})	VR_HOT# OPEN (°C, T1, %V_{CC})	HYSTERESIS (°C)
+85	83.1; 48.94%	80.3; 51.04%	2.7
+90	88.6; 45.52%	85.9; 47.56%	2.7
+95	94.3; 42.26%	91.4; 44.20%	2.9
+100	100.0; 39.12%	97.1; 40.98%	2.9
+105	106.1; 36.14%	103.0; 37.92%	3.1
+110	109.1; 33.32%	106.1; 35.00%	3.0
+115	115.5; 30.68%	112.3; 32.24%	3.2
+120	118.7; 28.24%	115.5; 29.7%	3.2

In addition, as the temperature increase, the voltage on the TM pin drops. The controller is disabled when the TM pin voltage drops below 0.95 (typically) and becomes active again when it is above 1.08V (typically).

NOTE: When the TM_EN_OTP pin is used for enable toggle input, it will flag STATUS_BYTE (78h) due to thermal alert prior to start-up, therefore, it needs to use CLEAR_FAULT (03h) command to clear STATUS_BYTE (78h).

Temperature Compensation

The ISL6381 supports inductor DCR sensing, or resistive sensing techniques. The inductor DCR has a positive temperature coefficient, which is about +0.385%/°C. Since the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR.

In order to obtain the correct current information, there should be a way to correct the temperature impact on the current sense component. The ISL6381 provides two methods: integrated temperature compensation and external temperature compensation.

Integrated Temperature Compensation

The ISL6381 utilizes the voltage at the TM pin and "TCOMP" register to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 23.

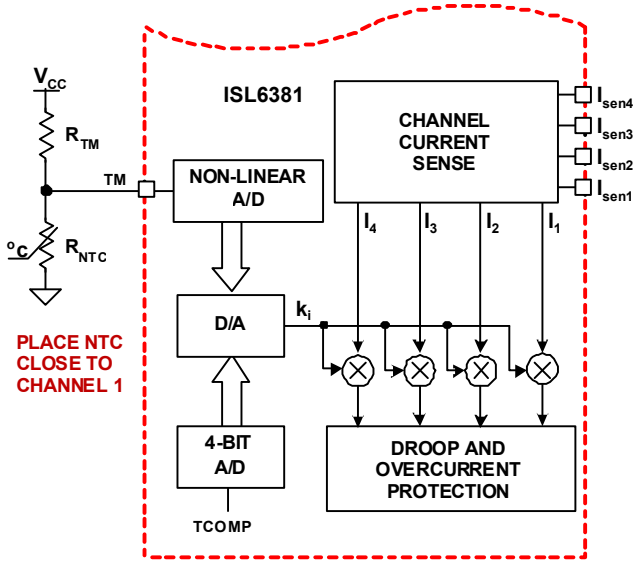


FIGURE 23. BLOCK DIAGRAM OF INTEGRATED TEMPERATURE COMPENSATION

When the NTC is placed close to the current sense component (inductor), the temperature of the NTC will track the temperature of the current sense component. Therefore, the TM voltage can be utilized to obtain the temperature of the current sense component. Since the NTC could pick up noise from the phase

node, a 0.1µF ceramic decoupling capacitor is recommended on the TM pin in close proximity to the controller.

Based on the V_{CC} voltage, the ISL6381 converts the TM pin voltage to a 6-bit TM digital signal for temperature For accurate temperature compensation, the ratio of the TM voltage to the NTC temperature of the practical design should be similar to that in Figure 21.

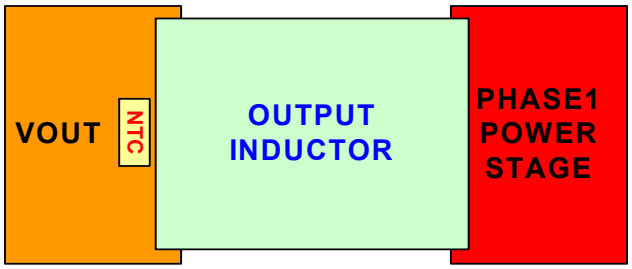


FIGURE 24. RECOMMENDED PLACEMENT OF NTC

Since the NTC attaches to the PCB, but not directly to the current sensing component, it inherits high thermal impedance between the NTC and the current sensing element. The "TCOMP" register values can be utilized to correct the temperature difference between NTC and the current sense component. As shown in Figure 24, the NTC should be placed in proximity to the PSI channel and the output rail; DO NOT place it close to the MOSFET side, which generates much more heat.

The ISL6381 multiplexes the "TCOMP" value with the TM digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated channel current signal is used for droop and overcurrent protection functions.

TABLE 8. "TCOMP" VALUES

TCOMP (°C)	TCOMP (°C)
-2.5	+18.9
+2.5	+24.3
+7	+29.7
+13	OFF

When a different NTC type or different voltage divider is used for the TM function, the TCOMP voltage can also be used to compensate for the difference between the recommended TM voltage curve in Figure 21 and that of the actual design. If the same type NTC (β = 3477) but different value is used, the pull-up resistor needs to be scaled, as shown in Equation 21:

$$R_{TM} = \frac{1k\Omega \cdot R_{NTC\_NEW}}{6.8k\Omega} \quad \text{(EQ. 21)}$$

Design Procedure

1. Properly choose the voltage divider for the TM pin to match the TM voltage vs temperature curve with the recommended curve in Figure 21.
2. Run the actual board under the full load and the desired cooling condition.
3. After the board reaches the thermal steady state, record the temperature (T_{CSC}) of the current sense component (inductor or MOSFET) and the voltage at TM and VCC pins.
4. Use Equation 22 to calculate the resistance of the NTC, and find out the corresponding NTC temperature T_{NTC} from the NTC datasheet or using Equation 23, where b is equal to 3477 for recommended NTC.

$$R_{NTC}(T_{NTC}) = \frac{V_{TM} \times R_{TM}}{V_{CC} - V_{TM}} \quad \text{(EQ. 22)}$$

$$T_{NTC} = \frac{\beta}{\ln\left(\frac{RTM}{R_{NTC}(T_{NTC})}\right) + \frac{\beta}{298.15}} - 273.15 \quad \text{(EQ. 23)}$$

5. In Intersil design worksheet, choose a number close to the result in Equation 24 in the "TCOMP" cell to calculate the needed resistor network for the register "TCOMP" pin.

NOTE: For worksheet, please contact Intersil Application support at www.intersil.com/design/.

$$T_{COMP} = T_{CSC} - T_{NTC} \quad \text{(EQ. 24)}$$

6. Run the actual board under full load again with the proper resistors connected to the "TCOMP" pin.
7. Record the output voltage as V1 immediately after the output voltage is stable with the full load. Record the output voltage as V2 after the VR reaches the thermal steady state.
8. If the output voltage increases over 2mV as the temperature increases, i.e. V2 - V1 > 2mV, reduce "TCOMP" value; if the output voltage decreases over 2mV as the temperature increases, i.e. V1 - V2 > 2mV, increase "TCOMP" values.

External Temperature Compensation

When the "OFF" code of TCOMP is selected, then the internal current source is not thermally compensated, i.e, the integrated temperature compensation function is disabled. However, one external temperature compensation network, shown in Figure 25, can be used to cancel the temperature impact on the droop (i.e; load-line).

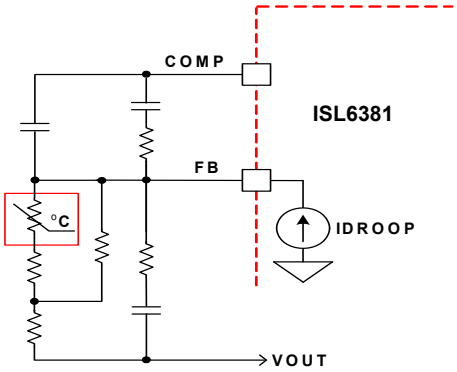


FIGURE 25. EXTERNAL TEMPERATURE COMPENSATION FOR LOAD-LINE

The sensed current will flow out of the FB pin and develop a droop voltage across the resistor equivalent (R_{FB}) between the FB pin and VOUT sensing node. If R_{FB} resistance reduces as the

temperature increases, the temperature impact on the droop can be compensated. An NTC resistor can be placed close to the power stage and used to form R_{FB}. Due to the nonlinear temperature characteristics of the NTC, a resistor network is needed to make the equivalent resistance between the FB pin and VOUT sensing node inversely proportional to the temperature.

This external temperature compensation network can only compensate the temperature impact on the droop, while it has no impact to the sensed current inside ISL6381. Therefore, this network cannot compensate for the temperature impact on the overcurrent protection function. In addition, the NTC could pick up phase switching noise and easily inject into the loop. This method is typically not recommended.

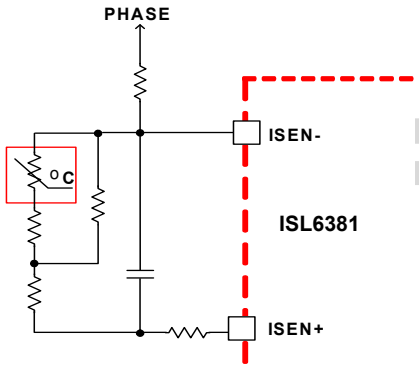


FIGURE 26. NTC WITH L/DCR MATCHING NETWORK FOR THERMAL COMPENSATION

Furthermore, the NTC can be placed with L/DCR matching network to thermally compensate the sensed current, or with IMON network to thermally compensate the IMON voltage (typically need to set internal overcurrent trip to be higher than IMON OCP trip), as shown in Figures 26 and 27, respectively. These methods are typically applicable for non-droop applications.

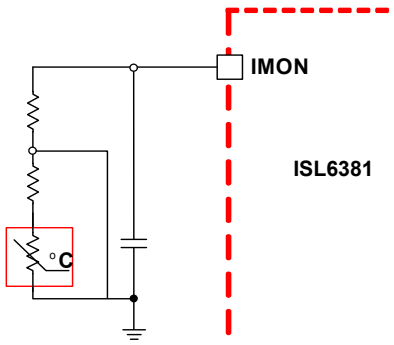


FIGURE 27. NTC WITH IMON NETWORK FOR THERMAL COMPENSATION

Hard-wired Registers (Patented)

To set registers using lowest pin-count package and with lowest overall cost, Intersil has developed a high resolution ADC using a patented technique with simple 1%, 100ppm/k or better temperature coefficient resistor divider, as shown in Figure 28. The same type of resistors are preferred so, that it has similar change over-temperature. In addition, the divider is compared to the internal divider off VCC and GND nodes and therefore must refer to VCC and GND pins, not through any RC decoupling network.

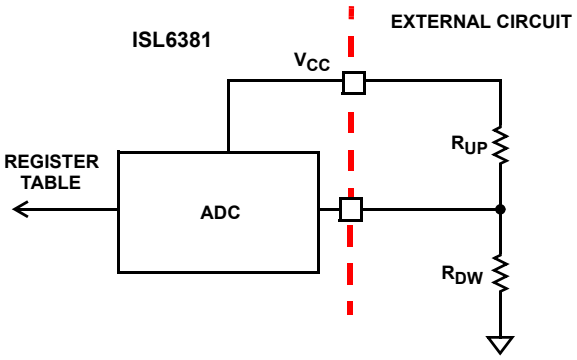


FIGURE 28. SIMPLIFIED RESISTOR DIVIDER ADC

As an example, Tables 12 and 13 show the R_{UP} and R_{DW} values of each pin for a specific system design; DATA for corresponding registers can be read out via SVID's Get(reg) command. In addition, some tie-high and tie-low options are available for easy programming (save resistor dividers) and can also be used to validate the VR operation during In-Circuit Test (ICT). For instance, when the system boot voltage is required at 0, the IMADR_BTRM pin can be tied to GND or VCC, prior to Enable, to get a known boot voltage to check VR operation with ICT. Resistor Register calculator is available, please contact Intersil Application support at www.intersil.com/design/.

TABLE 9. SYSTEM PARAMETER DESCRIPTION

REGISTER PIN NAME	DATA REGISTER CODE (SVID)	DATA REGISTER CODE (PMBus)
IMADR_BTRM	0C	DC
TMX_DRP_DE_TC	0D	DD
VDBAND_PMADR_VRSEL	0E	DE
ICL_SPDUPC_K	0F	B0

TABLE 10. SYSTEM PARAMETER DESCRIPTION

CODE NAME	DESCRIPTION	RANGE
ADDR	SVID	V_{CORE}: 0 with PMBus Address of 80, 82, 84, 86 V_{MEM}: 2, 4, 6, 8
PMADDR	PMBus	E0, E2, E4, E6, E8, EA, EC, EE, 88, 8A, 8C, 8E, C8, CA, CC, CE
BT	Boot Voltages (DVC_MEM = RC or OPEN)	0, 1.65, 1.7, 1.75V
	Boot Voltages (DVC_MEM = V_{CC})	0, 1.2, 1.35, 1.5
FDVID	setVID Fast Slew Rate	10, 20mV/µs via pin or 10 to 53mVµs via PMBus Command (F6h)
DE	Diode Emulation Option	Enable, or Disable
TMAX	Maximum Operating Temperature	+85°C to +120°C (5°C/Step)
IMAX	I_{CCMAX} of Platforms (1A/step via PMBus)	Limited by Pin in Table 11; Or 0-255A via PMBus
NPSI	Number of Operational Phases in PSI1 State	1 or 2-Phase
TCOMP	Mismatching Temperature Compensation Between Sensing Element and NTC	OFF, -2.5°C to +29.7°C
RAMP	UPRamp Amplitude	1.2V and 1.5V via PIn 0.75, 1.0, 1.2, 1.5V via PMBus Command (FD)
ICL	Cycle-by-Cycle Over Current Limit	70µA to 125µA
SPDUPC	Sensitivity Of Speed Up Control	2pF to 16pF (2pF/step, no 14pF selection), and ORIGINAL
K	COMP Voltage Clamp Control Threshold	ORIGINAL, 0.25, 0.5, 0.75
VDBAND	COMP Ripple Voltage Band	12.5V to 100mV (12.5mV/step)

TABLE 11. IMAX VALUE AT DIFFERENT PHASE COUNT BY "IMAX" PIN

4-PHASE (A)	3-PHASE (A)	2-PHASE (A)	1-PHASE (A)
80	60	40	10
90	70	46	15
100	75	52	20
120	52	60	25
140	95	65	30
165	100	70	35
175	112	75	40
190	135	85	45

TABLE 12. DESOGN EXAPLE (DVC_MEM = RC, 4-PHASE)

REG					R_{UP}	R_{DW}	DATA
0C	IMAX	ADDRS	BT	RAMP			
	215	0/80	1.7V	1.2V	665kΩ	187kΩ	C2h
0D	TMAX	DROOP	DE	TCOMP			
+100°C	ENABLED	ENABLED	+13°C	17.4kΩ	23.2kΩ	14h	+100°C
0E		VDBAND	PMADDR	VRSEL			
		D-BAND0	N/A	N/A	OPEN	10kΩ	0h
0F		ICL	SPDUPC	K			
		100%	4pF	0.25	OPEN	10kΩ	0h

TABLE 13. DESIGN EXAMPLE (DVC_MEM = V_{CC}, 2-Phase)

REG					R_{UP}	R_{DW}	DATA
0C	IMAX	ADDRS	BT	RAMP			
	60	2	127V	1.2V	200kΩ	69.8kΩ	64h
0D	TMAX	DROOP	DE	TCOMP			
	+100°C	ENABLED	ENABLED	+13°C	17.4kΩ	23.2kΩ	14h
0E		VDBAND	PMADDR	VRSEL			
		D-BAND0	E0	VR12.5	OPEN	10kΩ	0h
			E0	VR12	OPEN	499kΩ	E0h
0F		ICL	SPDUPC	K			
		100%	4pF	0.25	97.6kΩ	53.6kΩ	49h

High Frequency Compensation

Connect a resistor of the same or slightly higher (~ 150%) value as the feedback impedance (R_{FB}) to the VR output to compensate the level-shifted output voltage during high frequency load transient events. Connecting more than 3x of R_{FB} to this pin virtually disables this feature.

When the droop disabled, an additional 500kΩ from this pin to VCC, as shown in Figure 30, is needed to ensure proper operation when the integrator capacitance from COMP to FB is too low (typically les than ~68pF).

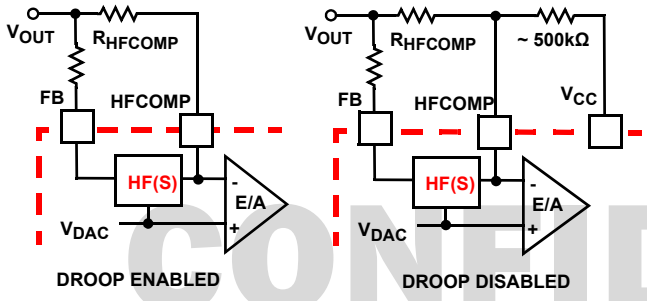


FIGURE 29. HIGH FREQUENCY COMPENSATION NETWORK

Dynamic VID Compensation (DVC)

During a VID transition, the resulting change in voltage on the FB pin and the COMP pin causes an AC current to flow through the error amplifier compensation components from the FB to the COMP pin. This current then flows through the feedback resistor, R_{FB}, and can cause the output voltage to overshoot or undershoot at the end of the VID transition. In order to ensure the smooth transition of the output voltage during a VID change, a VID-on-the-fly compensation network is required. This network is composed of a resistor and capacitor in series, R_{DVC} and C_{DVC}, between the DVC and the FB pin.

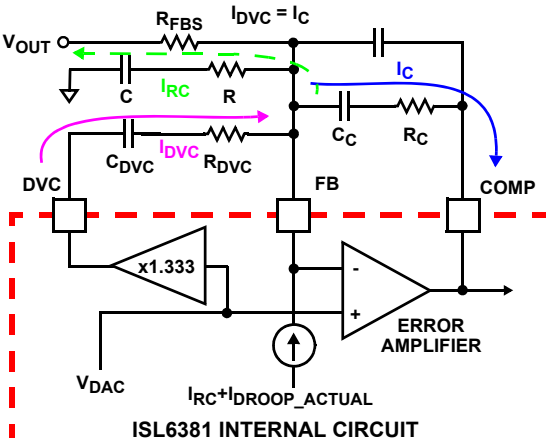


FIGURE 30. DYNAMIC VID COMPENSATION NETWORK

This VID-on-the-fly compensation network works by sourcing AC current into the FB node to offset the effects of the AC current flowing from the FB to the COMP pin during a VID transition. To create this compensation current, the controllers set the voltage on the DVC pin to be 4/3 of the voltage on the DAC. Since the error amplifier forces the voltage on the FB pin and the DAC to be equal, the resulting voltage across the series R_C between DVC and FB is equal to the DAC voltage. The R_C compensation components, R_{DVC} and C_{DVC}, can then be selected to create the desired amount of compensation current.

$$K1 = \frac{V_{IN}}{V_{RAMP}} \quad \text{(EQ. 25)}$$

$$R_{DVC} = A \cdot R_C \qquad A = \frac{K1}{3 \cdot (K1 - 1)} \quad \text{(EQ. 26)}$$

$$C_{DVC} = \frac{C_C}{A} \quad \text{(EQ. 27)}$$

The amount of compensation current required is dependant on the modulator gain of the system, k1, and the error amplifier R-C components, R_C and C_C, that are in series between the FB and COMP pins. Use Equations 25, 26, and 27 to calculate the R-C component values, R_{DVC} and C_{DVC}, for the VID-on-the-fly compensation network. For these equations: V_{IN} is the input voltage for the power train; V_{RAMP} is the oscillator ramp amplitude as in Equation 3; and R_C and C_C are the error amplifier R-C components between the FB and COMP pins.

During DVID transitions, extra current builds up in the output capacitors due to the C*dv/dt. The current is sensed by the controller and fed across the feedback resistor creating extra droop (if enabled) and causing the output voltage not properly tracking the DAC voltage. Placing a series R-C to ground from the FB pin can sink this extra DVID induced current.

$$C = \frac{C_{OUT} \cdot R_{LL}}{R_{FB}} \quad \text{(EQ. 28)}$$

$$R = \frac{C_{OUT} \cdot R_{LL}}{C} = R_{FB} \quad \text{(EQ. 29)}$$

When the output voltage overshoots during DVID, the RDVC-CDVC network can be used to compensate the movement of the error-amplifier compensation network. When the output voltage is lagging from DAC (or SVALERT#) or having a rough-off prior to the final settling of DVID, the R-C network can be used to compensate for the extra droop current generated by the C*dv/dt. Sometimes, both networks can work together to achieve the best result. In such cases, both networks need to be fine tuned in the board level for optimized performance. In memory mode, the DVC pin is not available for use.

Catastrophic Fault Protection

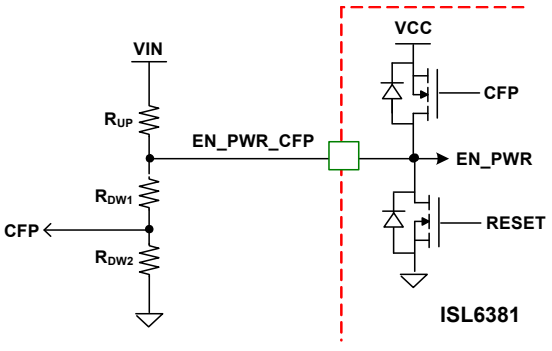


FIGURE 31. BIDIRECTIONAL EN_PWR_CFP

A catastrophic failure is a failure that will result in an exothermic event if the power source is not removed. A predominate catastrophic failure is a high-side FET shorting, which can cause

either an output overvoltage or an input overcurrent event. When the ISL6381 detects either event, an internal switch is turned on to pull the EN_PWR_CFP pin to VCC, as an indication of a component failure in the regulator's power train. As shown in Figure 31, a CFP fault signal can be generated by using a resistor divider on this pin. To be able to apply the signal to the PS_ON# switch of an ATX power supply or a simply external switch (2N7002), the CFP fault signal should be lower than 0.8V at maximum input voltage, VIN(max) and higher than 3V at lowest normal operational VCC (4.5V) when the input voltage (VIN) is removed. Given such conditions, the equivalent (in parallel) impedance of the upper leg (R_{UP}) and lower leg ($R_{DW} = R_{DW1} + R_{DW1}$) should be higher than 1kΩ. For instance, if we select the total lower leg impedance (R_{DW}) as 9.39kΩ, then the R_{UP} is calculated as in Equation 31, 100kΩ for an maximum POR of 10.72V, The lower leg impedance is then calculated by 2.74kΩ and 6.65kΩ, as in Equations 32 and 33, respectively.

$$R_{DW} = R_{DW1} + R_{DW2} \quad \text{(EQ. 30)}$$

$$R_{UP} = \frac{VIN(POR, max) - 0.92V}{0.92V} \cdot R_{DW} \quad \text{(EQ. 31)}$$

$$R_{DW1} = \frac{VIN(max)}{0.8V} \cdot (R_{UP} + R_{DW}) \quad \text{(EQ. 32)}$$

$$R_{DW2} = R_{DW} - R_{DW1} \quad \text{(EQ. 33)}$$

Prior to an exothermic event, the fault signal (CFP) should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply.

Input Current Sensing

The input current sensing uses Intersil patented technique to overcome the high common-mode input requirement challenge. An R-C network with thermal compensation across the inductor (LIN) extracts the DCR voltage, as shown in Figure 32, while the C might need to be split into 2; one close the LIN and one close to the controller. The input inductor can be used for current sensing and has the benefit of isolating noise from the rest of the board. However, when there are insufficient bulk capacitors on the power-stage side, a resonant tank can be formed by input ceramic capacitors and the inductor, yielding oscillation or audio noise during audio frequency range of heavy load transient. In addition, since Z_{NTC} network steals portion of sensed current from R_1, input current reading will have offset.

In many cases, a narrow input-rail PCB trace (but wide enough to carry DC current) is sufficient to serve as the isolation path. Thus, the input current sensing can simply be realized with an dedicated power resistor, as shown in Figure 33.

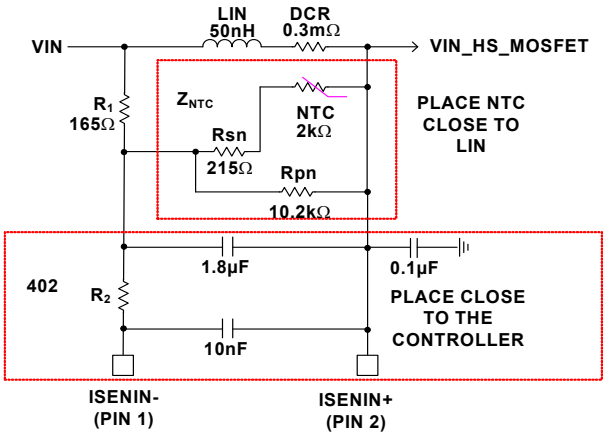


FIGURE 32. INPUT DCR-SENSING CONFIGURATION

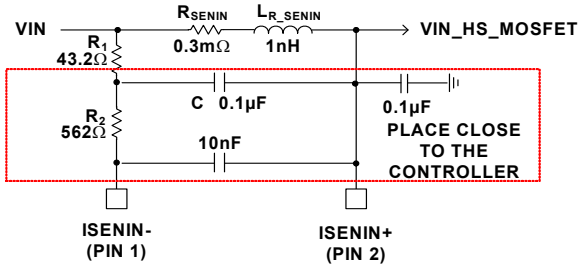


FIGURE 33. INPUT R-SENSING CONFIGURATION

The full scale of input current sensing is 10µA, read 1Fh with READ_IIN(89h), via PMBus, while the input overcurrent trip point is at 15µA. A design worksheet to select these components is available for use. Please contact Intersil Application support at www.intersil.com/design/.

When not used, connect ISENIN+ to V_{IN} and a resistor divider with a ratio of 1/3 on the ISENIN± pin (say 499kΩ) in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 34).

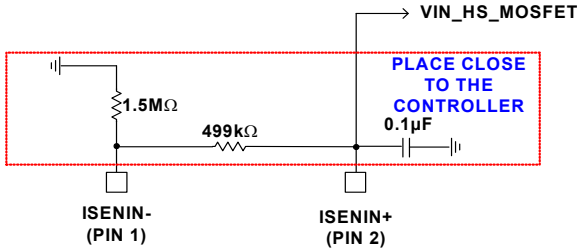


FIGURE 34. DISABLE PIN AND IIN CONFIGURATION

Auto-Phase Shedding

In addition to low power mode (PSI1/2/3/Decay) operation, the ISL6381 also incorporates auto-phase shedding feature to improve light to medium load range. The phase current dropping threshold is programmable with the IAUTO pin. The efficiency-optimized current trip point (I1) from 1-Phase to 2-Phase operation is approximated with Equation 34, which is K times larger than the efficiency-optimized current trip step (dI = I3 - I2) in between from 2-phase to 3-phase (I2) and from 3-phase to 4-phase (I3). The optimized-efficiency current trip point difference between phases remain constant I1/k.

$$I1 \approx \sqrt{\frac{2 \cdot (P_{QG} + P_{CORE} + P_{COSS})}{ESR_{IN} \cdot D + R_{ON} + L_{DS} \cdot F_{SW}}} \quad \text{(EQ. 34)}$$

$$R_{ON} = D \cdot r_{DS(ON)\_UP} + (1 - D) \cdot r_{DS(ON)\_LOW} + DCR$$

where P_{QG} is the per-phase gate charge loss, P_{CORE} is the inductor core loss, P_{QOSS} is the sum of high-side and low-side MOSFETs' output charge loss.

$$I_{IMON\_OPTIMIZED\_1\_PHASE} \approx \frac{64 \cdot DCR \cdot I1}{N_{MAX} \cdot R_{SET}} \quad \text{(EQ. 35)}$$

$$R_{AUTO} = \frac{1.2V}{I_{IMON\_OPTIMIZED\_1\_PHASE}} \quad \text{(EQ. 36)}$$

$$R_{AUTO} \approx \frac{1.2V \cdot N_{MAX} \cdot R_{SET}}{64 \cdot DCR \cdot I1} \quad \text{(EQ. 37)}$$

$$I_{(N)} \approx I1 \cdot \left(1 + \frac{1}{K} \cdot (N - 1)\right) \quad \text{(EQ. 38)}$$

TABLE 14. AUTO THRESHOLD AND NSPI SELECTION OPTIONS

C_{AUTO} (nF)	K	HYSTERESIS	NPSI
Auto Pin Shorted to VCC		AUTO OFF	SI2
0.82	1.5	12.5%	SI2
2.7	1.75	25%	SI2
8.2	1.75	25%	SI1
22	1.25	25%	SI1
56	1.5	12.5%	SI1
Auto Pin Shorted to GND		AUTO OFF	SI1

Equation 37 helps approximate the impedance on the AUTO pin, while the trip point hysteresis should be selected accordingly in Table 14. Typically, the higher the inductor ripple current, the higher percentage of hysteresis and K it requires. Following is an easy way to estimate R_{AUTO} value:

1. Disable AUTO mode via PMBus (E4 = 1h) or by tying AUTO pin GND and set VR at desired output level via PMBus or SVID bus.
2. Disable APA LEVEL via PMBus (F0 = 0h).
3. Obtain efficiency curve for 1 to 4-Phase by programming PMBus command, D0.
4. Determine I1 from the above test result.
5. Short AUTO pin to ground with a current meter to measure the IMON current ($I_{IMON\_OPTIMIZED\_1\_PHASE}$) when VR is at I1 load.
6. Calculate R_{AUTO} as in Equation 36.
7. Solder down both R_{AUTO} and C_{AUTO} (start with 56nF) and then enable AUTO mode by removing the short from AUTO pin.
8. Take efficiency curve and compare it with 1 to 4-Phase Efficiency Curves.
9. Tweak both R_{AUTO} and C_{AUTO} as needed for optimal Efficiency performance at targeted operating input and output voltage as well as airflow.
10. Obtain efficiency curve for couple boards and tweak both R_{AUTO} and C_{AUTO} to recenter overall efficiency of these boards.

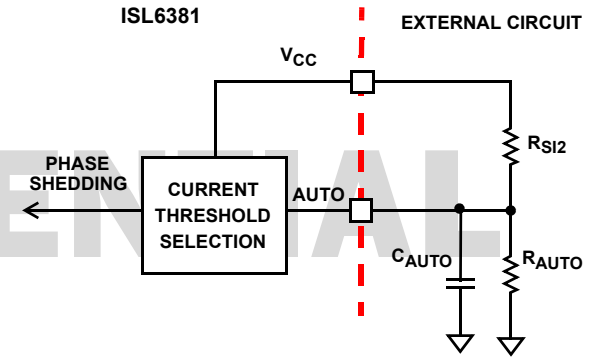


FIGURE 35. SIMPLIFIED AUTO-PHASE SHEDDING CIRCUIT

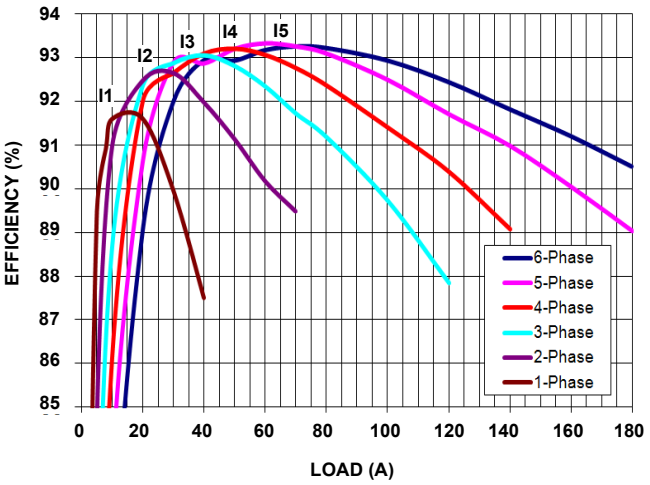


FIGURE 36. EFFICIENCY vs PHASE NUMBER

The auto-phase shedding feature can be disabled when this pin is tied high or shorted to GND. Although the auto-phase shedding is disabled, the low power mode operation still can be programmed via SVID bus.

In addition, the SMBus, PMBus, or I^2C gives flexibility to program number of operating phases. The minimum of auto-phase shedding is defaulted by NPSI in PSI1 mode (SI1 = 1-Phase and SI2 = 2-Phase), as in Table 3, and can also be programmed by the bus command code D1h, as in Table 20. The phase dropping sequence is summarized in Table 15.

To ensure dropped phases have sufficient energy to turn on the high-side MOSFET and sustain instant load apply after VR staying in light load condition for a long time (hours to days), a boot-refresh circuit turns on low-side MOSFET of each dropped phase to refresh the boot capacitor at a rate of slightly above 20kHz. The boot-fresh circuit is automatically turned off to boot efficiency when DAC drops to 0.60V.

To guarantee system reliability and robust operation during Auto mode operation, there are two actions:

1. The VR adds dropped phases back when the operational phase(s) carry too much current and triggers the thermal APA level, programmable via PMBus (EBh);
2. The VR immediately adds dropped phases back when the VR voltage drops and triggers the APA level, programmable via PMBus (F0h).

TABLE 15. PHASE DROPPING SEQUENCE

N	PWM# TIED TO V_{CC} (VCORE)	PWM# TIED TO V_{CC} (MEMORY)	PHASE SEQUENCE PSI# = PSI0
4		x_MEM= V_{CC}	4-2-3-1
3	PWM4	PWM4	3-2-1
2	PWM3	PWM3	2

SVID Operation

The device is compliant with Intel VR12.5/VR12/IMVP7 SVID protocol. To ensure proper CPU operation, refer to this document for SVID bus design and layout guidelines; each platform requires different pull-up impedance on the SVID bus, while impedance matching and spacing among DATA, CLK, and ALERT# signals must be followed. Common mistakes are insufficient spacing among signals and improper pull-up impedance. A simple operational instruction of SVID bus with Intel VTT Tool is documented in “VR12.5 Design and Validation” in Table 26.

TABLE 16. SVID SUPPORTED REGISTERS

INDEX	NAME	DESCRIPTION	ACCESS	DEFAULT
00h	Vendor ID	Intel Assigned VR Vendor ID	R	12h
01h	Product ID	Intersil Unique Product ID	R	61h
02h	Product Revision		R	01h
05h	Protocol ID	VR12 = 01h VR12.5 = 02h	R	“VRSEL” Pin
06h	Capability	VR capability Register 0h = Not supported; 1h = Supported Bit0 = IOUT (15h) = 1 Bit1 = VOUT (16h) = 1 Bit2 = POUT (18h) = 1 Bit3 = I Input (19h) = 1 Bit4 = V Input (1Ah) = 1 Bit5 = P Input (1Bh) = 1 Bit6 = Temperature (17h) = 0 Bit7 = 1 (1 if 15h is formatted FFh = ICC_MAX; 0 if 15h is formatted 1A per_LSB) ISENIN± IN USE = BFh ISENIN± NOT USED = 97h (NOT SUPPORT VIN, IIN, PIN 1/3 Divider on These Pins)	R	BFh or 97h
10h	Status_1	At End of Soft-Start	R	01h
11h	Status_2		R	00h
12h	TempZone		R	00h
15h	IOUT	Digital Reading of IMON	R	00h
1Ch	Status_last Read	A copy of the Status_2 data that was last read with GetReg (11h) command	R	00h
21h	ICC_MAX	Also Programmable via SMBus/PMBus/I^2C	R	“IM” and PWMx Pin
22h	Temp_max		R	“TMX” Pin
24h	SR_Fast	Programmable via “FDVID” and “MEM” pins: 0Ah = “>10mV/µs” 14h = “>20mV/µs” Or PMBus F6[3:0]: 10mV/µs to 53mV/µs	R	0Ah or 14h by Pin; or 0Ah to 35h by PMBus

TABLE 16. SVID SUPPORTED REGISTERS (Continued)

INDEX	NAME	DESCRIPTION	ACCESS	DEFAULT
25h	SR_Slow	Programmable via “FDVID” and “MEM” pins: 02h = “>2.5mV/µs” 05h = “>5mV/µs” Or PMBus F6[3:0]: 1/4 of SR_Fast	R	02h or 05h by Pin; or 02h to 0Dh by PMBus
26h	Vboot	Programmable via “BT” pin; or via PMBus E6h[7:0] prior to Enable High	RW	“BT” pin or PMBus E6h
30h	Vout_Max	Maximum Allowable DAC	RW	FFh
31h	VID Setting		RW	Vboot
32h	Power State		RW	00h
33h	Offset		RW	00h
34h	Multi_VR_Config	Set VR_Ready State when SetVID 0V after first Boot	RW	00h
35h	SetRegADR		RW	00h

NOTE: Capability (06h) depends upon ISENIN± configuration. Boot Voltage, ICC_MAX, TMAX, and Slew Rate (SR_FAST and SR_SLOW) can be programmed via PMBus/SMBus/I^{2}C prior VR Enable or during Operation. There is no NVM in the ISL6381, therefore, the configuration must be stored in BIOS or embedded PMBus controller to take effect for next power up. Alternatively, the ISL6381 can be biased by Standby Power to keep the configuration active.

The supported SVID/PMBus address are in pairs: 0/80, 0/82, 0/84 and 0/86 when “VR” = V_{CORE}; 2, 4, 6 and 8 when “VR” = Memory. A resistor register calculator is available for use to set the SVID address.

TABLE 17. SVID/PMBus ADDRESS (HEX)

“VR” = VCORE		“VR” = MEMORY	
SVID	PMBus	SVID	PMBus
0	80	2	Programmable via PMADDR register Pin
0	82	4	
0	84	6	
0	86	8	
E/F FOR ALL CALL			

SMBus, PMBus, and I^{2}C Operation

The ISL6381 features SMBus, PMBus, and I^{2}C with programmable address via hard-wired registers as in Figure 28, while SMBus/PMBus includes Packet Error Check (PEC) to ensure data properly transmitted. In addition, the output voltage, droop slope, enable, operating phase number, overvoltage setpoint, and the priority of SVID and SMBus/PMBus/I^{2}C can be written and read via this bus, as summarized in Table 20. Input, output, fault, and temperature telemetries can be read as summarized in Table 21. For proper operation, users should follow the SMBus, PMBus, and I^{2}C protocol, as shown Figure 39. Note that STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of register, as shown in Figure 39 (#3).

The supported SMBus/PMBus/I^{2}C addresses are in 8-bit format (including write and read bit): 80-8E, E0 to EE, and C8-CE. The least significant bit of the 8-bit address is for write (0h) and read (1h). For reference purpose, the 7-bit format addresses are also summarized in Table 18. There are a series set of read and write commands as summarized in Tables 20 and 21, respectively.

The SMBus/PMBus/I^{2}C allows to program the registers as in Table 10, except for SVID and SMBus/PMBus/I^{2}C addresses, 11ms after VCC above POR and prior to Enable pins (EN_PWR_CFP) high. The bus can also program default contents during this period. If all enable pins are high before the 9ms expires or no bus command is received during enable pins low, the register values are defaulted by the hard-wired 4-pin resister setting. If no PMBus WRITE command is successfully received during enable high or low, the register values can be reprogrammed by the using different resistor dividers during enable low; otherwise, other than the SVID and PMBus addresses, all other settings can be reprogrammed by the respective PMBus commands, as in Table 20. A resistor register calculator is available for use to set the SVID address. Please contact Intersil Application support at www.intersil.com/design/.

The 88h-8Eh are two-byte word reads with PEC (if applicable), while 78h, F2h, and other write command codes are one-byte word reads with PEC (if applicable).

TABLE 18. SMBus/PMBus/I²C 8-BIT AND 7-BIT FORMAT ADDRESS (HEX)

8-BIT	7-BIT	8-BIT	7-BIT	8-BIT	7-BIT
80/81	40	E0/E1	70	C8/C9	64
82/83	41	E2/E3	71	CA/CB	65
84/85	42	E4/E5	72	CC/CD	66
86/87	43	E6/E7	73	CE/CF	67
88/89	44	E8/E9	74		
8A/8B	45	EA/EB	75		
8C/8D	46	EC/ED	76		
8E/8F	47	EE/EF	77		

TABLE 19. EXAMPLE OF 4 CPUs ADDRESS PARTITIONING

4 CORES (V_{CORE})		16 MEMORIES	
SMBus/ PMBus/I²C	SVID	SMBus/ PMBus/I²C	SVID
80/81	0	88/89	2
82/83	0	8A/8B	4
84/85	0	8C/8D	6
86/87	0	8E/8F	8
		E0/E1	2
		E2/E3	4
		E4/E5	6
		E6/E7	8
		E8/E9	2
		EA/EB	4
		EC/ED	6
		EE/EF	8
		C8/C9	2
		CA/CB	4
		CC/CD	6
		CE/CF	8

NOTE: The ISL6381 alone can support 4 Cores and 16 Memories.

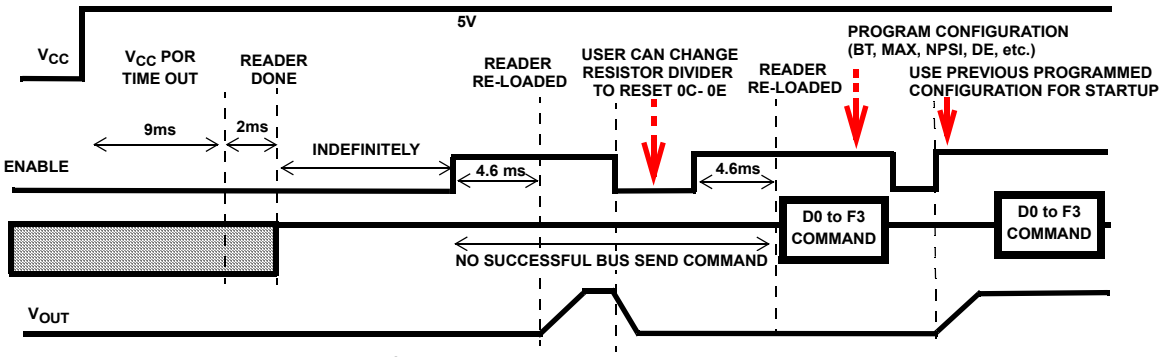


FIGURE 37. SIMPLIFIED SMBus/PMBus/I²C INITIALIZATION TIMING DIAGRAM WHEN NO BUS WRITE COMMAND RECEIVED

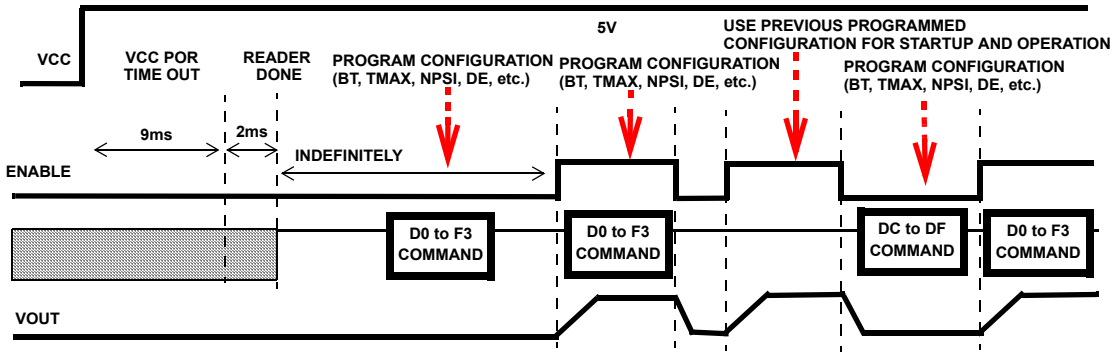
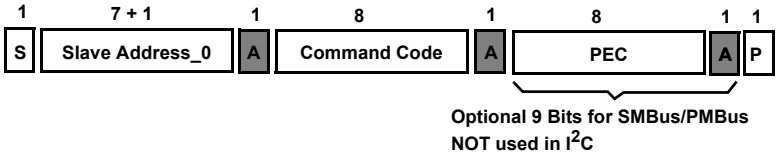


FIGURE 38. SIMPLIFIED SMBus/PMBus/I²C INITIALIZATION TIMING DIAGRAM WHEN BUS WRITE COMMAND

1. Send Byte Protocol

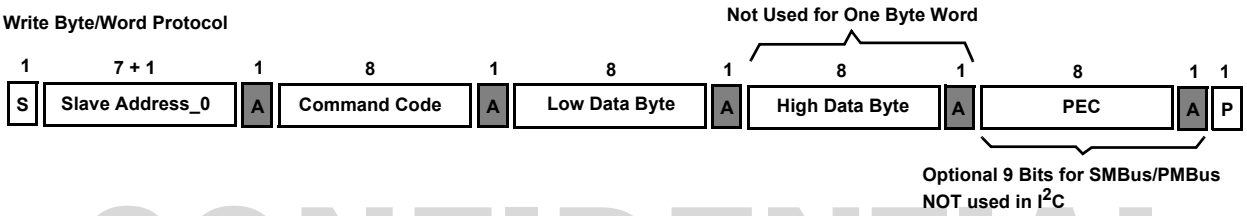


S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition

Acknowledge or DATA from Slave, ISL6381 Controller

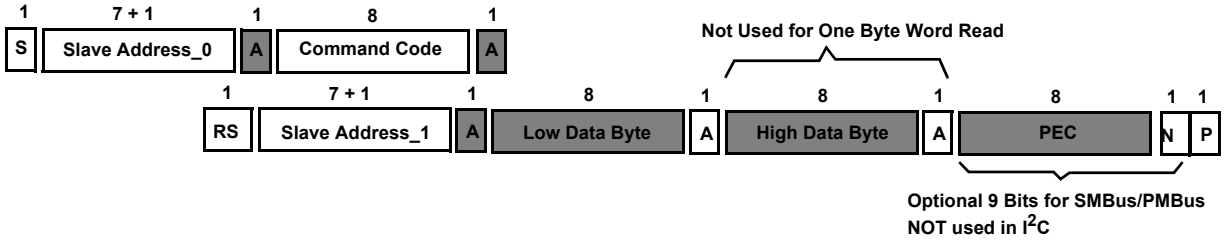
Example command: 03h Clear Faults
(This will clear all of the bits in Status Byte for the selected Rail)

2. Write Byte/Word Protocol



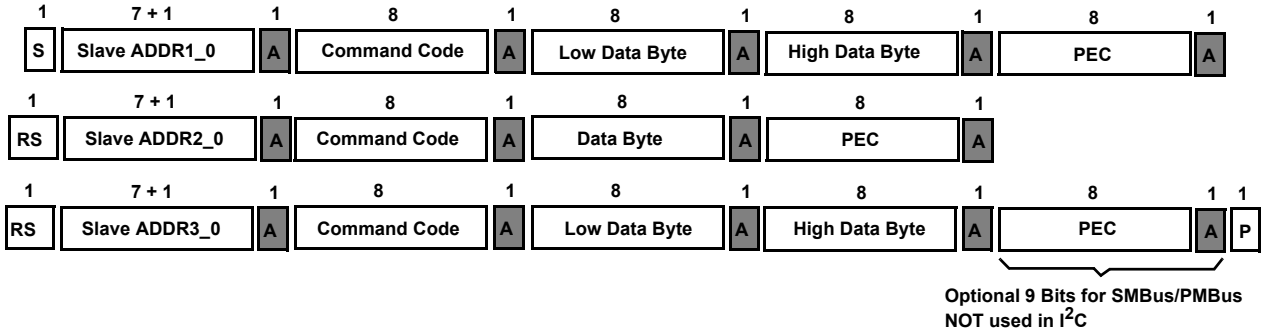
Example command: DAh SET_VID (one word, High Data Byte and ACK are not used)

3. Read Byte/Word Protocol



Example command: 8B READ_V_{OUT} (Two words, read voltage of the selected rail).
Note that all Writable commands are read with one byte word protocol.
STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

4. Group Command Protocol - No more than one command can be sent to the same Address



5. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus, not used for I^2C

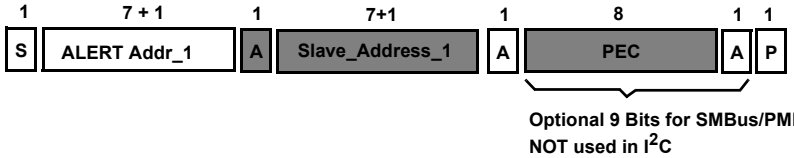


FIGURE 39. SMBus/PMBus/I^2C Protocol

TABLE 20. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION
D0h[2:0]	R/W	N_{PHASE}	OPERATE_PHASE_NUMBER	0h = 7h = N_{MAX}; 1h = 1 Phase; 2h = 2 Phases; 3h = 3 Phases; 4h = 4 Phases. N_{MAX} set by PWMx hard wired; for instance if PWM4 = VCC, N_{MAX} = 3 Phases. D0 should NOT be written until 50ms after soft-start and rewritten after DVID. When AUTO (RC to GND) function is enabled, D0h cannot use to program phase number but it reports the operating phase number.
D1h[1:0]	R/W	N_{PSI}	MIN_PHASE_NUMBER	Minimum Number of Auto Phase Shedding: 0h = 1-Phase; 1h = 2-Phase; 2h = 3-Phase; 3h = 4-Phase.
D2h[1:0]	R/W	00h	AUTO_BLANK	Time Between Subsequent Phase Drops: 0h = 4.6ms; 1h = 2.3ms; 2h = 1.2ms; 3h = 0.6ms
D3h[2:0]	R/W	00h	DROOP_TRIM	0h = 100%, 1h = 75%, 2h = 50%, 3h = 25%, 4h = 5%
D4h[0]	R/W	“DRP” Pin	DROOP_EN	0h = Droop disabled; 1h = Droop enabled; Default by pin.
D5h[1:0]	R/W	00h	FREQ_LIMITER	Maximum PWM Sustained Frequency Under Repetitive Load: 0h = 2 Fsw; 1h = 3/2 Fsw; 2h = 3h = Infinity Frequency limiter is not available for new speedup (B2 0h)
D6h[1:0]	R/W	00h	LOCK_SVID	set SVID and SMBus/PMBus/I^2C Priority (See Table 22 for details)
D7h[0]	R/W	01h	ENABLE	0h = Disabled; 1h = Enabled
D8h[2:0]	R/W	“VRSEL” pin AND 2.15V	SET_OVP	OVP During Operation (After End of Soft Start, Defaulted by VRSEL Pin): D8[0]: 0h = 175mV, 1h = 350mV; OVP = VID+ D8[0] DEFAULT: 0h for VR12 mode, 1h for VR12.5 mode; Prior to End of Soft-Start (Fixed OVP, default 2h): D8[2:1]: 0h = 3.350V, 1h = 2.65V; 2h = 2.150V; 3h = 1.85V;
D9h[0]	R/W	“DE” Pin	DIODE_EMULATION#	0h = Enabled; 1h = Disabled
DAh[7:0]	R/W	“BT” Pin	SET_VID	SVID Bus VID Code (See Table 4)
DBh[7:0]	R/W	00h	SET_OFFSET	SVID Bus OFFSET Code (See Table 4)
DC-DEh[7:0] B0h[7:0]	R	“IM”,“TMX” “VDBAND” “ICL” Pins	Config Registers	Reference to Resistor Reader. DC maps to config_0C, DD maps to config_0D, DE maps to config_0E; B0 maps config_0F.
DF[4:0]	R/W	0h	PROTECTION_DISABLE	Protection Disable [0, 0, 0, IPH_LIMIT, OCP_V, OCP_I, IIN_OCP, OVP] IPH_LIMIT = Phase Cycle-by-Cycle Current Limiting; OCP_V = Output OCP Trip at IMON pin; OCP_I = Output OCP Trip at 100µA; IIN_OCP = Input Overcurrent Trip; OVP = Output Overvoltage.
E1[1:0]	R/W	“AUTO” Pin	AUTO_K	Programmable AUTO Mode K Factor: 0h = 1.25; 1h = 1.5; 2h = 1.75; 3h = 1.0; Default by AUTO pin.
E2[1:0]	R/W	“AUTO” Pin	AUTO_HYS	Programmable AUTO Mode Hysteresis Factor: 0h = 50%; 1h = 25%; 2h = 16.6%; 3h = 12.5%; Default by AUTO pin.
E4[0]	R/W	“AUTO” Pin	AUTO_DISABLE	Disable AUTO Mode: 0h = Enabled; 1h = Disabled
E5[1:0]	R/W	00h	AUTO_I1	Programming I1 in AUTO Mode: 0h = 100%; 1h = 80%; 2h = 90%; 3h = 110%.
E6[7:0]	R/W	“BT” Pin	BOOT_Voltage	Program Vboot (26h) in SVID: VR12.5: 0, 0.5V to 3.04V; VR12: 0, 0.25 to 1.52V. See Table 4.
E7[0]	R/W	“NPSI” Pin	NPSI	PS1 Phase Count: 0h = 1-Phase; 1h = 2-Phase
E8[2:0]	R/W	“TMX” Pin	TMAX	Program Temp_max (22h) in SVID: 0h = 100°C; 1h = +105°C; 2h = +110°C; 3h = +115°C; 4h = +120°C; 5h = +85°C; 6h = +90°C; 7h = +95°C
E9[2:0]	R/W	“TC” Pin	TCOMP	0h = OFF; 1h = -2.5°C; 2h = +2.5°C; 3h = +7°C; 4h = +13°C; 5h =+18.9°C; 6h = +24.3°C; 7h = +29.7 °C.
EA[7:0]	R/W	“IM” and PWMx Pins	IMAX	Program ICC_MAX (21h) in SVID: 0 to 255A, 1A/step; 0h: FFh = 0A: 255A
EB[1:0]	R/W	00h	THERMAL_APA	Thermal Trigger APA Level to Add Phases in AUTO Mode: 0h = 75%; 1h = 82%; 2h = 91%; 3h = 100% of TMAX

TABLE 20. SMBus, PMBus, AND I²C WRITE AND READ REGISTERS (Continued)

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION
EC[0]	R/W	00h	POS_LL_EN	Positive Load-Line: 0h = Disabled; 1h = Enabled
ED[1:0]	R/W	00h	POS_LL	Positive Load-Line Range: 0h = 4mV, 1h = 8mV; 2h = 16mV, 3h = 32mV at IMON full scale of 3V. 0mV when IMON = 0V.
EE[0]	R/W	00h	FREQ_DITHER	Frequency Dithering: 0h = OFF; 1h = ON, -12.5kΩ, 0, 12.5kHz
EF[1:0]	R/W	00h	CFP	0h = 100%, 1h = 110%, 2h = 120%; 3h = 130%
F0h[2:0]	R/W	02h	APA_TRIGGER_LEVEL	APA Trigger Level to Add Phases in AUTO Mode: 0h = Disable; 1h = 10mV; 2h = 20mV; 3h = 30mV; 4h = 40mV; 5h = 50mV; 6h = 60mV; 7h = 70mV
F1h[1:0]	R/W	03h	APA_TIME_CONSTANT	0h = Tsw; 1h = Tsw/2; 2h = Tsw/4; 3h = Tsw/8.
F3h[0]	R/W	01h	BOOT_REFRESH_ENABLE	0h = Disabled; 1h = Enabled. Boot refresh circuits is automatically turned off when DAC is lower than 0.605V.
F4[1:0]	R/W	00h	OCP_TRIM	OCP Trim Level for Average OCP and Cycle-By-Cycle Limiting: 0h = 1.0, 1h = 1.1, 2h = 1.2; 3h = 1.4 of IMON
F5h[5:0]	R/W	0Fh	FREQ_TRIM	Programmable range -187.5kHz (0h) to 600kHz (3F) with ~12.5kHz/step above based frequency (set by FS pin). See Table 24.
F6h[3:0]	R/W	0h or 1h by "FDVID" and "MEM" Pins	FDVID	Program SetVID_FAST (24h) in SVID: 0h = 10mV/µs; 1h = 20mV/µs; 2h = 14mV/µs; 3h = 17mV/µs; 4h = 26mV/µs; 5h = 32mV/µs; 6h = 40mV/µs; 7h = 53mV/µs
F7h[2:0] F8h[2:0] F9h[2:0] FAh[2:0]	R/W	4h	F7 = BAL_TRIM_PHASE1 F8 = BAL_TRIM_PHASE2 F9 = BAL_TRIM_PHASE3 FA = BAL_TRIM_PHASE4	0h = -12% of full scale 1h = -9% of full scale 2h = -6% of full scale 3h = -3% of full scale 4h = No Offset 5h = +3% of full scale 6h = +6% of full scale 7h = +9% of full scale
FD[1:0]	R/W	2h or 3h by "RM" Pin	VRAMP	0h = 0.75V; 1h = 1V; 2h = 1.2V; 3h = 1.5V
BF[4:0]	R/W	Trim	IMON_TRIM	0h = 0.00µA .....10h = -0.25µA 1h = 0.25µA.....11h = -0.50µA 2h = 0.50µA.....12h = -0.75µA 3h = 0.75µA.....13h = -1.00µA 4h = 1.00µA.....14h = -1.25µA 5h = 1.25µA.....15h = -1.50µA 6h = 1.50µA.....16h = -1.75µA 7h = 1.75µA.....17h = -2.00µA 8h = 2.00µA.....18h = -2.25µA 9h = 2.25µA.....19h = -2.50µA Ah = 2.50µA.....1Ah = -2.75µA Bh = 2.75µA.....1Bh = -3.00µA Ch = 3.00µA.....1Ch = -3.25µA Dh = 3.25µA.....1Dh = -3.50µA Eh = 3.50µA.....1Eh = -3.75µA Fh = 3.75µA.....1Fh = -4.00µA
B1[2:0]	R/W	"ICL" Pin	CYCLE_LIMITING	Cycle-By-Cycle Limiting, On Top of F4h (Data Not Valid Until Enable): 0h = 125%; 1h = 110%; 2h = 100%; 3h = 95%; 4h = 90% 5h = 85%; 6h = 80; 7h = 70%
B2[2:0]	R/W	"SPDUPC" Pin	SPEEDUP_CTRL	Speed Up Capacitance Control (Data Not Valid Until Enable): 0h = ORIGINAL; 1h = 2pF;2h = 4pF; 3h = 6pF; 4h = 8pF; 5h = 10pF; 6h = 12pF;7h = 16pF; The higher the Capacitance, the faster the speed, but could lead to PS1/2 to PS0 transition oscillation. *Use Caution*.
B3[1:0]	R/W	"K" Pin	COMPBT_K	COMP Voltage Clamp to Fire PWM Pulses (Data Not Valid Until Enable): 0h = ORIGINAL; 1h = 0.25; 2h = 0.5; 3h = 0.75.

TABLE 20. SMBus, PMBus, AND I²C WRITE AND READ REGISTERS (Continued)

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION
B4[2:0]	R/W	"VDBAND" Pin	VDBAND	D-Band COMP Ripple Speed Up Control (Data Not Valid Until Enable): 0h = 12.5mV; 1h = 25mV; 2h = 37.5mV; 3h = 50mV; 4h = 62.5mV; 5h = 75mV; 6h = 87.5mV; 7h = 100mV;
03h	W		CLEAR_FAULTS	Clear "Latched" Fault Registers in 78h For Selected Rail
ARA	R		ALERT_RESPONSE_ADDRESS	8-bit Address: 0001_1001, 25h; 7-bit Address: 0C

NOTE: When the controller is reset by the Enable pins (TM_EN_OTP or EN_PWR), the programmed registers will be stored as long there is still have power on VCC. SVID's Boot Voltage, ICC_MAX, TMAX, and Slew Rate (SR_FAST and SR_SLOW) can be programmed via PMBus/SMBus/I²C prior VR Enable or during Operation. There is no NVM in the ISL6381, therefore, the configuration must be stored in BIOS or embedded PMBus controller to take effect for next power-up. Alternatively, the ISL6381 can be biased by Standby Power to keep the configuration active.

TABLE 21. SMBus, PMBus, AND I²C TELEMETRIES

CODE	WORD LENGTH (BYTE)	COMMAND NAME	DESCRIPTION	TYPICAL RESOLUTION
88h	TWO	READ_VIN	Input Voltage (25.5V = FF)	8-BIT, 100mV
89h	TWO	READ_IIN	Input Current (1Fh = 10µA)	5-BIT, IIN_FULL/31 (~1A)
8Bh	TWO	READ_VOUT	Output Voltage (Up to 3.04V) (See Figure 41)	10-BIT, 5mV
8Ch	TWO	READ_IOUT	Output Current (ICCMAX = 2.5V IMON)	8-BIT, ~1A
8Dh	TWO	READ_TEMPERATURE_1	TM Temperature (See Table 23)	8-BIT, ~1°C*
96h	TWO	READ_POUT	Output Power	~2W (at 2V,I 1A LSB)
97h	TWO	READ_PIN	Input Power	~12W (at 12V, 1A LSB)
78h	ONE	STATUS_BYTE (Read with One Byte Word + PEC)	Fault Reporting; Bit5 = Overvoltage; Bit4 = Overcurrent, ≥ I_{MAX}; Bit2= Over-temperature, ≥ T_{MAX}; Bit1 = Communication Error. When TM_EN_OTP is used as an Enable, Bit2 will flag OT (= 1), CLEAR_FAULTS (03h) command must be sent to clear the fault after VR start-up.	[0, 0, OV, OC, 0, OT, CML, 0]
F2h	ONE	CPU_POWER_STATE	VR Operating Power Stage: 0h = PSI0; 1h = PSI1; 2h = PSI2 (or Decay); 3h = PSI3	

NOTE: The 88h-8Eh are two bytes word, while all others are one byte word.

TABLE 22. LOCK_SVID

	SVID			SMBus, PMBus or I²C			
D6h	setVID	setPS (1/2/3) and setDecay	set OFFSET	setVID	set OFFSET	FINAL DAC	TARGETED APPLICATIONS
00h	Yes	Yes	Yes	Not	Not	SV_VID + SV_OFFSET	Not Overclocking
01h	Yes	Yes	ACK ONLY	Not	Yes	SV_VID + PM_OFFSET	Not Overclocking
02h	Yes	ACK ONLY	ACK ONLY	Not	Yes	SV_VID + PM_OFFSET	Overclocking
03h	ACK ONLY	ACK ONLY	ACK ONLY	Yes	Yes	PM_VID + PM_OFFSET	Overclocking

NOTE: The ISL6381 controller is designed to be such that all SVID commands are always acknowledged as if the SMBus, PMBus or I²C does not exist. To avoid the conflict between SMBus/PMBus/I²C and SVID bus during operation, the user should execute this command prior to Enable (TM_EN_OTP and EN_PWR_CFP) high or during the boot period. When operating in 01h option, SMBus/PMBus/I²C's OFFSET should only adjust slightly higher or lower (say ±20mV) than SVID OFFSET for margining purpose or PCB loss compensation so that CPU will not draw significantly more power in PSI1/2/3/Decay mode. To program full range of PM_OFFSET for overclocking applications, the user should select 02h or 03h options. 03h option gives users full control of the output voltage (VID+OFFSET) via SMBus/PMBus/I²C, commonly used in overclocking applications. Prior to a successful written PMBus VID or OFFSET, the controller will continue executing SVID VID or OFFSET command.

TABLE 23. TYPICAL TEMPERATURE (8Dh and 8Eh)

TEMP. (0°C)	$V_{TM(S)}$ OF VCC (%)	CODE (HEX)	TEMP. (0°C)	$V_{TM(S)}$ OF VCC (%)	CODE (HEX)
0	95.0	F2	71	58.9	96
1	94.8	F1	72	58.2	94
2	94.6	F1	73	57.5	92
3	94.4	F0	74	56.7	90
4	94.1	F0	75	56.0	8E
5	93.9	EF	76	55.3	8D
6	93.6	EE	77	54.6	8B
7	93.4	EE	78	53.9	89
8	93.1	ED	79	53.2	87
9	92.8	EC	80	52.4	85
10	92.6	EC	81	51.7	83
11	92.3	EB	82	51.0	82
12	92.0	EA	83	50.3	80
13	91.6	E9	84	49.6	7E
14	91.3	E8	85	48.9	7C
15	91.0	E7	86	48.2	7B
16	90.7	E7	87	47.6	79
17	90.3	E6	88	46.9	77
18	89.9	E5	89	46.2	75
19	89.6	E4	90	45.5	74
20	89.2	E3	91	44.9	72
21	88.8	E2	92	44.2	70
22	88.4	E1	93	43.5	6F
23	88.0	E0	94	42.9	6D
24	87.6	DF	95	42.3	6B
25	87.2	DE	96	41.6	6A
26	86.7	DD	97	41.0	68
27	86.3	DC	98	40.4	66
28	85.8	DA	99	39.7	65
29	85.4	D9	100	39.1	63
30	84.9	D8	101	38.5	62
31	84.4	D7	102	37.9	60
32	83.9	D6	103	37.3	5F
33	83.4	D4	104	36.7	5D
34	82.9	D3	105	36.1	5C
35	82.4	D2	106	35.5	5A
36	81.9	D0	107	35.0	59
37	81.3	CF	108	34.4	57
38	80.8	CD	109	33.9	56

TABLE 23. TYPICAL TEMPERATURE (8Dh and 8Eh) (Continued)

TEMP. (0°C)	$V_{TM(S)}$ OF VCC (%)	CODE (HEX)	TEMP. (0°C)	$V_{TM(S)}$ OF VCC (%)	CODE (HEX)
39	80.2	CC	110	33.3	54
40	79.7	CB	111	32.8	53
41	79.1	C9	112	32.2	52
42	78.5	C8	113	31.7	50
43	77.9	C6	114	31.2	4F
44	77.3	C5	115	30.7	4E
45	76.7	C3	116	30.2	4D
46	76.1	C2	117	29.7	4B
47	75.5	C0	118	29.2	4A
48	74.8	BE	119	28.7	49
49	74.2	BD	120	28.2	48
50	73.5	BB	121	27.8	46
51	72.9	B9	122	27.3	45
52	72.2	B8	123	26.9	44
53	71.6	B6	124	26.4	43
54	70.9	B4	125	26.0	42
55	70.2	B3	126	25.5	41
56	69.5	B1	127	25.1	40
57	68.8	AF	128	24.7	3E
58	68.2	AD	129	24.3	3D
59	67.5	AC	130	23.9	3C
60	66.8	AA	131	23.5	3B
61	66.1	A8	132	23.1	3A
62	65.4	A6	133	22.7	39
63	64.6	A4	134	22.3	38
64	63.9	A3	135	21.9	37
65	63.2	A1	136	21.6	36
66	62.5	9F	137	21.2	36
67	61.8	9D	138	20.8	35
68	61.1	9B	139	20.5	34
69	60.3	99	140	20.1	33
70	59.6	98			

TABLE 24. FREQUENCY TRIM TABLE

F5h	FREQ (kHz)	F5h	FREQ (kHz)	F5h	FREQ (kHz)	F5h	FREQ (kHz)
0	-187.5	10	12.5	20	212.5	30	412.5
1	-175.0	11	25.0	21	225.0	31	425.0
2	-162.0	12	37.5	22	237.5	32	437.5
3	-150.0	13	50.0	23	250.0	33	450.0
4	-137.5	14	62.5	24	262.5	34	462.5
5	-125.0	15	75.0	25	275.0	35	475.0
6	-112.5	16	87.5	26	287.5	36	487.5
7	-100.0	17	100.0	27	300.0	37	500.0
8	-87.5	18	112.5	28	312.5	38	512.5
9	-75.0	19	125.0	29	325.0	39	525.0
A	-62.5	1A	137.5	2A	337.5	3A	537.5
B	-50.0	1B	150.0	2B	350.0	3B	550.0
C	-37.5	1C	162.5	2C	362.5	3C	562.5
D	-25.0	1D	175.0	2D	375.0	3D	575.0
E	-12.5	1E	187.5	2E	387.5	3E	587.5
F	0.0	1F	200.0	2F	400.0	3F	600.0

Figure 40 shows a typical measurement of programmed switching frequency via PMBus (F5h). For lower than 400kHz, the step changes to ~10kHz/step.

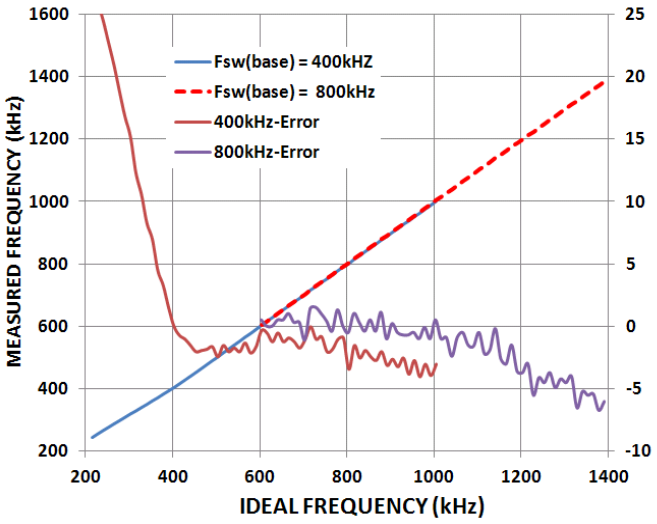


FIGURE 40. PROGRAMMABLE FREQUENCY ACCURACY

The output voltage reads out with a 10-bit ADC with a typical resolution of 5mV. For example, a 1CCh = 460DEC = 460*5mV/1000 = 2.3V. Figure 41 shows the VOUT_ADC accuracy at various VCC voltage. For a better accuracy, a higher range VCC, but below 5.5V, is preferred.

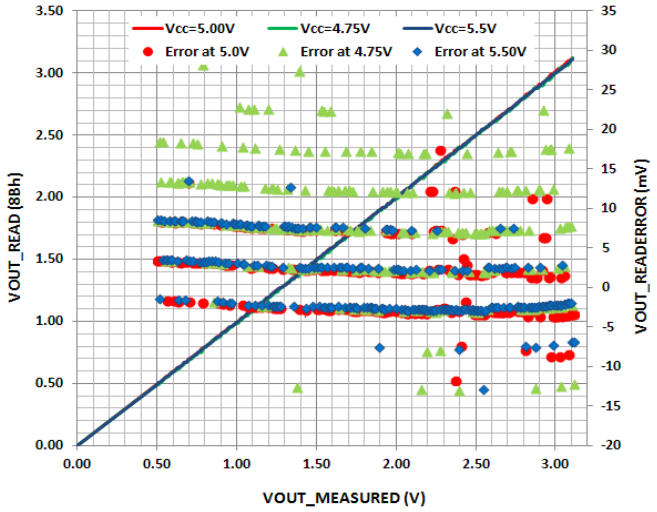


FIGURE 41. V_{OUT}_ADC vs V_{CC} AT ROOM TEMPERATURE

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs, which include schematics, bills of materials, and example board layouts for common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily upon the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 25A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat dissipating surfaces accuracy.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

Lower MOSFET Power Calculation

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$).

In Equation 39, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor current (see Equation 1 on page 14); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{PP}^2}{12}\right]\cdot(1-d) \quad \text{(EQ. 39)}$$

An additional term can be added to the lower MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, F_{sw}; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)}F_{SW}\left[\left(\frac{I_M}{N}+\frac{I_{PP}}{2}\right)t_{d1} + \left(\frac{I_M}{N}-\frac{I_{PP}}{2}\right)t_{d2}\right] \quad \text{(EQ. 40)}$$

Finally, the power loss of output capacitance of the lower MOSFET is approximated in Equation 41:

$$P_{LOW,3} \approx \frac{2}{3}\cdot V_{IN}^{1.5}\cdot C_{OSS\_LOW}\cdot\sqrt{V_{DS\_LOW}}\cdot F_{SW} \quad \text{(EQ. 41)}$$

where C_{OSS_LOW} is the output capacitance of lower MOSFET at the test voltage of V_{DS_LOW}. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

Thus, the total maximum power dissipated in each lower MOSFET is approximated by the summation of PLOW,1, PLOW,2 and PLOW,3.

Upper MOSFET Power Calculation

In addition to $r_{DS(ON)}$ losses, a large portion of the upper MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper MOSFET switching times; the lower MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 42, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N}+\frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right)F_{SW} \quad \text{(EQ. 42)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 43, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N}-\frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right)F_{SW} \quad \text{(EQ. 43)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across V_{IN}. The power dissipated as a result is $P_{UP,3}$ and is approximated in Equation 44:

$$P_{UP,3} = V_{IN}Q_{rr}F_{SW} \quad \text{(EQ. 44)}$$

The resistive part of the upper MOSFET's is given in Equation 45 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{PP}^2}{12}\right]\cdot d \quad \text{(EQ. 45)}$$

Equation 46 accounts for some power loss due to the drain-source parasitic inductance (L_{DS}, including PCB parasitic inductance) of the upper MOSFETs, although it is not the exact:

$$P_{UP,5} \approx L_{DS}\left(\frac{I_M}{N}+\frac{I_{PP}}{2}\right)^2 \quad \text{(EQ. 46)}$$

Finally, the power loss of output capacitance of the upper MOSFET is approximated in Equation 47:

$$P_{UP,6} \approx \frac{2}{3}\cdot V_{IN}^{1.5}\cdot C_{OSS\_UP}\cdot\sqrt{V_{DS\_UP}}\cdot F_{SW} \quad \text{(EQ. 47)}$$

where C_{OSS_UP} is the output capacitance of lower MOSFET at test voltage of V_{DS_UP}. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 42 to 47. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Current Sensing Resistor

The resistors connected to the ISEN+ pins determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point. Select values for these resistors by using Equation 48:

$$R_{ISEN} = \frac{R_X}{100\times10^{-6}}\frac{I_{OCP}}{N} \quad \text{(EQ. 48)}$$

where R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method, and I_{OCP} is the desired overcurrent trip point. Typically, I_{OCP} can be chosen to be 1.2 times the maximum load current of the specific application.

With integrated temperature compensation, the sensed current signal is independent of the operational temperature of the power stage, i.e. the temperature effect on the current sense element R_X is cancelled by the integrated temperature compensation function. R_X in Equation 48 should be the resistance of the current sense element at the room temperature.

When the integrated temperature compensation function is disabled by selecting "OFF" TCOMP code, the sensed current will be dependent on the operational temperature of the power stage, since the DC resistance of the current sense element may

be changed according to the operational temperature. The R_X in Equation 48 should be the maximum DC resistance of the current sense element at the all operational temperature.

In certain circumstances, especially for a design with an unsymmetrical layout, it may be necessary to adjust the value of one or more ISEN resistors for VR. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run cooler than the average, choose new, larger values of R_{ISEN} for the affected phases (see the section entitled "Current Sensing" on page 17). Choose $R_{ISEN,2}$ in proportion to the desired increase in temperature rise in order to cause proportionally more current to flow in the cooler phase, as shown in Equation 49:

$$R_{ISEN,2} = R_{ISEN}\frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 49)}$$

$$\Delta R_{ISEN} = R_{ISEN,2} - R_{ISEN}$$

In Equation 49, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. Since all channels' R_{ISEN} are integrated and set by one RSET, a resistor (ΔR_{ISEN}) should be in series with the cooler channel's ISEN+ pin to raise this phase current. While a single adjustment according to Equation 49 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labelled R_{FB} in Figure 12. Its value depends on the desired loadline requirement of the application.

The desired loadline can be calculated using Equation 50:

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}} \quad \text{(EQ. 50)}$$

where I_{FL} is the full load current of the specific application, and VR_{DROOP} is the desired voltage droop under the full load condition.

Based on the desired loadline R_{LL}, the loadline regulation resistor can be calculated using Equation 51:

$$R_{FB} = \frac{N \cdot R_{ISEN} \cdot R_{LL}}{R_X} \quad \text{(EQ. 51)}$$

where N is the active channel number, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SEN} depending on the sensing method.

If one or more of the current sense resistors are adjusted for thermal balance (as in Equation 49), the load-line regulation resistor should be selected based on the average value of the current sensing resistors, as given in Equation 52:

$$R_{FB} = \frac{R_{LL}}{R_X}\sum_n R_{ISEN(n)} \quad \text{(EQ. 52)}$$

where $R_{ISEN(n)}$ is the current sensing resistor connected to the n^{th} ISEN+ pin.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 53:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 53)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $DV < DV_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 14 and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance, as shown in Equation 54.

$$L \geq ESR \cdot \frac{V_{OUT} \cdot K_{RCM}}{F_{SW} \cdot V_{IN} \cdot V_{PP(MAX)}} \quad \text{(EQ. 54)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 55 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output voltage deviation than the leading edge. Equation 56 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \le \frac{2 \cdot N \cdot C \cdot V_{OUT}}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right] \quad \text{(EQ. 55)}$$

$$L \le \frac{1.25 \cdot N \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 56)}$$

Switching Frequency Selection

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 44, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output voltage ripple as outlined in "Output Filter Design" on page 46. Choose the lowest switching frequency that allows the regulator to meet the transient-response and output voltage ripple requirements.

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs, which is related to duty cycle and the number of active phases. The input RMS current can be calculated with Equation 57.

$$I_{IN,RMS} = \sqrt{K_{IN,CM}^2 \bullet Io^2 + K_{RAMP,CM}^2 \bullet I_{Lo,PP}^2} \quad \text{(EQ. 57)}$$

$$K_{IN,CM} = \sqrt{\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N^2}} \quad \text{(EQ. 58)}$$

$$K_{RAMP,CM} = \sqrt{\frac{m^2(N \bullet D - m + 1)^3 + (m-1)^2(m - N \bullet D)^3}{12N^2D^2}} \quad \text{(EQ. 59)}$$

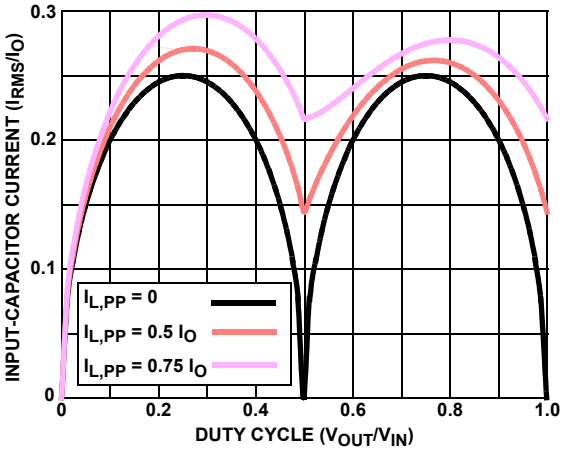


FIGURE 42. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

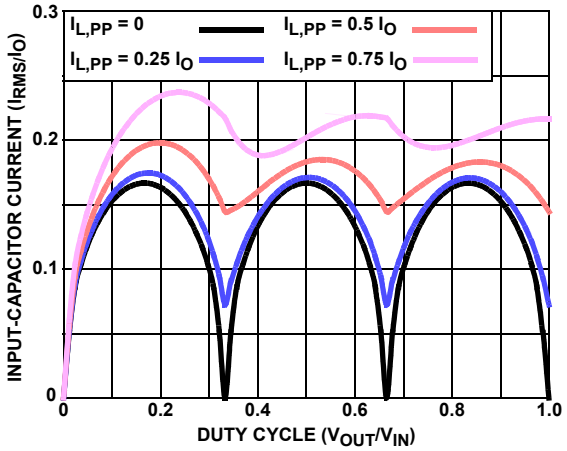


FIGURE 43. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

For a 2-phase design, use Figure 42 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

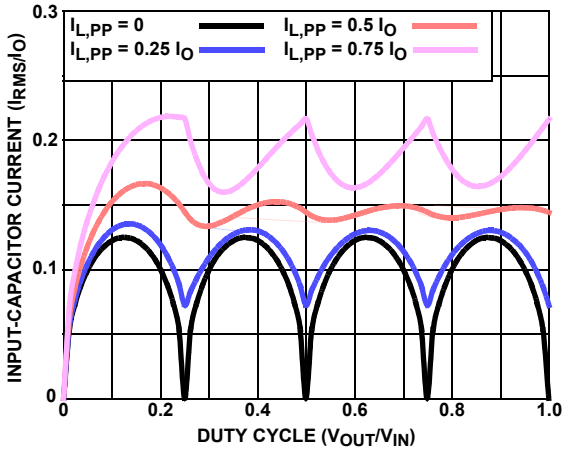


FIGURE 44. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

Figures 28 and 30 provide the same input RMS current information for 3 and 4-phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as previously described.

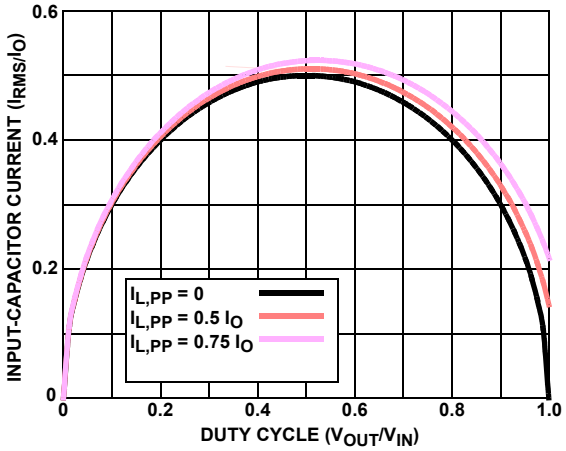


FIGURE 45. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize noise suppression.

MULTIPHASE RMS IMPROVEMENT

Figure 45 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a 2-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{L,PP}$ to I_O of 0.5. The single phase converter would require 17.3A_{RMS} current capacity while the 2-phase converter would only require 10.9A_{RMS}. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

Layout and Design Considerations

The following layout and design strategies are intended to minimize the noise coupling, the impact of board parasitic impedances on converter performance and to optimize the heat dissipating capabilities of the printed-circuit board. This section highlights some important practices, which should be followed during the layout process. A layout checklist in Excel format is available for use.

Pin Noise Sensitivity, Design and Layout Consideration

Table 25 shows the noise sensitivity of each pin and their design and layout consideration. All pins and external components should not be across switching nodes and should be placed in general proximity to the controller.

TABLE 25. PIN DESIGN AND/OR LAYOUT CONSIDERATION

PIN NAME	NOISE SENSITIVE	DESCRIPTION
ISENIN-	Yes	Connect to the input supply side of the input inductor or resistor pin with L/DCR or ESL/R matching network in close proximity to the controller. Place NTC in the close proximity to the input inductor for thermal compensation. A local 10nF decoupling capacitor between ISENIN+ and ISENIN- is preferred. The DCR sensing with thermal compensation will yield no load offset reading. Resistor sensing is preferred for accurate reporting.
ISENIN+	Yes	Connects to the Drain of High-side MOSFET side of the input inductor or resistor pin. A local 0.1µF ceramic capacitor is recommended. When it is not used, connect ISENIN+ to V_{IN} and a resistor divider with a ratio of 1/3 on ISENIN± pins (say 499kΩ) in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 34). ISENIN+ is used for feedfoward compensation; tie it to input and don't leave it OPEN.
EN_PWR_CFP	Yes	There is an internal 1µs filter. Decoupling capacitor is NOT needed, but if needed, use a low time constant one to avoid too large a shutdown delay. It will also be the output of CFP function: 34Ω strong pull-up. 25 mils spacing from other traces.
RGND	Yes	Pair up (within 20 mils) with the positive rail remote sensing line that connected to FB resistor, and routing them to the load sensing points.
VSEN	Yes	Used for Overvoltage protection sensing and APA level sensing. Caution should be taken to avoid noise coupling into this pin.
FB	Yes	Pair up (within 20 mils) with the negative rail of remote sensing line that connected to RGND, and route them to the load sensing points. Reserve an RC from FB to GND to compensate the output lagging from DAC during DVID transitions.
HFCOMP	Yes	Connect an R to the VR output. The R value is typically equal or slightly higher (~150%) than the feedback resistor (droop resistor), fine tuned according to the high frequency transient performance. Place the compensation network in close proximity to the controller.

TABLE 25. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVE	DESCRIPTION
PSICOMP	Yes	The series impedance typically should be 2x-3x the impedance in type III compensation to reduce noise coupling. Place the compensation network in close proximity to the controller.
COMP	Yes	Place the compensation network in close proximity to the controller. Typically use a 68pF or higher across FB to COMP depending upon the noise coupling of the layout.
DVC	Yes	4/3 of DAC voltage. Place the compensation network in close proximity to the controller.
IMON	Yes	Refer to GND, not RGND. Place R and C in general proximity to the controller. The time constant of RC should be sufficient, typically <200µs for VR12.5 Server Core and 1-2ms for Desktop Core applications, as an averaging function for the digital I_{OUT} of VR.
SVDATA; SVCLK	Yes	*Very Critical!* Greater than 13MHz signals when the SVID bus is sending commands, pairing up with SVALERT# and routing carefully back to CPU socket. 20 mils spacing within SVDATA, SVALERT#, and SVCLK; and more than 30 mils to all other signals. Refer to the Intel individual platform design guidelines and place proper termination (pull-up) resistance for impedance matching. Local decoupling capacitor is needed for the pull-up rail. These signals travel from CPU to the ISL6381 and return to CPU through ISL6381's ground and power ground. Separation between IC ground and power ground with 0Ω resistor is NOT advised.
SVALERT#	No	Open drain and high dv/dt pin during transitions. Route it in the middle of SVDATA and SVCLK. Also see above.
VR_RDY	No	Open drain and high dv/dt pin. Avoid its pull-up higher than VCC. Tie it to ground when not used.
I2CLK, I2DATA	Yes	The 50kHz to 1.5MHz signal when the SMBus, PMBus, or I^2C is sending commands, pairing up and routing carefully back to SMBus, PMBus or I^2C. 20 mils spacing within I2DATA, and I2CLK; and more than 30 mils to all other signals. Refer to the SMBus, PMBus or I^2C design guidelines and place proper terminated (pull-up) resistance for impedance matching. Tie to VCC with 1MΩ when not used.

TABLE 25. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVE	DESCRIPTION
IMADR_BTRM VDBAND_PMADR_VRSEL TMX_DRP_DE_TCICL_SPDUPC_K	No	Register setting is locked prior to soft-start. Since the external resistor-divider ratio compares with the internal resistor ratio of the VCC, their rail should be exactly tied to the same point as VCC pin, not through an RC filter. DON'T use decoupling capacitors on these pins.
TM_EN_OTP	Yes	Place NTC in close proximity to the output inductor of VR's Channel 1 and to the output rail, not close to MOSFET side (see Figure 24); the return trace should be 25 mils away from other traces. Place 1kΩ pull-up and decoupling capacitor (typically 0.1µF) in close proximity to the controller. The pull-up resistor should be exactly tied to the same point as VCC pin, not through an RC filter. If not used, connect this pin to 1MΩ/2MΩ resistor divider, or tie it to VCC.
VR_HOT#	No	Open drain and high dv/dt pin during transitions. Avoid its pull-up rail higher than VCC. 30 mils spacing from other traces.
AUTO_NPSI	Yes	Program number of operational phases in PSI1 mode and AUTO phase shedding threshold via a pair of paralleling resistor and capacitor from this pin to GND. AUTO phase shedding is disabled when this pin tied to GND or VCC disable.
RSET	Yes	Place the R in close proximity to the controller. No long PCB trace should hang on this pin or no noise node should be close to this pin. DON'T use decoupling capacitor on this pin.
FS_FDVID	Yes	Place the R in close proximity to the controller. No long PCB trace should hang on this pin, or no noise node should be close to this pin. Don't use decoupling capacitor on this pin.
VCC	Yes	Place the decoupling capacitor in close proximity to the controller. Minimize R-drop to this pin.
PWM1-4	NO	Avoid the respective PWM routing across or under other phase's power trains/planes and current sensing network. Don't make them across or under external components of the controller. Keep them at least 20 mils away from any other traces.
ISEN[4:1]+	Yes	Connect to the output rail side of the respective channel's output inductor or resistor pin. Decoupling is optional and might be required for long sense traces and a poor layout.

TABLE 25. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVE	DESCRIPTION
ISEN[4:1]-	Yes	Connect to the phase node side of the respective channel's output inductor or resistor pin with L/DCR or ESL/R_{SEN} matching network in close proximity to the ISEN± pins of VR. Differentially routing back to the controller by paring with respective ISEN+; at least 20 mils spacing between pairs and away from other traces. Each pair should not cross or go under the other channel's switching nodes [Phase, UGATE, LGATE] and power planes even though they are not in the same layer
GND	Yes	This EPAD is the return of PWM output drivers and SVID bus. Use 4 or more vias to directly connect the EPAD to the power ground plane. Avoid using only single via or 0Ω resistor connection to the power ground plane.
General Comments		The layer next to the Top or Bottom layer is preferred to be ground layers, while the signal layers can be sandwiched in the ground layers if possible.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position the high-frequency ceramic input capacitors next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

To improve the chance of first pass success, it is very important to take time to follow the above outlined design guidelines and Intersil generated layout check list, see more details in "Voltage Regulator (VR) Design Materials" on page 50. Proper planning for the layout is as important as designing the circuits. Running things in a hurry, you could end up spending weeks and months to debug a poorly designed and improperly laid out board.

Powering Up And Open-Loop Test

The ISL6381 features very easy debugging and powering up. For first-time powering up, an open-loop test can be done by applying sufficient voltage (current limiting to 0.25A) to VCC, proper pull-up to SVID bus, and signal high to TM_EN_OTP (>1.08V) and EN_PWR_CFP (>0.9V and less than 3.3V) pins with the input voltage (VIN) disconnected.

1. Each PWM output should operate at maximum duty cycle and correct switching frequency.
2. The 0C-0F registers can be read via SVID bus or DC-DE and B0 registers via PMBus to check its proper setting.
3. If 5V drivers are used and share the same rail as VCC, the proper switching on UGATEs and LGATEs should be seen.
4. If 12V drivers are used and can be disconnected from VIN and sourced by an external 12V supply, the proper switching on UGATEs and LGATEs should be observed.
5. If the above is not properly operating, you should check soldering joint, resistor register setting, Power Train connection or damage, i.e, shorted gates, drain and source. Sometimes the gate might measure short due to residual gate charge. Therefore, a measured short gate with ohmmeter cannot validate if the MOSFET is damaged unless the Drain to Source is also measured short.
6. When rework is needed for the L/DCR matching network, use an Ωmeter across the C to see if the correct R value is measured before powering the VR up; otherwise, the current imbalance due to improper rework could damage the power trains.
7. After everything is checked, apply low input voltage (1-5V) with appropriate current limiting (~0.5A). All phases should be switching evenly.
8. Remove the pull-up from EN_PWR pin, using bench power supplies, power up VCC with current limiting (typically ~ 0.25A if 5V drivers included) and slowly increase Input Voltage with current limiting. For typical application, VCC limited to 0.25A, VIN limited to 0.5A should be safe for powering up with no load. High core-loss inductors likely need to increase the input current limiting. All phases should be switching evenly.

Voltage Regulator (VR) Design Materials

To support VR design and layout, Intersil also developed a set of worksheets and evaluation boards, as listed in Tables 26 and 25, respectively. The tolerance band calculation (TOB) worksheets for VR output regulation and IMON have been developed using the Root-Sum-Squared (RSS) method with 3 sigma distribution point of the related components and parameters. Note that the "Electrical Specifications" table beginning on page 9 specifies no less than 6 sigma distribution point, not suitable for RSS TOB calculation. Contact Intersil's local office or field support for the latest available information.

TABLE 26. AVAILABLE DESIGN ASSISTANCE MATERIALS

ITEM	DESCRIPTION
0	VR12.5 Design and Validation
1	VR12.5 Design Worksheet for Compensation and Component Selection
2	Transient Response Optimization Guidelines
3	VOUT and IMON TOB Calculator
4	SVID and SMBus/PMBus/I^2C Communication Tool with Software
5	Resistor Register Calculator
6	Dynamic VID Compensation Calculator
7	Layout Design Guidelines
8	TCOMP and TM Selection Worksheet
9	Fine Tune OCP and Droop Worksheet
10	Evaluation Board Schematics in OrCAD Format and Layout in Allegro Format

NOTE: For worksheets, please contact Intersil Application support at www.intersil.com/design/.

TABLE 27. AVAILABLE EVALUATION BOARDS

EVALUATION BOARDS	PIN-TO-PIN	PACKAGE	SOCKET	TARGETED APPLICATIONS	SMBus/ PMBus/I^2C	PEAK EFFICIENCY	ICCMAX (A)
ISL6381EVAL1	ISL6373	5x5 40Ld	DDR4	VR12/VR12.5 Memory with Discrete Drivers and Dual MOSFETs (Configured to 2-Phase for Memory)	Yes	93%, 1.2V at 40A	60A
ISL6388EVAL1		5x5 40Ld	R3	VR12.5 High-End Desktop and Server with DrMOS (Digital, 6-Phase Core)	Yes	94%, 1.8V at 50A	215A
ISL6388EVAL3		5x5 40Ld	R3	VR12.5 High-End Desktop and Server with Discrete Drivers and MOSFETs (Digital, 6-Phase Core)	Yes	94%, 1.8V at 50A	215A
ISL6388EVAL5		5x5 40Ld	R3	VR12.5 Server and Memory with Discrete Drivers and Dual MOSFETs (All Digital, 6-Phase Core, 2x DDR3)	Yes	94%, 1.8V at 50A	215A
			2x DDR3		Yes	93%, 1.2V at 40A	60A
ISL6376EVAL1		6x6 48Ld	R3	VR12.5 High-End Desktop and Server with Discrete Drivers and MOSFETs	Yes	94%, 1.8V at 50A	215A
ISL6376EVAL2		6x6 48Ld	R3	VR12.5 High-End Desktop and Server with DrMOS	Yes	95%, 1.8V at 50A	215A
ISL6374EVAL1	ISL6375/73	5x5 40Ld	H3	VR12.5 Desktop/Server with Dual PowerPak and DPAK Footprint	No	89%, 1.8V at 40A	120A
ISL6373EVAL1	ISL6374/75	5x5 40Ld	DDR4	VR12/VR12.5 Memory with Discrete Drivers and Dual MOSFETs (Configured to 2-Phase for Memory)	Yes	93%, 1.2V at 40A	74A
ISL6373EVAL2	ISL6374/75	5x5 40Ld	DDR4	VR12/VR12.5 Memory with DrMOS (Configured to 2-Phase for Memory)	Yes	93%, 1.2V at 40A	60A
ISL6367_67HEVAL1		7x7 60Ld	R	VR12/VR12.5 High-End Desktop and Server with Discrete Drivers and MOSFETs	Yes	94%, 1.8V at 50A 93%, 1.2V at 50A	220A +25A
ISL6367_67HEVAL2		7x7 60Ld	R1	VR12/VR12.5 High-End Desktop and Server with DrMOS	Yes	95%, 1.8V at 50A 93%,1.2V at 50A	220A +25A
ISL6364AEVAL1		6x6 48Ld	H1	VR12 Desktop/Server (Vcore or Memory)	No	88%, 1.2V at 50A	120A +35A
ISL6363EVAL1		7x7 60Ld	H1	Desktop/Memory	No	88%, 1.2V at 50A	120A +35A
ISL6353EVAL1		5x5 40Ld	DDR3	Memory	No	94%, 1.5V at 25A	100A

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 12, 2014	FN8576.1	Page 4 : Updated label for pin 17 from “SM_PM_I2DA” to “SM_PM_I2DATA” to match the Functional Pin Decription. Page 4 : Remove Industrial Version (IRTZ) Page 9 : Remove Industrial Version (IRTZ) for DAC specs and Temperature Page 9 : Nominal Supply Min value - Change from 19 to 18.
March 28, 2014	FN8576.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

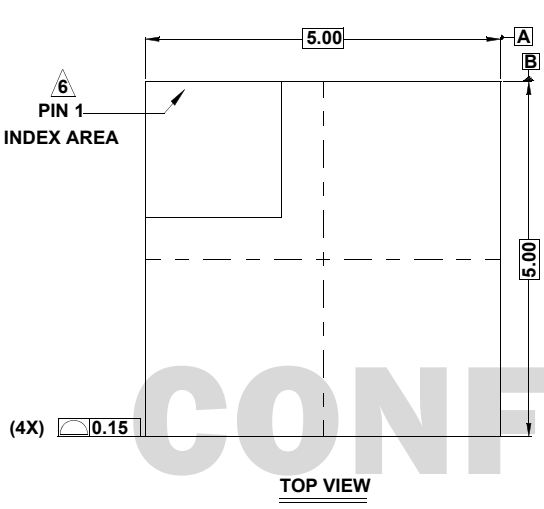
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

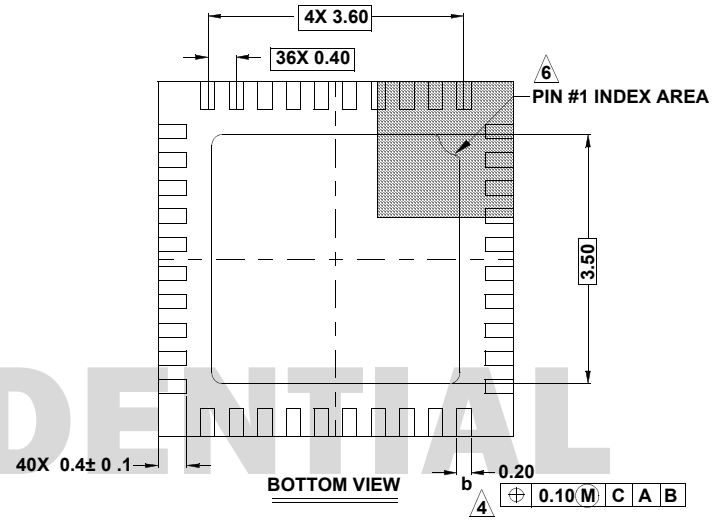
Package Outline Drawing

L40.5x5

40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 9/10

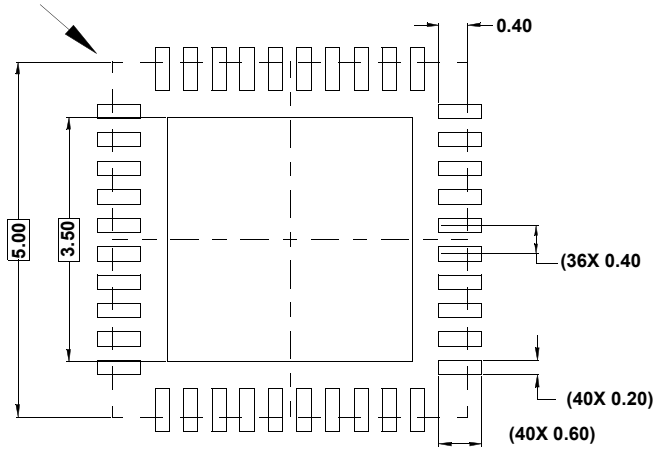


TOP VIEW

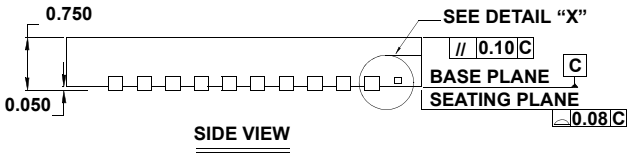


BOTTOM VIEW

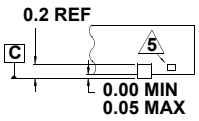
PACKAGE OUTLINE



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1