DP83924B

DP83924B Quad 10 Mb/s Ethernet Physical Layer - 4TPHY

Literature Number: SNLS033A

National Semiconductor

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DP83924BVCE
Quad 10 Mb/s Ethernet Physical Layer - 4TPHY™

General Description

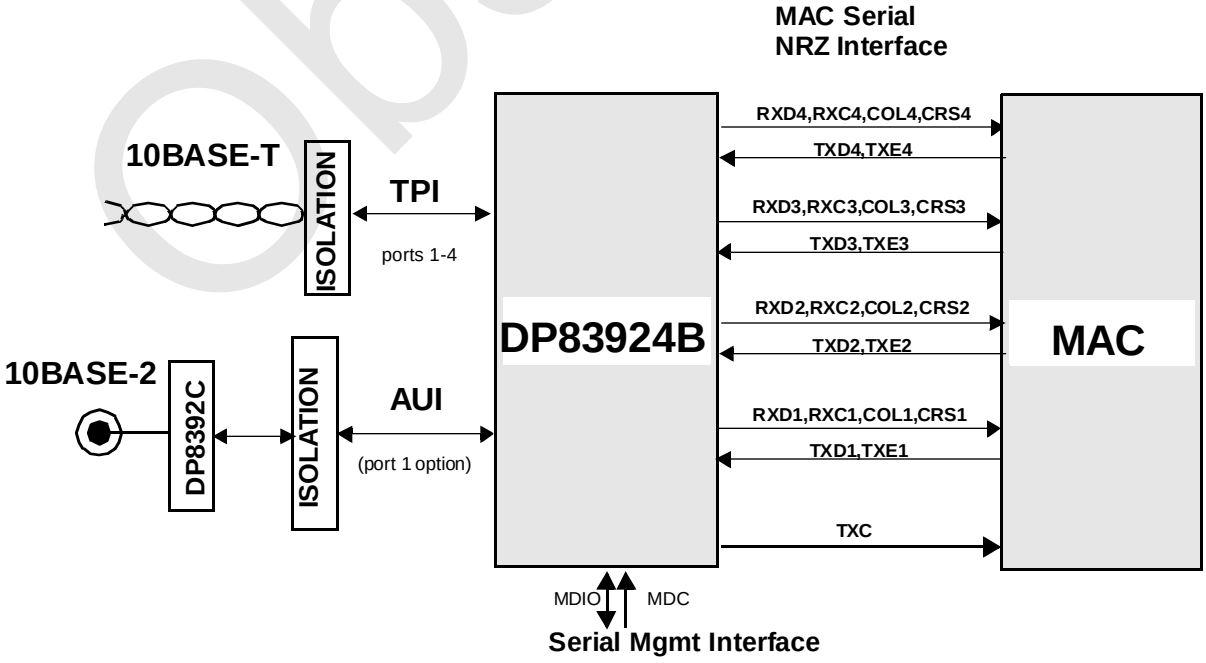
The DP83924B Quad 10Mbps Ethernet Physical Layer (4TPHY) is a 4-Port Twisted Pair PHYsical Layer Transceiver that includes all the circuitry required to interface four Ethernet Media Access Controllers (MACs) to 10BASE-T. This device is ideally suited for switch hub applications where 8 to 32 ports are commonly used.

The 4TPHY has three dedicated 10Base-T ports. There is an additional port that is selectable for either 10Base-T or for an Attachment Unit Interface (AUI). In 10Base-T mode, any port can be configured to be Half or Full Duplex. (Continued)

Features

- 100 pin package
- 10BASE-T and AUI interfaces
- Automatic or manual selection of twisted pair or Attachment Unit Interfaces on port 1
- Direct Interface to NRZ Compatible controllers
- IEEE 802.3u Auto-Negotiation between 10Mb/s Full and Half Duplex data traffic and parallel detection
- MII-like Serial management interface for configuration and monitoring of ENDEC/Transceiver operation.
- Programmable MAC Interface supports most standard 7 signal MAC interfaces
- Twisted Pair Transceiver Module
  - On-chip filters for transmit outputs
  - Low Power Driver
  - Heartbeat and Jabber Timers
  - Link Disable and Smart Receive Squelch
  - Polarity detection and correction
  - Jabber Enable/Disable
  - Isolate mode for diagnostics
  - Low Power Class AB Attachment Unit Interface (AUI) Driver for one port
  - Enhanced Supply Rejection
  - Enhanced Jitter Performance
  - Diagnostic Endec Loopback
  - Squelch on Collision and Receive Pair
- Serial LED interface for LINK, POLARITY, ACTIVITY, and ERROR.
- JTAG Boundary Scan per IEEE 1149.1

System Diagram



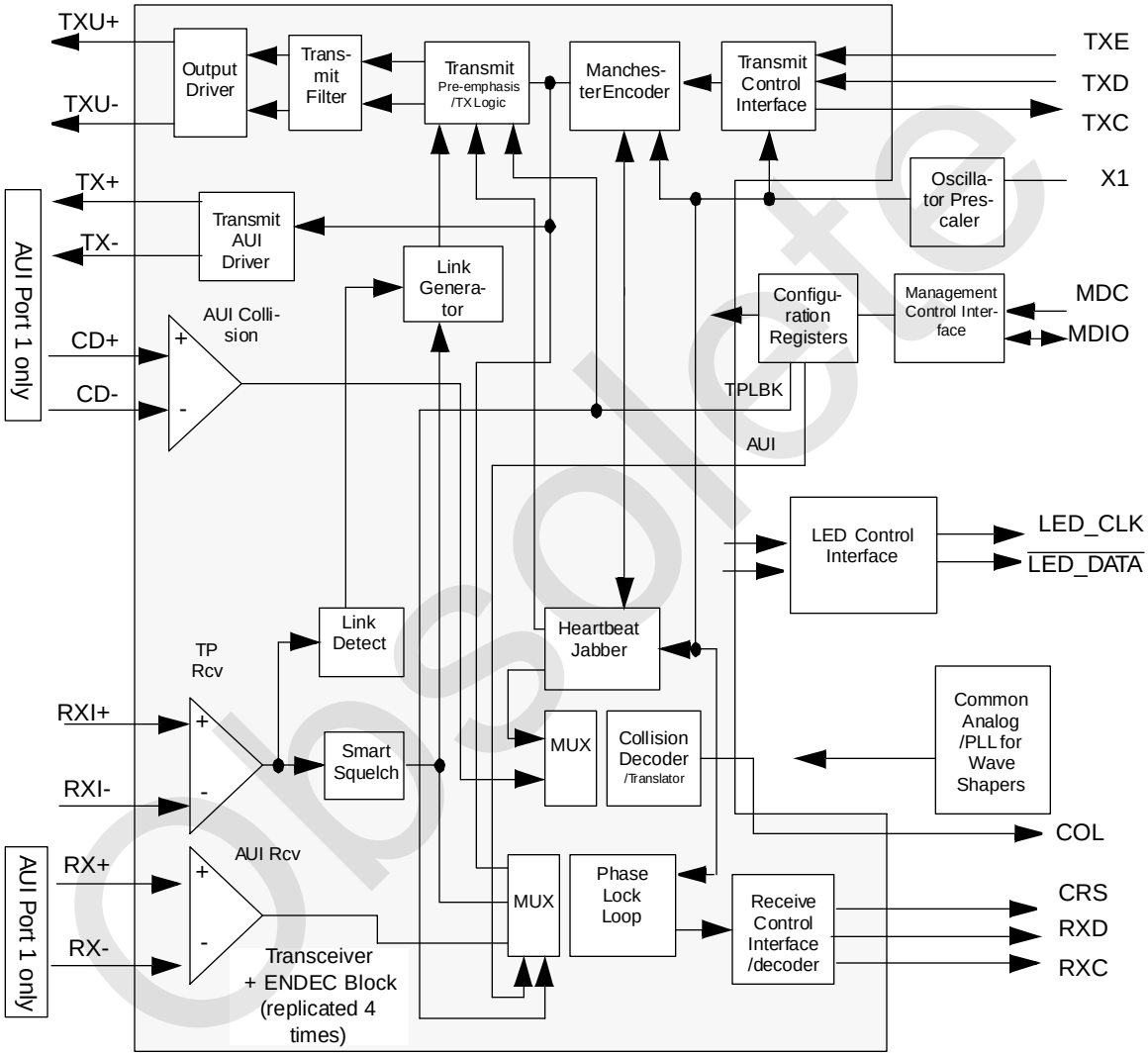
General Description (Continued)

The various modes on the 4TPHY can be configured and controlled via the MII management interface. This management interface makes inter-operability with other manufacturers MAC units relatively easy. If no management interface is desired, most of the critical operating modes of the transceiver can be set via strapping options (latching configuration information during reset). The ENDEC section of the transceiver also supplies a simple Non-Return-to-Zero (NRZ) interface to transmit and receive data to/from standard 10 Mb/s MACs.

The transceivers include on-chip filtered transmit outputs, which reduce emissions and eliminate the need for external filter.

The DP83924BVCE maintains complete hardware and software backwards compatibility with the DP83924AVCE with only a change to one resistor value and disconnecting a second resistor.

Block Diagram



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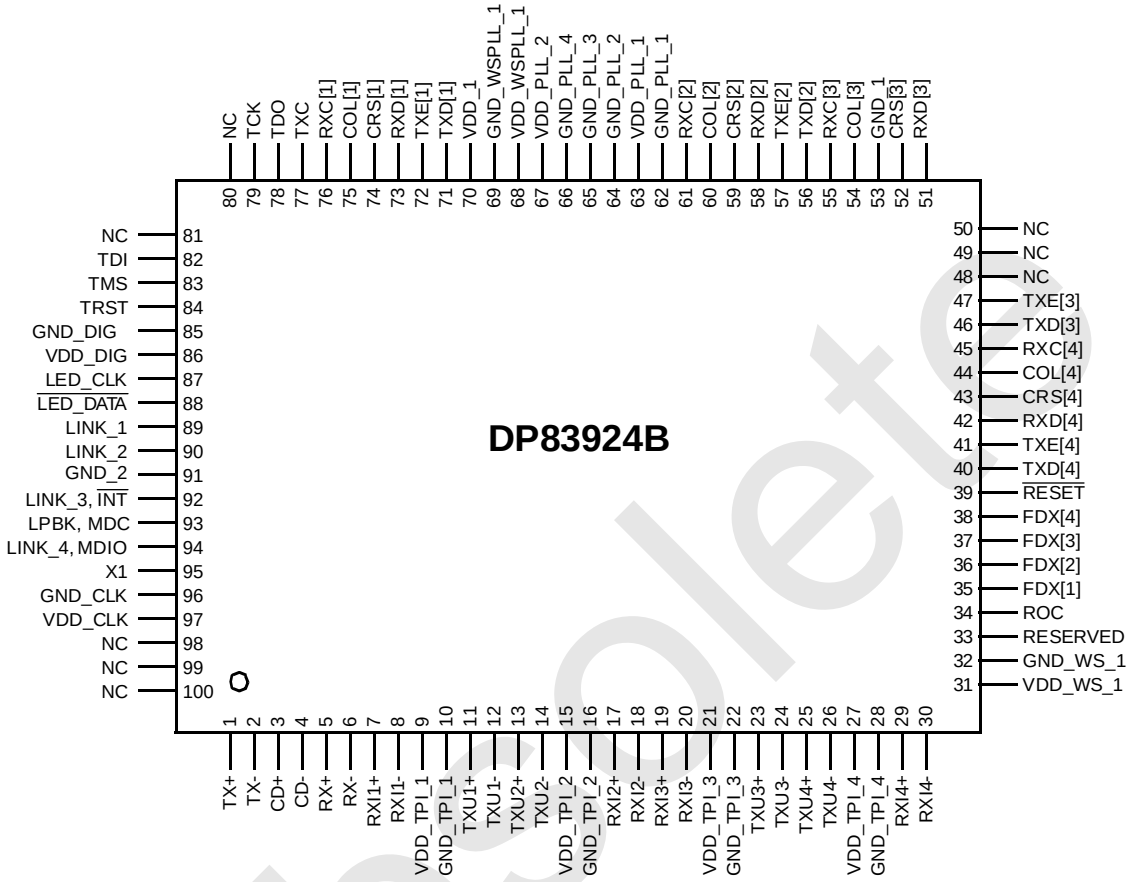
1.0 Pin Information

1.1 Pin Connection Diagram



Order Number DP83924BVCE
NS Package Number VCE100A

Figure 1. 100-Pin Plastic Quad Flat Pack (PQFP) Pinout

1.0 Pin Information (Continued)

1.2 Pin Description

Table 1. NRZ CONTROLLER INTERFACE and MANAGEMENT INTERFACE.

These pins provide the interface signalling between the Media Access Controller and the transceiver. (30 Pins)

Symbol	Pin #	Type	Description
TXC	77	O	**Transmit Clock:** This pin outputs a 10 MHz output clock signal synchronized to the transmit data (for all ports).
TXD[4] TXD[3] TXD[2] TXD[1]	40 46 56 71	I	**Transmit Data:** The serial TXD contains the transmit serial data output stream.
TXE[4] TXE[3] TXE[2] TXE[1]	41 47 57 72	I	**Transmit Enable:** This active high input indicates the presence of valid data on the TXD pins.
CRS[4] CRS[3] CRS[2] CRS[1]	43 52 59 74	O, pull-up O, pull-up O, pull-up O, pull-up	**Carrier Sense:** Active high output indicates that valid data has been detected on the receive inputs. CRS[3:1] are dual purpose pins. When $\overline{\text{RESET}}$ is active, the value on these pins are sampled to determine the transceiver address for the mgmt interface. These pins have internal pull-ups, a 2.7 kΩ pull down resistor is required to program a logic '0'.
COL[4] COL[3] COL[2] COL[1]	44 54 60 75	O, pull-up O, pull-up O, pull-up O, pull-up	**Collision:** This active high output is asserted when a collision condition has been detected. It is also asserted for 1µs at the end of a packet to indicate the SQE test function. COL[4:1] are dual purpose pins. When $\overline{\text{RESET}}$ is active, these pins are sampled and selects the operating mode for the device. These pins have internal pull-ups to select the default mode if no external pull-downs are connected. To select the non-default mode(s), a 2.7 kΩ pull down resistor(s) is required. The strappable functions are: COL[4]; selects the number of receive clocks after carrier sense deassertion (5 RXCs or continuous RXCs). Default is 5 RXCs. COL[3]; enables or disables the receive filter. Default is to disable the receive filter. COL[2]; Disables Management Interface and selects the Full Duplex operating mode (normal or enhanced). Default is normal full duplex mode. If the enhanced Full- Duplex mode is selected, the functions of pins 89, 90, 92, 93, and 94 are also changed. See the descriptions in Sectio n3.3.13 and Se ction3.3.14. COL[1]; selects the LED operating mode (normal or enhanced). Default is normal LED mode.
RXC[4] RXC[3] RXC[2] RXC[1]	45 55 61 76	O	**Receive Clock:** This 10 MHz signal is generated by the transceiver, and is the recovered clock from the decoded network data stream. This signal is 10 MHz. The number of RXCs after the deassertion of CRS is programmable via the Global Configuration Register, GATERXC bit, D0. The options are for 5 RXCs or continuous RXCs.
RXD[4] RXD[3] RXD[2] RXD[1]	42 51 58 73	O, Pull-up	**Receive Data:** Provides the decoded receive serial data. Data is valid on the risin edge of RXC. RXD[4:1] are dual purpose pins. When $\overline{\text{RESET}}$ is active, these pins are sampled and selects the operating mode for the device. These pins have internal pull-ups to select the default mode if no external pull-downs are connected. To select the non-default mode(s), a 2.7 kΩ pull down resistor(s) is required. The strappable functions are: RXD[4] enables/disables Auto-Negotiation. RXD[3:1] selects one of five MAC interface modes. See the table in the Interface Descriptions section.
MDC LPBK	93	I	**Management Data Clock:** When management interface is enabled (strap option, COL[2]=1), this clock signal (0-2.5MHz) is the clock for transferring data across the management interface. **LoopBack**: When "Disable Management Interface" mode is selected (strap option, COL[2]=0), then this pin is an active high input to configure all ports into diagnostic loopback mode.

1.0 Pin Information (Continued)

Table 1. NRZ CONTROLLER INTERFACE and MANAGEMENT INTERFACE.
These pins provide the interface signalling between the Media Access Controller and the transceiver. (30 Pins)

Symbol	Pin #	Type	Description
MDIO LINK_4	94	I/O	**Management Data I/O:** When management interface is enabled (strap option, COL[2]=1), this Bidirectional signal transfers data on the management interface between the controller and the transceiver. **Link Lost Status Port 4**: When "Disable Management Interface" mode is selected, (strap option, COL[2]=0), this pin outputs the link lost status for port 4. If link is lost, this output is high.
$\overline{\text{INT}}$ LINK_3	92	OD	**Interrupt:** When "Enable Management Interface" mode is selected (strap option, COL[2]=1), this output pin is driven low when an interrupt condition is detected within the Quad Transceiver. An interrupt can occur when link status changes or during jabber condition. This is an open-drain output. And requires an external pull-up resistor. **Link Lost Status Port 3**: When "Disable Management Interface" mode is selected, (strap option, COL[2]=0), this pin outputs the link lost status for port 3. If link is lost, this output is high.
LINK_2 LINK_1	90 89	O, pull-up O, pull-up	**Link Lost Status Ports 1,2**: These pins indicate the link lost status for ports 1 and 2. (During both management interface disable and enable modes) LINK_1 is also the strap option for RXD levels during idle . See Table7 on page11. A 2.7 kΩ pulldown resistor is needed to set RXD_IDLE = High. Default is LINK_1='1' and RXD_IDLE= Low

Table 2. NETWORK INTERFACES: Attachment Unit, Twisted Pair Interface (24 Pins)

Symbol	Pins	Type	Description
RXI4+ RXI4-	29 30	I	**Twisted Pair Receive Input:** This differential input pair receives the incoming data from the twisted pair medium via an isolation transformer.
RXI3+ RXI3-	19 20		
RXI2+ RXI2-	17 18		
RXI1+ RXI1-	7 8		
TXU4+ TXU4-	25 26	O	**UTP Transmit Outputs:** This pair of drivers provide pre-emphasized and filtered differential output for UTP (100 ohm cable). These drivers maintain the same common mode voltage during data transmission and idle mode.
TXU3+ TXU3-	23 24		
TXU2+ TXU2-	13 14		
TXU1+ TXU1-	11 12		
Reserved	33	I	**Reserved:** This pin must be left unconnected.
ROC	34	I	**On Chip Reference:** An external resistor connects to ground for an on chip reference. The resistor must be a precision (1%) resistor, the value of which should be determined by each user to center VOD around 5 Vpp.
Attachment Unit Interface			
RX+ RX-	5 6	I	**Port 1 Full AUI Receive Input:** In AUI mode this differential input pair receives the incoming data from the AUI medium via an isolation transformer.
TX+ TX-	1 2	O	**Port 1 Full AUI Transmit Output:** In AUI mode this differential pair sends encoded data from the AUI transceiver. These outputs are source followers and require 270 Ohm pull down resistors.
CD+ CD-	34	I	**Port 1 Full AUI Collision Detect**: In AUI mode, this differential input pair receives the collision detect signals from the AUI medium via an isolation transformer.

1.0 Pin Information (Continued)

Table 3. LED & GENERAL CONFIGURATION Pins (8 Pins)

Symbol	Pins	Type	Description
$\overline{\text{LED\_DATA}}$	88	O	**LED serial data output:** This pin outputs the serial LED data. See S ection2.3 for a description of the LED modes. This output should be connected to the input of the 1st (external) serial shift register.
LED_CLK	87	O	**LED Clock:** This is the clock for the serial shift registers
X1	95	I	**External Oscillator Input:** This signal is used to provide clocking signals for the internal ENDEC. A 20MHz oscillator module should be used to drive this pin.
$\overline{\text{RESET}}$	39	I	**Reset:** Active low input resets the transceiver, and starts the initialization of the device. This pin has a noise filter on it's input, which requires that the reset pulse must be greater than 30 X1 clocks.
$\overline{\text{FDX[4:1]}}$	38 -35	I	**Full Duplex:** These pins are sampled during reset. They control the full duplex (or half duplex) configuration of each port. If pulled low, Full Duplex operation is selected for the respective port. If pulled high, Half Duplex operation is selected. These pins have no internal pull-up or pull-down resistors.These pins are also used in "Enhanced full duplex" mode to dynamically select Full/Half duplex mode of operat i on. See Section3.3.14

Table 4. SCAN TEST Pins (5 Pins)

Symbol	Pins	Type	Description
TCK	79	I	**Test Clock:** This signal is used during boundary scan to clock data in and out of the device.
TDI	82	I	**Test Input:** The signal contains serial data that is shifted into the device by the TAP controller. An internal pullup is provided if not used. It is recommended that during normal transceiver operation a '1' should be applied to this pin.
TDO	78	O,Z	**Test Output:** The tristateable signal contains serial data that is shifted out of the device by the TAP controller.
TMS	83	I	**Test Mode Select:** This selects the operation mode of the TAP controller. An internal pullup is provided if not used
$\overline{\text{TRST}}$	84	I	**Test Reset:** When this signal is asserted low it forces the TAP (Test Access Port) controller into a logic reset state. An internal pullup is provided. This pin should be pulled low during normal transceiver operation.

1.0 Pin Information (Continued)

Table 5. POWER AND GROUND Pins (33 Pins)

Symbol	Pins	Type	Description
NC NC NC NC NC	48 49 50 80 81 98 99 100	NA	No Connect;
VDD_TPI_4 VDD_TPI_3 VDD_TPI_2 VDD_TPI_1	27 21 15 9	P	Power for TPI Ports 1-4;
GND_TPI_4 GND_TPI_3 GND_TPI_2 GND_TPI_1	28 22 16 10	G	Ground for TPI Ports 1-4;
VDD_PLL_2 VDD_PLL_1	67 63	P	Power for PLL Circuitry; (Digital PLL)
GND_PLL_4 GND_PLL_3 GND_PLL_2 GND_PLL_1	66 65 64 62	G	Ground for PLL Circuitry; (Digital PLL)
VDD_WSPLL_1	68	P	Power for Wave Shaper and PLL Circuitry; (Analog PLL)
GND_WSPLL_1	69	G	Ground for Wave Shaper and PLL Circuitry;
VDD_WS_1	31	P	Power for Wave Shaper Circuitry
GND_WS_1	32	G	Ground for Wave Shaper Circuitry
VDD_DIG	86	P	Power for Core Logic;
GND_DIG	85	G	Ground for Core Logic;
GND_CLK	96	G	Ground for Clock Circuitry;
VDD_CLK	97	P	Power for Clock Circuitry;
GND_2 GND_1	91 53	G	Ground for NRZ Circuitry;
VDD_1	70	P	Power for NRZ Circuitry;

Table 6. Pin Type Description

Pin Type	Description
I	Input Buffer
O	Output Buffer (driven at all times)
I/O	Bi-directional Buffer.
O, Z	Output Buffer with High Impedance Capability
OD	Open Drain-Like Output. Either driven Low or to a High Impedance State.

2.0 Interface Descriptions

Interface Overview

The 4TPHY's interfaces can be categorized into the following groups of signals:

1. Management Interface - Allows host to read status and set operating modes
2. Media Access Control Interface - Straight forward NRZ interface to Ethernet MACs
3. LED Interface - Serial LED interface to off chip shift registers
4. Network Interfaces - Integrated 10BASE-T and AUI.
5. Clock - Allows connection of an external clock module.

2.1 Management Interface

This interface is a simple serial interface that is modeled after the MII standard serial interface, though it does not adhere to the MII standard completely (the protocol is followed, but the register space is not). The interface signals consist of a clock and data line for transfer of data to and from the registers.

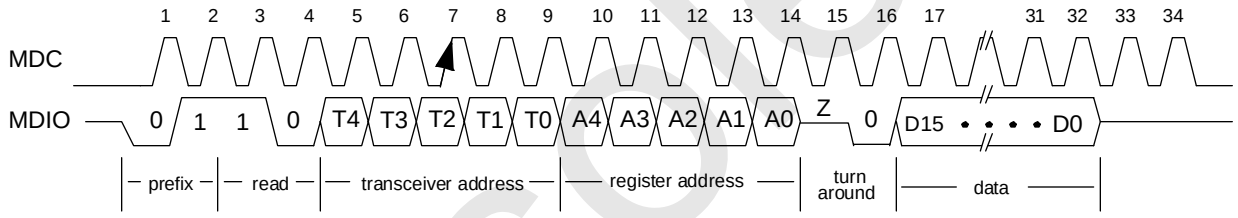
In a multiple 4TPHY system, it is necessary to distinguish between the devices in order to access the correct registers for configuration and status information. This is accomplished by assigning each 4TPHY a unique transceiver address. The lower 3 bits of the transceiver address, T[2:0], is latched in during reset based on the logic state of CRS[3:1]. The upper 2 bits of the transceiver address, T[4:3], must be zero. Therefore, 32 ports can be supported with a single MII bus.

The register address field indicates which register within the 4TPHY that is to be accessed (read or write).

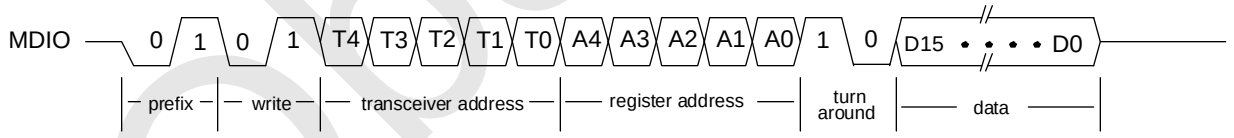
During a write operation, all 32 bits are driven onto MDIO by the host, indicating which transceiver and register the data is to be written.

During a read operation, the first 14 bits are driven onto MDIO by the host, then the bus is released, allowing the 4TPHY to drive the requested data onto MDIO.

The serial lines do not require any preamble on these pins, however if it is provided it is ignored so long as the 0110 or 0101 pattern is not present. If a continuous MDC is not supplied, then at the end of each command (read or write), 2 additional MDCs are required in order to allow the internal state machine to transition back to it's idle state. Refer to Figur e2.



Register Read



Register Write

Note 1: The management interface addressing includes a 5 bit field for the Transceiver Address, T[4:0], and a 5 bit field for the register address, A[4:0]. The MII assumes the transceiver address applies to a single port, but in this implementation a single address refers to a single IC. The transceiver address is set by 3 external pins, CRS[3:1]. T[4:3] must be zero to address the transceiver. Thus up to 32 10BASE-T ports can be addressed from a single interface (8 addr x 4 ports/addr).

Note 2: Two MDCs (clocks 33, 34) are required after each read or write in order to allow the internal state machine to transition back t o it's IDLE state.

Figure 2. Serial Management Interface Time Diagram (read/write)

2.2 MAC Interface

This interface connects the ENDEC/Transceiver to an Ethernet MAC controller. This interface consists of a serial data transmit interface and a serial receive interface. The interface clocks data out (on receive) or in (on transmit) on the rising edge of the clock. Refer t o Figure3. Most standard 10Mb/s controllers use this interface but they may differ in the polarity of the signals or on what edge of TXCs/RXCs that data is clocked in. In the default mode (NSC/TI mode), all signals are active high with rising edge sampling.

The 4TPHY utilizes a programmable MAC digital interface which enables it to directly interface to standard controllers from National Semiconductor, TI, AMD, Seeq, Fujitsu, and Intel. The compatibility modes are selected either by software via the Global Control/Status Register or by hardware strap options on pins RXD[3:1]. See Table 7 below.

2.0 Interface Descriptions (Continued)

In addition to the compatibility mode options, the recovered clock (RXC) is selectable for 5 RXCs after the deassertion of carrier sense (CRS) or for continuous RXCs after the deassertion of CRS. This is programmable through the serial MII or through the COL[4] strapping option only when the device is in the NSC mode.

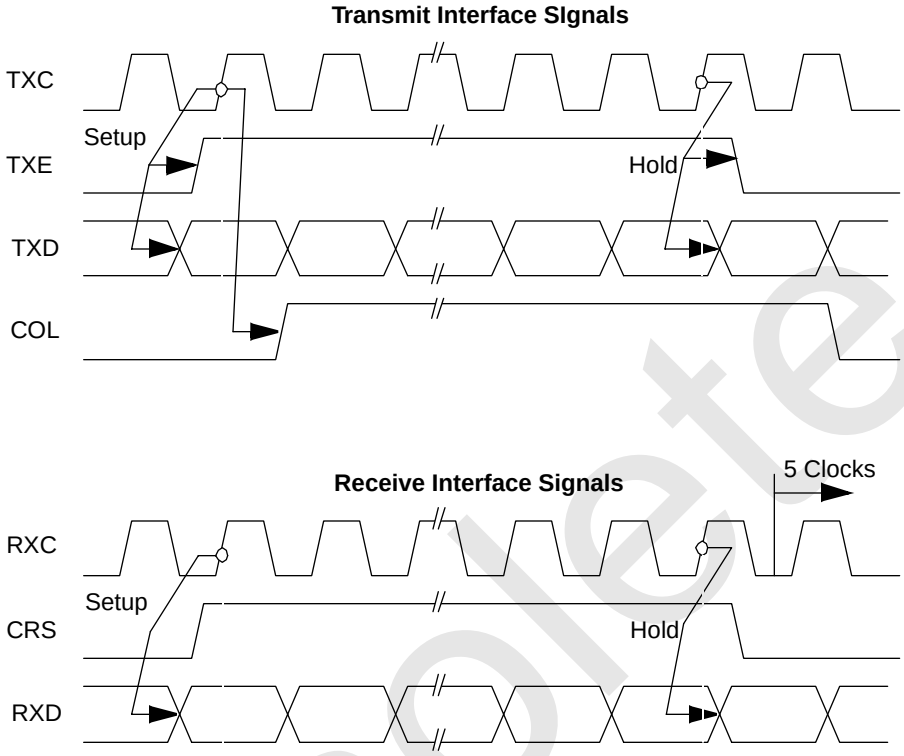


Figure 3. NRZ Interface Timing Diagram (NSC mode)

2.3 LED Interface

The LED interface consists of two modes. The first option, normal LED mode, requires an external 8-bit shift register. During every LED update cycle, 8-bits are shifted out to the external shift registers. This allows two LEDs per port. One LED indicates activity (TX or RX) and the second indicates port status (per Table 8). The status LEDs will blink at different rates depending on the associated ports status.If a port experiences both Bad Polarity and Link Lost, then the LEDs will go to the fast blink state (i.e. Link Lost). Port activity and status are shifted out port 1 first. The LED update rate is every 50ms. The LED clock rate is 1MHz. All port activity is extended to 50ms to make it visible. Data is valid on the rising edge of LED_CLK and is active low. Refer to Figur e4

The second option, enhanced LED mode, serially shifts a 16-bit stream out of the 4TPHY. This option outputs per port data for RX, TX, Full Duplex (FDX), and LinkCoded status. These four bits per port can be used to support two LEDs. One is a bi-color LED (decode of the FDX and LinkCoded bits) to indicate LINK status and duplex status as shown in Table 9. The second LED indicates activity (TX or RX). As with the first LED option, port 1 status is shifted out first and the data is active low. Refer to F igure5 for the timing sequence

To select the desired LED mode, the COL [1] pin has a strapping feature. If COL[1] is a logic '0' during reset, then "enhanced" LED mode is enabled. If COL[1] is a logic '1' during reset, then "normal" LED mode is enabled

(Application note:) During the update cycle data coming out of the shift register is not going to be valid until the cycle is completed and all the bits are shifted in place. These outputs should not be used to directly control a MAC unless the shift register outputs are latched during the update cycle. See Section 5.3 o n page28.

2.4 Network Interface

2.4.1 Twisted Pair Interface

The Quad 10Mb/s Transceiver provides two buffered and filtered 10Base-T transmit outputs (for each port) that are connected to the output isolation transformer via two impedance matching resistor/capacitor networks. See Figur e6. The twisted pair receiver implements an intelligent receive squelch on the RXI+ differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. This smart squelch circuitry (which is described in detail under the Functional Description) employs a combination of amplitude and timing measurements to determine the validity of data on the twisted pair inputs. Only after these conditions have been satisfied will Carrier Sense (CRS) be generated to indicate that valid data is present.

2.4.2 Attachment Unit Interface

A single port (port 1) on the transceiver has a separate (non- multiplexed) AUI interface. This interface is a full 802.3 standard AUI interface capable of driving the full 50m cable. The schematic for connecting this interface to the AUI connector is shown in Fi gure7.

2.0 Interface Descriptions (Continued)

Table 7. MAC Interface Selection

Parameter	Mode 1	Mode 2	Mode 3	Mode 4
RXCs Active	CRS + 5 clks	CRS asserted[a]	Continuous	Continuous
Edge of TXc that TXD is sampled	Rising	Rising	Falling	Falling
Polarity of active TXE	High	High	High	High
Edge of RXC that RXD is clocked	Rising	Rising	Rising	Falling
Polarity of CRS asserted	High	High	High	High
Level of RXD during CRS deassertion	Low	High	Low	Low
Polarity of active COL	High	High	High	Low
Polarity of active Loopback (LPBK)	High	High	Low	High
How to select MAC interface mode[b]				
Using registers to select mode				
Global Control & Status Register (GCSR, addr 08H) bits D[8:6]	111	001	010	011
GCSR bit D[4] (select RXD_Idle level)	0	1	0	0
GCSR bit D[0] (select RXC mode[c])	1	1	0	0
Using strap options to select mode				
RXD[3:1] strap option (same as GCSR D[8:6])	111	001	010	011
LINK[1] strap option (RXD idle level)	1	0	1	1
COL[4] strap option (RXC mode)	1	1	0	0

a. No extra clocks are added after CRS. (CRS + 0 clocks RXC mode)
b. The mode can be selected by either strap options or writing to the registers. The default for both is NSC,TI.
c. GCSR D[0] or COL[4] strap can't be used to select CRS + 0 clocks RXC mode. This mode is selected by the GCSR bits D[8:6] or RXD[3:1] strap option.

Table 8. Normal LED Mode

LED Condition	Status Indication
Off	Good Status
On - Solid	Error Status[a]
Fast Blink (400 ms)	Link Lost
Slow Blink (1600 ms)	Bad Polarity

a. Bit 7 of registers 00-03 can be set by the user /management entity based on any criteria they choose and will be used to turn on Error Status LED.

Table 9. Enhanced LED Mode - Bit Decode

FDX	LinkCoded	LED Status	Comments
0	0	OFF	Link Fail, Full Duplex
0	1	ON - Color A	Good Link, Full Duplex
1	0	ON - Color B	Good Link, Half Duplex
1	1	OFF	Link Fail, Half Duplex

If the standard 78 ohm transceiver cable is used, the receive differential input must be externally terminated with two 39 ohm resistors connected in series. In thin Ethernet applications, these resistors are optional. To prevent noise from falsely triggering the decoder, a squelch circuit at the input rejects signals with levels less than ± 160mV. Signals with levels greater than ± 300 mV are decoded.

If the AUI interface is not used, the unused AUI inputs can be left floating or the +/- inputs could be shorted to each other and the unused AUI outputs should be left floating.

2.4.3 Oscillator Clock

When using an oscillator, additional output drive may be necessary if the oscillator must also drive other components. The X1 pin is a simple TTL compatible input. See Figur e8.

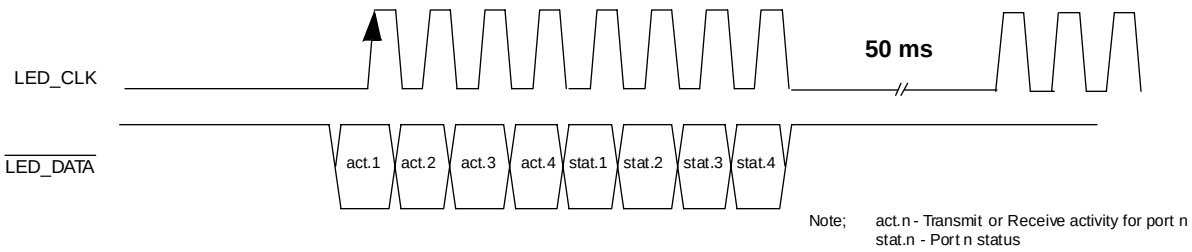


Figure 4. Normal LED Mode Timing Diagram

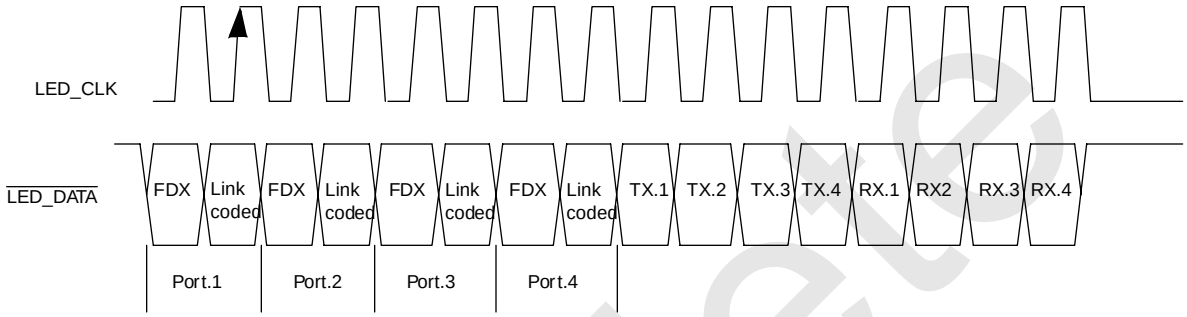


Figure 5. Enhanced Mode LED Timing Diagram

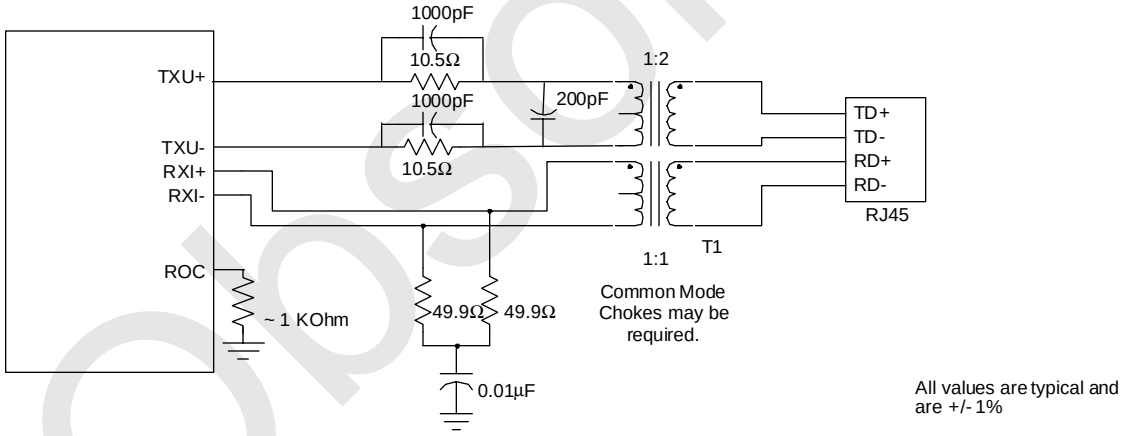


Figure 6. Twisted Pair Interface Schematic Diagram

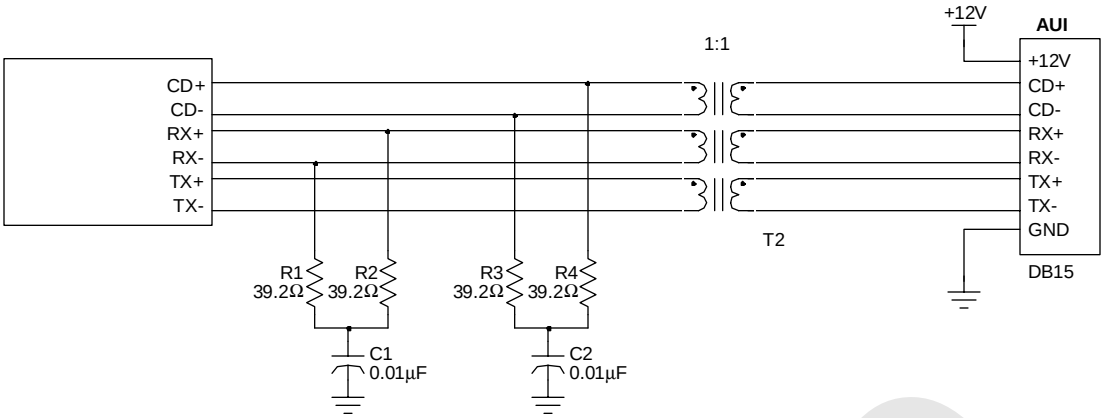


Figure 7. AUI Interface Schematics.

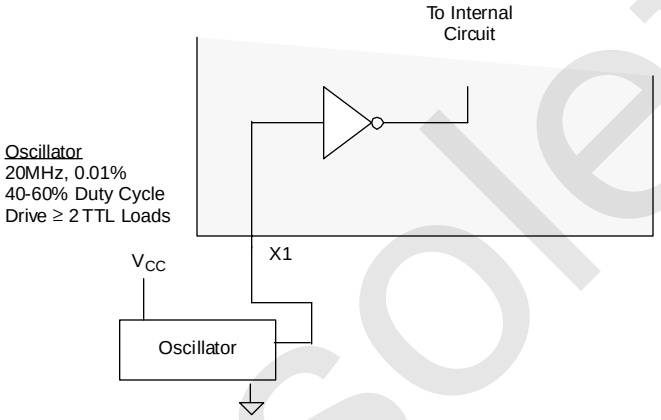


Figure 8. External Oscillator Connection Diagram

3.0 Detailed Functional Description

This product utilizes the standard 10BASE-T and AUI interface core building blocks which are replicated on this device, one per port. The basic function of these blocks are described in the following sections. Also described are the common digital blocks. Refer to “Block Diagra m” on page2.

3.1 Twisted Pair Functional Description

3.1.1 Smart Squelch

The Smart Squelch is responsible for determining when valid data is present on the differential receive inputs (RXI±). The Twisted Pair Transceiver (TPT) implements an intelligent receive squelch on the RXI ± differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal.

The squelch circuitry employs a combination of amplitude and timing measurements to determine the validity of data on the twisted pair inputs. The operation of the smart squelch is shown in Fi gure9.

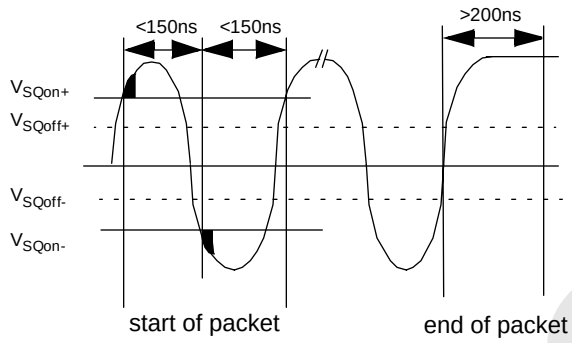


Figure 9. Twisted Pair Squelch Operation Diagram

The signal at the start of packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected. The checking procedure results in the loss of typically three bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart squelch circuitry is reset.

Valid data is considered to be present until squelch level has not been generated for a time longer than 150ns, indicating End of Packet. Once good data has been detected the squelch levels are reduced to minimize the effect of noise causing premature End of Packet detection.

3.1.2 Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity once valid data is detected via the Smart squelch function.

For 10 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mb/s Full Duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

3.1.3 Collision Detect and Heartbeat

A collision is detected on the twisted pair cable when the receive and transmit channels are active simultaneously. If the ENDEC is receiving when a collision is detected (AUI only) it is reported to the MAC block immediately (through the COL signal). If, however, the ENDEC is transmitting when a collision is detected the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The COL signal remains for the duration of the collision.

Approximately 1 µusec after the transmission of each packet a signal called the Signal Quality Error (SQE) consisting of typically 10 cycles of a 10MHz signal is generated by a10 Mbps transceiver. This 10MHz signal, also called the Heartbeat, assures the continued functioning of the collision circuitry. The transceiver attached to the AUI port will send this signal to the 4TPHY through the CD pins. 4TPHY will respond by sending a pulse on the COL line to the MAC. See Section 7.2.16 on page41.

Also after each transmission, the 4TPHY itself will generate a Hearbeat signal by applying a 1 us pulse on the COL lines which go into the MAC. See Sec tion7.2.10 on pa ge38.

3.1.4 Link Detector/Generator

The link generator is a timer circuit that generates a link pulse as defined by the 10 Base-T specification that will be sent by the transmitter section. The pulse which is 100ns wide is transmitted on the transmit output, every 16ms, in the absence of transmit data. The pulse is used to check the integrity of the connection to the remote MAU.

The link detection circuit checks for valid pulses from the remote MAU and if valid link pulses are not received the link detector will disable the twisted pair transmitter, receiver and collision detection functions.

3.1.5 Jabber

The Jabber function disables the transmitter if it attempts to transmit a much longer than legal sized packet. The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than 20-30ms. The transmitter is then disabled for the entire time that the ENDEC module's internal transmit is asserted. The transmitter signal has to be deasserted for approximately 400-600ms (the unjab time) before the Jabber re-enables the transmit outputs.

There is also a jabber disable bit in each of the port control/status registers which when activated, disables the jabber function.

3.1.6 Transmit Driver

The transmit driver function utilizes the internal filters to provide a properly matched and waveshaped output which directly drives the isolation transformer/choke.

3.1.7 Transmit Filter

There is no need for external filters on the twisted pair transmit interface because the filters are integrated. Only an isolation transformer and impedance matching resistors are needed for the transmit twisted pair interface (see Figur e6 in the previous section). The transmit filter ensures that all the harmonics in the transmit signal are attenuated by at least 27dB. The transmit signal requires a

1:2 (1 on the chip side and 2 on the cable side) isolation transformer.

3.2 ENDEC Module

The ENDEC consists of two major blocks:

— The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester, and transmits it differentially to the transceiver, through the differential transmit driver.

— The Manchester decoder receives Manchester data from the transceiver, converts it to NRZ data and recovers clock pulses and sends them to the controller.

3.2.8 Manchester Encoder and Differential Driver

The encoder begins operation when the Transmit Enable input (TXE) goes high and converts the clock and NRZ data to Manchester data for the transceiver. For the duration of TXE remaining high, the Transmit Data (TXD) is encoded for the transmit-driver pair (TX ±). TXD must be valid on the rising edge of Transmit Clock (TXC). Transmission ends when TXE goes low. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

3.2.9 Manchester Decoder

The decoder consists of a differential receiver and a PLL to separate the Manchester encoded data stream into internal clock signals and data. Once the input exceeds the squelch requirements, Carrier Sense (CRS) is asserted off the first edge presented to the decoder. Once the decoder has locked onto the incoming data stream, it provides data (RXD) and clock (RXC) to the MAC.

The decoder detects the end of a frame when no more mid-bit transitions are detected. Typically, within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for at least five more bit times after CRS goes low, to guarantee the receive timings of the controller.

The GATERXC bit, D0, in the Global Control and Status Register, controls the receive clock (RXC) gated function. This allows the selection between 5 RXCs after the deassertion of carrier sense (CRS) or continuous RXCs after the deassertion of CRS. See Figure10. The GATERXC function which is programmable through the serial management interface is also available via a strap option. The default mode is to enable 5 RXCs after the deassertion of CRS. If a 2.7 kΩ resistor is connected to the COL[4] pin (and the device is reset), then the continuous RXCs mode is enabled. There is a third RXC Mode which is used for certain MACs. In this mode there are no RXC clocks added after CRS deassertion. Please see Table7 on page11

3.2.10 Collision Translator/Decoder

When in AUI Mode and the external Ethernet transceiver detects a collision, it generates a 10 MHz signal to the differential collision inputs (CD ±) of the 4TPHY. When these inputs are detected active, the transceiver asserts COL which signals the MAC controller to back off its current transmission and reschedule another one.

The differential collision inputs are terminated the same way as the differential receive inputs. The squelch circuitry is the same, rejecting pulses with levels less than ±160mV.

3.3 Additional Features

3.3.11 Transceiver Loopback

When diagnostic loopback is programmed (in twisted pair mode), the transceiver redirects its transmitted data back into its receive path. The transmit driver and receive input circuitry are disabled in diagnostic loopback mode, hence, the transceiver is isolated from the network cable. This allows for diagnostic testing of the data path all the way up to the transceiver without transmitting or being interrupted by the media. This test can be performed regardless of the link status (i.e. a twisted pair cable does not have to be connected to perform transceiver loopback).

3.3.12 AUI/TP AutoSwitching - Port 1

The AUI/TP autoswitching lets the transceiver auto-switch between the AUI and TP outputs. At power up, the autoswitch function is enabled (AUTOSW bit = 1). When the auto-switch function is enabled, it allows the transceiver to automatically switch between TP and AUI outputs. If there is an absence of link pulses, the transceiver will switch to AUI mode. Similarly, when the transceiver starts detecting link pulses it will switch to TP mode. The switching from one mode to the next is only done after the current packet has been transmitted or received. If the twisted pair output is jabbering and it gets into the link fail state, then the switch to AUI mode is made only after the jabbering has stopped (this includes the time it takes to unjab). Also, if TP mode is selected, transmit packet data will only be driven by the twisted pair outputs and the AUI transmit outputs will remain idle. Similar behavior applies when AUI mode is selected. In TPI mode, the twisted pair drivers will continue to send link pulses, however, no packet data will be transmitted. It must also be noted that when switching from TP to AUI mode, it might take a few msec to completely power-up the AUI before it becomes fully operational. Switching in the opposite direction (AUI to TP) does not have this power-up time, since the TP section is already powered (the twisted pair transmit section still sends link pulses in AUI mode).

3.3.13 Disable Management Interface Mode

This is also called the “enhanced full duplex” mode. In this mode the management interface signals MDC and MDIO are not available, hence the 4TPhy registers can’t be read or written to. MDC pin 93 becomes the loopback select pin, and MDIO becomes LINK_4. The advantage of this mode is that the LINK status pins for all 4 ports are directly accessible as well as the direct control of the loopback mode of operation. Also, in this mode the duplex operation of the 4TPHY can be directly controlled by the FDX[4:1] pins as described in the section below.

3.3.14 Full Duplex Operation

Full duplex operation is supported by the transceiver being able to simultaneously transmit and receive without asserting collision. The ENDEC has been implemented such that it can encode and decode simultaneously and also be robust enough to reject crosstalk noise with both transmit and receive channels enabled.

The full duplex feature has two modes of operation. The first option (normal FDX mode), allows full duplex configuration of the ports only after a device reset (through the FDX[4:1] pins). The FDX[4:1] pins are sampled during device reset to determine which ports to configure into full duplex mode. Changing the logic state on the FDX[4:1]

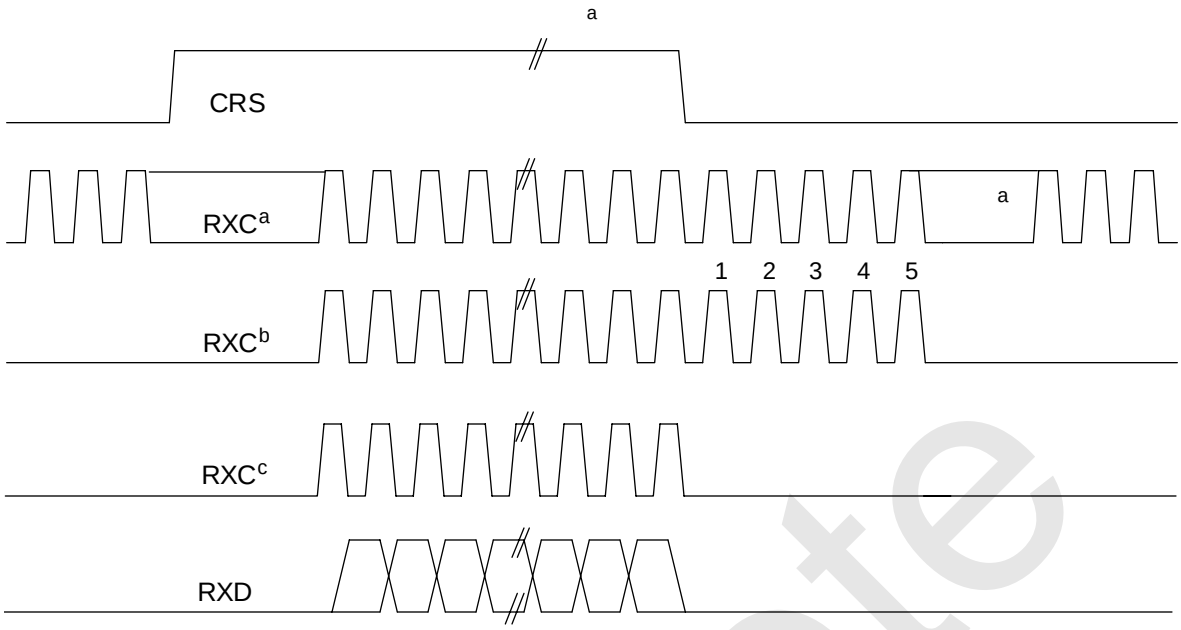


Figure 10. Receive Clock Timing - Continuous RXC Mode vs. 5 RXC Mode

a. There will be a transition period where the RXC switches from the internal clock to received clock.
b. There are 5 RXCs after CRS is deasserted
c. There are no RXCs after CRS is deasserted. ple as e see Table7 on page11

pins will not take affect until a device reset is performed. A logic '0' enables full duplex and a logic'1' enables simplex mode. In addition, the full duplex capability of a port can also be changed dynamically by writing the FDX bit (D12) of the Port Control Register via the Mgmt Interface.

The second option (enhanced FDX mode), allows changing the full duplex configuration of each port dynamically through the FDX[4:1] pins. As soon as the logic state on the FDX[4:1] pins are changed, the corresponding ports full duplex mode will be enabled or disabled.

In order to select the desired full duplex mode, the COL[2] pin has a strapping feature. The default is normal full duplex mode. If enhanced full duplex mode is desired, then a 2.7K pull-down resistor is required on the COL[2] pin. During device reset, the COL[2] pin is sampled to determine the correct full duplex mode configuration.

Regardless of the full duplex mode, the logic state of the FDX[4:1] pins are sampled during reset to determine a port's initial configuration for full duplex capability.

3.3.15 Strapping Options and Reset

Tabl e10 shows the various strapping options and the associated pins used to configure the device at power-up.

Table 10. Strapping Option Description (Default = '1', except FDX[4:1] pins have no default)

Pin Name	Function	'1'	'0'	Comments
COL[4]	Gate RXC	5 RXCs	Continuous	Selects the # of RXCs after CRS deassertion
COL[3]	Rx Filter Select	Disable	Enable	Enables/disables the Rx filter. Suggest enable
COL[2]	Full Duplex Mode Select	Normal	Enhanced	Selects normal or enhanced full duplex mode
COL[1]	LED Mode Select	Normal	Enhanced	Selects normal or enhanced LED mode
CRS[3:1]	Transceiver Address Select	Addr	Addr	Sets the Tcvr address for MII access
FDX[4:1]	Per Port Full Duplex Select	Half duplex	Full Duplex	Selects full or half duplex configuration per port (no internal pull-ups)
RXD[4]	Auto-Negotiation Enable	Disable	Enable	Enables/disables Auto-Negotiation.
RXD[3:1] LNK[1]	Programmable MAC Interface	Mode 1	See Tab le7 on page11	Selects one of five MAC interface modes. See the table in the MAC interface section.

These pins are sampled during device reset.(Power up or hardware reset, but not software port reset.)These pins have internal pull-ups, if the default modes are desired, no external resistors are required. (Except FDX[4:1] which have no pull-up resistors.) A 2.7 k Ω pull down resistor(s) are required to select non-default modes. If some type of

control logic is used to select the non-default modes, instead of pull down resistors, then the level on the strapping pins must be maintained for approximately 10 clocks after the RESET signal deasserts.

There are 3 different ways to reset the device or ports. One of them is during power-up. The second method is hardware reset where a low active pulse is applied to the RESET pin. The third method is software reset of individual ports by writing a '1' to bit D15 of the port status/control registers 0000h-0003h. This reset doesn't reset the device and doesn't sample the strap options. Please see register definitions for details.

3.3.16 On Chip Reference (ROC)

This pin connects to an external precision (1%) resistor to ground for the on chip reference. The recommended value of this resistor will be determined when device characterization is complete. The user should adjust this value based on the specific board design. (Estimated range is between 0-5 kΩ.)

3.4 Auto-negotiation Block

3.4.17 IEEE 802.3u AUTO-NEGOTIATION

The Auto-Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) bursts provide the signaling used to communicate Auto-Negotiation abilities between two devices at each end of a link segment. For further detail regarding Auto-Negotiation, refer to clause 28 of the IEEE 802.3u specification. The 4TPHY supports two Ethernet protocols (10Mb/s Half Duplex and 10Mb/s Full Duplex), so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the ability of the Link Partner.

Upon hardware reset, RXD[4] is sampled (strapping option) to determine if Auto-Negotiation is enabled. The 4TPHY uses default register values to advertise its full set of abilities (10 Mb/s Half Duplex, 10 Mb/s Full Duplex) unless subsequent software accesses modify the mode.

3.4.18 Auto-Negotiation Register Control

When Auto-Negotiation is enabled, the 4TPHY transmits the abilities programmed into the Auto-Negotiation Advertisement Register (ANAR) via FLP Bursts. Either 10Mb/s Half-Duplex or Full Duplex modes may be selected.

The Basic Mode Control/Status Register (BMCR) provides software with a mechanism to control the operation of the 4TPHY. The status of Auto-Negotiation Enable and Duplex mode independent of configuration via Auto-Negotiation, or software may be obtained by reading the BMCR and Port Status Register (respectively). These bits are valid if Auto-Negotiation is disabled or after Auto-Negotiation is complete.

The contents of the Auto-Negotiation Link Partner Ability Register (ANLPAR) register are used to automatically configure to the highest performance protocol between the local and far-end ports. If external software needs to find out the result of Auto_Negotiation, it can determine which mode has been configured by Auto-Negotiation by comparing the contents of the ANAR and ANLPAR registers and then selecting the technology whose bit is set in both the ANAR and ANLPAR of highest priority relative to the following list. (Please note that 4TPHY does this automatically and configures itself without need for software. The software might be used by management entity etc. to find out the results of auto-negotiation.)

Auto-Negotiation Priority Resolution:

— 10BASE-T Full Duplex

— 10BASE-T Half Duplex (Lowest Priority)

The BMCR provides control of enabling, disabling, and restarting of the Auto-Negotiation function. When Auto-Negotiation is disabled the Duplex Mode bits in the Port Status Register controls switching between full duplex operation and half duplex operation. The Duplex Mode bits have no effect on the mode of operation when the Auto-Negotiation Enable bit is set.

The BMCR also provides status on:

— Whether Auto-Negotiation is complete.

— Whether the Link Partner is advertising that a remote fault has occurred.

The Auto-Negotiation Advertisement Register (ANAR) indicates the Auto-Negotiation abilities to be advertised by the 4TPHY. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR. Updating the ANAR to suppress an ability is one way for a management agent to change (force) the technology that is used.

The Auto-Negotiation Link Partner Ability Register (ANLPAR) indicates the abilities of the Link Partner as indicated by Auto-Negotiation communication. The contents of this register are considered valid when the Auto-Negotiation Complete bit is set.

The Auto-Negotiation Expansion Register (ANER) indicates additional Auto-Negotiation status. The ANER provides status on:

— Whether a Multiple Link Fault has occurred.

— Whether the Link Partner supports the Next Page function.

— Whether the 4TPHY supports the Next Page function. (The 4TPHY does support the Next Page function.)

— Whether the current page being exchanged by Auto-Negotiation has been received.

— Whether the Link Partner supports Auto-Negotiation.

3.4.19 Auto-Negotiation Parallel Detection

The 4TPHY supports the Parallel Detection function as defined in the IEEE 802.3u specification. Parallel Detection requires the 10 Mb/s receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation yet is transmitting link signals that the 10BASE-T PMAs recognize as valid link signals.

If the 4TPHY completes Auto-Negotiation as a result of Parallel Detection the appropriate bits in the ANLPAR register will be set to reflect the mode of operation present in the Link Partner. Software may determine that negotiation completed via Parallel Detection by reading a zero in the Link Partner Auto-Negotiation Able bit once the Auto-Negotiation Complete bit is set.

As an example of Parallel Detection, when the Link Partner supports 10BASE-T full duplex, but does not support Auto-Negotiation. Parallel Detection will allow the 4TPHY to

negotiate to 10Mb/s Half Duplex operation by detecting link pulses separated by 8-24 ms.

3.4.20 Auto-Negotiation Restart

Once Auto-Negotiation has completed it may be restarted at any time byfirst resetting and then setting bit 9 of the BMCR to one. If the mode configured by a successful Auto-Negotiation loses a valid link, then the Auto-Negotiation process will resume and attempt to determine the configuration for the link. This function ensures that a valid configuration is maintained if the cable becomes disconnected.

A renegotiation request fromany entity, such as a management agent, will cause the 4TPHY to halt any transmit data and link pulse activity until the break_link_timer expires (1500ms). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The 4TPHY will resume Auto-Negotiation after the break_link_timer has expired by issuing FLP (fast Link Pulse) bursts.

3.4.21 Enabling Auto-Negotiation via Software

It is important to note that if the 4TPHY has been initialized upon power-up as a non-auto-negotiating device (forced technology), and it is then required that auto-negotiation of re-auto-negotiation be initiated via software, bit 0 of the Basic Mode Control Register must first be cleared and then set for any auto-negotiation function to take effect.

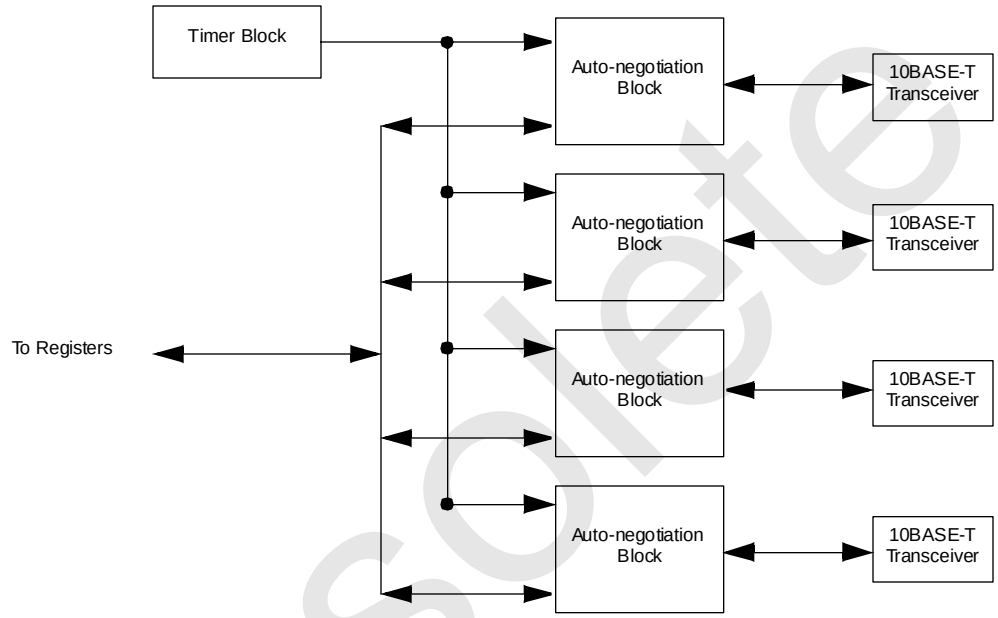


Figure 11. Auto-Negotiation Block Diagram

3.5 JTAG Boundary Scan

The 4TPHY supports JTAG Boundary Scan per IEEE 1149.1 via test clock (TCK), test data input (TDI), test data output (TDO), test mode select (TMS), and test reset (TRST). The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. Figur e12 depicts the IEEE 1149.1 architecture

The standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. It also provides a means of accessing and controlling design-for-test features built into the digital integrated circuits. Such features include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product. The IEEE 1149.1 Boundary Scan Architecture document should be referenced for additional detail.

The circuitry defined by this standard allows test instructions and associated data to be input serially into a device. The instruction execution results are output serially.

The DP83924B reserves five pins, called the Test Access Port (TAP), to provide test access: TMS, TCK, Test Data Input (TDI), Test Data Output (TDO) and Test Reset (TRST). These signals are describe d in T able4 on page7. To ensure race-free operation all input and output data is synchronous to the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK while output signal (TDO) is clocked on the falling edge.

3.5.22 Test Logic

The IEEE 1149.1 Test Logic consists of a Test Access Port (TAP) controller, an instruction register, and a group of test data registers including Bypass, Device Identification and Boundary Scan registers.

TheTAP controller is a synchronous 16 state machine that responds to changes at the TMS and TCK signals.

This controls the sequence of operations by generating clock and control signals to the instruction and test data registers. The control signals switch TDI and TDO between instruction and test data registers

The DP83924B implements 4 basic instructions: ID_Code, bypass, Sample/Preload and Extest. Upon reset, the ID_Code instruction is selected by default.

3.0 Detailed Functional Description (Continued)

3.5.23 ID_Code Instruction

The ID_Code instruction allows users to select the 32-bit IDCODE register and interrogate the contents which consist of the manufacturer's ID, part ID and the version number. For DP83924B the ID code register holds the value h'1800801F.

3.5.24 Bypass Instruction

The bypass instruction uses the bypass register. The bypass register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the DP83924B when test operation is not required. This allows more rapid movement of test data to and from other testable devices in the system.

3.5.25 Sample/Preload Instruction

The Sample/Preload instruction allows scanning of the boundary-scan register without causing interference to the normal operation of the on-chip system logic.

Two functions are performed when this instruction is selected.

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload allows an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells which are connected to system output pins. This ensures that known data is driven through the system output pins upon entering the Extest instruction.

Without Preload, indeterminate data would be driven until the first scan sequence has been completed. The shifting of data for the Sample and Preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

3.5.26 Extest Instruction

The Extest instruction allows circuitry external to the DP83924B (typically the board interconnections) to be tested.

Prior to executing the Extest instruction, the first test stimulus to be applied will be shifted into the boundary-scan registers using the Sample/Preload instruction. Thus, when the change to the Extest instruction takes place, known data will be driven immediately from the DP83924B to its external connections.

This provides stimulus to the system input pins of adjacent devices on the assembled printed circuit board s. Figure12 below illustrates the IEEE 1149.1 architecture.

3.5.27 Device Testing

IEEE 1149.1 provides a simple solution for testing many of the standard static pin parametrics. Reasonably accurate limits may be tested as a functional pattern.

The IEEE 1149.1 test circuitry is tested itself as a consequence of testing pin parametrics. Specific tests are:

- TRI-STATE® conditions of TDO when serial shift between TDI and TDO is not selected
- Input leakage of TCK, TMS, TDI and TRST
- Output has TRI-STATE leakage of TDO
- Opens and shorts of TCK, TMS, TDI,TRST, and TDO
- IDCODE register, the bypass registerand the TAP controller state machine sequences

Open and shorted pins can be identified by placing an alternating bit pattern on the I/O pins. Any shorted bond wires would either cause an input to be misinterpreted in the inputs scan phase, or the test comparator would fail an output during data scan.

Repeating the test with the inverse bit pattern provides coverage of V_{CC} and GND short/open circuits.

3.5.28 Boundary Scan Description Language File

A Boundary Scan Description Language (BSDL) file is available. Contact your local National Semiconductor representative to obtain the latest version.

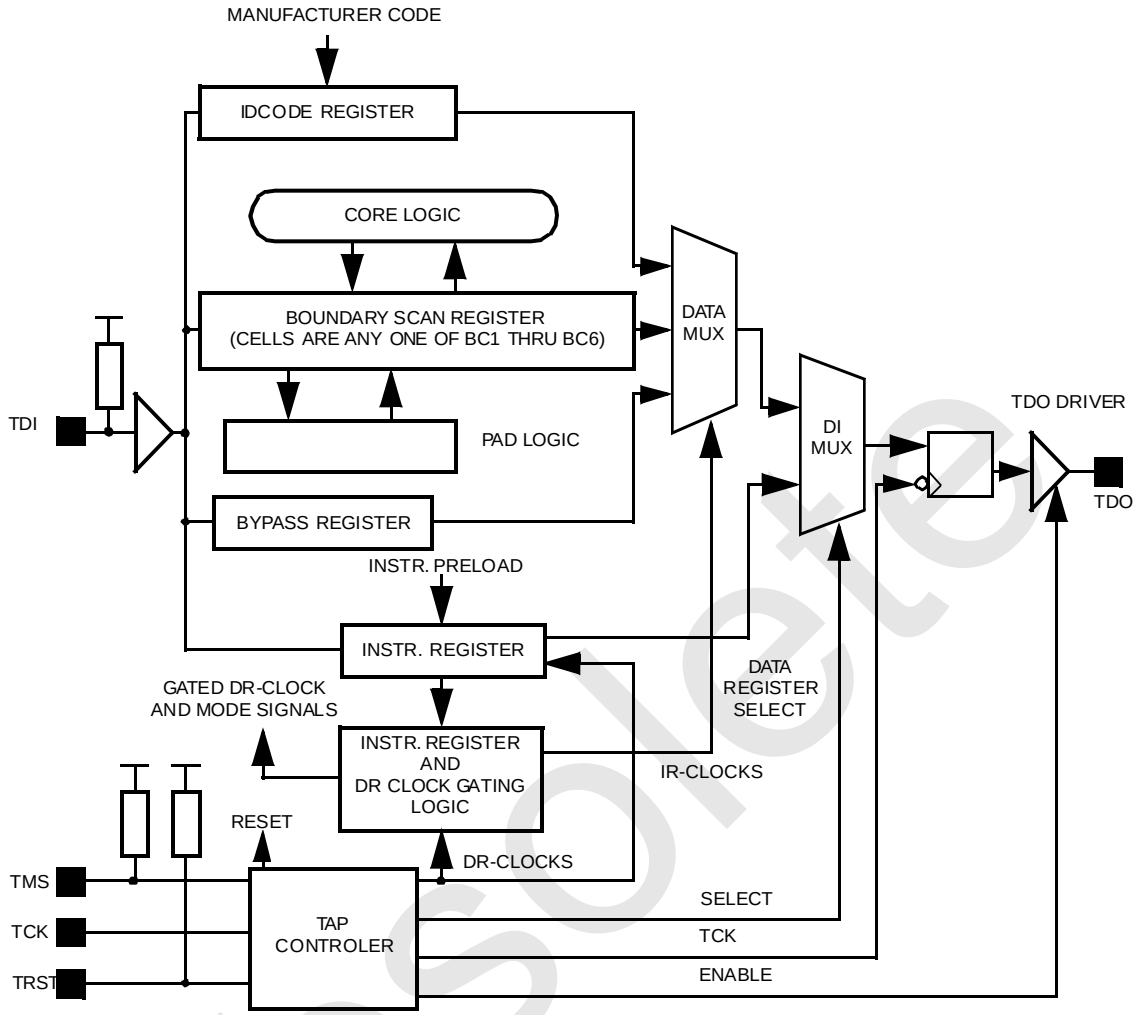


Figure 12. IEEE 1149.1 Architecture

4.0 Register Descriptions

4.1 Register Map and Descriptions

The following is an overall register map for the transceiver/ENDEC. There are two groups of registers. The first group provides individual port control which configures and reports status for functions applicable on a port basis. The second group provides global control which enables configuration of operations that are common to all the ports.

Table 11. DP83924B Register Map Accessible via the Management Interface

Register Address	Name	Description	Access
00H	Port 1 Control/Status.	Configuration setting and Operational Status for Port 1.	R/W
01H	Port 2 Control/Status.	Configuration setting and Operational Status for Port 2.	R/W
02H	Port 3 Control/Status.	Configuration setting and Operational Status for Port 3.	R/W
03H	Port 4 Control/Status.	Configuration setting and Operational Status for Port 4.	R/W
04H - 07H	reserved	reserved	R
08H	Global Control/Status Register.	Global setting and interrupt capabilities.	R/W
09H	Port 1 Basic Mode Control Register.	Port 1's Auto-Negotiation Control And Status Register.	R/W
0AH	Port 2 Basic Mode Control Register.	Port 2's Auto-Negotiation Control And Status Register.	R/W
0BH	Port 3 Basic Mode Control Register.	Port 3's Auto-Negotiation Control And Status Register.	R/W
0CH	Port 4 Basic Mode Control Register.	Port 4's Auto-Negotiation Control And Status Register.	R/W
0DH	Silicon Revision.	Programmed with a number representing the design revision.	R
0EH	Port 1 Auto-Negotiation Advertisement Register.	Auto-Negotiation advertisement register for port 1.	R/W
0FH	Port 2 Auto-Negotiation Advertisement Register.	Auto-Negotiation advertisement register for port 2.	R/W
10H	Port 3 Auto-Negotiation Advertisement Register.	Auto-Negotiation advertisement register for port 3.	R/W
11H	Port 4 Auto-Negotiation Advertisement Register.	Auto-Negotiation advertisement register for port 4.	R/W
12H	Port 1 Link Partner Ability Register.	Link Partner Ability Register for Port 1.	R/W
13H	Port 2 Link Partner Ability Register.	Link Partner Ability Register for Port 2.	R/W
14H	Port 3 Link Partner Ability Register.	Link Partner Ability Register for Port 3.	R/W
15H	Port 4 Link Partner Ability Register.	Link Partner Ability Register for Port 4.	R/W
16H	Port 1 Auto-Negotiation Expansion Register.	Port 1 Expansion Register for Auto-Negotiation.	R/W
17H	Port 2 Auto-Negotiation Expansion Register.	Port 2 Expansion Register for Auto-Negotiation.	R/W
18H	Port 3 Auto-Negotiation Expansion Register.	Port 3 Expansion Register for Auto-Negotiation.	R/W
19H	Port 4 Auto-Negotiation Expansion Register.	Port 4 Expansion Register for Auto-Negotiation.	R/W
1AH	Port 1 Next Page Transmit Register.	Port 1's Auto-Negotiation Next Page Transmit Register.	R/W
1BH	Port 2 Next Page Transmit Register.	Port 2's Auto-Negotiation Next Page Transmit Register.	R/W
1CH	Port 3 Next Page Transmit Register.	Port 3's Auto-Negotiation Next Page Transmit Register.	R/W
1DH	Port 4 Next Page Transmit Register.	Port 4's Auto-Negotiation Next Page Transmit Register.	R/W
1EH	reserved	reserved	R
1FH	Test Control.	Controls test functions for manufacturing test of the device.	R/W

4.0 Register Descriptions (Continued)

Table 12. Port N Control/Status Register, addr = 00h - 03h (port 1 to port 4)

D15	D14	D13	D12	D11	D10 : D9	D8	D7	D6 : D3	D2	D1	D0
RST	LPBK	LNKPLS	FDX	JABE	RESV	LNKDIS	ERR	RESV	POLST	LNK ST	JAB ST

This register controls the various operating modes available for the transceiver and ENDEC functions. There is one register per ENDEC/Transceiver on this device.

Name	Bit	Reset Value	Description	Type
RST	D15	0	**Software Reset/Enable:** If this bit is set to '1', then this port's transceivers and ENDEC modules are reset back to their idle state (IEEE state diagram idle state, i.e. it will reestablish link, re auto-negotiate). If this bit is '0', then normal operation is expected. Software reset doesn't sample the strap options. (See Sec tion3.3 .15 on page16) This bit is self clearing.	R/W
LPBK	D14	0	**Loopback Transceiver:** If this bit is set, then this port's 10base-T transceiver will loop data from near the network interface pins back to the MAC, to test the operation of the transceiver. If reset, loopback is disabled.	R/W
LINKPLS	D13	0	**Link pulse transmission**: Transmission of Link Pulses can be turned off by setting this bit to '1'. If this bit is set to '0', normal operation (Link Pulse Transmission Enabled) is resumed.	R/W
FDX	D12	Opposite of the strap option FDX[4:1]	**Full Duplex Operation**: If this bit is '1', then the ports full duplex capability is enabled. If '0', then half-duplex is enabled. The reset value is determined by the mode selected by the FDX[4:1] pins and is opposite of the strap value. (i.e. if strap FDX='1' then reset value of this bit = '0')	R/W
JABE	D11	1	**Jabber Enable:** If this bit is set, then the ports jabber function is enabled. If reset, then the jabber feature is disabled.	R/W
resv	D10-9	0	**Reserved**: must be written with '0'.	R/W
LNKDIS	D8	0	**Link Detect Disable:** If this bit is set, this port's link detection circuitry will be disabled and regardless of the link condition, good_link will be established. If reset, then normal link operation is enabled.	R/W
ERR	D7	0	**LED Error**: If this bit is set, this port's status LED will go solid. If reset, normal LED operation is resumed.This bit can be set by management entity based on any criteria and will be used only as a visual prompt. The status LED is only available during normal LED mode of operation.	R/W
resv	D6-3	0	**Reserved**: must be written with '0'.	R/W
POL ST	D2	1	**Polarity Status**: This bit is set when bad polarity has been detected. Status bit, read-only. This bit is only meaningful if ENPOLSW bit D9 of register 08h has been set.	R
LNK ST	D1	1	**Link Status**: This bit is set, when the port is in the link-fail state. (Even in forced AUI mode on port 1, this bit will still indicate TPI link status for port1). If link detect is disabled by setting bit D8 above, then this bit is always = 0 (good link state).	R
JAB ST	D0	0	**Jabber Status**: This bit is set, when the port is in the jabber condition. Status bit, read-only. This bit is always = 0 (no jabber condition) if bit D11 above is reset (jabber disabled).	R

Table 13. Global Control/Mask Register, addr = 08h

D15 : D14	D13	D12	D11	D10	D9	D8 : D3	D2	D1	D0
RESV	LNKJABINT	AUTOSW	TPIAUI	HBEN	ENPOLSW	RESV	KLED	LJINTMASK	GATERXC

This register controls the various operating modes available for the transceiver and ENDEC functions. This register will affect the operation of ALL ports of the 4TPhy.

Name	Bit	Reset Value	Description	Type
resv	D15-14	0	**Reserved**; must be written with '0'.	R/W
LNKJABINT	D13	0	**Link Jabber Interrupt Status**; This bit is set when an interrupt occurs due to a link status change or a jabber condition on any port. This bit is cleared on a register read (the interrupt is also cleared).	R
AUTOSW	D12	1	**Auto Switching**; If this bit is set, automatic selection of TPI or AUI on port 1 is enabled. If reset, port 1 configuration is determined by the TPIAUI bit.	R/W
TPIAUI	D11	1	**TPI Select**; If this bit is set, then port 1 is placed into TP mode. If reset, then port 1 is configured for AUI mode. This bit is ignored if the AUTOSW bit is set.	R/W
HBEN	D10	1	**Heartbeat Enable**; If this bit is set, then heartbeat is enabled. If reset, it is disabled for all ports.	R/W
ENPOLSW	D9	1	**Enable Polarity Switching**; If this bit is set, then auto polarity detection and correction is enabled for all ports. If reset, it is disabled.	R/W
MAC I/F	D[8:6]	Strap RXD[3:1]	MAC Interface selection; Selects between one of 5 Serial NRZ MAC interface protocols. See the table in the Interface Description chapter for details on the different modes.	R/W
resv	D5	0	**Reserved**; must be written with '0'.	R/W
RXD_IDLE	D4	Opposite of strap option LINK_1	**RXD Level During Idle -** selects the level of RXD during Rx Idle (CRS deasserted). '1' selects RXD_IDLE = High, '0' selects RXD_IDLE= Low. Default condition is for RXD to be low during Idle.The reset value is determined by the mode selected by the LINK_1 pin and is opposite of the strap value. (i.e. if strap LINK_1 ='1' then reset value of this bit = '0')	R/W
resv	D3	0	**Reserved**; must be written with '0'.	R/W
KLED	D2	0	**Enhanced LED Mode**; If this bit is set, "enhanced" LED mode is selected. If reset, "normal" LED mode is selected.	R/W
LJINTMASK	D1	0	**Link Jabber Interrupt Mask**; If this bit is set, an interrupt will NOT be generated on a link-fail or jabber condition experienced on any port. If reset, interrupt generation is enabled.	R/W
GATERXC	D0	Strap COL[4]	**RXC Gated**; If this bit is set, five RXC clocks are forced after CRS is deasserted. If reset, then RXC clocks are continuous after CRS deasserts.	R/W

Table 14. Basic Mode Control/Status Register, addr 09 - 0CH (port 1 to port 4)

D15 : D5	D4	D3	D2	D1	D0
RESV	ANCA	RF	ANC	RAN	ANE

This register controls the Auto-Negotiation functions and reports status for this port.

Name	Bit	Description	Type
resv	D15:5	Reserved	R
ANCA	D4	Auto-Negotiation Configuration Ability: 1 = Capable of Auto-Negotiation. 0 = Not capable of Auto-Negotiation.	R
RF	D3	Remote Fault: 1 = Remote Fault detected or reported by Link Partner 0 = No fault detected.	R
ANC	D2	Auto-Negotiation Complete: 1 = Auto-Negotiation completed. 0 = Auto-Negotiation not completed.	R
RAN	D1	Restart Auto-Negotiation: 1 = Restart Auto-Negotiation. (This bit has to be first reset and then set to be able to restart Auto-Negotiation) 0 = Normal operation.	R/W
ANE	D0	Auto-Negotiation Enable: 1 = Auto-Negotiation enabled. 0 = Auto-Negotiation disabled.	R/W

Table 15. Silicon Revision Register, addr = 0Dh

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register indicates the current revision of this silicon.

Name	Bit	Description	Type
ID	D15-0	**Revision ID:** 16'h0001	R

Table 16. Auto-Negotiation Advertisement Register, addr 0EH - 11H (port 1 to port 4)

D15	D14	D13	D12:7	D6	D5	D4:D0
NPI	RESV	RF	RESV	FDX	HDX	RESV

This register contains the advertised abilities of this device as they will be transmitted to it's Link Partner during Auto-Negotiation.

Name	Bit	Description	Type
NPI	D15	Next Page Indication: 0 = Next Page Transfer not desired. 1 = Next Page Transfer desired.	R/W
resv	D14	Reserved	R
RF	D13	Remote Fault: 1 = Advertises that this device has detected a remote fault. 0 = No remote fault detected.	R/W
resv	D12:7	Reserved	R
FDX	D6	Full Duplex Capable: 1 = 10BASE-T Full Duplex supported by the local device. 0 = 10BASE-T Full Duplex not supported. The strap option on pins FDX[4:1] have no effect on what is advertised during auto-negotiation	R/W
HDX	D5	Half Duplex Capable: 1 = 10BASE-T Half Duplex supported by the local device. 0 = 10BASE-T Half Duplex not supported.	R/W
resv	D4:0	Reserved	R

Table 17. Auto-Negotiation Link Partner Ability Register, addr 12H - 15H (port 1 to port 4)

D15	D14	D13	D12:7	D6	D5	D4:D0
NPI	ACK	RF	RESV	FDX	HDX	PRO

This register contains the advertised abilities of the Link Partner during Auto-Negotiation.

Name	Bit	Description	Type
NPI	D15	Next Page Indication: 0 = The Link Partner does not desire a Next Page Transfer. 1 = The Link Partner desires a Next Page Transfer.	R
ACK	D14	Acknowledge: 1 = Link Partner acknowledges the reception of the ability data word. 0 = Not acknowledged.	R
RF	D13	Remote Fault: 1 = Remote Fault indicated by Link Partner. 0 = No remote fault reported by Link Partner.	R
resv	D12:7	Reserved	R
FDX	D6	Full Duplex Capable: 1 = 10BASE-T Full Duplex supported by Link Partner. 0 = 10BASE-T Full Duplex not supported by Link Partner.	R
HDX	D5	Half Duplex Capable: 1 = 10BASE-T Half Duplex supported by Link Partner. 0 = 10BASE-T Half Duplex not supported by Link Partner.	R
PRO	D4:0	Protocol Selection Bits: Link Partners binary encoded protocol selector.	R

Table 18. Auto-Negotiation Expansion Register, addr 16H - 19H (port 1 to port 4)

D15:D5	D4	D3	D2	D1	D0
RESV	PDF	LPNPA	NPA	PRX	LPANA

Name	Bit	Description	Type
resv	D15:5	Reserved	R
PDF	D4	Parallel Detection Fault: 1 = A fault has been detected via parallel detection. 0 = No fault detected via parallel detection.	R
LPNPA	D3	Link Partner Next Page Able: 1 = Link Partner supports Next Page negotiation. 0 = Link Partner does not.	R
NPA	D2	Next Page Able: 1 = The local device is able to send additional Next Pages. 0 = The local device is not able.	R
PRX	D1	Page Received: 1 = New Link Code Word Page received. Cleared on read. 0 = New Link Code Word Page not received.	R
LPANA	D0	Link Partner Auto-Negotiation Able: 1 = Link Partner supports Auto-Negotiation. 0 = Link Partner does not support Auto-Negotiation.	R

Table 19. Auto-Negotiation Next Page Transmit Register, addr 1AH - 1DH (port 1 to port 4)

D15:D5	D14	D13	D12	D11	D10:0
NPI	RESV	MP	ACK2	TOG	CODE

Name	Bit	Description	Type
NP	D15	Next Page Indication: 1 = No other Next Page transfers desired. 0 = Another Next Page transfer is desired.	R/W
resv	D14	Reserved	R
MP	D13	Message Page: 1 = Message Page. 0 = Unformatted Page.	R/W
ACK2	D12	Acknowledge2: 1 = Will comply with message. 0 = Cannot comply with message.	R/W
TOG	D11	Toggle: 1 = Previous value of transmitted Link Code Word was ‘0’. 0 = Previous value of transmitted Link Code Word was ‘1’.	R
CODE	D10:0	Code: This field represents the code field of the Next Page transmission.	R/W

5.0 Application Information

5.1 Magnetics Specifications

This section describes the required magnetics to be used with the 4TPHY. The external filter/transformer used in conventional twisted pair ports is now replaced by a transformer. By integrating the transmit filter, the transformer is the only magnetics required. In this configuration, a transformer with 1:2 turn ratio on the transmit path and a 1:1 turn ratio on the receive path is required. The system designer must determine if a choke is required. Careful layout may eliminate the need.

The following is a list of suppliers that may provide magnetic components with the electrical specifications listed in Table 20. This is not an exclusive list and National Semiconductor makes no warranty as to the suitability of any of the magnetics. It is the responsibility of the user to verify the performance of any magnetics prior to production use.

BEL FUSE
HALO Electronics
PCA
PULSE Engineering
VALOR Electronic

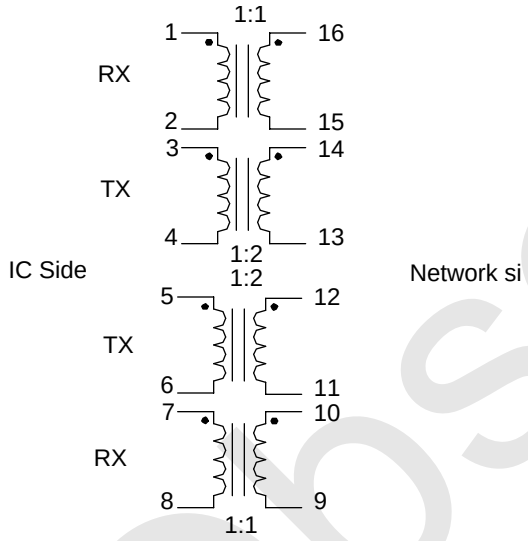


Figure 13. Typical Dual Transformer Pinout

5.2 Layout Considerations

5.2.1 Power Plane

— Minimize signal traces which traverse across multiple islands to reduce reflections and impedance mismatches. Therefore, the ground should extend from the 4TPHY to under the magnetics (transformer).

— Use a single power plane.

5.2.2 Ground Plane

— Use a single ground plane, similar to the Power Plane.

5.2.3 4TPHY Placement and Routing

— The 4TPHY should be placed as close as possible to the external transformer module/RJ45 connector.

— Each trace of a differential pair (i.e. TXU+, TXU-) between the 4TPHY and the transformer module should be as follows:

Table 20. Transformer Electrical Specifications

Parameter	Pins	Value
Open Circuit Inductance (OCL)	3-4, 5-6	50 uH (min)
	1-2, 7-8, 9-10, 11-12, 13-14, 15-16.	200 uH (min)
Inter-winding Capacitance (C_{ww})	1-2 to 15-16, 3-4 to 13-14 5-6 to 11-12 7-8 to 9-10	12 pF (max)
Leakage Inductance (LL)	1-2, short 15-16 3-4, short 13-14 5-6, short 11-12 7-8, short 9-10	0.3 uH(max)
DC Resistance (DCR)	3-4, 5-6	0.35 Ω (max)
	1-2, 7-8, 9-10, 15-16.	0.5 Ω (max)
	11-12, 13-14	1.0 Ω (max)
High Potential	1-2 to 15-16 3-4 to 13-14 5-6 to 11-12 7-8 to 9-10	2000 Vrms for 1 min.

RX +/- pair trace lengths should be matched. The width should be 8 mils min, with a trace-to-trace spacing of 8 mils min.

TX+/- pair trace lengths should be matched. The width should be 15 mils min, with a trace-to-trace spacing of 15 mils min (if the total trace length between the 4TPHY and the RJ45 connector is less than 1.5”, then 8 mil spacing and width can be used).

The TX and RX spacing should be 15 mils min.

— The source termination (R,C) must be placed as close to the device as possible.

— 100 Ω traces between the transformer module and the RJ45 connector.

5.2.4 Analog Power and Ground Circuit

Recommended low pass filter for the Analog PLL and Waveshaper circuitry to eliminate any power supply injected noise. (There is no need to filter the digital PLL pins 62-67) This should improve jitter performance. Refer to Figur e14.

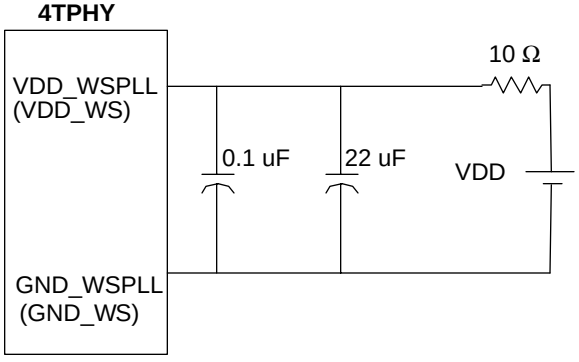


Figure 14. Pins 68-69 and 31-32 circuit diagram

5.0 Application Information (Continued)

Bypass for all other supplies should use a 0.01uF capacitor.Additional bypass for the VDD_TPI supplies should use a 1.0 uF capacitor.

5.3 LED interface considerations

The 4TPHY will update the LEDs every 50 ms. LED data is shifted out serially in bursts of 8 or 16 LED_CLKs depending on normal or enhanced LED mode selected. This data typically will be shifted into an external serial shift register to control LEDs. However if one intents to use this data for controlling a MAC, care has to be taken: During the update cycle data coming out of the shift register is not going to be valid until the cycle is completed and all the bits are shifted in place. These outputs should not be used to directly control a MAC unless the shift register outputs are latched during the update cycle. A possible implementation would be to have a one-shot which will latch the outputs of the shift register > 16 LED_CLKs once the burst begins. Since LED_CLK is 1 MHz, 20 us should be sufficient to make sure all the bits are shifted to their correct positions within the shift register before allowing the outputs to change.

6.0 User Information

6.1 CRS Assertion Connected to a 100M Node

Issue:

CRS may be asserted when connected to a non-AutoNegotiating, 100Mb/s node and the DP83924B is also in the non-AutoNegotiating mode. The 4TPHY could also establish link as a result of 100 Mb/s scrambled IDLEs. The LED could also indicate receive activity.

(All of the above are IEEE 802.3 compliant and included in the User Info Sheet for clarification purposes.)

Description:

When connected to a 100M node that is configured into non Auto Negotiation mode, the scrambled Idles transmitted by this 100M node may cause the DP83924B to assert CRS.

Since 100 Mbps scrambled idles can have waveforms passing the smart squelch levels and frequency requirements, this is to be expected. Also IEEE 802.3 Clause 14, Figure 14.6 shows that it's permissible to indicate "link test pass" based on receive data activity even in the absence of link pulses.

In Auto-negotiation mode, activity on the receive line will not cause "link test pass" state to be entered.

Compatibility:

This behavior is consistent with the DP83924A, which is a non-Auto Negotiating device.

Impact:

Problem can be resolved by enabling Auto-Negotiation via the BMCSR or through the strap option during reset.

Die Revision Plan:

The non Auto-negotiation behavior of the 4TPHY is consistent with IEEE 802.3 and doesn't require any fix.

6.2 Link Fail Inhibit Timer

Problem:

The DP83924B's Link Fail Inhibit Timer within the Auto_Negotiation block can time-out after 650ms rather than the 750ms minimum specified in 802.3u, Clause 28. (Based on simulation results)

Description:

The Link Fail Inhibit Timer, which monitors whether a valid link has been established at the end of either an FLP exchanger a parallel detection, may expire after 650 ms in DP83924B.

Impact:

There is no current solution to this problem, however, there should be no decrease in performance due to this anomaly.The 10 Mb negotiation will resolve within ~250 ms max for a parallel detection, and within ~440 ms max based on FLP detection. In both cases, it is well within the 650 ms allowed by the Link Fail Inhibit Timer.

Die Revision Plan:

There are currently no plans. Although the DP83924B does not meet the 750 ms minimum specified in IEEE 802.3u, this should not affect functionality in an otherwise compliant system environment.

6.3 Lockup during duplex mode change:

Problem:

The 4TPHY can lock up during change of the duplex mode from half duplex to full duplex.

Description:

If a port is transmitting and receiving while the duplex mode of that port is changed from half duplex to full duplex then the receive logic of the port will lock up. (The duplex mode can be changed by writing to the port register or by direct control of the duplex mode by using the FDX_n pins while in enhanced full duplex mode. In either method the lockup problem is seen) While locked up, CRS will stay high even if the cable is disconnected. A hard reset will resume regular operation.

Impact:

The users should disable transmit before changing the duplex status.

Die Revision Plan:

None.

6.4 Start of TP_IDL, 45 Bit Times to 50 mV:

Problem:

TP_IDL output should settle to a value between ±50 mV within 45 BT of the last bit transmitted. The level is typically +/- 80 mV.

Description:

The IEEE 802.3 specification defines that the output waveform should settle to ±50mV, 45 bit times after the last low to high transition of a transmitted packet. This parameter is typically +/- 80mV.

Impact:

We expect no customer impact.

Die Revision Plan:

None.

6.5 Polarity detection:

Issue:

The 924B polarity detection is based on NLPs only. It will not detect polarity inversion based on packet data.

Description:

The 4TPHY will automatically detect and correct wiring polarity reversal on the UTP receive pins. To be able to do this it has to see seven consecutive NLPs with the wrong polarity. It would not detect polarity errors based on data.

Impact:

If the link partner starts sending packets before the 4TPHY receives 7 consecutive inverted polarity NLPs then the 4TPHY will not be able to detect/correct polarity errors until there is a gap between packets such that 7 consecutive NLPs are received.

Die Revision Plan:

None.

6.0 User Information (Continued)

6.6 Link pulse template:

Issue:

The 924B will not link if the received NLPs have undershoot exceeding 800 mV for a duration exceeding 80 ns.

Description:

IEEE 802.3 Clause 14, section 14.3.1.2.1 Figure 14-12 shows the template for link test pulse. This template allows undershoot up to -3.1V. For link pulses fitting this template but having large undershoot, the 924B will not correctly detect link.

Impact:

We don't believe the above is a problem, because there are no NIC cards which have the extreme undershoots allowed in the above template. The 924B is robust enough to link even with NLPs having large undershoot, as long as the undershoot doesn't exceed -800 mV and lasts less than 80 ns.

Die Revision Plan:

None.

7.0 AC and DC Electrical Specifications

Absolute Maximum Ratings

Supply Voltage (V_{DD})	-0.5 V to 7.0 V
DC Input Voltage (V_{IN})	-0.5 V to V_{CC} + 0.5 V
DC Output Voltage (V_{OUT})	-0.5 V to V_{CC} + 0.5 V
Storage Temperature Range (T_{STG})	-65°C to 150°C
On Chip Power Dissipation (P_D)	1.6W
Lead Temp. (T_L) (Soldering, 10 sec)	260°C
ESD Rating (R_{ZAP} = 1.5k, C_{ZAP} = 120 pF)	2 kV HBM

Recommended Operating Conditions

Supply voltage (V_{DD})	5 Volts ± 5%
Ambient Temperature (T_A)	0 to 70 °C
Max. die temperature (Tj)	125°C
Max. case temperature (Tc)	105°C

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.*

Thermal Characteristics

	Max	Units
Theta Junction to Case (T_{jc})	13.7	°C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - No Airflow @ 1.0W	34.2	°C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - 225 LFPM Airflow @ 1.0W	28.6	°C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - 500 LFPM Airflow @ 1.0W	25.2	°C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - 900 LFPM Airflow @ 1.0W	21.5	°C / W

7.1 DC Specifications

T_A = 0°C to 70°C, 5V ±5%.

Symbol	Parameter	Conditions	Min	Max	Units
DIGITAL PINS (LED_CLK,$\overline{\text{LED\_DATA}}$,MDIO,MDC,CRS,RXC,RXD,COL,TXE,TXD,TXC,X1,$\overline{\text{RESET}}$,LINK, $\overline{\text{INT}}$,TCK,TDI,TDO,TMS,TRST)					
V_{OH1}	Minimum High Level Output Voltage	I_{OH} = -2mA (except MDIO, TXC, INTz)	3.0		V
V_{OH2}	Minimum High Level Output Voltage	I_{OH} = -8ma (MDIO and TXC only)	3.0		V
V_{OL1}	Maximum Low Level Output Voltage	I_{OL} = 2mA (except MDIO, TXC, INTz)		0.4	V
V_{OL2}	Maximum Low Level Output Voltage	I_{OL} = 8mA (MDIO, Extend INTZ only)		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Pull-up Resistor Current (Note 1,3)	V_{IN} = GND, VDD=5V	-250	-40	µA
I_{IL}, I_{IH}	Input Leakage (Note 2)	V_{IN} = V_{CC} or GND	-10	10	µA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND	-10	10	µA
I_{CC}	Average Operating Supply Current	TXU± Transmitting (Note 4)		250	mA
AUI INTERFACE PINS (TX±, RX±, and CD±)					
V_{OD}	Diff. Output Voltage (TX±)	78 Ω Termination	±550	±1200	mV
V_{DS}	Diff. Squelch Threshold (RX± and CD±)		±160	±300	mV
TWISTED PAIR INTERFACE PINS					
V_{ODT}	TXU+/- Differential Output Voltage		4.4	5.6	Vpp
V_{SRON1}	Receive Threshold Turn-On Voltage 10BASE-T Mode		±300	±585	mV
V_{SROFF}	Receive Threshold Turn-Off Voltage	Not tested 100%	±175	±300	mV

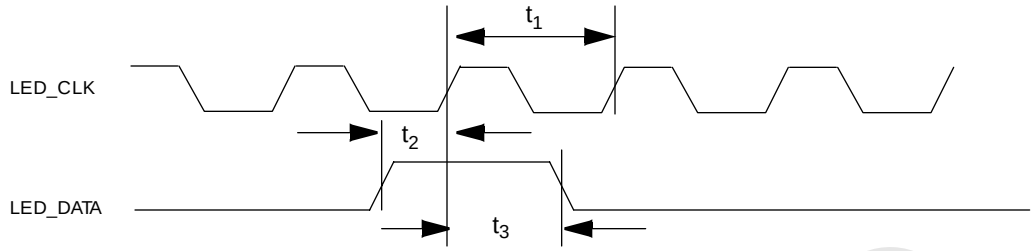
Note 1: CRS[4:1], COL[4:1], TDI, RXD[4:1], TMS, TRST
Note 2: MDIO, MDC, TXE[4:1]. TXD[4:1], X1, $\overline{\text{RESET}}$, TCK
Note 3: Internal pull-up resistor typically 20kΩ -125kΩ
Note 4: This does NOT include the current consumed off chip by the load. Typically, the power dissipated off-chip is about 76mW/ port. The total power dissipated will be: [the off-chip power dissipation (4 ports x 76mW/port)] + [on-chip power dissipation (5.25 V x 250 mA)] = (0.3 + 1.32) = 1.62 W

7.0 AC and DC Electrical Specifications (Continued)

7.2 AC Switching Specifications

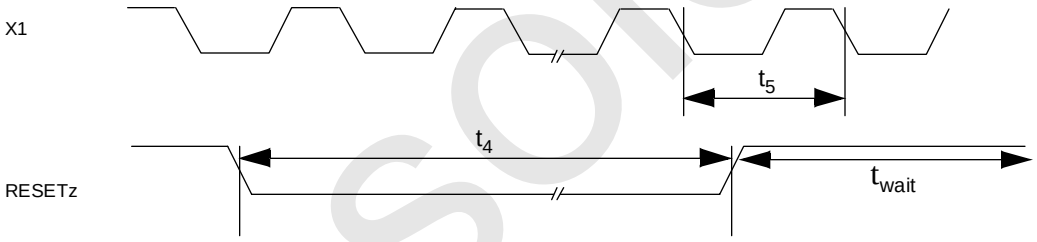
T_A = 0°C to 70°C, 5V ±5%

7.2.1 LED Interface Timing



Symbol	Parameter	Min	Max	Units
t_0	LED Clock Duty Cycle	40	60	%
t_1	LED Clock Cycle Time	900	1100	ns
t_2	LED_Data Valid to LED_Clk	25		ns
t_3	LED_Data Valid from LED_Clk	25		ns

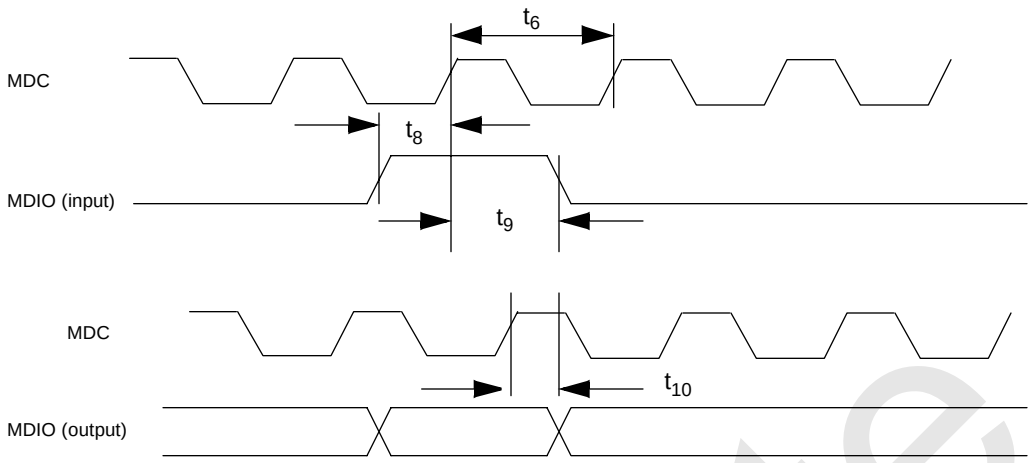
7.2.2 Reset and Strapping Timing



Symbol	Parameter	Min	Max	Units
t_4	Reset Pulse Width (X1 must be active during RESETz).	30		us
twait	min wait time after reset before 4TPHY is fully functional.	30		us
t_5	X1 Duty Cycle	40	60	%

7.0 AC and DC Electrical Specifications (Continued)

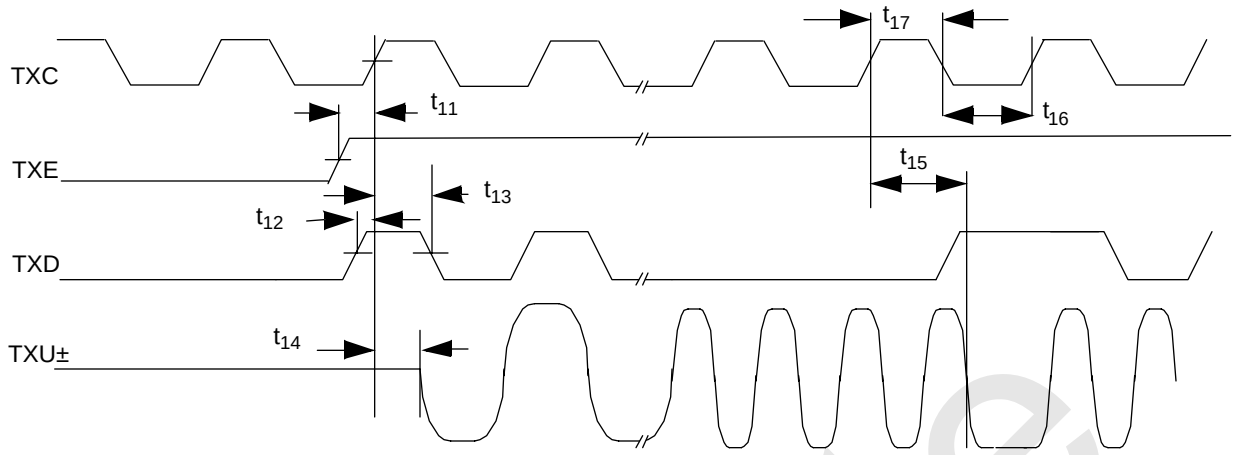
7.2.3 Management Interface Timing



Symbol	Parameter	Min	Max	Units
t_6	Mdc Frequency		2.5	MHz
t_7	Mdc Duty Cycle	40	60	%
t_8	Mdio (input) Set Up to Mdc rising edge	10		ns
t_9	Mdio (input) Hold Mdc from rising edge	10		ns
t_{10}	Mdc to Mdio (output) Delay Time		300	ns

7.0 AC and DC Electrical Specifications (Continued)

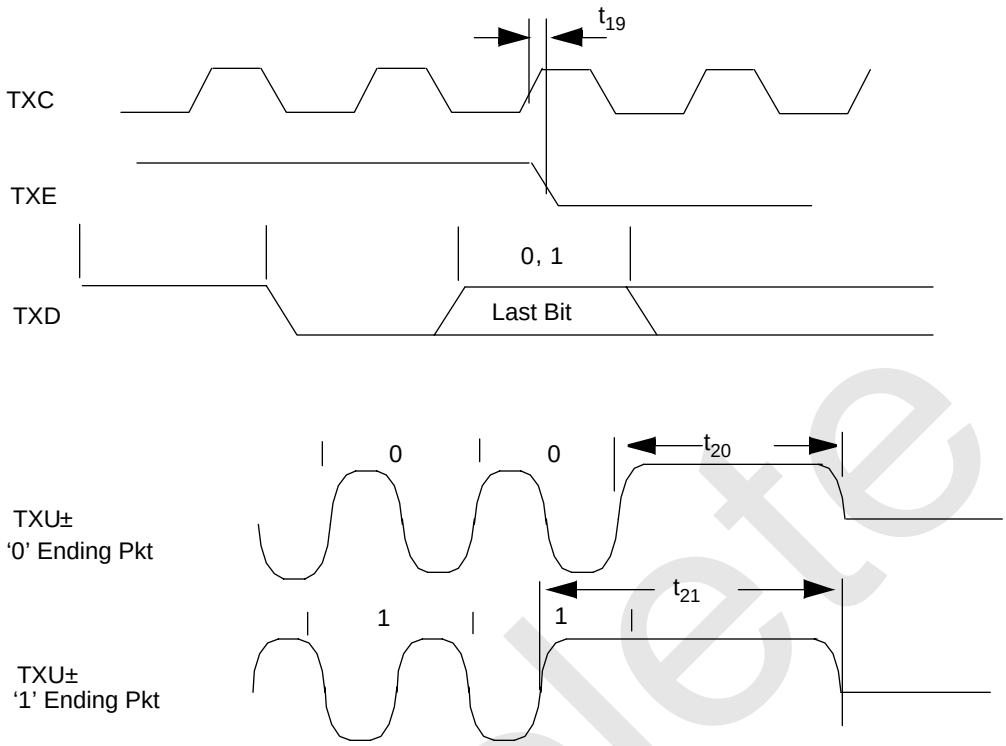
7.2.4 Twisted Pair Start of Transmit Packet



Symbol	Parameter	Min	Max	Units
t_{11}	TXE Setup time to TXC rising edge	20		ns
t_{12}	TXD Setup time to TXC rising edge	20		ns
t_{13}	TXD hold time from TXC rising edge	5		ns
t_{14}	TXU start-up delay from TXC rising edge		400	ns
t_{15}	TXU prop Delay (TXC rising edge to TXU+/-)		350	ns
t_{16}	TXC Low Time	40		ns
t_{17}	TXC High Time	40		ns
t_{18}	TXC Duty Cycle	40	60	%

7.0 AC and DC Electrical Specifications (Continued)

7.2.5 Twisted Pair Transmit End of Packet

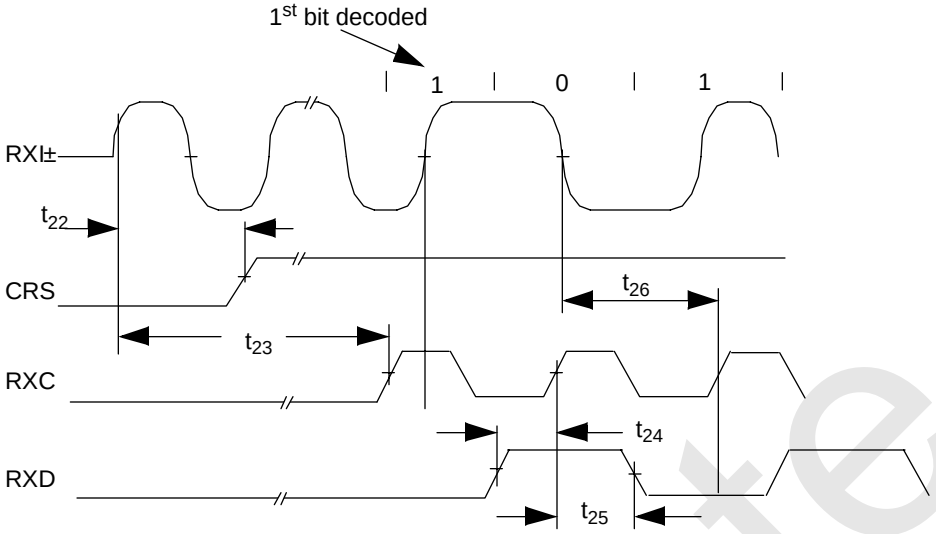


Symbol	Parameter	Min	Max	Units
t_{19}	TXE Hold Time from TXC rising edg	5		ns
t_{20}	TXU End of Packet Hold Time with "0" ending bit	250[1]		ns
t_{21}	TXU End of Packet Hold Time with "1" ending bit	250		ns

1. This is measured between two zero crossings. If measured between a zero crossing and when the differential output voltage falls below 585 mV, then this limit is = 225 ns as per IEEE 802.3 Clause 14 Figure 14-10.

7.0 AC and DC Electrical Specifications (Continued)

7.2.6 Twisted Pair Start of Receive Packet

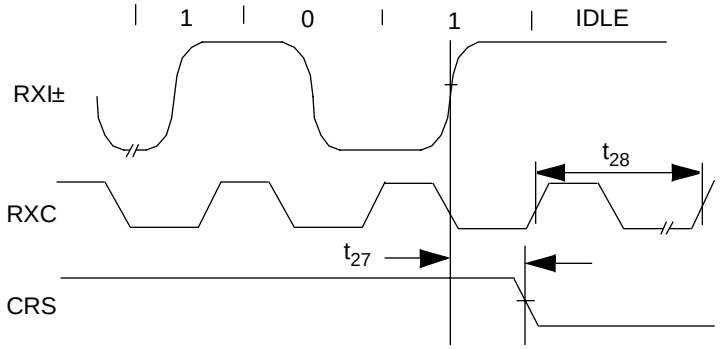


Symbol	Parameter	Min	Max	Units
t_{22}	Carrier Sense Turn On Delay (RXI± to CRS)		550	ns
t_{23}	Decoder Acquisition Time (Note)		2200	ns
t_{24}	Receive Data Valid to RXC rising edge	25		ns
t_{25}	Receive Data Invalid from RXC rising edge	25		ns
t_{26}	Receive Data Bit Delay		400	ns

Note: This parameter includes TPI smart squelch turn on time plus ENDEC data acquisition time.

7.0 AC and DC Electrical Specifications (Continued)

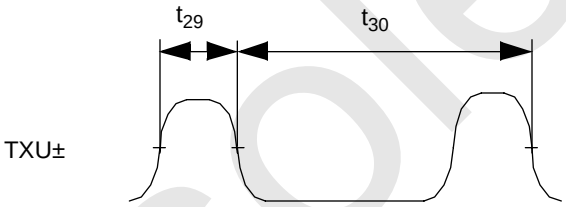
7.2.7 Twisted Pair End of Receive Packet



Symbol	Parameter	Min	Max	Units
t_{27}	Carrier Sense Turn Off Delay		500	ns
t_{28}	Number of RXCs after CRS low [1]	5		Bit Times

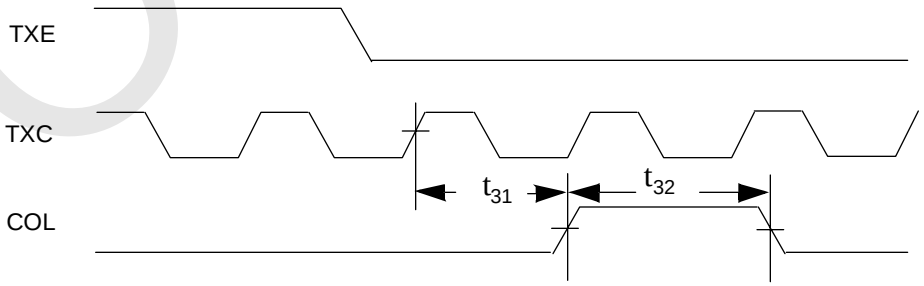
1. This only applies when the GATERXC bit, D0, in the Global Configuration Register is set

7.2.8 Link Pulse Timing



Symbol	Parameter	Min	Max	Units
t_{29}	Link Integrity Output Pulse Width	80	130	ns
t_{30}	Time between Link Output Pulses	8	24	ms

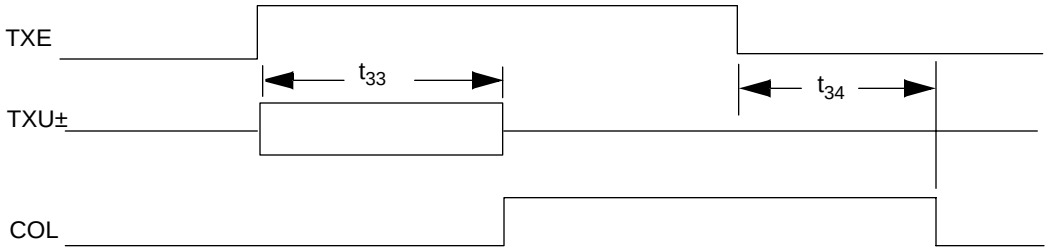
7.2.9 Heartbeat Specifications



Symbol	Parameter	Min	Max	Units
t_{31}	CD Heartbeat Delay	600	1600	ns
t_{32}	CD Heartbeat Duration	500	1500	ns

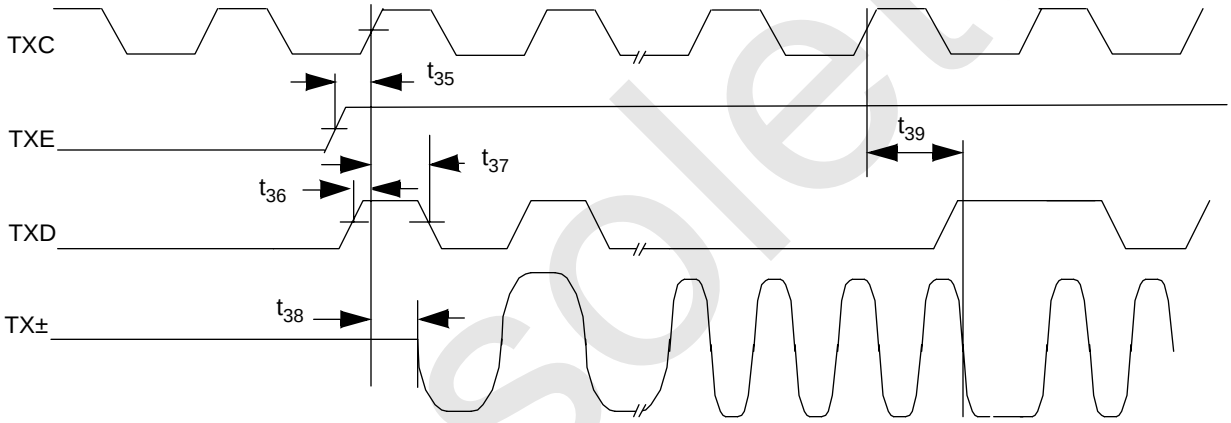
7.0 AC and DC Electrical Specifications (Continued)

7.2.10 Jabber Specifications



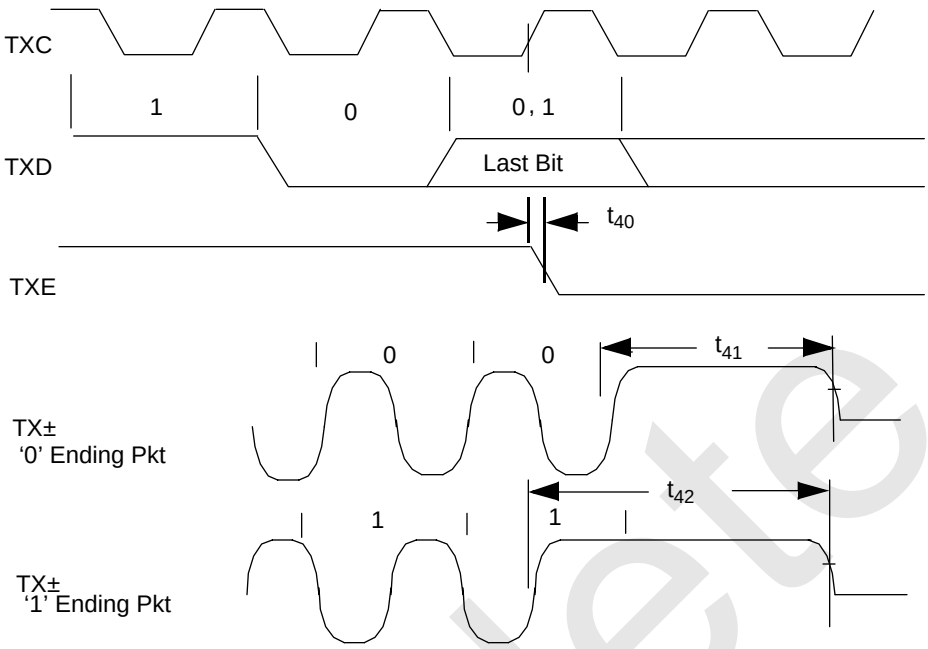
Symbol	Parameter	Min	Max	Units
t_{33}	Jabber Activation Time	20	60	ms
t_{34}	Jabber Deactivation Time	250	750	ms

7.2.11 AUI Start of Packet Transmit Timing



Symbol	Parameter	Min	Max	Units
t_{35}	TXE Setup time to TXC rising edge	20		ns
t_{36}	TXD Setup time to TXC rising edge	20		ns
t_{37}	TXD hold time from TXC rising edge	5		ns
t_{38}	TX+/- Start-up Delay from TXC rising edge		300	ns
t_{39}	TX Prop Delay (TXC rising edge to TX+/-)		300	ns

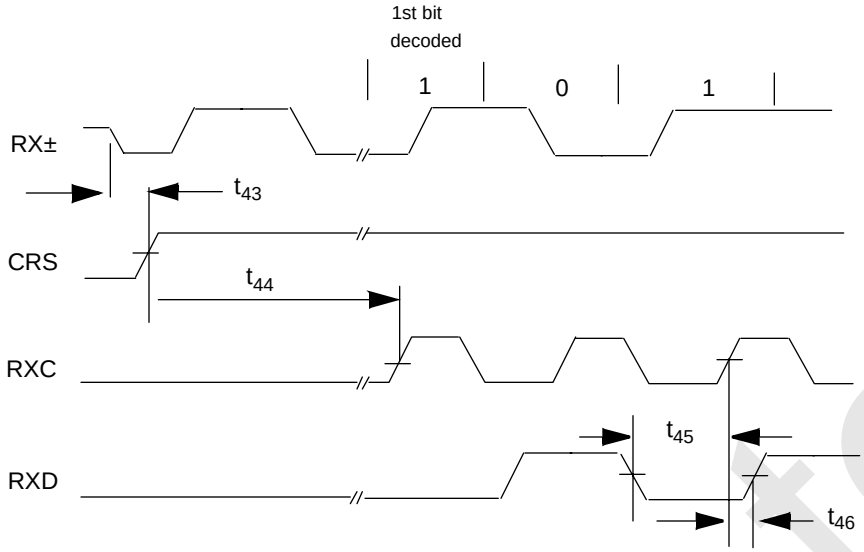
7.2.12 AUI End of Packet Transmit Timing



Symbol	Parameter	Min	Max	Units
t_{40}	TXE Hold Time from TXC rising edg	5		ns
t_{41}	TX End of Packet Hold Time with "0" ending bit	195[1]		ns
t_{42}	TX End of Packet Hold Time with "1" ending bit	195		ns

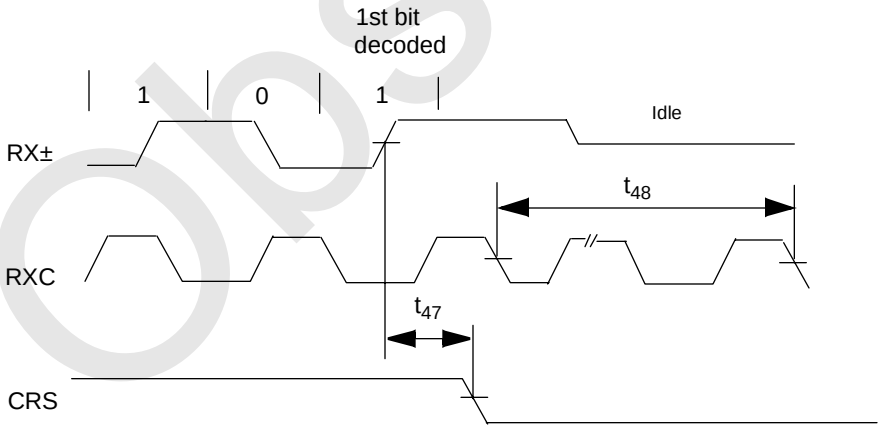
1. This is measured from zero crossing to when the output goes below 380 mV as per IEEE 802.3 page 512.

7.2.13 AUI Start of Packet Receive Timing



Symbol	Parameter	Min	Max	Units
t_{43}	Carrier Sense Turn On Delay (RX± to CRS)		550	ns
t_{44}	Decoder Acquisition Time		2200	ns
t_{45}	Receive Data Valid to RXC Rising Edge	25		ns
t_{46}	Receive Data Invalid from RXC Rising Edge	25		ns

7.2.14 AUI End of Packet Receive Timing

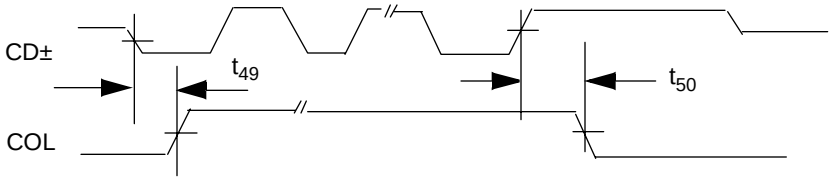


Symbol	Parameter	Min	Max	Units
t_{47}	Carrier Sense Turn Off Delay		500	ns
t_{48}	Number of RXCs after CRS Low[1]	5		Bit Times

1. This only applies when GATERXC, bit D0, in the Global Configuration Register is set.

7.0 AC and DC Electrical Specifications (Continued)

7.2.15 AUI Collision Specifications



Symbol	Parameter	Min	Max	Units
t_{49}	Collision Turn On Delay (CD± to COL)		600	ns
t_{50}	Collision Turn Off Delay (CD± to COL)		900	ns

7.2.16 Network Test Loads

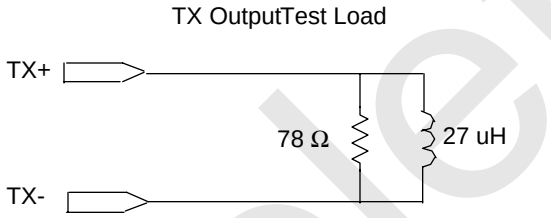


Figure 15. Attachment Unit Interface Load for ATE testing

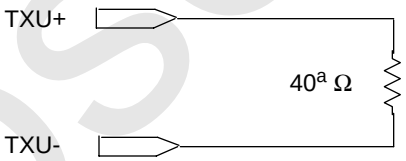


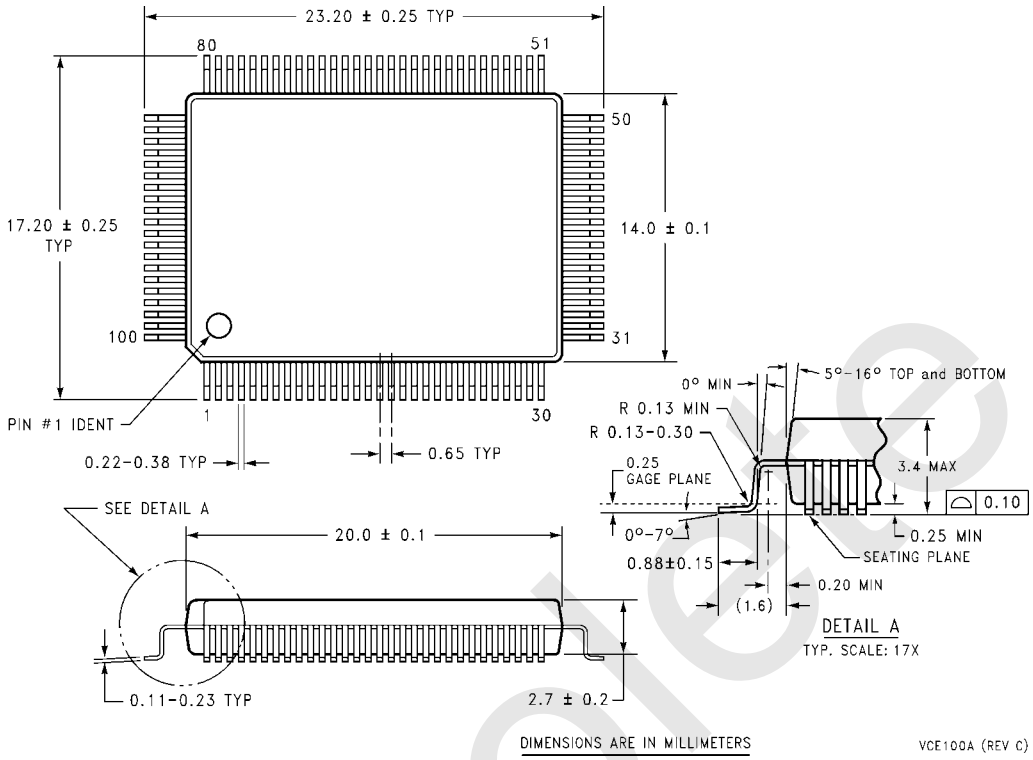
Figure 16. Twisted Pair Interface Load for ATE testing

Note: The 40 Ω load is the effective differential resistance seen by the TXU pins during normal operation. P lease see Figure6 which shows a 1:2 transformer for the TXU pins. Since a 100Ω load on the other side of a 1:2 transformer looks like a 25Ω load to the TXU side of the transformer, the equivalent differential resistance seen by the transmitting port is = 10.5//Zc + 25 + 10.5//Zc ~= 40 Ω where Zc is the impedance of the 1000 pf capacitors. For 10BASE-T frequencies between 5 MHz and 10 MHz this impedance varies between 32 to 16 Ω in // with the 10.5 Ω resistors.

7.2.17 AC Timing Test Condition

Reference	Limits
Input Levels (Digital Pins, $t_R = t_F$ = 3ns)	0 V - 3.0 V
Input/Output Reference Levels (Digital Pins)	1.5 V
Differential Input Reference Levels	2.0 Vpp
Differential Input/Output Reference Levels	50% of Differential

8.0 Physical Dimensions inches (millimeters) unless otherwise noted



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