4018B

PRESETTABLE DIVIDE-BY-N COUNTER

OBSOLETE

DESCRIPTION — The 4018B is a 5-Stage Johnson Counter with a Clock Input (CP), a Data Input (D), an asynchronous Parallel Load Input (PL), five Parallel Inputs (P_0–P_4), five active LOW buffered Outputs ($\overline{Q}_0$–$\overline{Q}_4$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0–P_4) is asynchronously loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Data (D) Inputs. Data present in the counter is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL). When the Parallel Load Input is LOW, the counter advances on the LOW-to-HIGH transition of the Clock Input (CP). By connecting the Outputs ($\overline{Q}_0$–$\overline{Q}_4$) to the Data Input (D), the counter operates as a divide-by-n counter ($2 \leq n \leq 10$); see below.

A HIGH on the Master Reset Input (MR) resets the counter ($\overline{Q}_0$–$\overline{Q}_4$ = HIGH) independent of all other inputs.

- **ASYNCHRONOUS MASTER RESET INPUT (ACTIVE HIGH)**
- **ACTIVE LOW FULLY BUFFERED DECODED OUTPUTS**
- **DIVIDE-BY-N WITH $2 \leq N \leq 10$**
- **CLOCK INPUT L→H EDGE-TRIGGERED**
- **ASYNCHRONOUS PARALLEL LOAD INPUT (ACTIVE HIGH)**

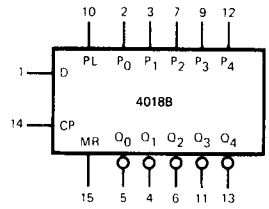
PIN NAMES

PL	Parallel Load Input
P_0–P_4	Parallel Inputs
D	Data Input
CP	Clock Input (L→H Edge-Triggered)
MR	Master Reset Input
$\overline{Q}_0$–$\overline{Q}_4$	Buffered Outputs (Active LOW)

DIVIDE-BY-N MODE SELECTION

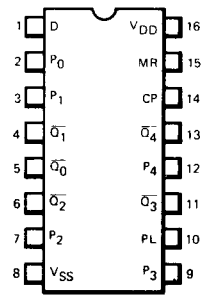
DIVIDE BY	D INPUT
2	$\overline{Q}_0$
3	$\overline{Q}_0 \cdot \overline{Q}_1$
4	$\overline{Q}_1$
5	$\overline{Q}_1 \cdot \overline{Q}_2$
6	$\overline{Q}_2$
7	$\overline{Q}_2 \cdot \overline{Q}_3$
8	$\overline{Q}_3$
9	$\overline{Q}_3 \cdot \overline{Q}_4$
10	$\overline{Q}_4$

LOGIC SYMBOL



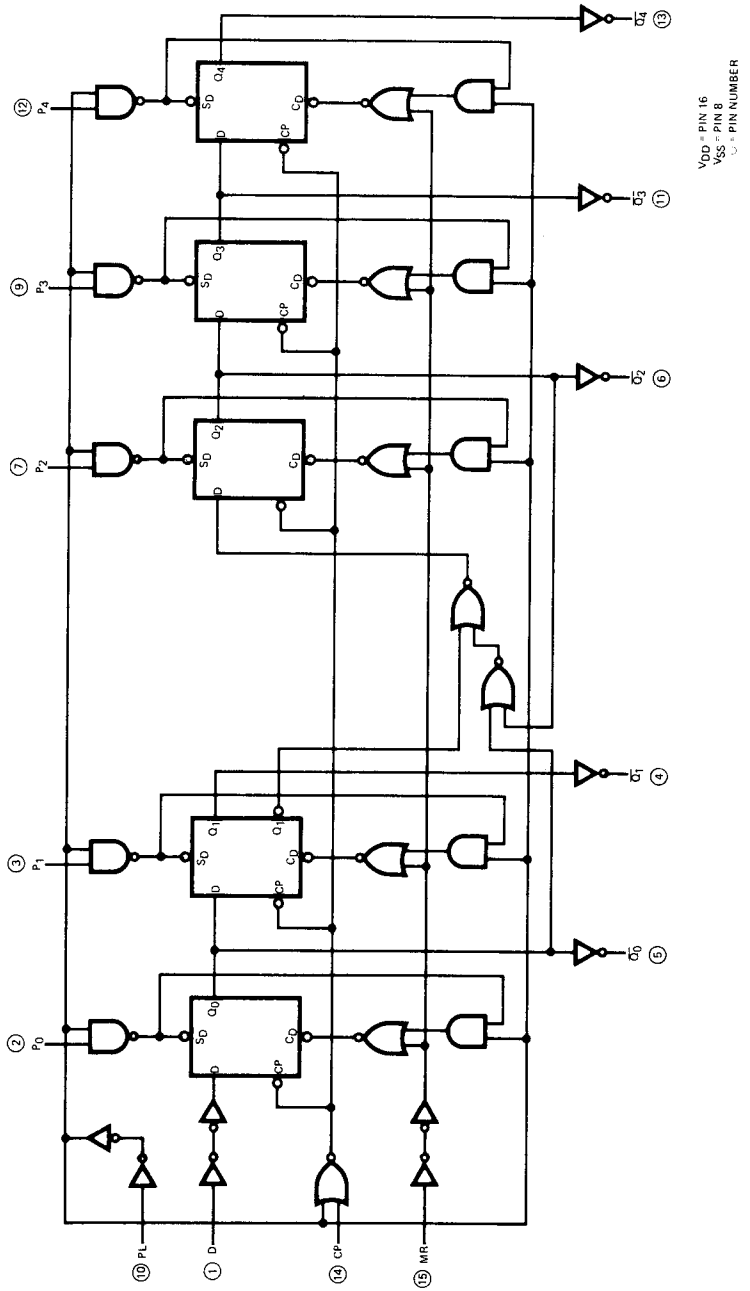
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

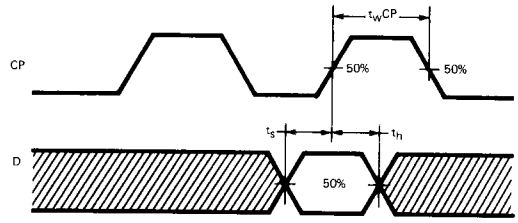
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN. 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN. 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

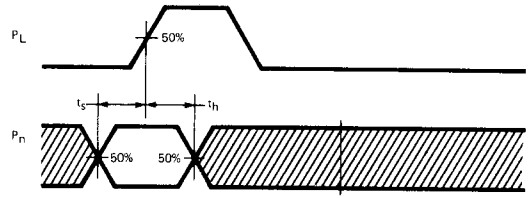
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		280	500		115	200		80	160	ns	C_L = 50 pF, R_L = 200 kΩ, Input Transition Times ⩽ 20 ns
t_{PHL}	CP to $\overline{Qn}$		280	600		115	240		80	170	ns	
t_{PLH}	Propagation Delay, MR to $\overline{Qn}$		280	600		115	240		80	170	ns	
t_{PLH}	Propagation Delay,		280	600		115	240		80	170	ns	
t_{PHL}	PL to $\overline{Qn}$		280	740		115	300		80	200	ns	
t_{TLH}	Output Transition		59	135		31	75		23	45	ns	
t_{THL}	Time		63	135		26	75		19	45	ns	
t_{rec}	MR Recovery Time	250	150		110	50		90	40		ns	
t_WMR	MR Minimum Pulse Width	130	65		60	30		48	22		ns	
t_WCP	CP Minimum Pulse Width	260	100		130	50		100	40		ns	
t_s	Set-Up Time, D to CP	175	85		75	25		60	35		ns	
t_h	Hold Time, D to CP		0			0			0		ns	
t_s	Set-Up Time, Pn to PL	175	85		75	25		60	35		ns	
t_h	Hold Time, Pn to PL		0			0			0		ns	
f_{MAX}	Input Count Frequency (Note 3)	1.5	3		3.5	8		4.5	10		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

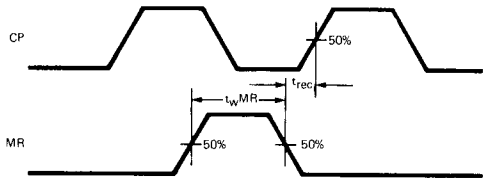
SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D TO CP



SET-UP AND HOLD TIMES, P_n to PL



MR RECOVERY TIME AND MINIMUM MR PULSE WIDTH

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.