STGW35NC60WD

40 A, 600 V ultra fast IGBT

Features

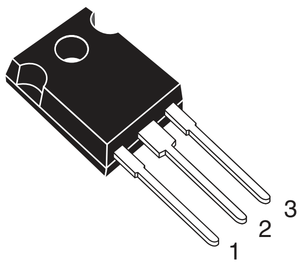
- High frequency operation
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode

Applications

- High frequency motor controls, inverters, UPS
- HF, SMPS and PFC in both hard switch and resonant topologies

Description

This IGBT utilizes the advanced Power MESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.



TO-247 long leads

Figure 1. Internal schematic diagram

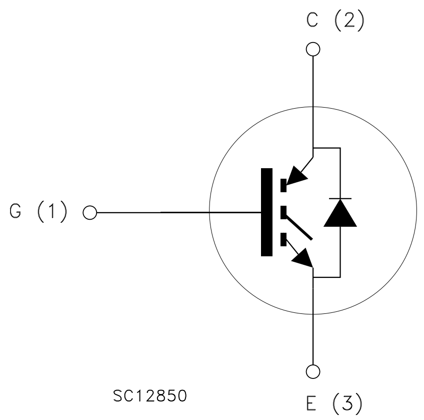


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW35NC60WD	GW35NC60WD	TO-247 long leads	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0)	600	V
I_C (1)	Collector current (continuous) at 25 °C	70	A
I_C (1)	Collector current (continuous) at 100 °C	40	A
I_{CP}(2)	Collector current (pulsed)	150	A
I_{CL} (3)	Turn-off latching current	150	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Diode RMS forward current at T_C = 25 °C	30	A
I_{FSM}	Surge not repetitive forward current t_p= 10 ms sinusoidal	120	A
P_{TOT}	Total dissipation at T_C = 25 °C	260	W
T_{stg}	Storage temperature	– 55 to 150	°C
T_j	Operating junction temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

2. Pulse width limited by max junction temperature
3. V_{CLAMP} = 80% (V_{CES}), V_{GE} = 15 V, R_G = 10 Ω, T_J = 150 °C

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case IGBT max.	0.48	°C/W
	Thermal resistance junction-case diode max.	1.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.	50	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage (V_{GE} = 0)	I_C = 1 mA	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C= 20 A V_{GE} = 15 V, I_C = 20 A,T_C= 125 °C		2.2 1.8	2.6	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 250 µA	3.75		5.75	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE} = 600 V V_{CE} = 600 V, T_C = 125 °C			250 1	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} = ±20 V			± 100	nA
g_{fs}	Forward transconductance	V_{CE} = 15 V, I_C = 20 A		15		S

Table 5. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0		2080 175 52		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390 V, I_C = 20 A, V_{GE} = 15 V, *(see Figure 18)*		102 17.5 47	140	nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390 V, I_C = 20 A R_G = 10 Ω, V_{GE} = 15 V, *(see Figure 17)*		29.5 12 1640		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390 V, I_C = 20 A R_G = 10 Ω, V_{GE} = 15 V, T_C = 125 °C *(see Figure 17)*		29 13.5 1600		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390 V, I_C = 20 A, R_{GE} = 10 Ω, V_{GE} = 15 V *(see Figure 17)*		19.5 118 27		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390 V, I_C = 20 A, R_{GE} = 10 Ω, V_{GE} =15 V, T_C = 125 °C *(see Figure 17)*		46 151 38		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on} (1) E_{off} E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390 V, I_C = 20 A R_G = 10 Ω, V_{GE} = 15 V, *(see Figure 19)*		305 181 486		µJ µJ µJ
E_{on} (1) E_{off} E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390 V, I_C = 20 A R_G = 10 Ω, V_{GE} = 15 V, T_C = 125°C *(see Figure 19)*		455 355 810		µJ µJ µJ

1. Eon is the tun-on losses when a typical diode is used in the test circuit in *Figure 19*. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C). Eon include diode recovery energy.

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on-voltage	I_F = 20 A I_F = 20 A, T_C = 125 °C		2.6 1.6		V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 20 A,V_R = 50 V, di/dt = 100 A/µs *(see Figure 20)*		40 50 2.5		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 20 A,V_R = 50 V, T_C =125 °C, di/dt = 100 A/µs *(see Figure 20)*		80 180 4.5		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

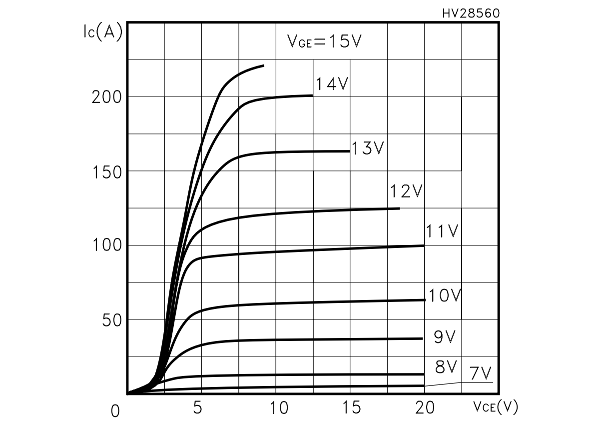


Figure 3. Transfer characteristics

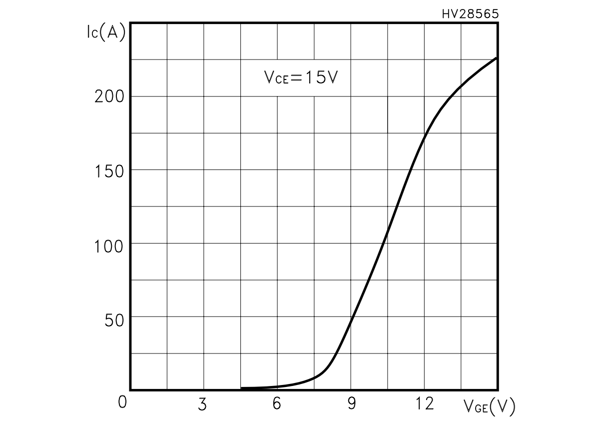


Figure 4. Transconductance

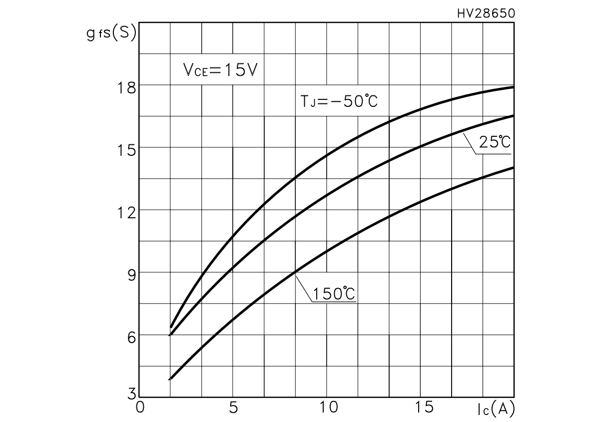


Figure 5. Collector-emitter on voltage vs temperature

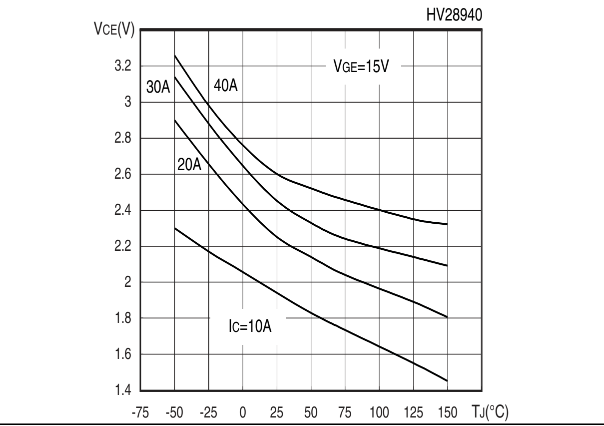


Figure 6. Gate charge vs gate-source voltage

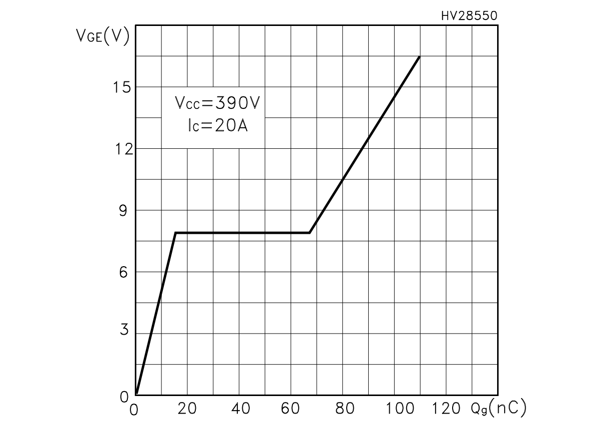


Figure 7. Capacitance variations

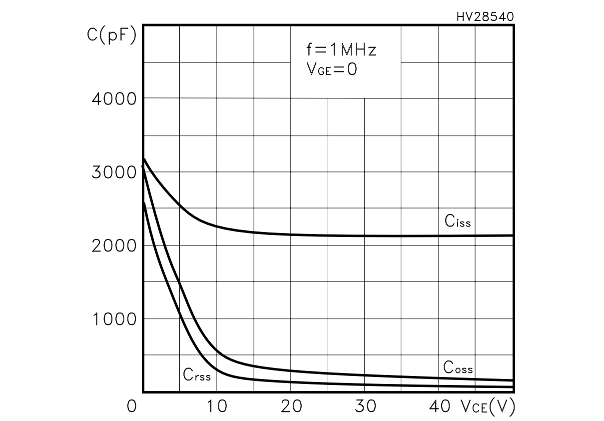


Figure 8. Normalized gate threshold voltage vs temperature

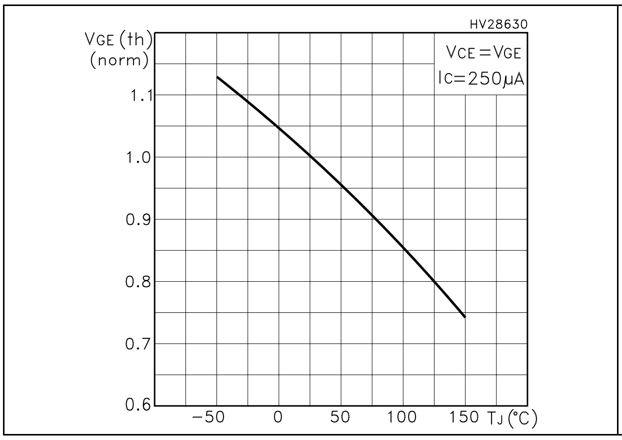


Figure 9. Collector-emitter on voltage vs collector current

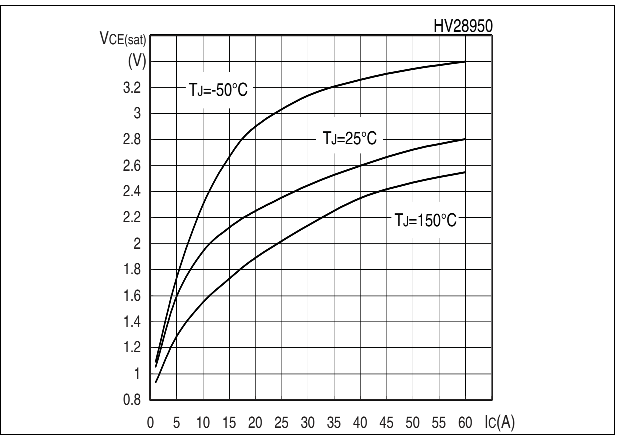


Figure 10. Normalized breakdown voltage vs temperature

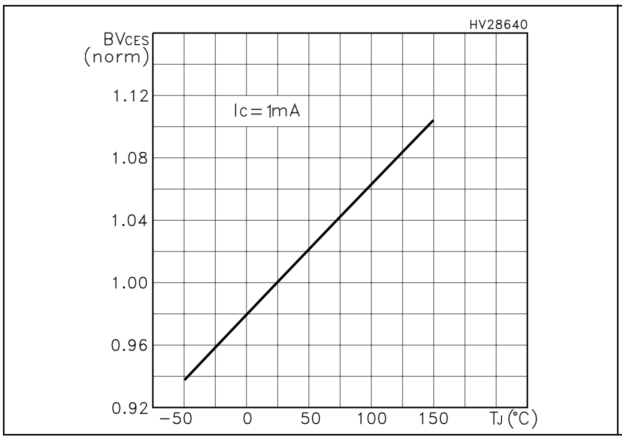


Figure 11. Switching losses vs temperature

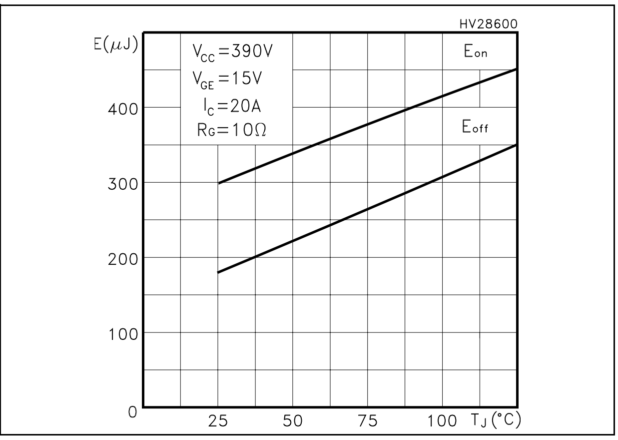


Figure 12. Switching losses vs gate resistance

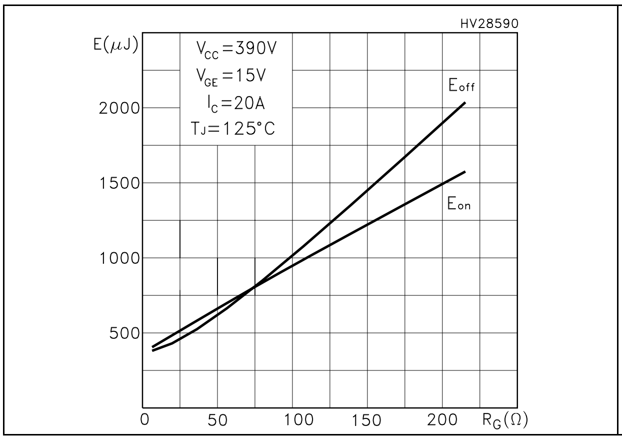


Figure 13. Switching losses vs collector current

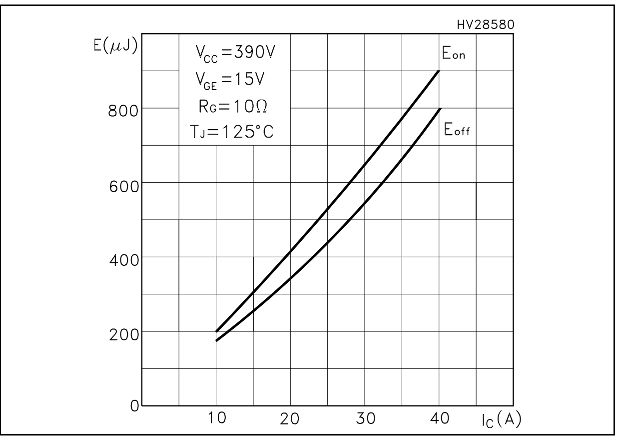


Figure 14. Thermal impedance

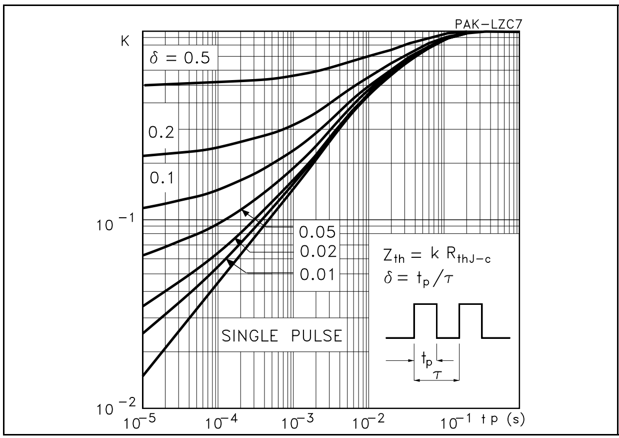


Figure 15. Turn-off SOA

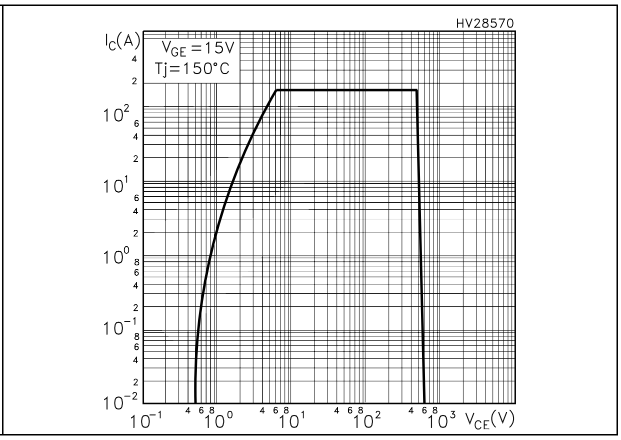
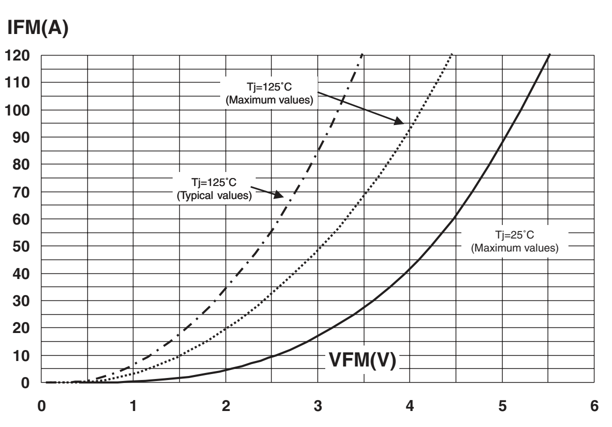


Figure 16. Emitter-collector diode characteristics



3 Test circuit

Figure 17. Test circuit for inductive load switching

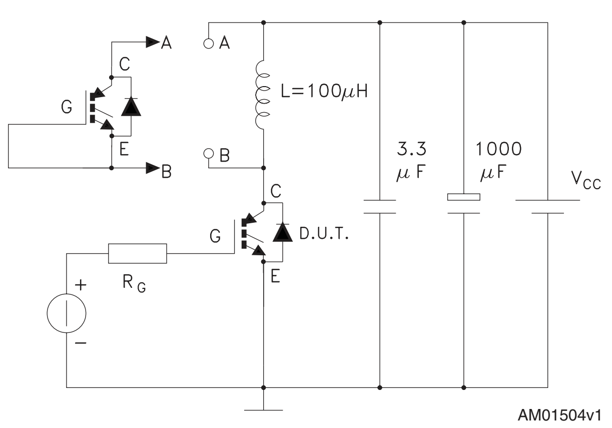


Figure 18. Gate charge test circuit

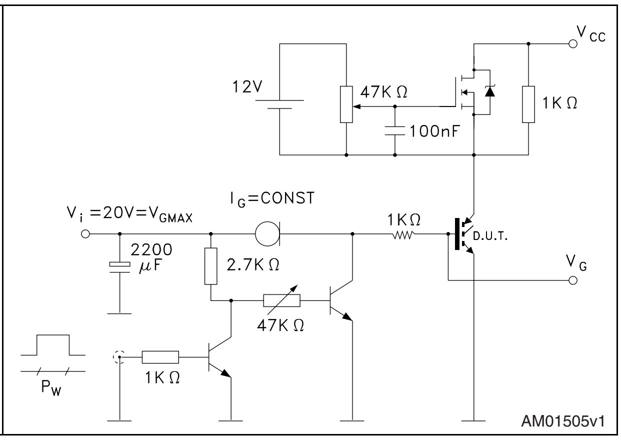


Figure 19. Switching waveform

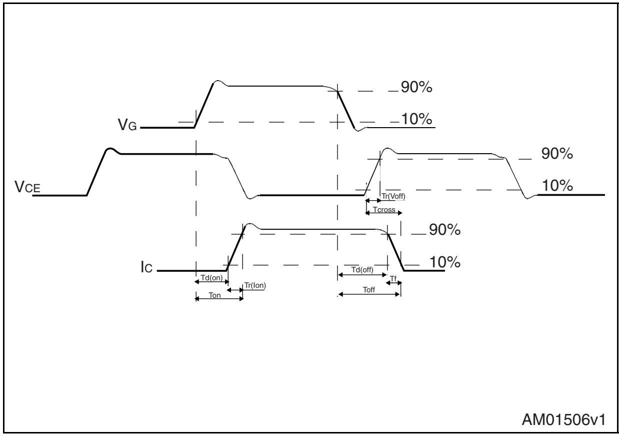
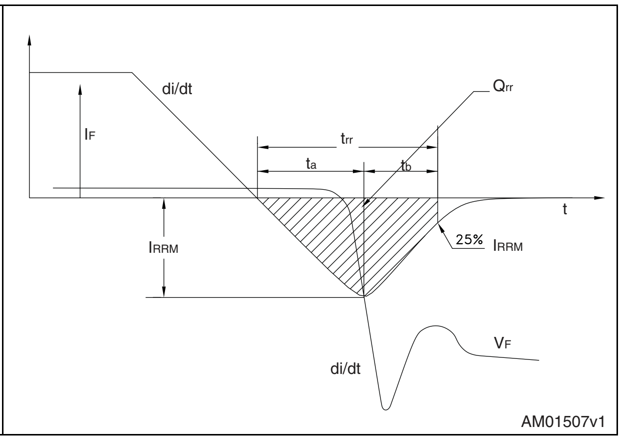


Figure 20. Diode recovery time waveform

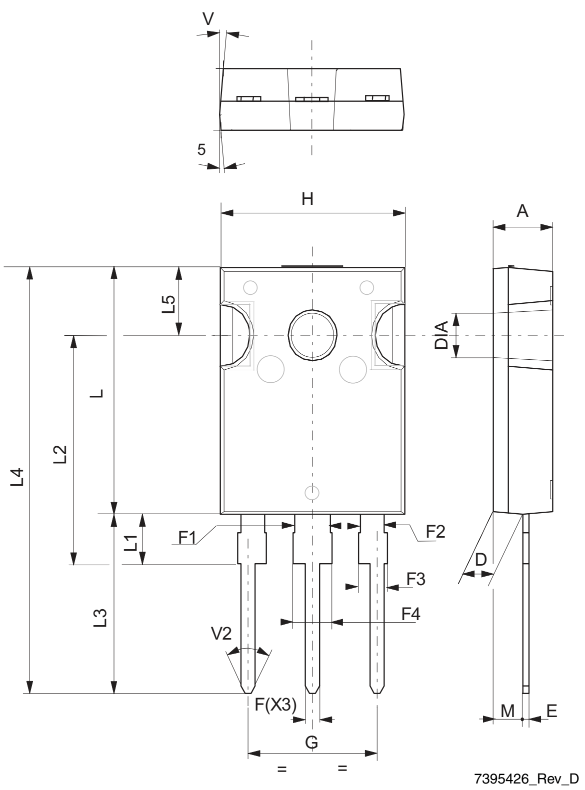


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 long leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.16
D	2.2		2.6
E	0.4		0.8
F	1		1.4
F1		3	
F2		2	
F3	1.9		2.4
F4	3		3.4
G		10.9	
H	15.45		16.03
L	19.85		21.09
L1	3.7		4.3
L2	18.3		19.13
L3	14.2		20.3
L4	34.05		41.38
L5	5.35		6.3
M	2		3
V		5°	
V2		60°	
DIAM	3.55		3.65



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Jul-2007	1	Initial release.
11-Nov-2008	2	Document status promoted from preliminary data to datasheet.