

# 74LVTH646

## Low Voltage Octal Transceiver/Register with 3-STATE Outputs

### General Description

The LVTH646 consists of registered bus transceiver circuits, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). (See Functional Description)

The LVTH646 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The bus transceivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

### Features

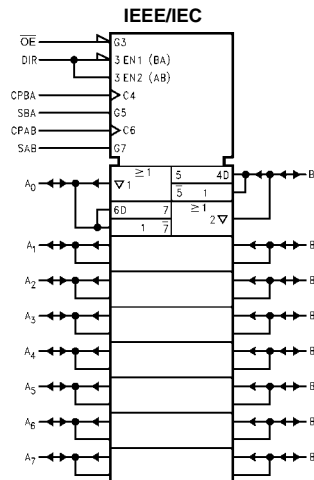
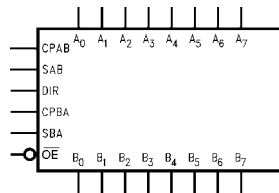
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 646
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

### Ordering Code:

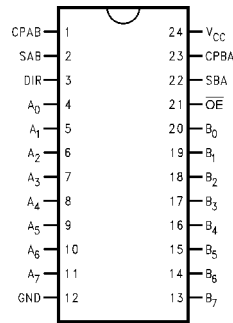
Order Number	Package Number	Package Description
74LVTH646WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LVTH646MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending letter suffix "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

### Truth Table

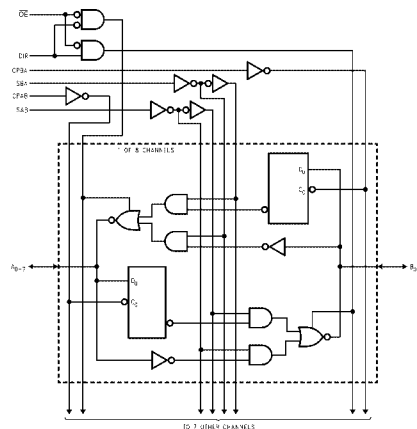
(Note 1)

Inputs						Data I/O		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X			Isolation
H	X	↗	X	X	X	Input	Input	Clock A <sub>n</sub> Data into A Register Clock B <sub>n</sub> Data into B Register
H	X	X	↗	X	X			
L	H	X	X	L	X			A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	↗	X	L	X	Input	Output	Clock A <sub>n</sub> Data into A Register A Register to B <sub>n</sub> (Stored Mode)
L	H	H or L	X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	H	↗	X	H	X			
L	L	X	X	X	L			B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	↗	X	L	Output	Input	Clock B <sub>n</sub> Data into B Register B Register to A <sub>n</sub> (Stored Mode)
L	L	X	H or L	X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>
L	L	X	↗	X	H			

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↗ = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

### Logic Diagram

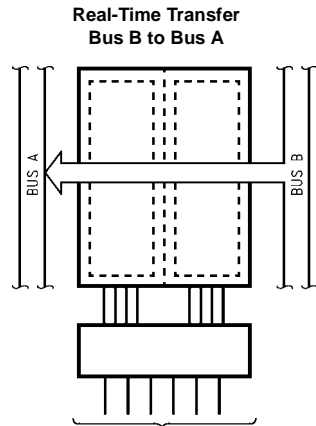


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

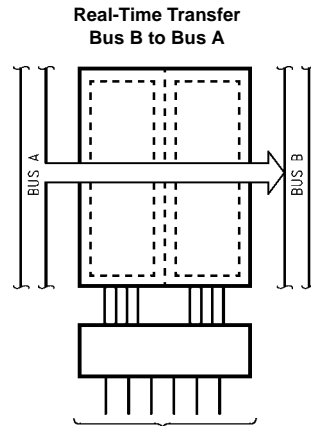
## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time. The examples below demonstrate the four fundamental bus-management functions that can be performed.

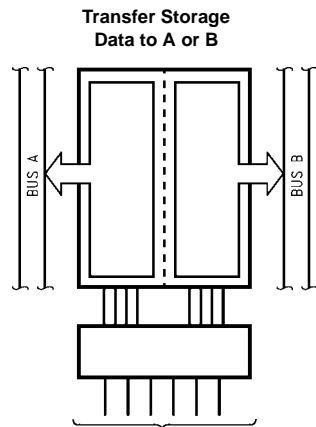
The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is LOW. In the isolation mode ( $\overline{OE}$  HIGH), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time.



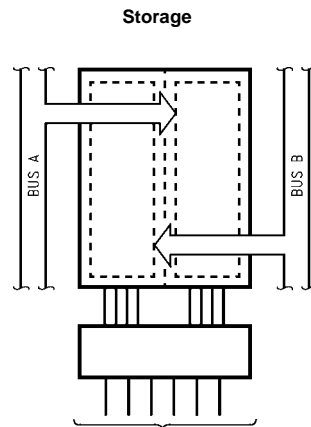
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	↗	X	L	X
L	L	X	↖	X	L
H	X	↗	X	X	X
H	X	X	↖	X	X

**Absolute Maximum Ratings**(Note 2)

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}C$

**Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH Level Output Current		-32	mA
$I_{OL}$	LOW Level Output Current		64	
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

**Note 2:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

DC Electrical Characteristics							
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions	
			Min	Max			
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7		-1.2	V	I <sub>I</sub> = -18 mA	
V <sub>IH</sub>	Input HIGH Voltage	2.7-3.6	2.0		V	V <sub>O</sub> ≤ 0.1V or V <sub>O</sub> ≥ V <sub>CC</sub> - 0.1V	
V <sub>IL</sub>	Input LOW Voltage	2.7-3.6		0.8	V		
V <sub>OH</sub>	Output HIGH Voltage	2.7-3.6	V <sub>CC</sub> - 0.2		V	I <sub>OH</sub> = -100 μA	
		2.7	2.4		V	I <sub>OH</sub> = -8 mA	
		3.0	2.0		V	I <sub>OH</sub> = -32 mA	
V <sub>OL</sub>	Output LOW Voltage	2.7		0.2	V	I <sub>OL</sub> = 100 μA	
		2.7		0.5	V	I <sub>OL</sub> = 24 mA	
		3.0		0.4	V	I <sub>OL</sub> = 16 mA	
		3.0		0.5	V	I <sub>OL</sub> = 32 mA	
		3.0		0.55	V	I <sub>OL</sub> = 64 mA	
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive	3.0	75		μA	V <sub>I</sub> = 0.8V	
			-75		μA	V <sub>I</sub> = 2.0V	
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 4)	
			-500		μA	(Note 5)	
I <sub>I</sub>	Input Current	3.6		10	μA	V <sub>I</sub> = 5.5V	
		Control Pins	3.6		±1	μA	V <sub>I</sub> = 0V or V <sub>CC</sub>
		Data Pins	3.6		-5	μA	V <sub>I</sub> = 0V
I <sub>OFF</sub>	Power Off Leakage Current	0		±100	μA	V <sub>I</sub> = V <sub>CC</sub>	
					±100	μA	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V
I <sub>PU/PD</sub>	Power up/down 3-STATE Output Current	0-1.5V		±100	μA	V <sub>O</sub> = 0.5V to 3.0V V <sub>I</sub> = GND or V <sub>CC</sub>	
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6		-5	μA	V <sub>O</sub> = 0.0V	
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6		5	μA	V <sub>O</sub> = 3.6V	
I <sub>OZH+</sub>	3-STATE Output Leakage Current	3.6		10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V	
I <sub>CCH</sub>	Power Supply Current	3.6		0.19	mA	Outputs HIGH	
I <sub>CCL</sub>	Power Supply Current	3.6		5	mA	Outputs LOW	
I <sub>CCZ</sub>	Power Supply Current	3.6		0.19	mA	Outputs Disabled	
I <sub>CCZ+</sub>	Power Supply Current	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V Outputs Disabled	
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 6)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND	

**Note 4:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 5:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 6:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

### Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 8)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 8)

**Note 7:** Characterized in SOIC package. Guaranteed parameter, but not tested.

**Note 8:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				Units
		$C_L = 50\text{ pF}, R_L = 500\Omega$				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
Min	Max	Min	Max			
$t_{MAX}$	Maximum Clock Frequency	150		150		MHz
$t_{PLH}$	Propagation Delay Data to Output	1.8	5.7	1.8	6.3	ns
$t_{PHL}$	Clock to A or B	1.8	5.0	1.8	5.6	
$t_{PLH}$	Propagation Delay Data to Output	1.3	4.6	1.3	5.0	ns
$t_{PHL}$	Data to A or B	1.3	4.6	1.3	5.3	
$t_{PLH}$	Propagation Delay Data to Output	1.5	5.5	1.5	6.5	ns
$t_{PHL}$	SBA or SAB to A or B	1.5	5.5	1.5	6.3	
$t_{PZH}$	Output Enable Time	1.1	5.7	1.1	6.8	ns
$t_{PZL}$	OE to A or B	1.1	6.3	1.1	7.3	
$t_{PHZ}$	Output Disable Time	1.9	5.7	2.3	6.1	ns
$t_{PLZ}$	OE to A or B	1.6	5.5	2.3	5.9	
$t_{PZH}$	Output Enable Time	1.3	6.1	1.3	6.7	ns
$t_{PZL}$	DIR to A or B	1.3	6.7	1.3	7.7	
$t_{PHZ}$	Output Disable Time	1.5	6.2	1.5	7.1	ns
$t_{PLZ}$	DIR to A or B	1.5	5.6	1.5	6.3	
$t_W$	Pulse Duration	Clock HIGH or LOW		3.3		ns
$t_S$	Setup Time	A or B Before Clock, Data HIGH		1.2	1.5	ns
		A or B Before Clock, Data LOW		1.6	2.2	
$t_H$	Hold Time	A or B after Clock		0.8	0.8	ns
$t_{OSHL}$	Output to Output Skew (Note 9)		1.0		1.0	ns
$t_{OSLH}$			1.0		1.0	

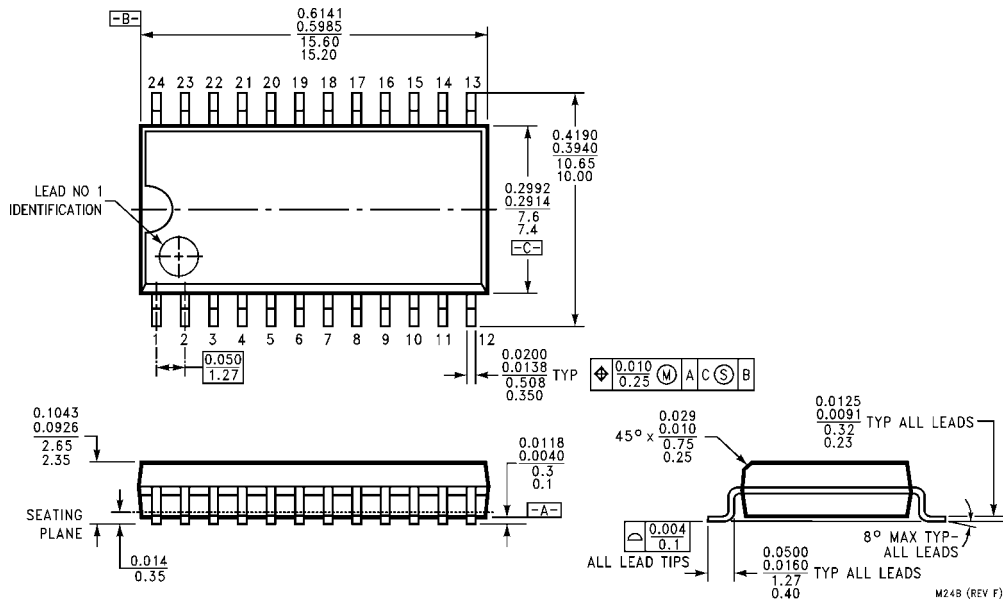
**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

## Capacitance (Note 10)

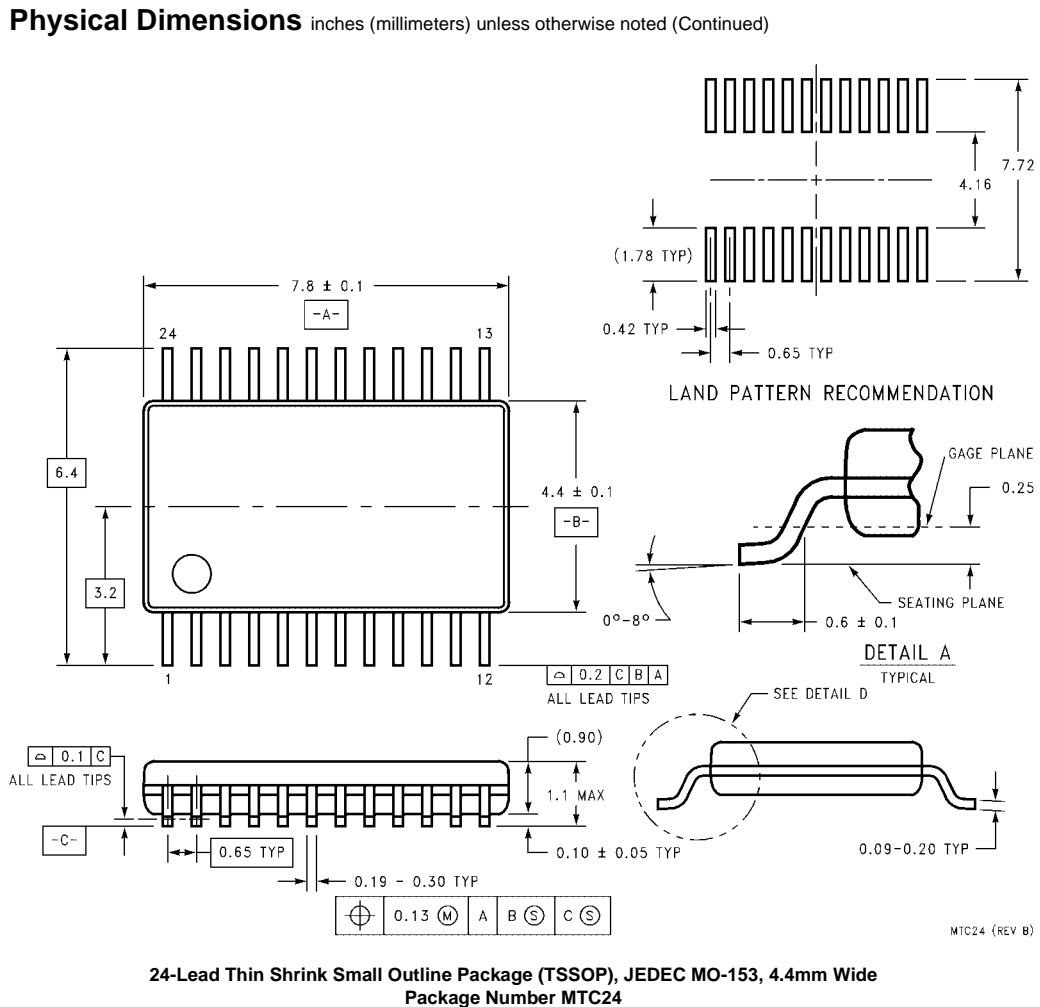
Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 0V, V_I = 0V$ or $V_{CC}$	4	pF
$C_{IO}$	Input/Output Capacitance	$V_{CC} = 3.0V, V_O = 0V$ or $V_{CC}$	8	pF

**Note 10:** Capacitance is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**



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