

## 3.3V ECL/PECL/HSTL/LVDS $\div 2/4$ , $\div 4/5/6$ Clock Generation Chip

The MC100ES6139 is a low skew  $\div 2/4$ ,  $\div 4/5/6$  clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the  $V_{BB}$  output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the  $V_{BB}$  output should be connected to the  $\overline{CLK}$  input and bypassed to ground via a 0.01  $\mu\text{F}$  capacitor.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

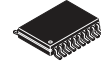
Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple ES6139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one ES6139, the MR pin need not be exercised as the internal divider design ensures synchronization between the  $\div 2/4$  and the  $\div 4/5/6$  outputs of a single device. All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to power supply to guarantee proper operation.

The 100ES Series contains temperature compensation.

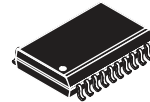
### Features

- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range:  $V_{CC} = 3.135 \text{ V to } 3.8 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- ECL Mode Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -3.135 \text{ V to } -3.8 \text{ V}$
- Open Input Default State
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- $V_{BB}$  Output
- LVDS and HSTL Input Compatible

## MC100ES6139



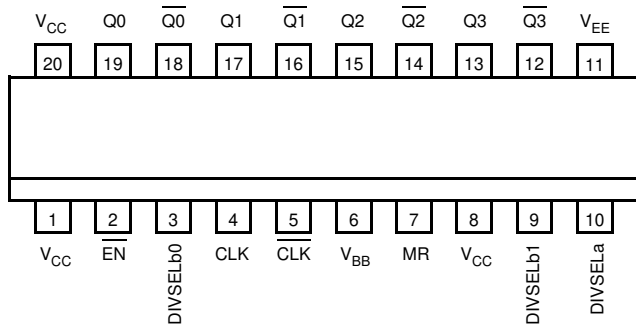
**DT SUFFIX**  
20 LEAD TSSOP PACKAGE  
CASE 948E-02



**DW SUFFIX**  
20 LEAD SOIC PACKAGE  
CASE 751D-06

### ORDERING INFORMATION

Device	Package
MC100ES6139DT	TSSOP-20
MC100ES6139DTR2	TSSOP-20
MC100ES6139DW	SO-20
MC100ES6139DWR2	SO-20



Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. Pin Description

Pin	Function
CLK <sup>1</sup> , $\overline{\text{CLK}}^1$	ECL Diff Clock Inputs
$\overline{\text{EN}}^1$	ECL Sync Enable
MR <sup>1</sup>	ECL Master Reset
V <sub>BB</sub>	ECL Reference Output
Q0, Q1, $\overline{\text{Q0}}$ , $\overline{\text{Q1}}$	ECL Diff ÷2/4 Outputs
Q2, Q3, $\overline{\text{Q2}}$ , $\overline{\text{Q3}}$	ECL Diff ÷4/5/6 Outputs
DIVSELa <sup>1</sup>	ECL Freq. Select Input ÷2/4
DIVSELb0 <sup>1</sup>	ECL Freq. Select Input ÷4/5/6
DIVSELb1 <sup>1</sup>	ECL Freq. Select Input ÷4/5/6
V <sub>CC</sub>	ECL Positive Supply
V <sub>EE</sub>	ECL Negative Supply

1. Pins will default low when left open.

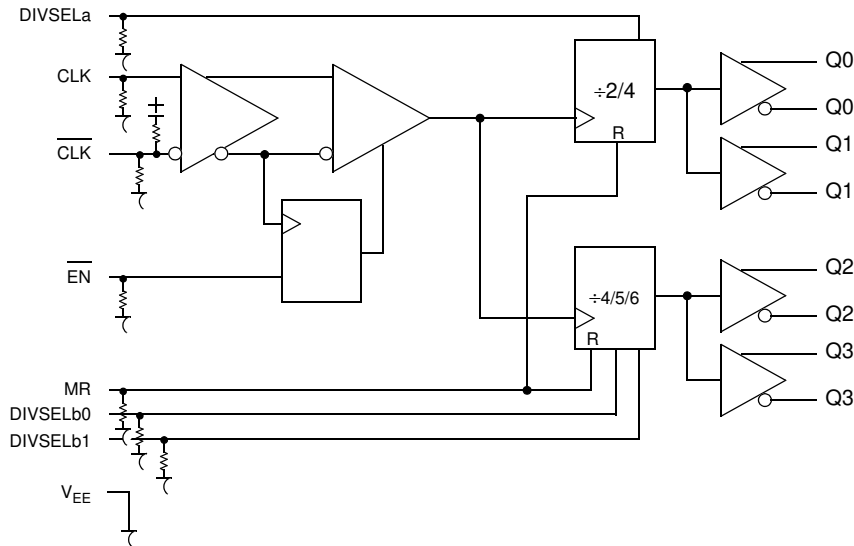


Figure 2. Logic Diagram

Table 2. Function Tables

CLK	$\overline{\text{EN}}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

X = Don't Care  
 Z = Low-to-High Transition  
 ZZ = High-to-Low Transition

DIVSELa		Q0:1 Outputs
L		Divide by 2
H		Divide by 4
DIVSELb0	DIVSELb1	Q2:3 Outputs
L	L	Divide by 4
H	L	Divide by 6
L	H	Divide by 5
H	H	Divide by 5

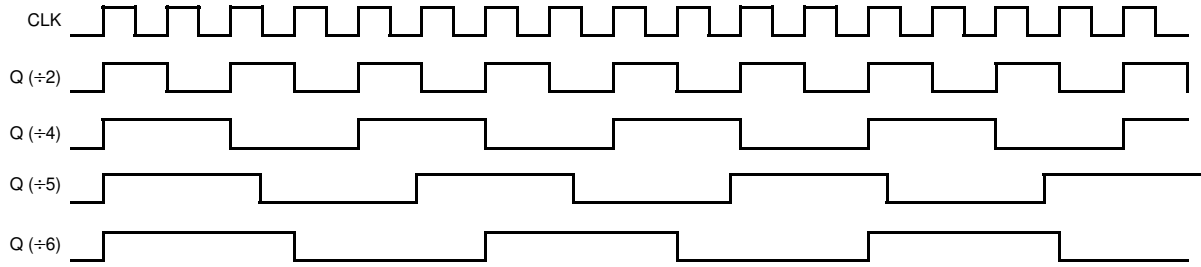


Figure 3. Timing Diagram

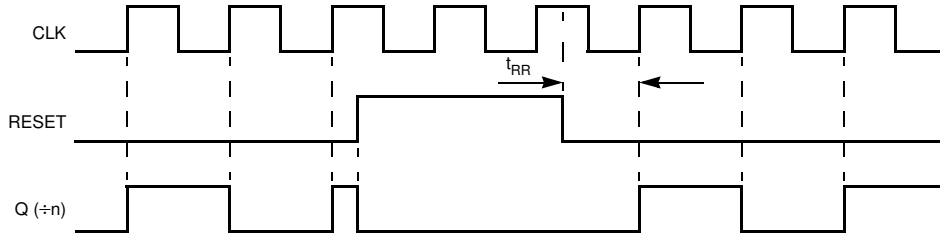


Figure 4. Timing Diagram

Table 3. Attributes

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model	> 4 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

## MC100ES6139

**Table 4. Maximum Ratings<sup>1</sup>**

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		3.9	V
V <sub>EE</sub>	ECL Mode Power Supply	V <sub>CC</sub> = 0 V		-3.9	V
V <sub>I</sub>	PECL Mode Input Voltage ECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	3.9 -3.9	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	74 64	°C/W °C/W
		0 LFPM 500 LFPM	20 SOIC 20 SOIC	TBD TBD	°C/W °C/W

1. Maximum Ratings are those values beyond which device damage may occur.

**Table 5. DC Characteristics** (V<sub>CC</sub> = 0 V, V<sub>EE</sub> = -3.8 V to -3.135 V or V<sub>CC</sub> = 3.135 V to 3.8 V, V<sub>EE</sub> = 0 V)<sup>1</sup>

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		35	60		35	60	mA
V <sub>OH</sub>	Output HIGH Voltage <sup>2</sup>	V <sub>CC</sub> -1150	V <sub>CC</sub> -1020	V <sub>CC</sub> -800	V <sub>CC</sub> -1200	V <sub>CC</sub> -970	V <sub>CC</sub> -750	mV
V <sub>OL</sub>	Output LOW Voltage <sup>2</sup>	V <sub>CC</sub> -1950	V <sub>CC</sub> -1620	V <sub>CC</sub> -1250	V <sub>CC</sub> -2000	V <sub>CC</sub> -1680	V <sub>CC</sub> -1300	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	V <sub>CC</sub> -1165		V <sub>CC</sub> -880	V <sub>CC</sub> -1165		V <sub>CC</sub> -880	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	V <sub>CC</sub> -1810		V <sub>CC</sub> -1475	V <sub>CC</sub> -1810		V <sub>CC</sub> -1475	mV
V <sub>BB</sub>	Output Reference Voltage	V <sub>CC</sub> -1400		V <sub>CC</sub> -1200	V <sub>CC</sub> -1400		V <sub>CC</sub> -1200	mV
V <sub>PP</sub>	Differential Input Voltage <sup>3</sup>	0.12		1.3	0.12		1.3	V
V <sub>CMR</sub>	Differential Cross Point Voltage <sup>4</sup>	V <sub>EE</sub> +0.2		V <sub>CC</sub> -1.1	V <sub>EE</sub> +0.2		V <sub>CC</sub> -1.1	V
I <sub>IH</sub>	Input HIGH Current			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			μA

- MC100ES6139 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.
- All loading with 50 Ω to V<sub>CC</sub>-2.0 volts.
- V<sub>PP</sub> (DC) is the minimum differential input voltage swing required to maintain device functionality.
- V<sub>CMR</sub> (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V<sub>CMR</sub> (DC) range and the input swing lies within the V<sub>PP</sub> (DC) specification.

Table 6. AC Characteristics ( $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.8\text{ V}$  to  $-3.135\text{ V}$  or  $V_{CC} = 3.135\text{ V}$  to  $3.8\text{ V}$ ,  $V_{EE} = 0\text{ V}$ )<sup>1</sup>

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency		> 1			> 1			> 1		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay CLK, Q (Diff) MR, Q	550 400		850 850	550 400		850 850	550 400		850 850	ps
$t_{RR}$	Reset Recovery	200	100		200	100		200	100		ps
$t_s$	Setup Time $\overline{EN}$ , $\overline{CLK}$ DIVSEL, CLK	200 400	120 180		200 400	120 180		200 400	120 180		ps
$t_h$	Hold Time $\overline{CLK}$ , $\overline{EN}$ CLK, DIVSEL	100 200	50 140		100 200	50 140		100 200	50 140		ps
$t_{PW}$	Minimum Pulse Width MR	550	450		550	450		550	450		ps
$t_{SKEW}$	Within Device Skew Q, $\overline{Q}$ Q, $\overline{Q}$ @ Same Frequency Device-to-Device Skew <sup>2</sup>			100 50 300			100 50 300			100 50 300	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter (RSM $1\sigma$ )			1			1			1	ps
$V_{PP}$	Input Voltage Swing (Differential)	200		1200	200		1200	200		1200	mV
$V_{CMR}$	Differential Cross Point Voltage	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	V
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$	50		300	50		300	50		300	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

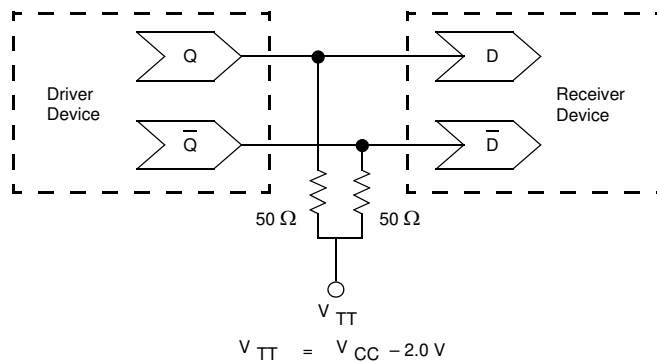


Figure 5. Typical Termination for Output Driver and Device Evaluation

# Freescale Semiconductor, Inc.

## MC100ES6139

### Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6139DT	6139	
MC100ES6139DW		MC100ES6139

### Trace Code Identification for 20 SOIC: AWLYYWW

“A” - The First character indicates the Assembly location.

“WL” - The Second & Third characters indicate the Source Wafer Lot Tracking Code.

“YY” - The Fourth & Fifth characters indicate the Year device was assembled.

“WW” - The Sixth & Seventh characters indicate the Work Week device was assembled.

### Trace Code Identification for 20 TSSOP: ALYW

“A” - The First character indicates the Assembly location.

“L” - The Second character indicates the Source Wafer Lot Tracking Code.

“Y” - The Third character indicates the “ALPHA CODE” of the year device was assembled.

“W” - The Fourth character indicates the “ALPHA CODE” of the Work Week device was assembled.

### The “Y” Year ALPHA CODES

Year	Month	Work Week Code
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

### The “W” Work Week ALPHA CODES

1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

### 20 TSSOP Tracecode Marking Example:

5ABR

| | |

5 | | | = Assembly Location

| | |

A | | = First Lot Assembled of this device in the designated  
| | Work Week

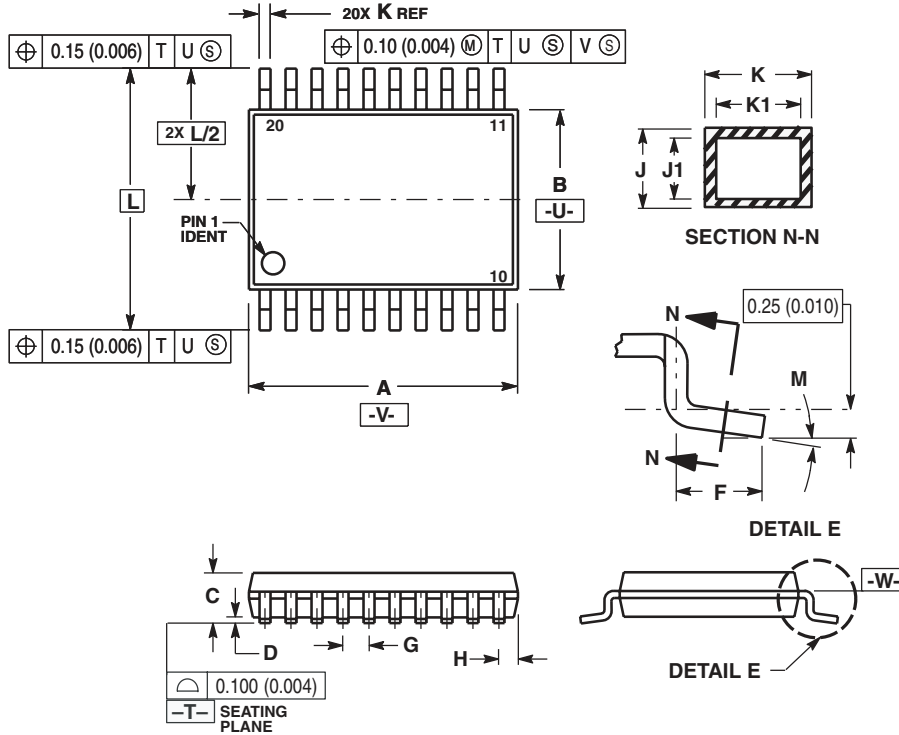
B | = 2003 Second 6 Months, WW27 - WW52

|

R = WW44 of 2003

OUTLINE DIMENSIONS

DT SUFFIX  
20 LEAD TSSOP PACKAGE  
CASE 948E-02  
ISSUE A



NOTES:

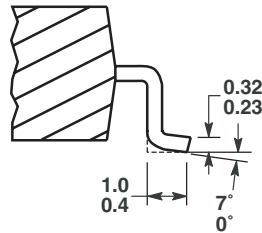
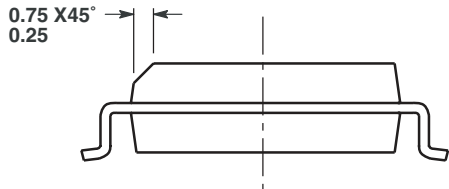
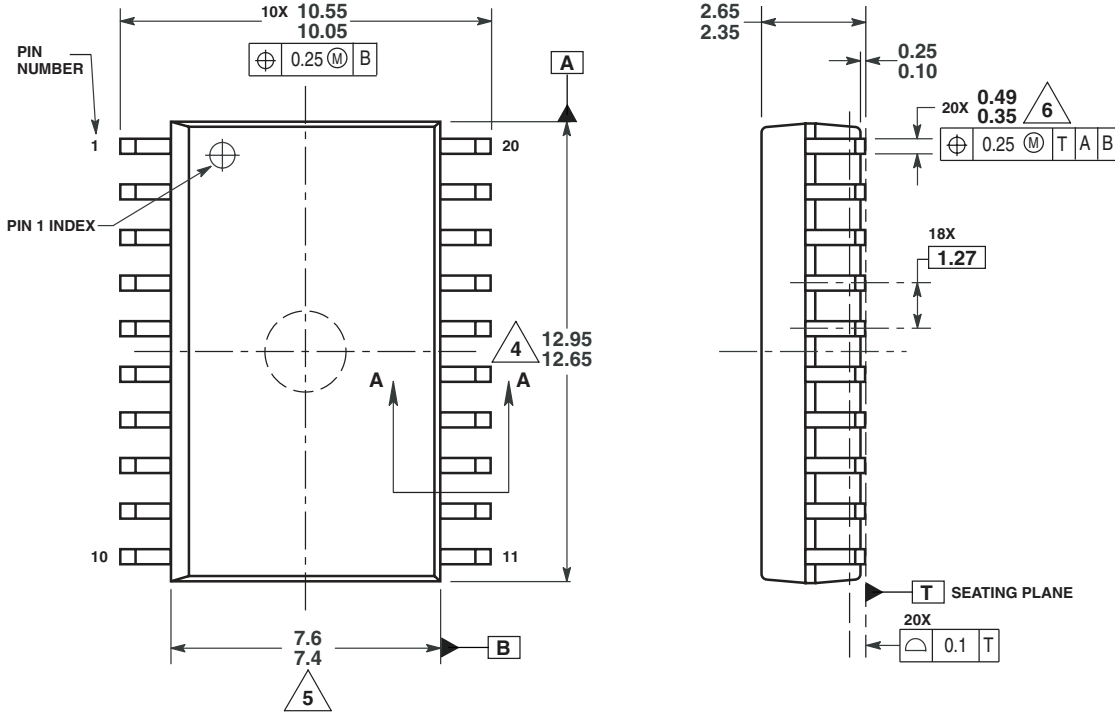
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0'	8'	0'	8'

Freescale Semiconductor, Inc.

OUTLINE DIMENSIONS

DW SUFFIX  
20 LEAD SOIC PACKAGE  
CASE 751D-06  
ISSUE H



SECTION A-A

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE WIDTH TO EXCEED 0.62 MM.



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