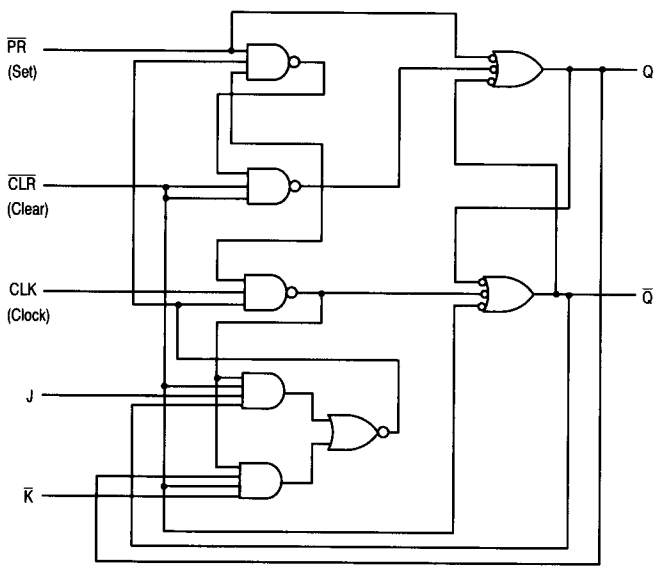
MOTOROLA

Dual J-$\overline{K}$ Flip-Flop With Clear and Preset

ELECTRICALLY TESTED PER:
MIL-M-38510/30109

The 54LS109A consists of two high-speed completely independent transition clocked J-K flip-flops. The clocking operation is independent of the rise and fall times of the clock waveform. The J-$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

*Both outputs will be HIGH while both $\overline{PR}$ and $\overline{CLR}$ are LOW, but the output states are unpredictable if $\overline{PR}$ and $\overline{CLR}$ go HIGH simultaneously.

Military 54LS109A

AVAILABLE AS:

1) JAN: JM38510/30109BXA
2) SMD: N/A
3) 883: 54LS109A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{CLR}_1$	1	1	2	GND
J_1	2	2	3	V_{CC}
$\overline{K}_1$	3	3	4	V_{CC}
CLK_1	4	4	5	GND
$\overline{PR}_1$	5	5	7	GND
Q_1	6	6	8	V_{CC}
$\overline{Q}_1$	7	7	9	V_{CC}
GND	8	8	10	GND
$\overline{Q}_2$	9	9	12	V_{CC}
Q_2	10	10	13	V_{CC}
$\overline{PR}_2$	11	11	14	GND
CLK_2	12	12	15	GND
$\overline{K}_2$	13	13	17	V_{CC}
J_2	14	14	18	V_{CC}
$\overline{CLR}_2$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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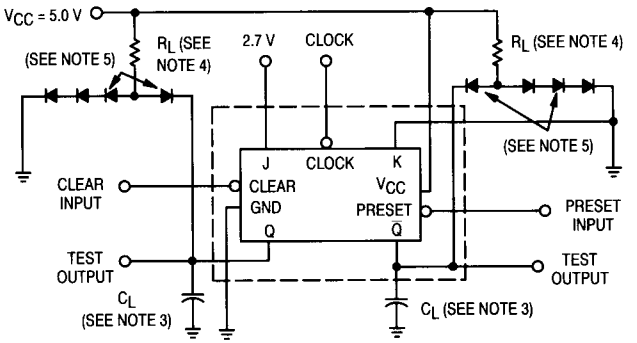
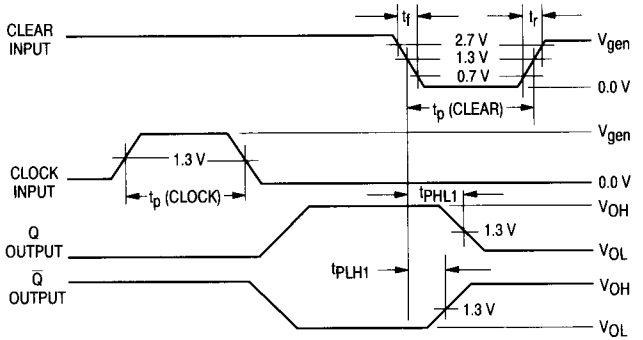
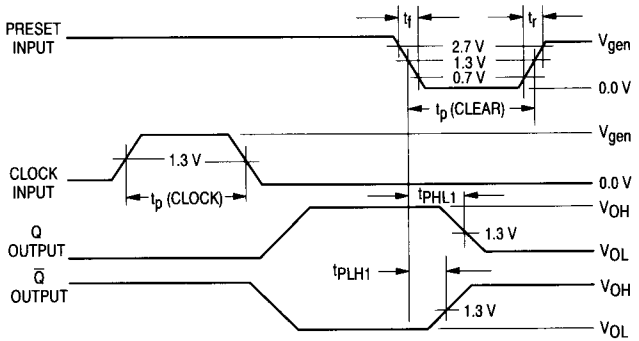
AC TEST CIRCUIT



WAVEFORMS





NOTES:

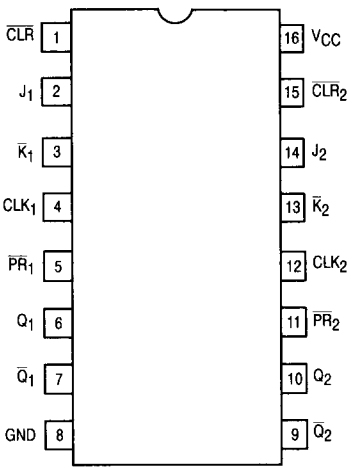
1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, t_p (clear) = t_p (preset) = 30 ns, $Z_{OUT} \approx 50\ \Omega$.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table).
7. Clock input pulse characteristics: t_p (clock) ≥ 25 ns, V_{gen} = 3.0 V, PRR ≤ 1.0 MHz.

MODE SELECT — TRUTH TABLE

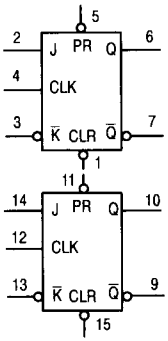
Operating Mode	Inputs				Outputs	
	$\overline{PR}$	$\overline{CLR}$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

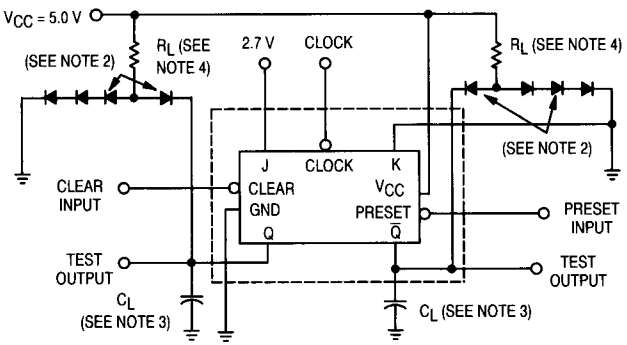
CONNECTION DIAGRAM



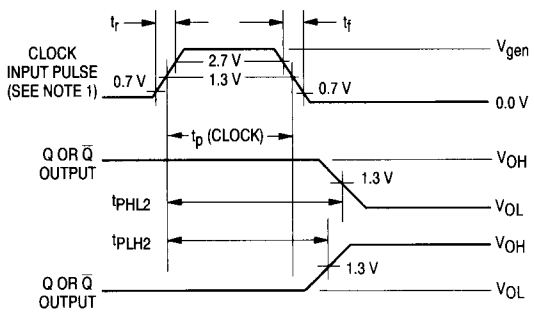
LOGIC SYMBOL



SYNCHRONOUS SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output): V_{gen} = 3.0 V, $t_r \leq 15$ ns, t_f = 6.0 ns, t_p (clock) = 25 ns and PRR ≤ 1.0 MHz. When testing f_{MAX} the clock input characteristics are: V_{gen} = 3.0 V, $t_r = t_f \leq 6.0$ ns, t_p (clock) ≤ 25 ns and PRR = (see table on next page).
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current (J & K inputs)		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 4.5 V, CLR = GND.
I_{IHH}	Logical "1" Input Current (J & K inputs)		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, CLK = 4.5 V, other inputs = 0 V.
I_{IH}	Logical "1" Input Current (CLK & PR)		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 4.5 V, CLR & PR = GND.
I_{IHH}	Logical "1" Input Current (CLK & PR)		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = 4.5 V, CLK = GND.
I_{IH}	Logical "1" Input Current (CLR inputs)		80		80		80	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, CLK = GND, other inputs = 4.5 V.
I_{IHH}	Logical "1" Input Current (CLR inputs)		400		400		400	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, CLK = GND, other inputs = 4.5 V.
I_{IL}	Logical "0" Input Current (J & K inputs)	− 0.135	− 0.37	− 0.135	− 0.37	− 0.135	− 0.37	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, PR & K = 4.5 V, CLK = (See Note 2).
I_{IL} CLK	Logical "0" Input Current (CLK & PR)	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, J & K = 4.5 V, CLK & CLR = 4.5 V.
I_{IL} PR		− 0.28	− 0.76	− 0.28	− 0.76	− 0.28	− 0.76		
I_{IL}	Logical "0" Input Current (CLR inputs)	− 0.28	− 0.76	− 0.28	− 0.76	− 0.28	− 0.76	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CLK – J & K = 4.5 V, PR = 0 V.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, CLK – CLR & J = GND, V_{OUT} = 0 V, other inputs are open.
I_{CC}	Power Supply Current		8.0		8.0		8.0	mA	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{IN} = 5.5 V, other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. = 0.0 V — 2.5 V min/5.5 V max
2. = 0.0 V — 2.5 V min/5.5 V max

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	5.0 —	32 40	5.0 —	59 54	5.0 —	59 54	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	5.0 —	20 25	5.0 —	39 34	5.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output Output High-Low	5.0	35	5.0	59	5.0	59	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output Output Low-High	5.0	24	5.0	39	5.0	39	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	20		20		20		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.

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