Fully Integrated, Hall-Effect Based Current Sensor IC With I²C Digital Output and Low-Resistance Current Conductor

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 5, 2016

Recommended Substitutions: no direct replacement

For existing customer transition, and for new customers or new applications, contact Allegro Marketing.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Fully Integrated, Hall-Effect Based Current Sensor IC With I²C Digital Output and Low-Resistance Current Conductor

Features and Benefits

- Fully integrated current sensor IC in a compact QSOP package eliminates the need for shunt resistors
- Hall effect sensing technology eliminates the error associated with shunt resistor variation due to temperature
- High accuracy: typical error < 2% over operating temperature range
- Fast response digital fault output with programmable level through I²C bus interface
- Digital output through I²C interface with 9-bit A-to-D conversion for high resolution current measurement
- User-selectable decimation averaging of current output; up to 256 samples
- Freeze pin for holding current measurement value while reading many sensors serially
- User-selectable (via I²C) coarse sensitivity and OC fault levels, for exceptional flexibility to meet application requirements

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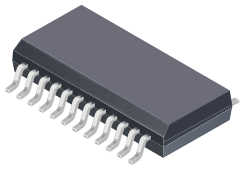
Package: 24-pin QSOP (suffix LF)



Not to scale

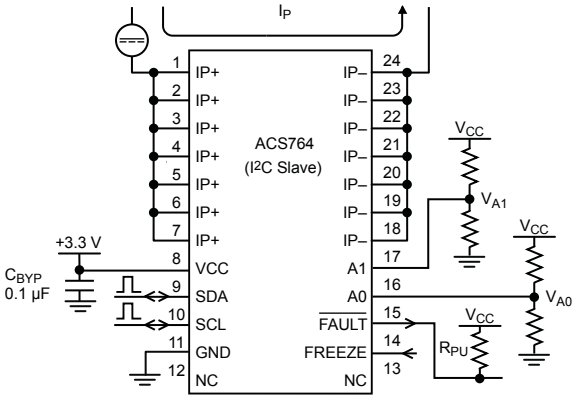
Description

The Allegro™ ACS764 fully integrated Hall-effect current sensor IC is designed for applications that require digital current sensing and reporting through an I²C™ bus. Allegro factory programming of the offset and gain, including the temperature coefficients, stabilizes the offset and gain over the operating temperature range. This programming greatly reduces the device total error, typically less than 2% over the operating temperature range. A fast response digital fault output is also provided. Both coarse sensitivity and fault level can be programmed via an I²C control register, and can be used for enhanced diagnostic functions.

The integrated low resistance conductor eliminates the requirement for external shunt resistors and, by employing Hall-effect sensing technology, eliminates the error associated with changing sense resistance due to temperature. The device allows 16 unique I²C bus addresses, selectable via external pins. The sensor IC gain can be selected by the user through the I²C bus. The device uses a BiCMOS process that allows a highly stable chopper-stabilized small signal amplifier design.

The ACS764 is provided in a compact 24-pin QSOP package (suffix LF). The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS.

Typical Application Diagrams



Features and Benefits (continued)

- Less than 0.5 mΩ series resistance greatly reduces power dissipation and heat generation
- Factory programmed temperature compensation stabilizes sensitivity and offset voltage throughout the operating temperature range
- 16 programmable I²C addresses
- Unidirectional DC current sensing and reporting
- Immunity to stray magnetic fields simplifies PCB layout

Selection Guide

Part Number	Packing*	Operating Ambient Temperature, T_A (°C)	Optimized Current Sensing Range (A)	Optimized Nominal Resolution (mA/LSB)
ACS764XLFTR-32AU-T	Tape and reel, 2500 pieces/reel	–20 to 125	32	62.62
ACS764XLFTR-16AU-T	Tape and reel, 2500 pieces/reel	–20 to 125	16	31.31

*Contact Allegro™ for additional packing options.

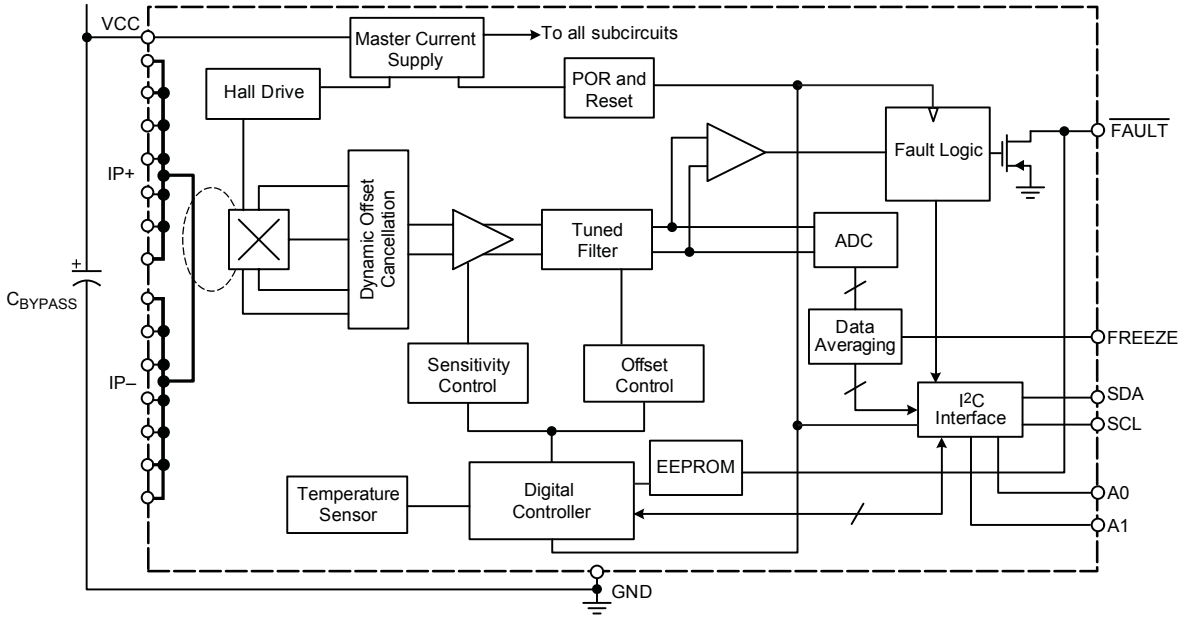
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		7	V
Forward $\overline{\text{FAULT}}$ Pin Voltage	V_{FAULT}		24	V
DC Forward Voltage (A0, A1, FREEZE pins)	V_{FDCx}		7	V
DC Reverse Voltage (VCC, A0, A1, $\overline{\text{FAULT}}$, FREEZE pins)	V_{RDCx}		–0.5	V
Operating Ambient Temperature	T_A	X temperature range	–20 to 125	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 165	ºC

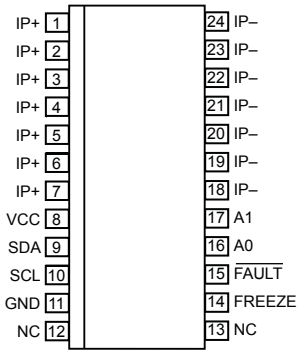
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Value	Unit
Steady State Package Thermal Resistance	$R_{\theta JA}$	Tested with 30 A DC current and based on ACS764 demo board in 1 cu. ft. of still air. Please refer to product FAQs page on Allegro website for detailed information on ACS764 demo board.	27	ºC/W

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Function
1 to 7	IP+	Primary current path input terminals
8	VCC	Device power supply
9	SDA	I²C control: interface data signal input/output
10	SCL	I²C control: clock signal input/output
11	GND	Device ground
12,13	NC	No internal connection; connect to GND for optimal ESD performance
14	FREEZE	Digital output register freezing control input; pull-up to stop Data register updating
15	$\overline{\text{FAULT}}$	I_P fault flag output; active low
16	A0	I²C control: address input 0
17	A1	I²C control: address input 1
18 to 24	IP–	Primary current path output terminals

OPERATING CHARACTERISTICS[1] Valid throughout an ambient temperature range of –20°C to 125°C, C_{BYPASS} = 0.1 µF, V_{CC} = 3.3 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Electrical Characteristics						
Supply Voltage	V_{CC}		3.0	–	3.6	V
Supply Current	I_{CC}	No load on SDA and SCL	–	9	14	mA
Power-On Time	t_{PO}	T_A = 25°C; C_{BYPASS} = open	–	64	–	µs
Internal Bandwidth	BW_i	Small signal –3 dB; T_A = 25°C	–	2	–	kHz
Leadframe Resistance	R_P	IP+ to IP– through primary current path	–	0.5	–	mΩ
Current Sensing Range Selection						
Current Sensing Range[2,3]	CSR	[GAIN_RANGE] = 10b	–	8	–	A
		[GAIN_RANGE] = 11b	–	16	–	A
		[GAIN_RANGE] = 00b	–	32	–	A
		[GAIN_RANGE] = 01b	–	64	–	A
Nominal Resolution[3]	RES	[GAIN_RANGE] = 10b	–	15.66	–	mA/LSB
		[GAIN_RANGE] = 11b	–	31.31	–	mA/LSB
		[GAIN_RANGE] = 00b	–	62.62	–	mA/LSB
		[GAIN_RANGE] = 01b	–	125.24	–	mA/LSB
Output Signal Characteristics						
A-to-D Conversion Resolution	Res_{ADC}		–	9	–	bit
A-to-D Conversion Time	t_{ADC}		–	375 × N	–	µs
Average Quantity of Data Points Included in Moving Average Calculation[4]	N	[N7:N0]=[0000 0000] through [1111 1111] represents 1 data point through 256 data points	1	–	256	data point
Analog Noise	$I_{NOISE(rms)(A)}$	T_A = 25°C	–	15	–	mA
Analog Noise Density	$I_{NOISE(den)(A)}$	T_A = 25°C	–	0.27	–	$mA/Hz^{1/2}$
A-to-D Linear Range[5]	ADC_{LIN}		15	–	496	ADC Code
Digital Noise	$I_{NOISE(rms)(D)}$	T_A = 25°C	–	$I_{NOISE(rms)(A)} / N^{1/2}$	–	mA
Accuracy Performance						
Offset Error	Err_{OS}	GAIN_RANGE set for optimized CSR, ADC code is within ADC_{LIN}; measured at 2 A; T_A = 25°C to 125°C	–8	±5	+8	LSB
		GAIN_RANGE set for optimized CSR; ADC code is within ADC_{LIN}; measured at 2 A; T_A = –20°C to 25°C	–15	±7	+15	LSB

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OPERATING CHARACTERISTICS[1] (continued) Valid throughout an ambient temperature range of –20°C to 125°C, C_{BYPASS} = 0.1 µF, V_{CC} = 3.3 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Accuracy Performance (continued)						
Resolution Accuracy	Res_{ACC}	GAIN_RANGE set for optimized CSR, ADC code is within ADC_{LIN}; T_A = 25°C to 125°C; measured at 0.94 × CSR	–2.5	±1	+2.5	%
		GAIN_RANGE set for optimized CSR, ADC code is within ADC_{LIN}; T_A = –20°C to 25°C; measured at 0.94 × CSR	–3.5	±1.5	+3.5	%
Nonlinearity Error	Err_{LIN}	GAIN_RANGE set for optimized CSR, ADC code is within ADC_{LIN}	–	±0.75	–	%
Total Error	Err_{TOT}	GAIN_RANGE set for optimized CSR; ADC code is within ADC_{LIN}; Current = 0.94 × CSR; T_A = 25°C to 125°C	–2.5	±1	+2.5	%
		GAIN_RANGE set for optimized CSR; ADC code is within ADC_{LIN}; Current = 0.94 × CSR; T_A = –20°C to 25°C	–3.5	±2	+3.5	%
Lifetime Drift Characteristics						
Resolution Lifetime Drift	Res_{DRIFT}		–	±3.0	–	%
Total Error Lifetime Drift	Err_{TOT_DRIFT}		–	±3	–	%
Overcurrent Fault Detection Resolution/Timing						
Fault Current Maximum Setpoint	$I_{FAULT(MAX)}$	FAULT_LEVEL = 0000b	–	1.46 × CSR	–	A
Fault Current Minimum Setpoint	$I_{FAULT(MIN)}$	FAULT_LEVEL = 1111b	–	0.5 × CSR	–	A
Digital Fault Level Resolution	Res_{FAULT}		–	4	–	bit
Fault Level Error[6]	$E_{FAULT(MIN)}$	GAIN_RANGE set for optimized CSR; measured at FAULT_LEVEL = 0000b	–4	±2.5	+4	%
	$E_{FAULT(MAX)}$	GAIN_RANGE set for optimized CSR; measured at FAULT_LEVEL = 1111b	–	±7	–	%
Pull up Resistance at $\overline{FAULT}$ Pin	R_{PU}		10	–	–	kΩ
$\overline{FAULT}$ Output Voltage	V_{FAULT}	RPU = 10 kΩ, under fault condition	–	–	0.4	V
Fault Response Time	t_{FAULT}	Delay from I_P rising above I_{FAULT} until V_{FAULT} < 0.4 V	–	100	–	µs
FREEZE Pin Characteristics						
FREEZE Pin Input Level (Low)	$V_{FREEZE(IL)}$		–	–	0.2 × V_{CC}	V
FREEZE Pin Input Level (High)	$V_{FREEZE(IH)}$		0.8 × V_{CC}	–	–	V
FREEZE Pin Input Impedance	$R_{FREEZE(IN)}$		–	10	–	kΩ

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OPERATING CHARACTERISTICS[1] (continued) Valid throughout an ambient temperature range of –20°C to 125°C, C_{BYPASS} = 0.1 µF, V_{CC} = 3.3 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Address Pin Characteristics[7]						
Address Value 0 Voltage	V_{ADDR0}	A0, A1 pins	–	0	0.08 × V_{CC}	V
Address Value 1 Voltage	V_{ADDR1}	A0, A1 pins	0.28 × V_{CC}	0.31 × V_{CC}	0.34 × V_{CC}	V
Address Value 2 Voltage	V_{ADDR2}	A0, A1 pins	0.53 × V_{CC}	0.56 × V_{CC}	0.59 × V_{CC}	V
Address Value 3 Voltage	V_{ADDR3}	A0, A1 pins	0.8 × V_{CC}	V_{CC}	–	V
Input Bias Current	I_{A0}	A0 pin	–	100	–	nA
	I_{A1}	A1 pin	–	100	–	nA

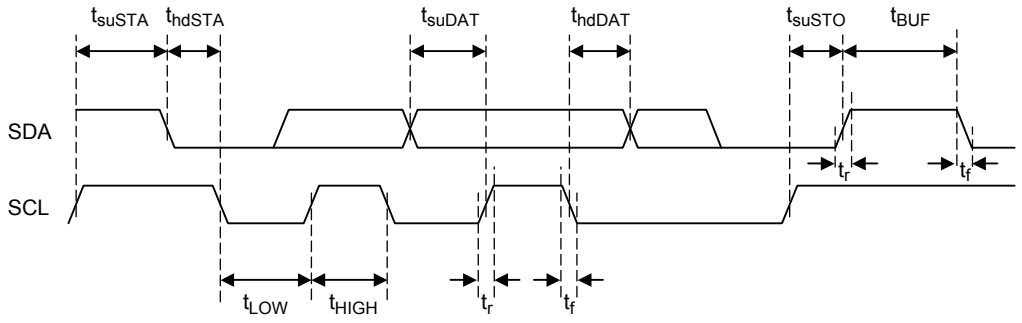
[1]All current measurement accuracy specifications listed in this datasheet apply only for the optimized current sensing range.
[2]The ACS764 will be most accurate in its optimized gain range.
[3]The GAIN_RANGE setting of 11b selects the Optimized Nominal Resolution for the 16AU variant, and the GAIN_RANGE setting of 00b selects the Optimized Nominal Resolution for the 32AU variant.
[4]Programmable by user through the I²C interface.
[5]The ADC is most linear within ADC_{LIN}, so code readings outside ADC_{LIN} should not be used for precise measurement.
[6]Percentage of CSR. See table 3 and Definitions of Accuracy Characteristics section.
[7]Address pin characteristics are ensured by designed but are not factory tested.

I²C INTERFACE CHARACTERISTICS* Valid at an ambient temperature range of –20°C to 125°C and V_{CC} = 3.3 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Bus Free Time Between Stop and Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	t_{hdSTA}		0.6	–	–	µs
Setup Time for Repeated Start Condition	t_{suSTA}		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	t_{suDAT}		100	–	–	ns
Data Hold Time	t_{hdDAT}		0	–	900	ns
Setup Time for Stop Condition	t_{suSTO}		0.6	–	–	µs
Logic Input Low Level (SDA, SCL pins)	V_{IL}		–	–	$0.3 \times V_{CC}$	V
Logic Input High Level (SDA, SCL pins)	V_{IH}		$0.7 \times V_{CC}$	–	–	V
Logic Input Current	I_{IN}	VIN = 0 V to V_{CC}	−1	–	1	µA
Output Voltage (SDA pin)	V_{OL}	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	$0.2 \times V_{CC}$	V
Logic Input Rise Time (SDA, SCL pins)	t_r		–	–	300	ns
Logic Input Fall time (SDA, SCL pins)	t_f		–	–	300	ns
SDA Output Rise Time	t_r	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	300	ns
SDA Output Fall Time	t_f	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	300	ns
Clock Frequency (SCL pin)	f_{CLK}		–	–	400	kHz
SDA and SCL Bus Pull-up Resistor	R_{PU}		–	1	–	kΩ
Total Capacitive Load for Each of SDA and SCL Buses	C_B		–	–	100	pF

*I²C interface characteristics are ensured by designed but are not factory tested.

I²C Interface Timing Diagram



Application Information

The ACS764 is a fully integrated Hall-effect based current sensor IC with a digital current output and an overcurrent fault output for current monitoring and reporting applications. The digital output can be read from the ACS764 by a master controller through the I²C interface. The I²C interface can also be used to control some features of the ACS764. Sixteen device addresses are available through two input pins (A0, A1), allowing multiple devices to be connected to the same I²C bus in the application.

The output data that can be read from the ACS764 through the I²C interface includes the following:

- Current amplitude (9 bits)
- Unlatched overcurrent fault flag (1 bit)
- Latched overcurrent fault flag (1 bit)
- Unread new current data flag (1 bit)

The control data that can be written to the ACS764 through I²C interface includes the following:

- Current range selection (2 bits)
- Overcurrent fault level selection (4 bits)
- Digital averaging filter data point selection (8 bits)
- Latched overcurrent fault flag reset (1 bit)

I²C Interface

I²C is a serial interface that uses two bus lines, SCL and SDA, to access the internal device registers. Data is exchanged between a master controller (for example, a microcontroller) and the ACS764 (slave). The clock input to SCL is generated by the master, while the SDA line functions as either an input or an open drain output, depending on the direction of the data transfer. The I²C input thresholds depend on the V_{CC} voltage of the ACS764.

Timing Considerations

I²C communication is composed of several steps in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address Cycle. 7 device (slave) address bits, plus 1 bit to indicate write (0) or read (1), followed by an acknowledge bit.
3. Data Cycles. Reading or writing 8 data bits, followed by an acknowledge bit. This cycle can be repeated for multiple bytes of data transfer. If there are multiple registers in a device (for example, EEPROM), the first data byte could be the register address. See the following sections for further information.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low.

It is possible for the Start or Stop condition to occur at any time during a data transfer. The ACS764 always responds by resetting the data transfer sequence.

The state of the Read/Write bit is set low to indicate a write cycle and set high to indicate a read cycle.

The master monitors for an acknowledge pulse to determine if the slave device is responding to the address byte sent to the ACS764. When the ACS764 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the ACS764 pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow the handshaking to occur.

Writing to ACS764 Registers Through the I²C Interface Bus

The master controls the ACS764 by programming it as a slave. To do so, the master transmits data bits to the SDA input of the ACS764 in synchronization with the clocking signal it transmits simultaneously on the SCL input.

A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA line (Stop bit). Between these points, the master transmits a pattern of slave device (ACS764) address bits with a write command (D0 = 0), and then the target register address (within that device),

and finally the data for the register. Each register in the ACS764 device is three bytes, or 24 bits, long. The address consists of two bytes, comprising: the ACS764 (device) address (7 bits) and the read/write bit, followed by the address byte of the individual register. The data stream of writing data to an individual register is shown in figure 1.

After each byte, the slave ACS764 acknowledges by transmitting a low to the master on the SDA line. After writing data to a register the master must provide a Stop bit if writing is completed. If the stop bit is not set, then the next three bytes will be written to the current register address + 1. Writing will continue in this fashion until the Stop bit is received. If the total data byte count (that is, not including the Register Address byte) is not modulo three, then the write operation that would contain less than three bytes is not done.

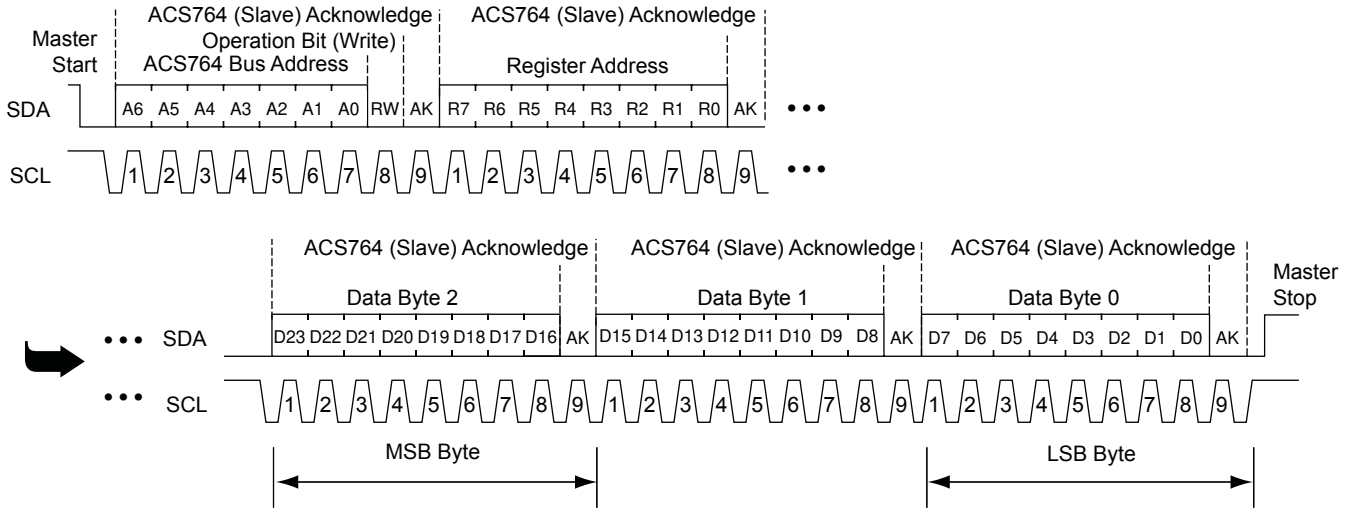


Figure 1. I²C interface typical data write to an individual register in the ACS764

Reading from ACS764 Registers Through the I²C Interface Bus

When the master controller performs a data read from an ACS764 internal register, a so-called *combined data transmission* format is used. The I²C master provides the Start bit, the ACS764 device (slave) address, the read/write bit set to write (0), and then the initial source register address. The master then issues another Start bit (referred to as *restart*) followed by the same slave address and the read/write bit set to read (1). The ACS764 then provides three bytes of read data, one byte at a time. The data stream of reading data from an individual register is shown in figure 2.

After each byte of data received, the master acknowledges by transmitting a low to the slave on the SDA line. After receiving three bytes of data from a register, the master must provide a Stop bit if reading is completed. If the Stop bit is not set, then the next three bytes will be read from the initial register address + 1. Reading will continue in this fashion until the Stop bit is received. Please note that the acknowledge bit immediately before the Stop bit should be a non-acknowledge (AK = 1).

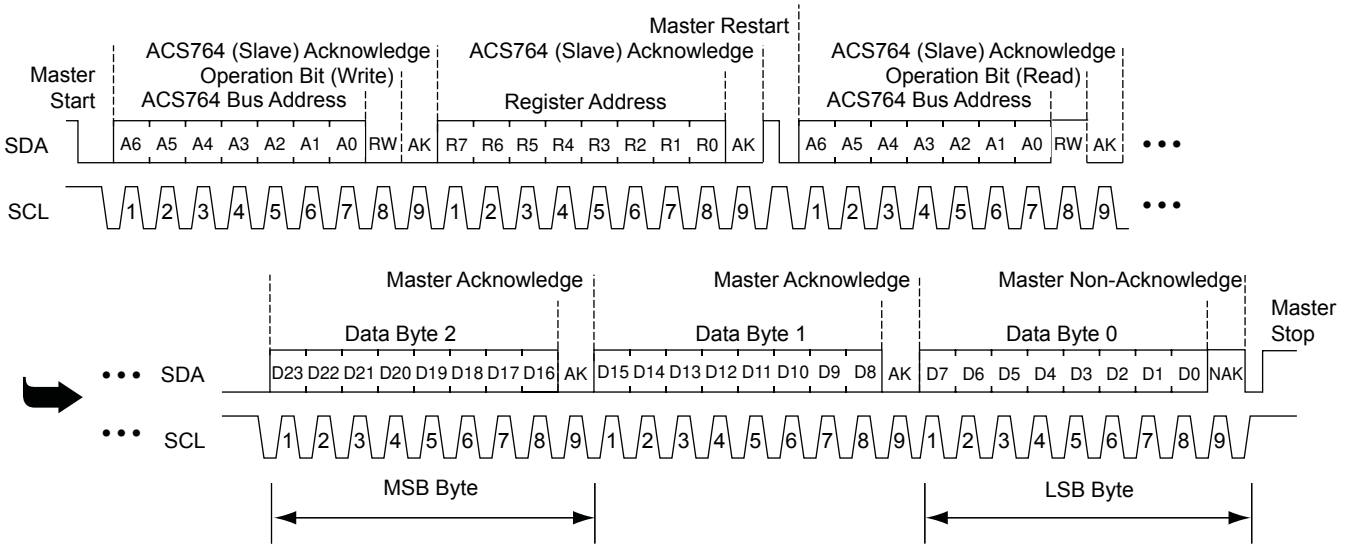


Figure 2. I²C interface typical data read from an individual register in the ACS764

I²C Device (Slave) Address Coding

The four LSBs of the device (slave) address (A3, A2, A1, and A0) can be set by applying different voltages to pins A0 and A1 as show in figure 3 and defined in table 1.

Note: Different values for the three MSBs of the address (A6, A5, and A4) are available for factory programming if a conflict with other units occurs in the application design.

ACS764 Bus Address Byte Definitions

Address Bit						
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Binary Device Address Value						
1	1	0	0/1	0/1	0/1	0/1

Table 1. I²C Device Address Coding (Refer to figure 3)

Voltage on A1 Pin, V_{A1}	Voltage on A0 Pin, V_{A0}	Device Address #	
		Decimal	Binary (A3, A2, A1,A0)
0 V	0 V	0	0000
0 V	0.31 × V_{CC}	1	0001
0 V	0.56 × V_{CC}	2	0010
0 V	V_{CC}	3	0011
0.31 × V_{CC}	0 V	4	0100
0.31 × V_{CC}	0.31 × V_{CC}	5	0101
0.31 × V_{CC}	0.56 × V_{CC}	6	0110
0.31 × V_{CC}	V_{CC}	7	0111
0.56 × V_{CC}	0 V	8	1000
0.56 × V_{CC}	0.31 × V_{CC}	9	1001
0.56 × V_{CC}	0.56 × V_{CC}	10	1010
0.56 × V_{CC}	V_{CC}	11	1011
V_{CC}	0 V	12	1100
V_{CC}	0.31 × V_{CC}	13	1101
V_{CC}	0.56 × V_{CC}	14	1110
V_{CC}	V_{CC}	15	1111

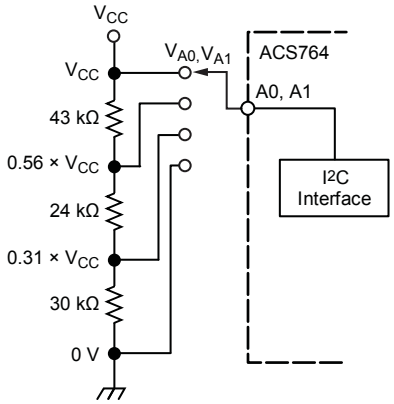


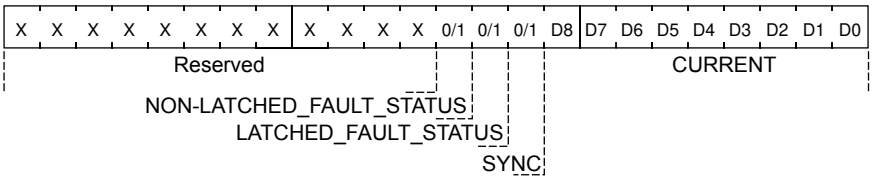
Figure 3. External equivalent circuit for I²C device address selection

Table 2. User-Accessible Volatile Memory Registers

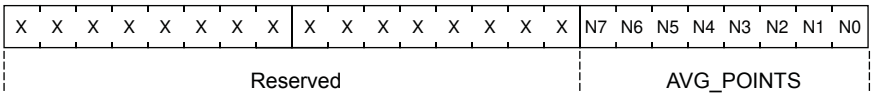
Data Register				
I²C Register Address	**Bits**	**Parameter Name**	**Description**	
0x00	23:12	Reserved	Read as all 0s	
0x00	11	NON-LATCHED_FAULT_STATUS	Non-Latched Fault bit (Read only)	
0x00	10	LATCHED_FAULT_STATUS	Latched Fault bit; resets with 1 written to this bit (Read/Write)	
0x00	9	SYNC	Sync (new data) bit; resets when this register is read (Read only)	
0x00	8:0	CURRENT	Current Sensor output value (digital filter output) (Read only)	
Control Registers				
I²C Register Address	**Bits**	**Parameter Name**	**Description**	**Default**
0x02	7:0	AVG_POINTS	Number of averaging points (Read/Write)	0
0x04	1:0	GAIN_RANGE	Current sensing range selection (Read/Write)	0 (32AU version) 3 (16AU version)
0x06	3:0	FAULT_LEVEL	Fault threshold selection (Read/Write)	0

User-Accessible Register Bit Descriptions

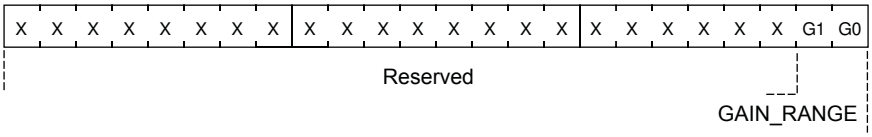
Volatile Register Bits (Address: 0x00)



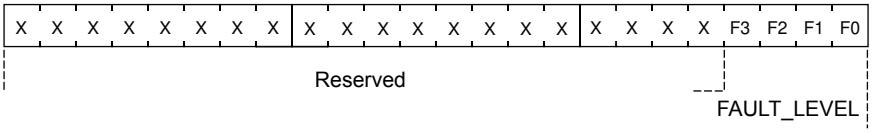
Volatile Register Bits (Address: 0x02)



Volatile Register Bits (Address: 0x04)



Volatile Register Bits (Address: 0x06)



Working with Internal Device Registers Through I²C

Control Registers

On power-up the control registers will be loaded to their default values from the EEPROM. The settings can be changed after powering on the device by overwriting the control registers through the I²C interface. However, the control registers will revert to their previous levels if the sensor IC is power cycled. Contact your local sales representative if you need the default control register values to be factory-programmed differently.

Data Registers

The volatile register at 0x00 holds all the output data of the device. It includes nine bits of current measurement data and three flag bits: one bit for current output update (SYNC), one bit for latched overcurrent fault (LATCHED_FAULT_STATUS), and one bit for non-latched overcurrent fault (NON-LATCHED_FAULT_STATUS), in that order.

After the current measurement data has been updated, SYNC is set. It will be reset when the data is read by a master controller through the I²C interface.

When an overcurrent fault condition is detected, both the LATCHED_FAULT_STATUS and the NON-LATCHED_FAULT_STATUS bits will be set. The NON-LATCHED_FAULT_STATUS bit will be reset after the overcurrent condition is removed. However, the LATCHED_FAULT_STATUS bit will remain set until a 24-bit word in the format:

XXXX XXXX XXXX X1XX XXXX XXXX

is written to the register.

Setting the Overcurrent Fault Threshold

The Overcurrent Fault threshold, $I_{\overline{FAULT}}$, is determined by setting the four FAULT_LEVEL bits. The combined settings determine the threshold as a percentage of current sensing range, CSR. The $\overline{FAULT}$ pin will be pulled low when the current is above the programmed I_FAULT level. The $\overline{FAULT}$ pin will be released when the current drops below the programmed I_FAULT level.

The digital NON-LATCHED FAULT STATUS bit will be 1 when the current is above I_FAULT and 0 when the current is below I_FAULT. The LATCHED FAULT STATUS bit will be 1 when the current is above I_FAULT and will only return to being 0 when the current is below I_FAULT and the bit is reset by writing a 1 to it.

Table 3. I²C Control: Settings for Overcurrrent Fault Threshold

FAULT_LEVEL Bits				$I_{\overline{FAULT}}$	
F3	F2	F1	F0	Level	Setting (%CSR)
0	0	0	0	0	50
0	0	0	1	1	56
0	0	1	0	2	63
0	0	1	1	3	69
0	1	0	0	4	76
0	1	0	1	5	82
0	1	1	0	6	88
0	1	1	1	7	95
1	0	0	0	8	101
1	0	0	1	9	108
1	0	1	0	10	114
1	0	1	1	11	120
1	1	0	0	12	127
1	1	0	1	13	133
1	1	1	0	14	140
1	1	1	1	15	146

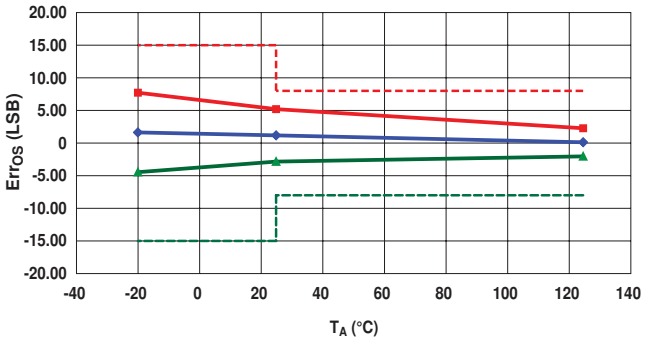
Example: If the required overcurrent fault threshold is 88% of the CSR, then the required FAULT_LEVEL values are: 0110 (Level 6).

Characteristic Performance Data

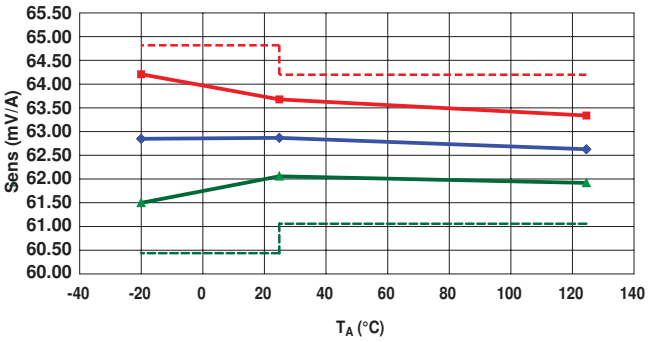
Data taken using the ACS764-32AU

Accuracy Data

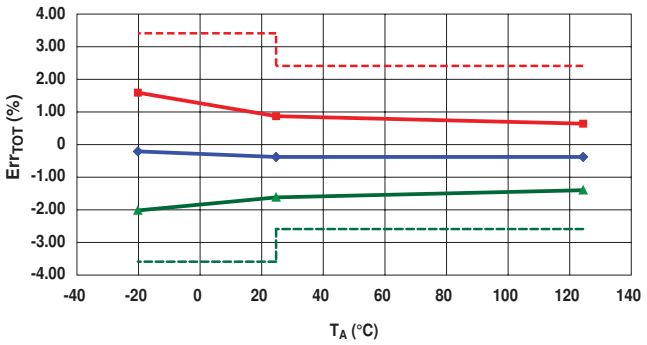
Offset Error versus Ambient Temperature



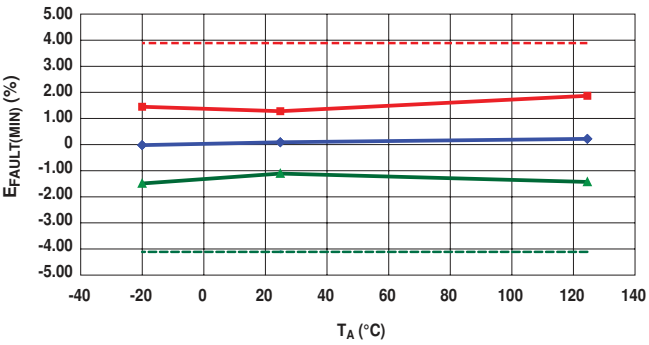
Resolution versus Ambient Temperature



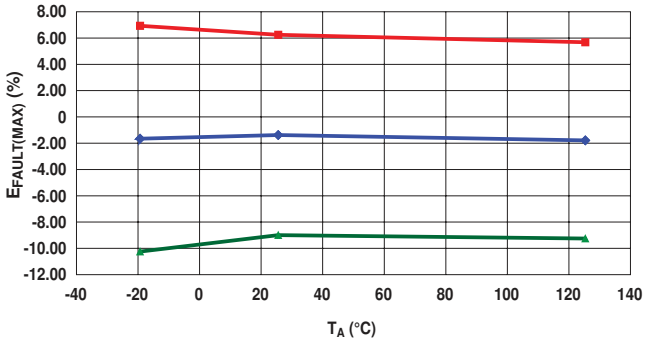
Total Error versus Ambient Temperature



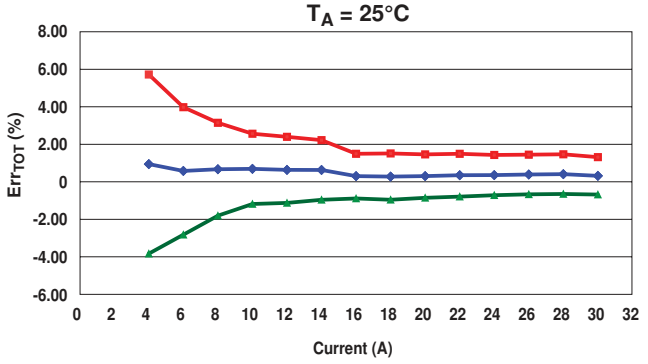
Fault Minimum Error versus Ambient Temperature

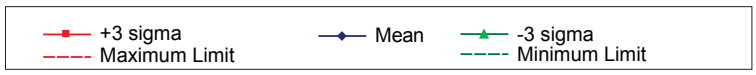


Fault Maximum Error versus Ambient Temperature



Total Error versus Current
T_A = 25°C



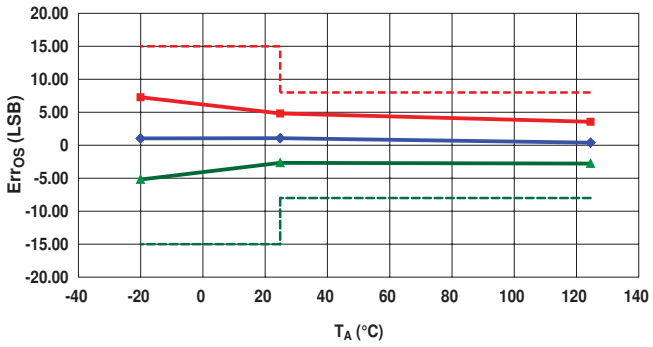


Characteristic Performance Data

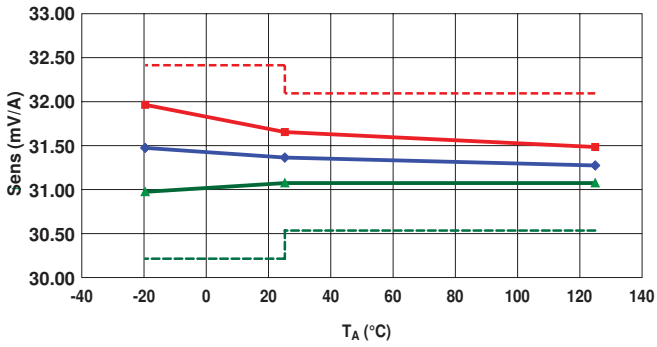
Data taken using the ACS764-16AU

Accuracy Data

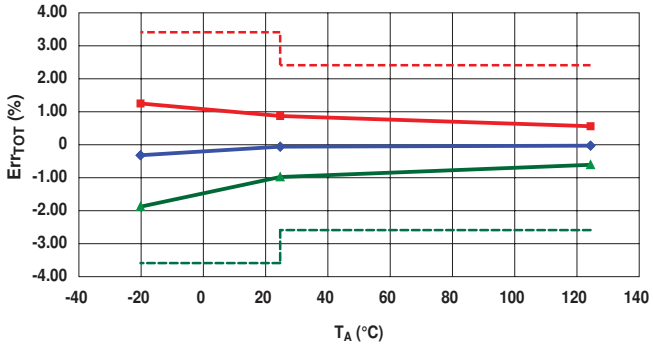
Offset Error versus Ambient Temperature



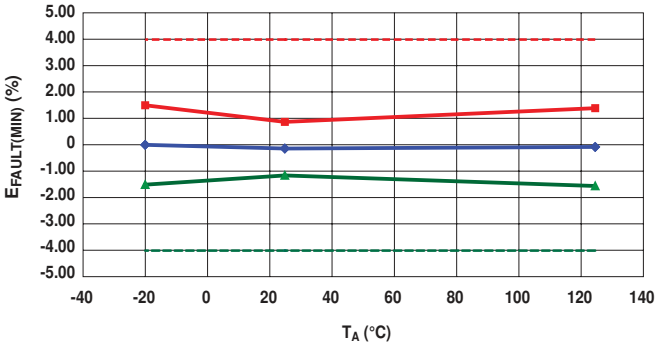
Resolution versus Ambient Temperature



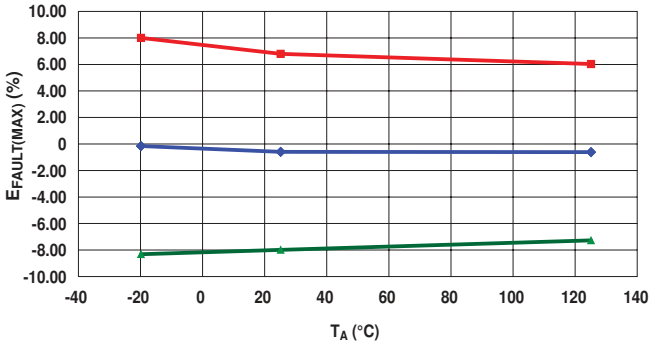
Total Error versus Ambient Temperature



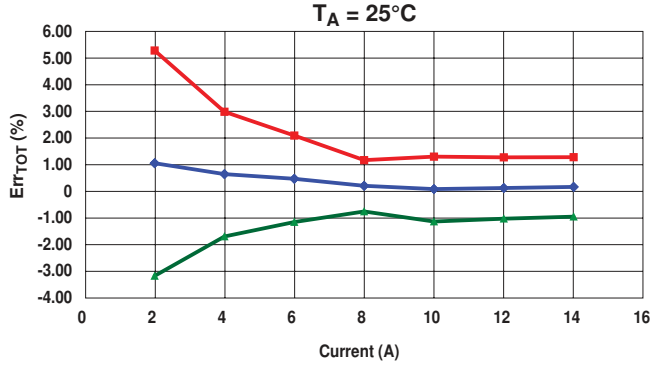
Fault Minimum Error versus Ambient Temperature

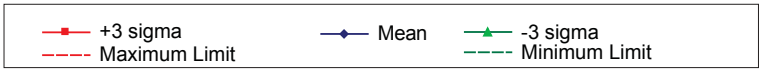


Fault Maximum Error versus Ambient Temperature



Total Error versus Current
T_A = 25°C





Definitions of Accuracy Characteristics

A-to-D Linear Range (ADC_{LIN})

The range of the ADC over which the ADC code is proportional to the current being sensed. One should consider the ADC saturated outside this range. See figure 4.

Offset Error (Err_{OS})

The offset of the ADC code versus the measured current from the ideal of zero. See figure 4. This parameter is measured at 2 A, as the ADC is below ADC_{LIN} at zero current. The offset error is calculated as:

$$Err_{OS} = ADC_{CODE} \text{ at } 2\text{ A} - 2000\text{ (mA)} \times \frac{1}{RES}$$

Resolution Accuracy (Res_{ACC})

The resolution of the sensor is given in mA/LSB, which is the inverse of the slope of the ADC code versus the measured current (see figure 4). Multiplying the ADC code by the resolution yields the measured current. The Resolution Accuracy (Res_{ACC}) is how close the actual resolution is to the Nominal Resolution (RES). The Resolution Accuracy is calculated as:

$$Res_{ACC} = \frac{\text{Measured Resolution} - RES}{RES} \times 100\ (\%)$$

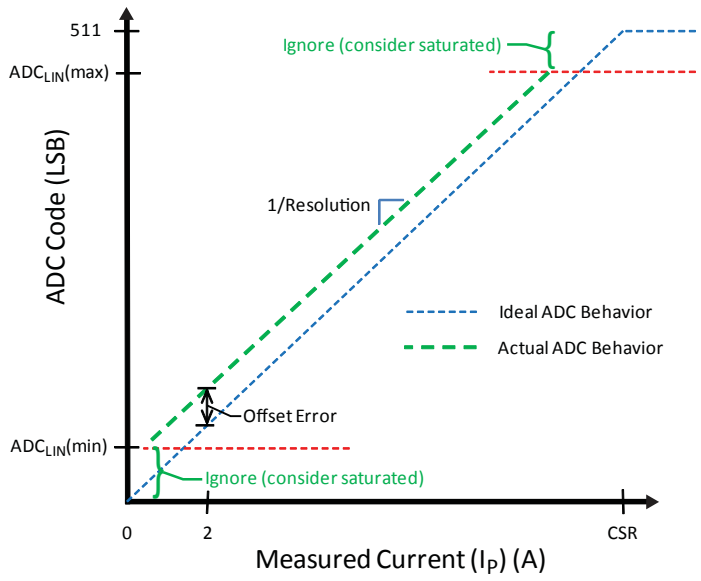


Figure 4. A-to-D Linear Range

Nonlinearity Error (Err_{LIN})

The Nonlinearity Error is a measure of how linear the ADC code versus measured current curve is. The nonlinearity is calculated as:

$$Err_{LIN} = \left\{1 - \frac{0.5}{0.94}\left[\frac{ADC_{CODE}\ (0.94 \times CSR) - Err_{OS}}{ADC_{CODE}\ (0.5 \times CSR) - Err_{OS}}\right]\right\} \times 100\ (\%)$$

Total Error (Err_{TOT})

The percentage difference between the current measurement from the sensor IC and the actual current being measured (I_P), relative to the actual current. This is equivalent to the percentage difference between the ideal ADC code and the actual ADC code, relative to the ideal ADC code:

$$Err_{TOT}(I_P) = \frac{ADC_{IDEAL}(I_P) - ADC(I_P)}{ADC_{IDEAL}(I_P)} \times 100\ (\%)$$

The Total Error incorporates all sources of error and is a function of the measured current (I_P). At relatively high currents, Err_{TOT} will be mostly due to the Resolution Accuracy, and at relatively low currents, Err_{TOT} will be mostly due to the Offset Error.

Fault Level Error ($E_{FAULT(MIN)}$, $E_{FAULT(MAX)}$)

The Fault Level Error is a measure of the accuracy of the overcurrent fault function. $E_{FAULT(MIN)}$ is E_{FAULT} measured at FAULT_LEVEL = 0000b, and $E_{FAULT(MAX)}$ is E_{FAULT} measured at FAULT_LEVEL = 1111b. The Fault Level Error is calculated as:

$$E_{FAULT}(FAULT\_LEVEL) = \frac{\text{Fault Trip Current}}{CSR \times 100\ (\%)} - I_{FAULT\_Percent}$$

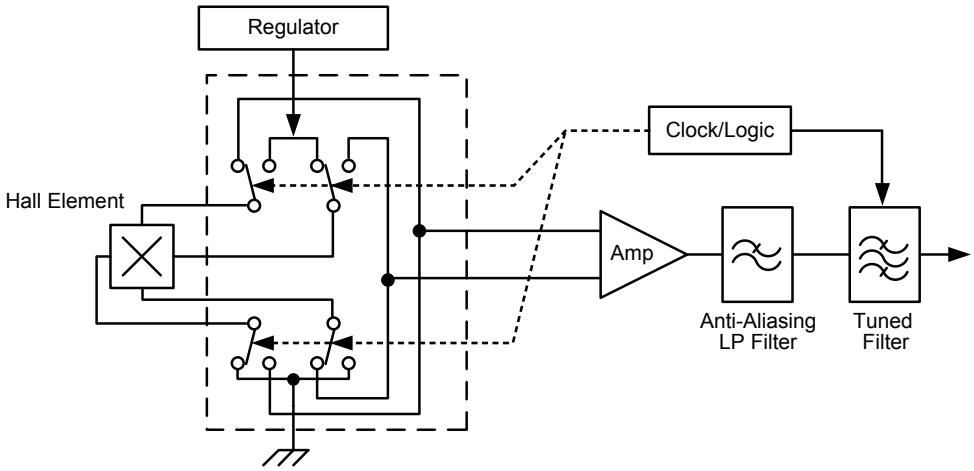
where $I_{FAULT\_Percent}$ is the ideal percentage of CSR at which the overcurrent fault should trip, based on the FAULT_LEVEL settings as given in table 3. For example, if FAULT_LEVEL is set to 0000b, the ideal trip point is at 50% of CSR. An $E_{FAULT(MIN)}$ specification of ±4% means the actual trip point ia between 46% and 54% of CSR.

Dynamic Response Characteristics

Power-On Time (t_{PO}):
When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to a magnetic field due to current flow through the sensor. Power-On Time, t_{PO}, is defined as the time it takes from when the supply voltage (V_{CC}) reaches its minimum specified voltage to when the value from the ADC is valid, as well as the fault bits and fault output.

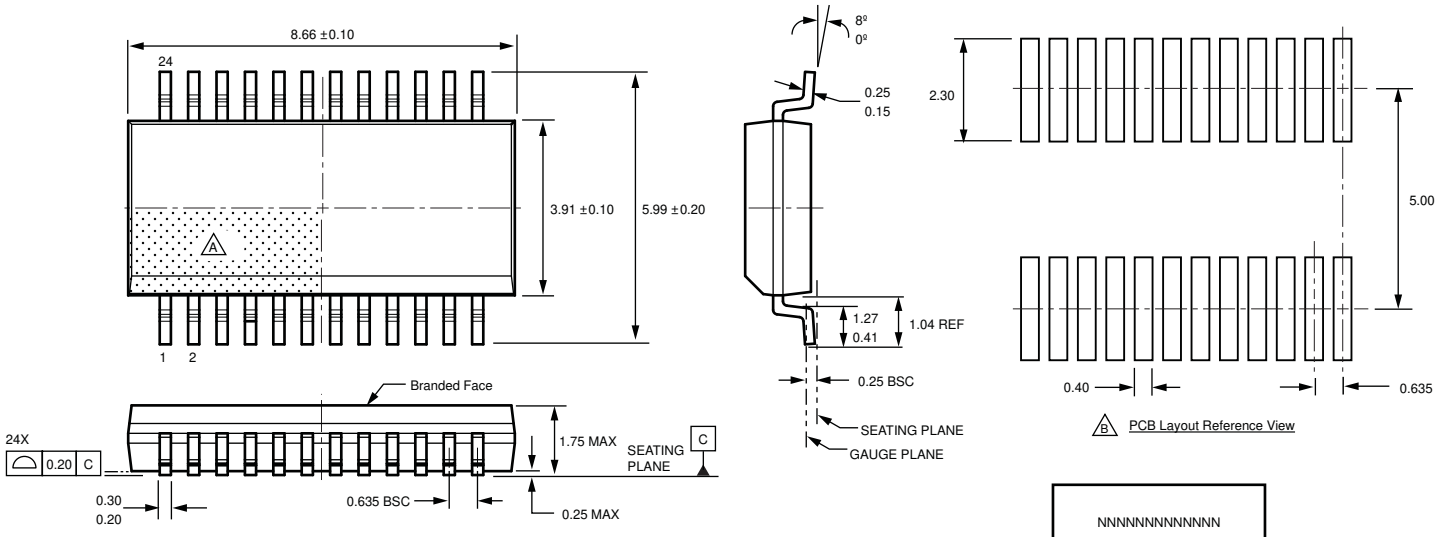
Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a patented technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

Package LF, 24-Pin QSOP



For Reference Only, not for tooling use (reference JEDEC MO-137 AE)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC7351 SOP63P600X175-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

N = Device part number
T = Temperature code
LF = (Literal) Package type
A = Amperage

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