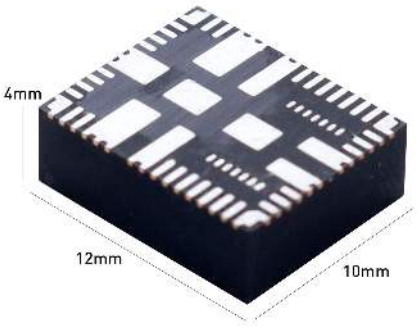
mEZDPD1620AS-84DF

mEZ20A-12Vin-1.8Vout-18A

DESCRIPTION

This is a fully integrated power module with a PMBus interface. This device offers a complete power solution with excellent load and line regulation over a wide input voltage range. It operates with high efficiency over a wide load range and can be paralleled to deliver a higher load current.

This power module adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control, which provides ultra-fast transient response and simple loop compensation. The PMBus interface provides module configurations and monitoring of key parameters.



SPECIFICATION OVERVIEW

I_{OUT}	18A
V_{OUT}	1.8V
Typical V_{IN}	12V
V_{IN} Min	9V
V_{IN} Max	15V

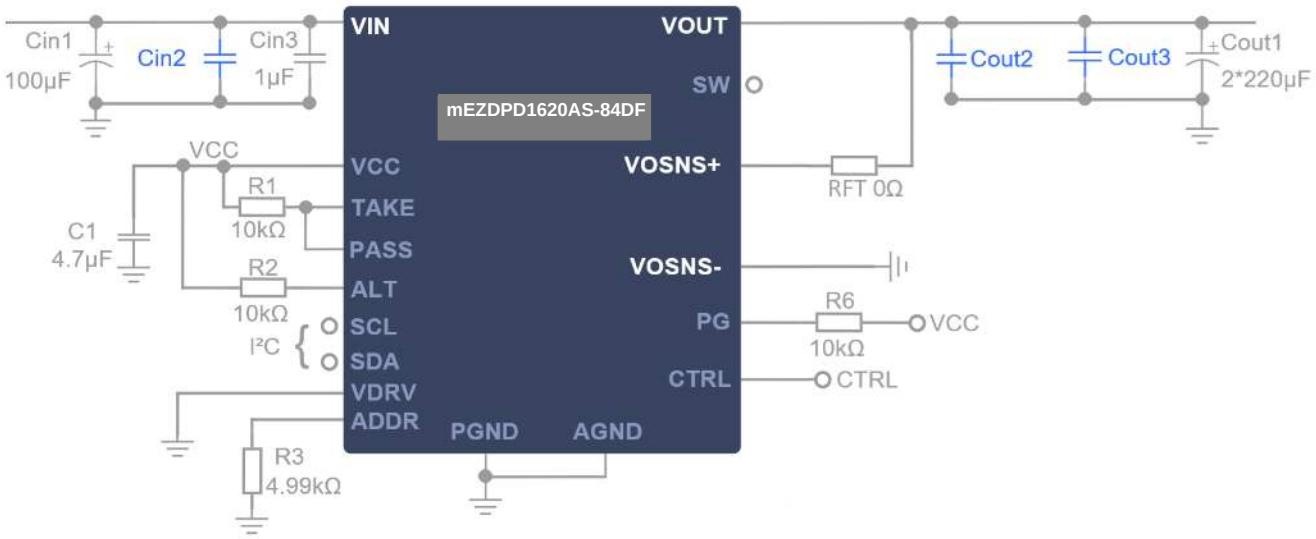
FEATURES

- Auto-Interleaving for Multi-Phase Operation
- Auto-Compensation with Adaptive MCOT for Ultra-Fast Transient Response
- 1% Reference Voltage over 0°C to +70°C Junction Temperature Range
- True Remote Sense of Output Voltage
- PMBus 1.3 Compliant
- Telemetry Readback, Including V_{IN}, V_{OUT}, I_{OUT}, Temperature, and Faults
- Available in a QFN-59 (10mmx12mmx4mm) Package

EFFICIENCY

Vin = 12V, Vout = 1.8V, Iout = 18A

TYPICAL APPLICATION



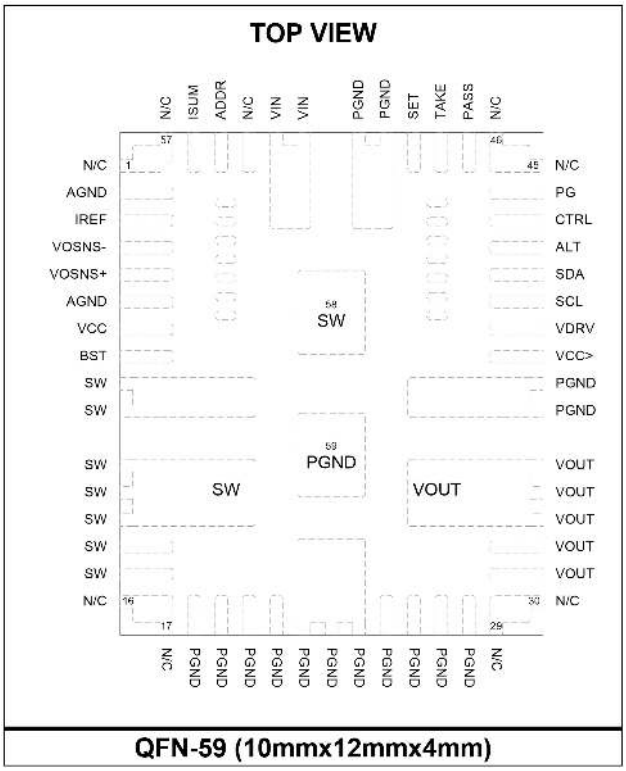
BOM

Reference	Quantity	Value	Description	Package	Manufacturer	Part Number
Cin1	1	100uF	Cap, Electrolytic, 35V	SMD	NIPPON CHEMI-CON	EMZJ350ADA101MF80G
Cin2	4	4.7uF	Cap,Ceramic,50V,X7R(material)	'1206'	MuRata	GRM31CR71H475K
Cin3	1	1uF	Cap, Ceramic, 25V, X7R	'0603'	Murata	GRM188R71E105KA12D
Cout1	2	220uF	Cap, Electrolytic, 6.3V, Tantalum	D2	Panasonic	EEFCX0J221R
Cout2	6	47uF	Cap,Ceramic,16V,X5R(material)	'1210'	MuRata	GRM32ER61C476K
Cout3		NS	NS			
C1	1	4.7uF	Cap, Ceramic, 25V, X7R	'0603'	Murata	GRM188R61E475KE11D
C2	1	4.7uF	Cap, Ceramic, 25V, X7R	'0603'	Murata	GRM188R61E475KE11D
R1	1	10kohm	Film Res,1%	'0603'	YAGEO	RC0603FR-0710KL
R2	1	10kohm	Film Res,1%	'0603'	YAGEO	RC0603FR-0710KL
R3	1	4.99kohm	Film Res,1%	'0603'	YAGEO	RC0603FR-074K99L
R6	1	10kohm	Film Res,1%	'0603'	YAGEO	RC0603FR-074K99L
RFT	1	0ohm	Film Res,1%	'0603'	YAGEO	RC0603FR-070RL
U1	1	-	Programmable 16V DC/DC Power module supply up to 20A	QFN-59 (10x12x4mm)	MPS	mEZDPD1620AS

ORDERING INFORMATION

Part Number	Finalize Design to Order
mEZDPD1620AS-84DF	https://www.monolithicpower.com/mezdpd1620as.html

PACKAGE REFERENCE



QFN-59 (10mmx12mmx4mm)

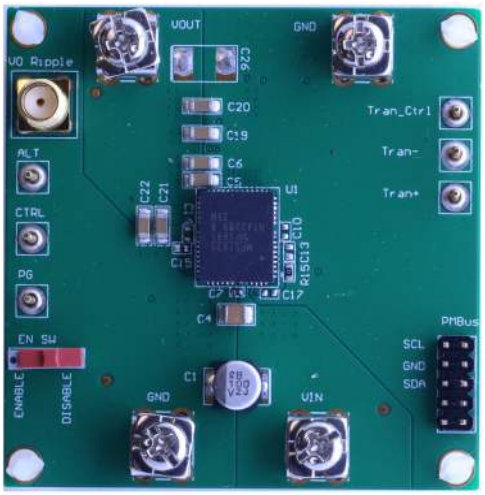
OTHER ORDERING OPTIONS

Evaluation Board for Surface Mount Device

The evaluation board is designed to demonstrate the capabilities of your custom MPS mEZDPD1620AS-84DF.

The EVB device is programmed with custom configuration.

Part Number
EVmEZDPD1620AS-00A



DIP Mount (Pin Out Version)

The mEZDPD1620AS-84DF is your custom device on a DIP mount for an easy-to-use, plug-and-play form factor.

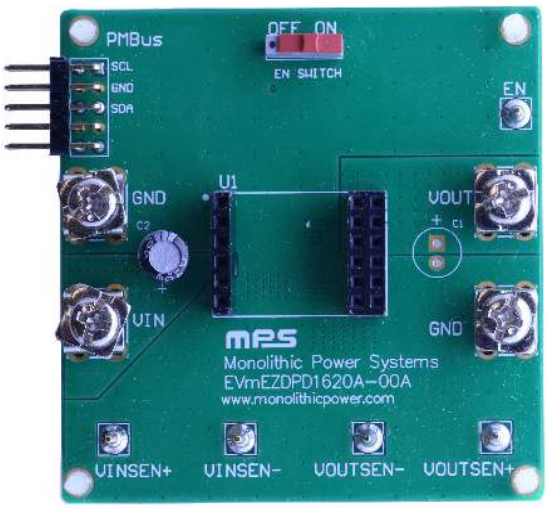
The pin out module device is programmed with custom configuration.

Part Number
mEZDPD1620A

Socket Evaluation Board for DIP Mount

DIP mount socket only. For easy evaluation of pin out module.

Part Number
EVmEZDPD1620A-00A



All EVB schematic and layout files can be found at:
https://www.monolithicpower.com/mezdpd1620as.html

PIN FUNCTIONS

PIN #	Name	Description
2, 6	AGND	**Analog ground.** Reference point of the control circuit.
3	IREF	**Current reference output.** Keep this pin floating.
4	VOSNS-	**Output voltage sense negative return.** Connect directly to the GND sense point of the load. Short to GND if remote sense is not used.
5	VOSNS+	**Output voltage sense positive return.** Connect this pin to the positive sense point of the output voltage to provide feedback voltage to the system.
7	VCC	**Output of the internal 3.3V LDO.** The driver and control circuits are powered by this voltage. Must be connected to pin 38.
8	BST	**Bootstrap.** Keep this pin floating.
9, 10, 11, 12, 13, 14, 15, 58	SW	**Switch node.** Keep them floating.
31, 32, 33, 34, 35	VOUT	**Module output voltage node.** Connect with wide PCB copper plane.
18-28, 36, 37, 50, 51, 59	PGND	**Power ground.** This pin is the reference point of the regulated output voltage. Connect with PCB copper planes as wide as possible.
38	VCC>	**Input of driver circuit.** Must be connected to pin 7.
39	VDRV	**Decoupling pin for 3.3V driver power supply.**
40	SCL	**PMBus serial clock.**
41	SDA	**PMBus serial data.**
42	ALT	**PMBus alert.** Open-drain output, active low. A pull-up resistor must be connected to a 3.3V rail.
43	CTRL	**Converter control.** CTRL is a digital input that turns the regulator on or off. Drive CTRL high to turn the regulator on, drive it low to turn the regulator off. Do not float this pin.
44	PG	**Multi-purpose power good output.** This pin can be configured as an output pin for single-phase operation, or as an input and output pin for multi-phase configuration. A pull-up resistor connected to a DC voltage must indicate high if the output voltage exceeds 90% of the nominal voltage. See the Application Information section for detailed configuration.
47	PASS	**Passes run signal to the next phase.** See the Applications Information section for connection details.
48	TAKE	**Receives run signal from the previous phase.** See the Typical Application on page 2 for connection details.
49	SET	**PWM signal.** The set signal turns on the HS-FET when a run signal appears. For multi-phase operation, tie the SET pins of all the phases together.
52, 53	VIN	**Supply voltage.** This pin provides power to the module. Decoupling capacitors must be connected between VIN and GND. Connect VIN with a wide copper plane.
55	ADDR	**PMBus slave address setting pin.** Connect a resistor between this pin and AGND to set the address of this device.
56	ISUM	**Reference current output.** For single-phase operation, keep this pin floating. For multi-phase operation, connect the ISUM pins of all phases together.
1, 16, 17, 29, 30, 45, 46, 54, 57	NC	**No internal connection.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN})..... 18V
$V_{SW (DC)}$.....-0.3V to V_{IN} + 0.3V
V_{SW} (25ns) (2) ..... -3V to +25V
V_{SW} (25ns)..... -5V to +25V
V_{OUT} 5.5V
V_{BST} .....V_{SW} + 4V
V_{CC}..... 4.5V
CTRL current (I_{CTRL}) 2.5mA
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A = +25°C) (3)
.....5W
Junction temperature ..... 170°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +170°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}).....4V to 16V
Output voltage (V_{OUT}) .....0.5V to 5.5V
External V_{CC} bias.....3.12V to 3.6V
CTRL current (I_{CTRL}) 1mA
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JB}	
QFN-59 (10x12x4mm)	17	3.4	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVM3695-25-RF-02A, 6-layer demo board PCB.

PROGRAMMABLE ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage						
Input voltage range	V_{IN}	Programmed value		9		V
Input over-voltage fault limit		Programmed value		16.5		V
Input over-voltage warning limit		Programmed value		16.5		V
Input voltage under-voltage warning limit		Programmed value		4		V
Output Voltage						
V_{OUT} command (6)	V_{OUT}	Programmed value		1.8		V
Output voltage scale	V_{OUT_SCALE}	Programmed value		0.25		
Output voltage margin high	$V_{OUT\_MARGIN\_HIGH}$	Programmed value		2.016		V
Output voltage margin low	$V_{OUT\_MARGIN\_LOW}$	Programmed value		1.535		V
Output voltage min	V_{OUT_MIN}	Programmed value		0.5		V
Output voltage max	V_{OUT_MAX}	Programmed value		6		V
Output voltage step	V_{OUT_STEP}	Programmed value		10		µs/mV
Current Limit						
Valley current limit	I_{LIM_VALLEY}	Programmed value		39		A
Min valley current limit programmable value (6)	$I_{LIM\_VALLEY\_MIN}$	Programmed value		0		A
Max current limit programmable value (6)	$I_{LIM\_VALLEY\_MAX}$	Programmed value		46.5		A
Low-side negative current limit in OVP	$I_{LIM\_NEG\_OVP}$	Programmed value		-10		A
Delay time after low-side negative current limit in OVP	t_{DELAY_NOCP}	Programmed value		100		ns
Output current limit (DC)	I_{LIM_DC}	Programmed value		38.962		A
Output over-current warning (DC)	I_{WARN_DC}	Programmed value		35.09		A
Over-current fault hiccup interval time	t_{ITV_HICCUP}	Programmed value		0		ms
Frequency						
Switching frequency	f_{SW}	Programmed value		800		kHz
Output Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}	Programmed value		115%		V_{REF}
UVP threshold	V_{UVP}	Programmed value		50%		V_{REF}
Soft Start and Turn On/Off Delay						
Soft-start time	t_{SS}	Programmed value		2		ms
Turn-on delay (6)	t_{ON_DELAY}	Programmed value		0		ms
Turn-off delay	t_{OFF_DELAY}	Programmed value		0		ms

Under-Voltage Lockout (UVLO)						
Input programmable turn-on voltage	V_{IN_ON}	Programmed value		8		V
Input programmable turn-off voltage	V_{IN_OFF}	Programmed value		5		V
Min input programmable turn-on voltage	$V_{IN\_ON\_MIN}$	Programmed value, V_{CC} = 3.3V		3		V
Max input programmable turn-on voltage	$V_{IN\_ON\_MAX}$	Programmed value		15		V
Min input programmable turn-off voltage (6)	$V_{IN\_OFF\_MIN}$	Programmed value, V_{CC} = 3.3V		2.75		V
Max input programmable turn-off voltage	$V_{IN\_OFF\_MAX}$	Programmed value		7.75		V
Power Good						
Power good high threshold, PG_ON	PG_{Vth_Hi}	Programmed value		90%		V_{REF}
Power good low threshold, PG_OFF	PG_{Vth_Lo}	Programmed value		70%		V_{REF}
Power good low-to-high delay, PG delay	PG_{Td}	Programmed value		1		ms
Thermal Protection (TP)						
TP fault rising threshold (6)	T_{SD_RISE}	Programmed value		155		°C
TP warning rising threshold (6)	T_{WARN_RISE}	Programmed value		145		°C
TP hysteresis		Programmed value		20		°C
Compensation						
Ramp		Programmed value		5.6		mV

PROGRAMMABLE OPERATION SETTINGS

Name	Selected Mode	Description	Notes
Output Voltage			
Output voltage discharge	1	0: No active 1: At CTRL low	
Output voltage range	10	Chooses the internal voltage divider ratio. 00: External divider (0.5~0.672V) 01: Internal divider2:1 (0.5~1.344V) 10: Internal divider4:1 (0.7~2.688V) 11: Internal divider8:1 (1.3~5.376V)	
Light-Load Operation Mode			
Skip CCM (SYNC)	1	0: Pulse skip mode 1: Forced CCM	
Protection Response			
Over-current response	0	0: Latch-off 1: Retry	
Output over-voltage response	0	0: Latch-off with output discharge 1: Latch-off without output discharge 2: HICCUP with output discharge 3: HICCUP without output discharge	
TP response	0	0: Latch-off 1: Retry	
Compensation			
Slave Fault Detection	1	Enable or disable the slave fault detection function through the PG pin. 0: Enable 1: Disable	
Operation			
Operation	0	Operation is a paged register. The operation command turns the converter output on/off in conjunction with input from the CTRL pin. It also sets the output voltage to the upper or lower MARGIN voltages. 0: On 1: Soft off 2: Immediate off 3: Margin low (ignore fault) 4: Margin low (act on fault) 5: Margin high (ignore fault) 6: Margin high (act on fault)	

On/Off Configuration			
PON	1	0: Enable converter (converter powers up any time the input voltage is present regardless of the state of the CTRL pin) 1: Disable converter (converter does not power up until commanded by the CTRL pin and operation command)	
OP	1	0: Ignore (converter ignores the "on" bit in the operation command from the PMBus) 1: Response (converter responses the "on" bit in the operation command from the PMBus)	
EN	1	0: Ignore CTRL pin (on/off controlled only by the operation command) 1: Require CTRL pin	
POL	1	0: Active low (Pull the CTRL pin low to start the converter) 1: Active high (Pull the CTRL pin high to start the converter)	
Write Protect			
Write protect	0	Controls writing to the converter. 0: Enable all 1: Disable function 1 (disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands) 2: Disable function 2 (disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands) 3: Disable function 3 (disable all writes except to the WRITE_PROTECT command)	
Address PMBus			
Enable	0	Address selection method 0: The address is decided by the ADDR pin 1: The address is decided by MFR_ADDR_PMBUS	
Address	0	Device Address	ADDR
Extra Functions			
Total OC hiccup interval	0	0: Fixed OCP hiccup interval 1: Adjustable OCP hiccup	
OSM	0	0: Enable OSM (output sink mode) 1: Disable OSM	
Phase operation	0	0: For single-phase operation 1: For multi-phase operation	

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A= -40°C to 125°C, typical values refer to T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Supply Current						
Supply current (shutdown)	I_{IN}	V_{CTRL} = 0V		2.5	4	mA
Output Voltage						
Load regulation (6)	$V_{OUT\_DC\_LOAD}$	I_{OUT} from 0A to 25A		±0.5		% V_{OUT}
Line regulation (6)	$V_{OUT\_DC\_LINE}$	V_{IN} from 4V to 16V, I_{OUT} = 20A		±0.5		% V_{OUT}
CTRL						
CTRL on threshold	$CTRL_{ON}$			2.04	2.2	V
CTRL off threshold	$CTRL_{OFF}$			1.66		V
Frequency and Timer						
Minimum on time (6)	t_{ON_MIN}	f_{SW} = 1000kHz, V_O = 0.6V		50		ns
Minimum off time (6)	t_{OFF_MIN}	V_{FB} = 580mV		220		ns
Output Over-Voltage and Under-Voltage Protection						
OSM threshold rising	V_{OSM_RISE}			104%		V_{REF}
OSM threshold falling	V_{OSM_FALL}			102%		V_{REF}
ADC (6)						
Voltage range			0		1.28	V
ADC resolution				10		Bits
DNL				1		LSB
Sample rate				3		kHz
DAC (Feedback Voltage)						
Range			500	600	672	mV
Feedback accuracy	V_{FB}	T_J = 25°C	594	600	606	mV
Feedback accuracy	V_{FB}	T_J = -40°C to +125°C	591	600	609	mV
Resolution (6)		Per LSB		2		mV
Feedback voltage with margin high (6)	$V_{FB\_MG\_HIGH}$			672		mV
Feedback voltage with margin low (6)	$V_{FB\_MG\_LOW}$			500		mV
Error Amplifier						
Feedback current	I_{FB}	V_{FB} = V_{REF}		50	100	nA
Soft Shutdown						
Soft shutdown discharge FET	R_{ON_DISCH}			60		Ω
Under-Voltage Lockout (UVLO)						
VCC under-voltage lockout threshold rising	VCC_{Vth}	Default setting	2.6	2.75	2.9	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}	Default setting	200	Default setting		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
Power good leakage current	$I_{PG\ LEAK}$	V_{PG} = 3V		1.5		µA
Power good low-level output voltage	$V_{OL\ 100}$	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor, T_J = 25°C		600	720	mV
	$V_{OL\ 10}$	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor, T_J = 25°C		700	820	
Monitoring Parameters						
Output voltage monitor accuracy	$M_{VOUT\ ACC}$	V_O = 0.6V	-2%	0.6	2%	V
Output voltage bit resolution				1.5		mV
Output current monitor accuracy (6)	$M_{IOUT\ ACC}$	V_O = 1.2V, f_{SW} = 600kHz, I_O = 20A	-10%	20	10%	A
Output current bit resolution (6)				62.5		mA
Input voltage monitor accuracy	$M_{IN\ ACC}$		-2%	12	2%	V
Input voltage bit resolution (7)				25		mV
PMBus DC Characteristics (SDA, SCL, ALERT) (6)						
Input high voltage	V_{IH}				2.1	V
Input low voltage	V_{IL}		0.8			V
Output low voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Input leakage current	I_{LEAK}	SDA, SCL, ALERT = 3.3V	-10		10	µA
Maximum voltage (SDA, SCL, ALERT, CTRL)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	3.6	V
Pin capacitance on SDA,SCL	C_{PIN}				10	pF
PMBus Timing Characteristics (7)						
Min operating frequency				10		kHz
Max operating frequency				1000		kHz
Bus free time		Between stop and start conditions	4.7			µs
Holding time			4.0			µs
Repeated start condition set-up time			4.7			µs
Stop condition set-up time			4.0			µs
Data hold time			300			ns
Data set-up time			250			ns
Clock low time out			25		35	ms
Clock low period			4.7			µs
Clock high period			4.0		50	µs
Clock/data fall time					300	ns
Clock/data rise time					1000	ns

Notes:

6) Guaranteed by design, not tested in production. The parameter is tested during parameters characterization.
7) Typical Performance Characteristics.

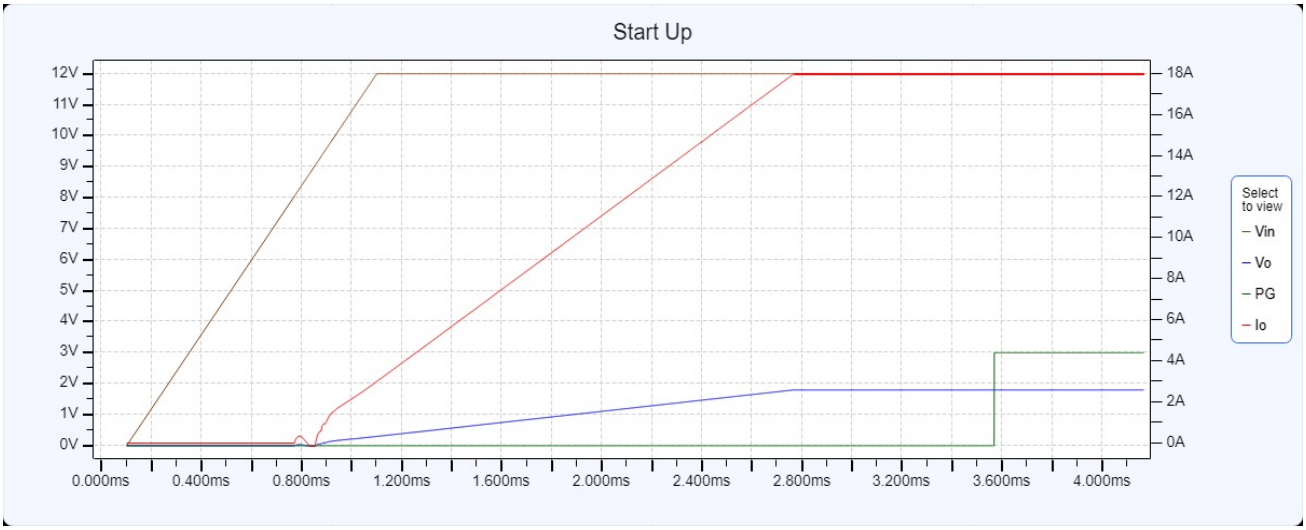
TYPICAL PERFORMANCE CHARACTERISTICS

All waveforms simulated.

EFFICIENCY

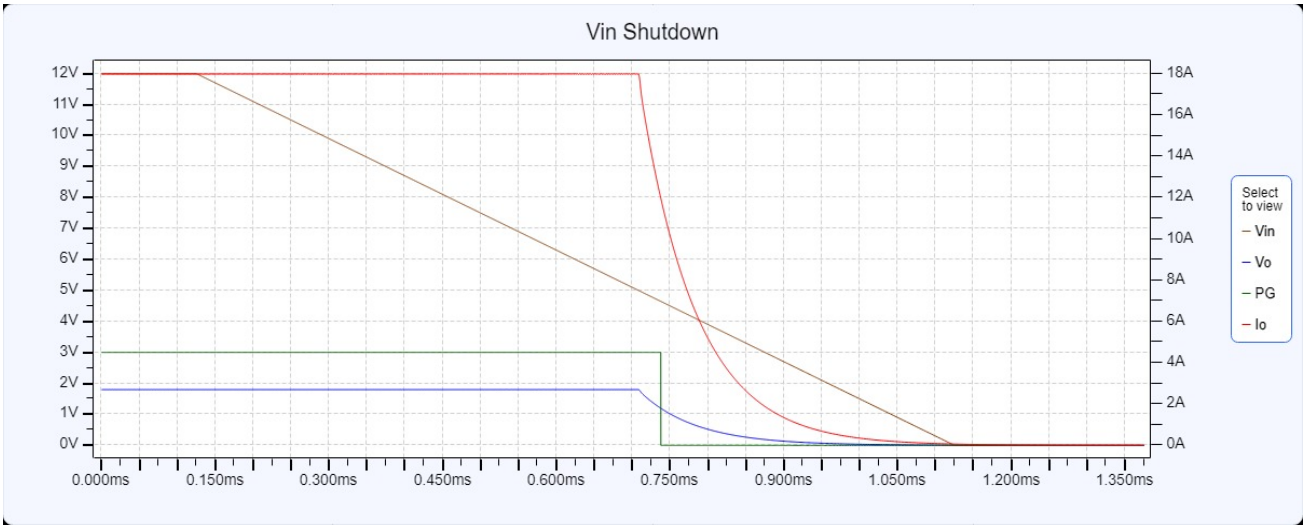
Vin = 12V, Vout = 1.8V, Iout = 18A

START UP



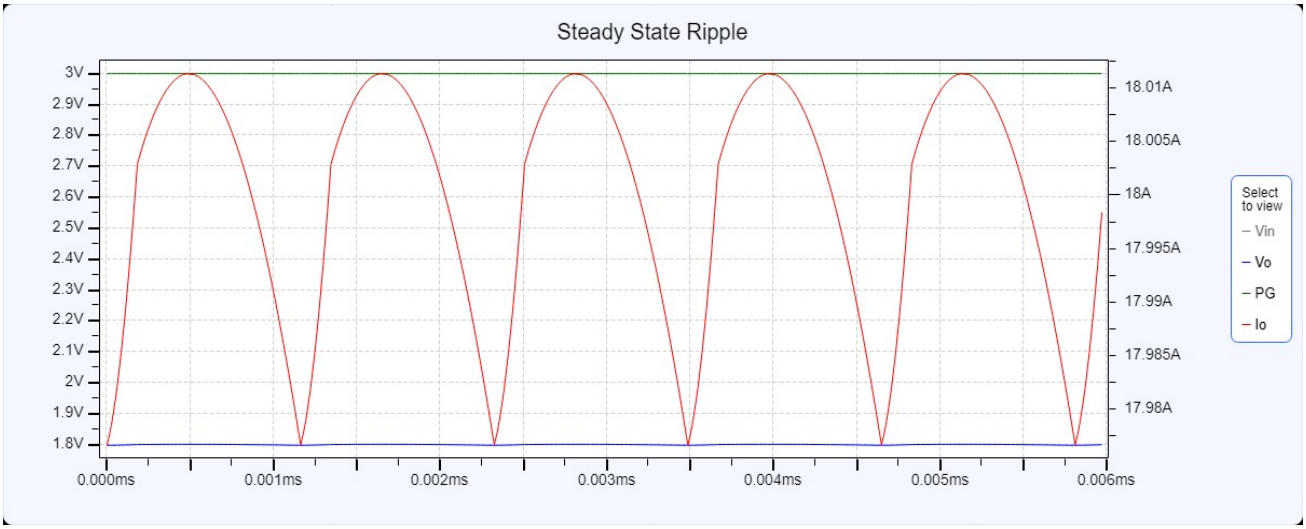
Vin = 12V, Iout = 18A

VIN SHUTDOWN



Vin = 12V, Iout = 18A

STEADY STATE RIPPLE



Vin = 12V, Iout = 18A

LOAD TRANSIENT

Vin = 12V, Ihigh = 18A, Ilow =9A, Slew rate = 1A/µs

FUNCTIONAL BLOCK DIAGRAM

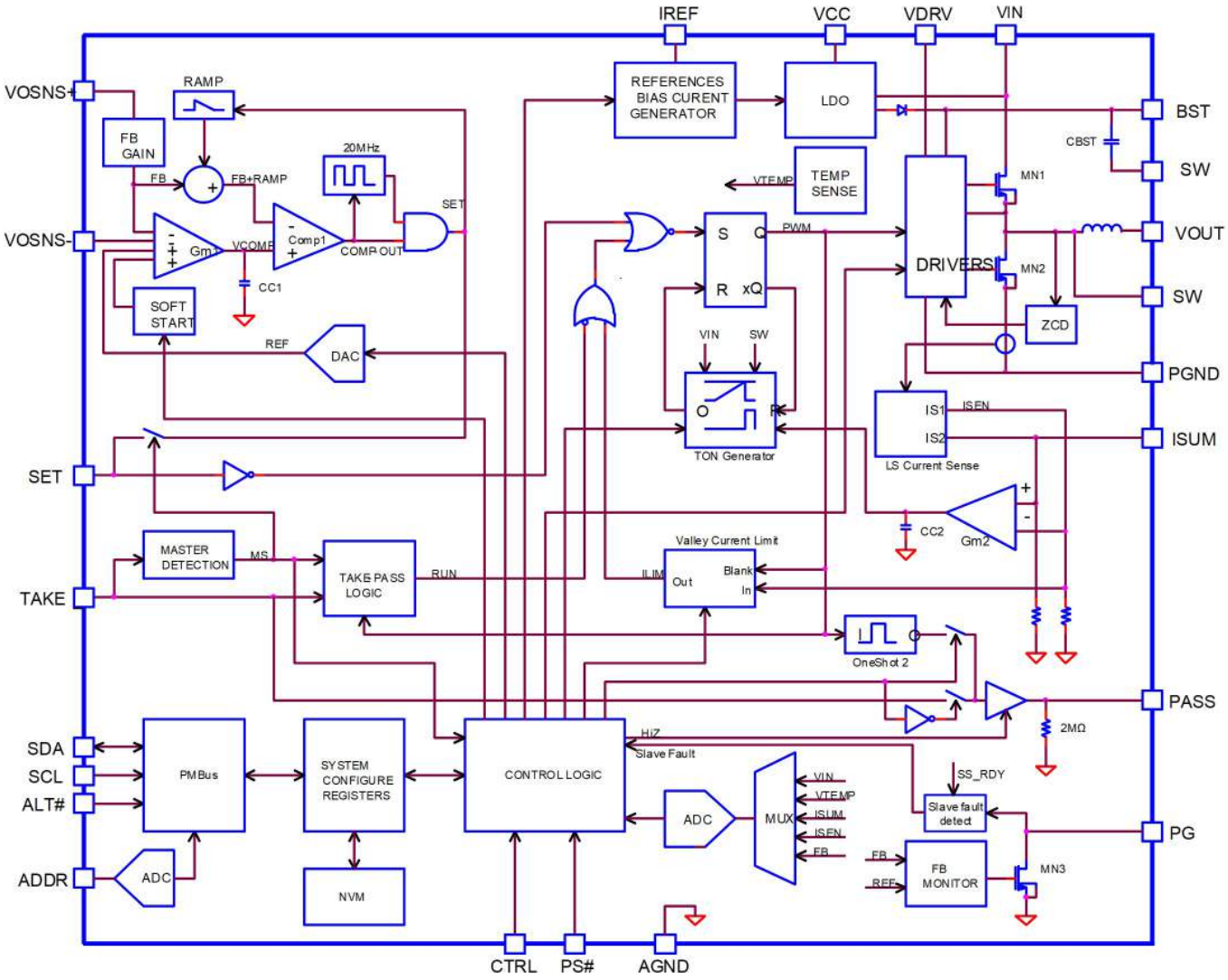


Figure 1: Functional Block Diagram

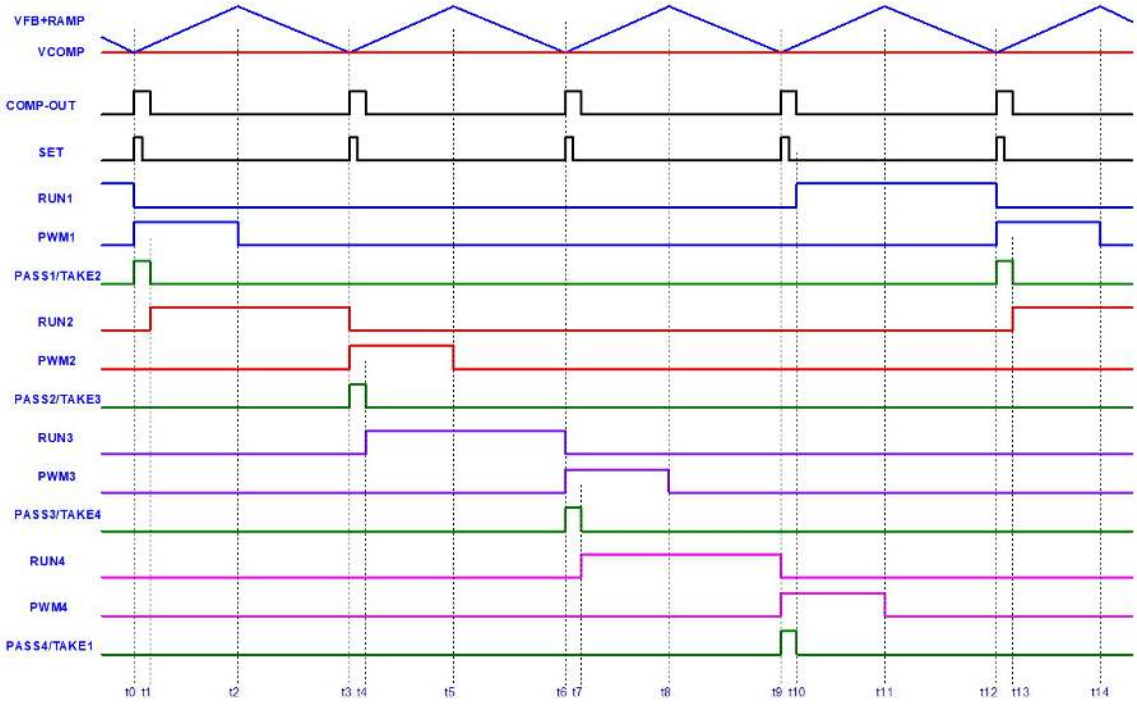


Figure 2: Multi-Phase Operation Timing Diagram (Steady State)

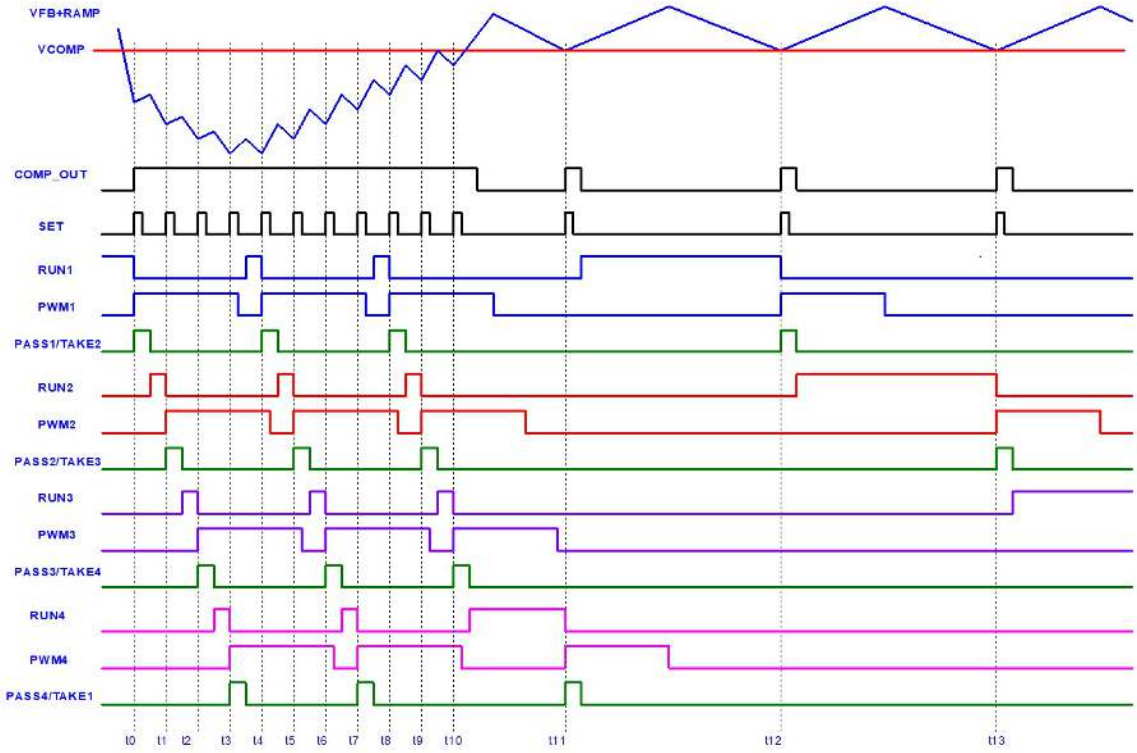


Figure 3: Multi-Phase Operation Timing Diagram (Transient)

OPERATION

This device is a fully integrated power solution in a 10mmx12mmx4mm QFN package. For higher current applications, this device can be connected in parallel to provide a higher output current. This device employs constant-on-time (COT) control to provide fast transient response. The internal ramp compensation guarantees stable operation for applications using zero-ESR ceramic output capacitors.

RAMP Compensation

This device guarantees stable operation with zero-ESR ceramic output capacitors by using internal RAMP compensation. A triangular RAMP signal is generated internally, and is superimposed on the FB signal. The triangular RAMP signal starts to rise once RAMP+FB drops below the REF signal, and a SET pulse is generated. The rise time of the RAMP signal is fixed. The amplitude of the RAMP compensation is selectable through the PMBus command of D0h[3:1] to support wide operation configurations. There is a trade-off between the stability and load transient response. A larger RAMP signal provides higher stability, but a slower load transient response, and vice versa. Consequently, it is necessary to optimize the RAMP compensation selection based on the design criteria for each application.

APPLICATION INFORMATION

Operation Mode Selection

This device provides both forced CCM and pulse-skip operation in a light-load condition.

Output Voltage Setting

A feedback resistor divider is required to set the proper feedback gain. The values of the feedback resistors are determined using Equation (1):

$$R_2(k\Omega) = \frac{0.6}{V_O - 0.6} \times R_1(k\Omega) \quad (1)$$

where V_O is the output voltage. The output voltage feedback gain is determined with Equation (2):

$$G_{FB} = \frac{R_2}{R_1 + R_2} \quad (2)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) must be placed in parallel with R1. Table 1 lists the values of the feedback resistors and the feed-forward capacitor for common output voltages.

Table 1: Common Output Voltages

V_O	R_1 (kΩ)	R_2 (kΩ)	C_{FF} (nF)
0.9	0.5	1	33
1.2	1	1	33
1.8	2	1	33
3.3	4.53	1	4.7
5	7.32	1	4.7

This device offers output voltage programmability through the PMBus. In addition, the output voltage can be adjusted within a certain range through the PMBus by adjusting the internal reference voltage of the PMW controller (V_{REF}). The reference voltage, which has a default value of 0.6V, can be adjusted between 0.5V and 0.672V. For a given feedback resistor network, the upper and lower limits of the output voltage are determined with Equation (3a) and Equation (3b):

$$V_{o,max} = \frac{0.672}{G_{FB}} \quad (3a)$$

$$V_{o,min} = \frac{0.5}{G_{FB}} \quad (3b)$$

Two steps must be followed to program the output voltage through the PMBus:

1. Write the G_{FB} value determined by Equation (2) to register VOUT_SCALE_LOOP (29h).
2. Write the output voltage command to register VOUT_COMMAND (21h).

V_{REF} is updated automatically based on the output voltage command and G_{FB}.

Output voltage monitoring through the PMBus is enabled by setting the register VOUT_SCALE_LOOP (29h) with a value that matches the G_{FB} value from Equation (2).

For applications where a PMBus interface is not required, V_{REF} = 0.6V is used by default, and operates in analog mode. The feedback resistors should be determined based on Equation (1).

Soft Start

The soft-start (SS) time can be programmed through the PMBus.

Pre-Bias Start-Up

The device is designed for monotonic start-up into pre-biased loads. If the output voltage is pre-biased to a certain voltage during start-up, both the high-side and low-side switches are disabled until the internal reference voltage exceeds the sensed output voltage at FB.

Output Voltage Discharge

The output voltage discharge mode is enabled if the device is disabled through the CTRL pin. In such a case, both the high-side and low-side switches are latched off. A discharge FET connected between SW and GND turns on to discharge the output capacitor. A typical on resistance of the discharge FET is 60Ω. Once the FB voltage drops below 10% of the reference output voltage, the discharge FET turns off.

This feature can be enabled or disabled through the MFR_CTRL_VOUT (D1h) command.

Current Sense and Over-Current Protection (OCP)

This device features on-die current sense and a programmable positive current limit threshold.

The device provides both inductor valley current limits (set by register D7h).

Inductor Valley Over-Current Protection (D7h)

During the LS-FET on state, the inductor current is sensed and monitored cycle by cycle. The HS-FET is only be allowed to turn on if over-current is not detected during the LS-FET on state. If 31 consecutive cycles of an OC condition are detected, OCP is triggered.

During an over-current condition or output short-circuit condition, if the output voltage drops below the under-voltage protection (UVP) threshold, the device enters OCP immediately.

Once OCP is triggered, it either enters hiccup mode or latch-off mode, depending on the register. It should be noted that V_{CC} or CTRL must be power recycled to re-enable the device once it latches off.

The inductor valley over-current limit can be programmed through register D7h, which sets the per-phase inductor valley current limit for both single-phrase and multi-phase operation.

Negative Inductor Current limit

When the LS-FET detects a negative current lower than the limit set through register D5h[2], the part turns off its LS-FET for a period of time to limit the negative current. The period is set through register D5h[3].

Under-Voltage Protection (UVP)

The device monitors the output voltage through the FB pin to detect an under-voltage condition. If the FB voltage drops below the UVP threshold (set through register VOUT_UV_FAULT_LIMIT), UVP is triggered. After UVP is triggered, the device enters either hiccup or latch-off mode, depending on the PMBus selection. Please note that V_{CC} or CTRL must be power recycled to re-enable the device once it latches off.

Over-Voltage Protection (OVP)

The device monitors the output voltage using the FB pin connected to the tap of a resistor divider to detect an over-voltage condition. See the register VOUT_OV_FAULT_RESPONSE section for additional information on OVP.

Output Sinking Mode (OSM)

The device enters OSM when the output voltage is more than 5% above the reference and below the OVP threshold. Once OSM is triggered, the device runs in forced CCM. The device exits OSM when the HS-FET turns back on.

Over-Temperature Protection (OTP)

The device monitors the junction temperature. If the junction temperature exceeds the threshold value (set by register OT_FAULT_LIMIT), the converter enters either hiccup or latch-off mode depending on the PMBus selection. Please note that V_{CC} or CTRL must be power recycled to re-enable the device once it latches off.

Power Good (PG)

The device has an open-drain power-good (PG) output. The PG pin can be configured as an output only, or as an input and output pin by bit [0] of register MRF_CTRL_COMP (D0h). For single-phase configuration, PG should be configured as output-only. For multi-phase operation, PG should be configured as an input and output pin to detect faults from the slave phases. PG must be pulled high to V_{CC} or a voltage source with less than 3.6V through a pull-up resistor (typically 100kΩ).

PG is pulled low initially once input voltage is applied to the device. After the FB voltage reaches the threshold set by register POWER_GOOD_ON, and a delay set by the register MFR_CTRL_VOUT, PG is pulled high.

PG is latched low if any fault occurs, and the relevant protection feature is triggered (e.g. UV, OV, OT, UVLO, etc.). After PG is latched low, it cannot be pulled high again unless a new soft start is initialized.

If the input supply fails to power the device, PG is latched low. Figure 4 shows the relationship between the PG voltage and the pull-up current.

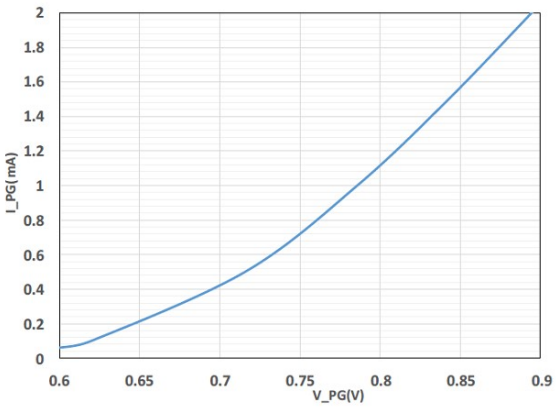


Figure 4: Power-Good Current vs. Power-Good Voltage

Input Capacitor

The buck converter has a discontinuous input current, and requires a capacitor to supply the AC current to the step-down module while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to the IN pin as possible.

The capacitance can vary significantly with temperature. It is recommended to use capacitors with X5R and X7R ceramic dielectrics, because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current using Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple using Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (7)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs. Estimate the output voltage ripple using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (8)$$

Where the module internal inductor is 0.36µH.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The ESR dominates the impedance at the switching frequency for POSCAPs, so the output voltage ripple is determined by the ESR value.

For simplification, the output ripple can be approximated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

PCB Layout Guidelines

PCB layout plays an important role to achieve stable operation. For optimal performance, refer to Figure 5 and follow the guidelines below:

1. Place the input ceramic capacitors as close to the VIN and PGND pins as possible on the same layer of the DEVICE.
2. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
3. Place VIN vias at least 1cm from the part to minimize noise coupling from input pulsating current.
4. Connect AGND to a solid ground plane through a single point.
5. Place sufficient output GND vias close to the GND pins to minimize both parasitic impedance and thermal resistance.
6. Keep the ISUM trace as short as possible. The ISUM trace should be away from the VIN copper in a multi-phase configuration. Vias should be avoided whenever possible.
7. The keep-out area must be kept clean.
8. Signal traces should avoid the area directly beneath the SW pad unless a PGND layer is used to provide shielding.

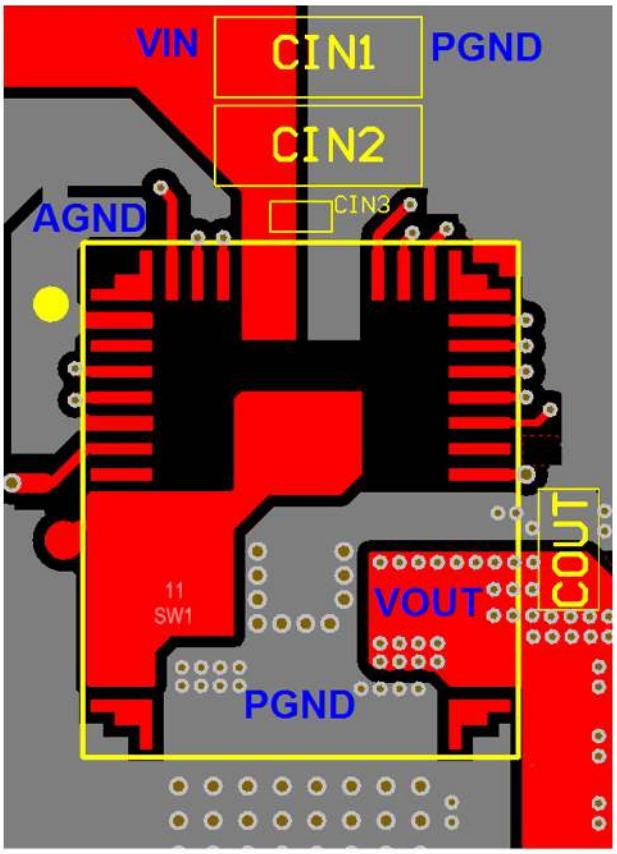
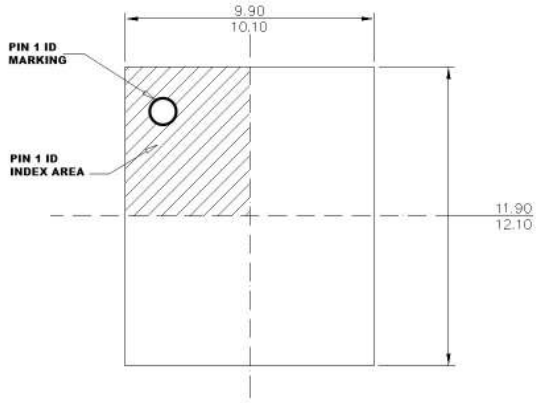


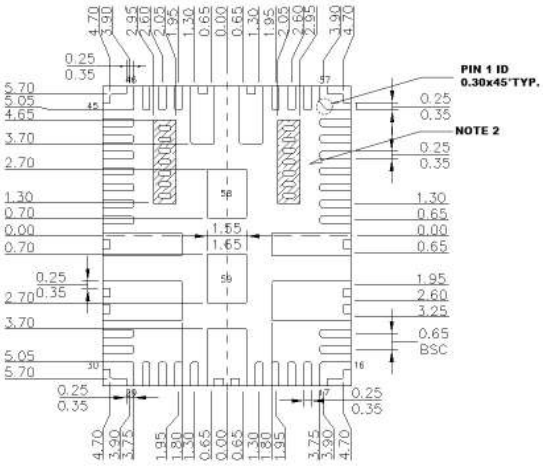
Figure 5: Example Layout - Top Layer

PACKAGE INFORMATION

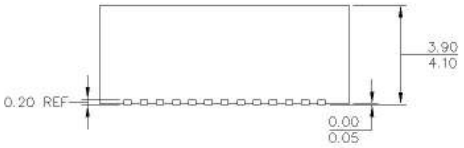
QFN-59 (10mmx12mmx4mm)



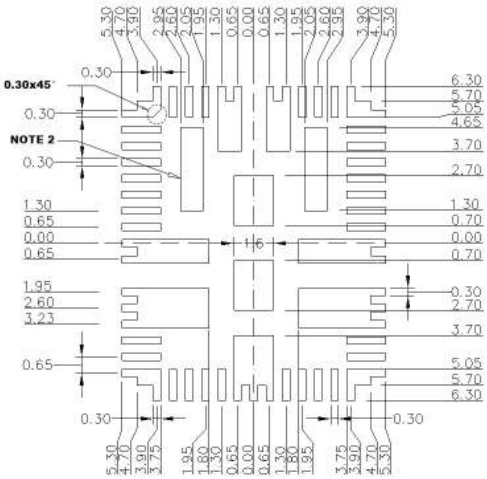
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.