

### SOP-8



#### Pin Definition:

- |           |          |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate   | 5. Drain |

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
-30	14 @ $V_{GS} = -10V$	-11
	20 @ $V_{GS} = -4.5V$	-8.5

### Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

### Application

- Load Switches
- Notebook PCs
- Desktop PCs

### Ordering Information

Part No.	Package	Packing
TSM4425CS RLG	SOP-8	2.5Kpcs / 13" Reel

**Note:** "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

### Absolute Maximum Rating ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	-11	A
Pulsed Drain Current	$I_{DM}$	-50	A
Continuous Source Current (Diode Conduction) <sup>a,b</sup>	$I_S$	-2.1	A
Maximum Power Dissipation	$P_D$	$T_a = 25^\circ C$	2.5
		$T_a = 75^\circ C$	1.6
Operating Junction Temperature	$T_J$	+150	$^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	$^\circ C$

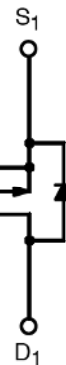
### Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot Thermal Resistance	$R_{\theta JF}$	18	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	52.5	$^\circ C/W$

#### Notes:

- Pulse width limited by the Maximum junction temperature
- Surface Mounted on FR4 Board,  $t \leq 10$  sec.

### Block Diagram



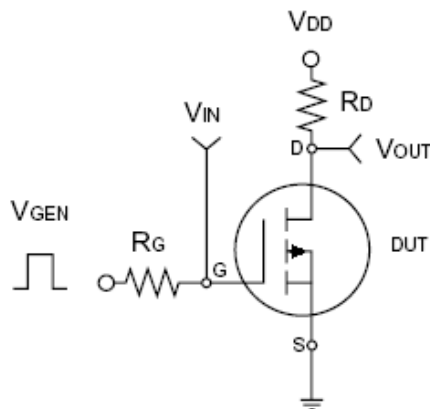
P-Channel MOSFET

**Electrical Specifications** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

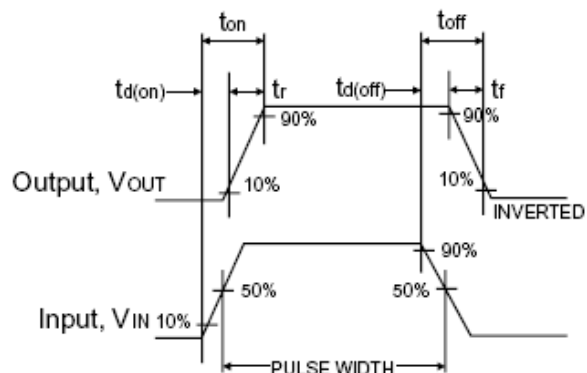
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	$BV_{DSS}$	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1	--	-3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = -30V, V_{GS} = 0V$	$I_{DSS}$	--	--	-1.0	$\mu A$
On-State Drain Current <sup>a</sup>	$V_{DS} = -5V, V_{GS} = -10V$	$I_{D(ON)}$	-50	--	--	A
Drain-Source On-State Resistance <sup>a</sup>	$V_{GS} = -10V, I_D = -11A$	$R_{DS(ON)}$	--	10	12	m $\Omega$
	$V_{GS} = -4.5V, I_D = -8.5A$		--	15	19	
Forward Transconductance <sup>a</sup>	$V_{DS} = -15V, I_D = -11A$	$g_{fs}$	--	23	--	S
Diode Forward Voltage	$I_S = -2.1A, V_{GS} = 0V$	$V_{SD}$	--	--	-1.3	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$V_{DS} = -15V, I_D = -11A, V_{GS} = -10V$	$Q_g$	--	64	--	nC
Gate-Source Charge		$Q_{gs}$	--	11	--	
Gate-Drain Charge		$Q_{gd}$	--	25	--	
Input Capacitance	$V_{DS} = -8V, V_{GS} = 0V, f = 1.0MHz$	$C_{iss}$	--	3680	--	pF
Output Capacitance		$C_{oss}$	--	930	--	
Reverse Transfer Capacitance		$C_{rss}$	--	620	--	
<b>Switching<sup>c</sup></b>						
Turn-On Delay Time	$V_{DD} = 15V, R_L = 15\Omega, I_D = -11A, V_{GEN} = -10V, R_G = 6\Omega$	$t_{d(on)}$	--	15	--	ns
Turn-On Rise Time		$t_r$	--	13	--	
Turn-Off Delay Time		$t_{d(off)}$	--	100	--	
Turn-Off Fall Time		$t_f$	--	53	--	

Notes:

- a. pulse test:  $PW \leq 300\mu s$ , duty cycle  $\leq 2\%$
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.



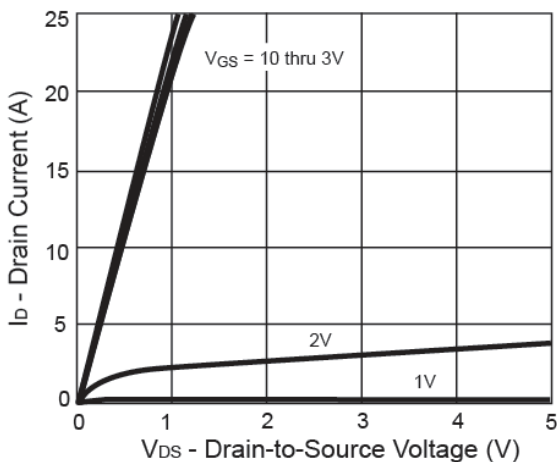
**Switching Test Circuit**



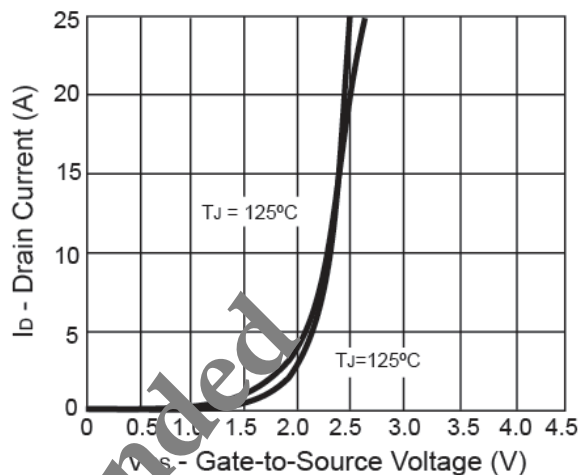
**Switchin Waveforms**

**Electrical Characteristics Curve**

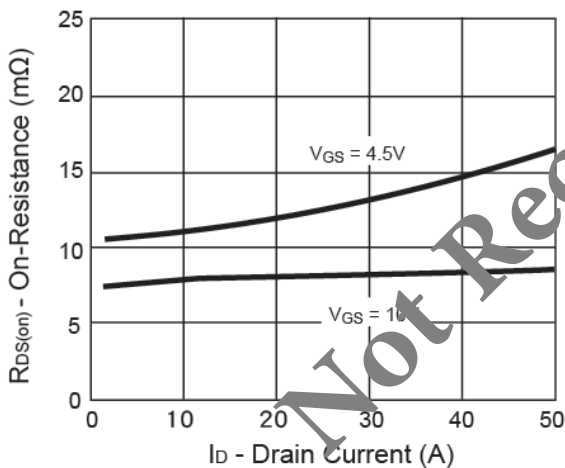
**Output Characteristics**



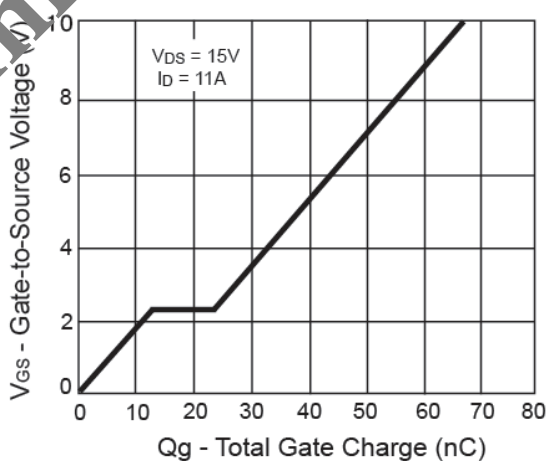
**Transfer Characteristics**



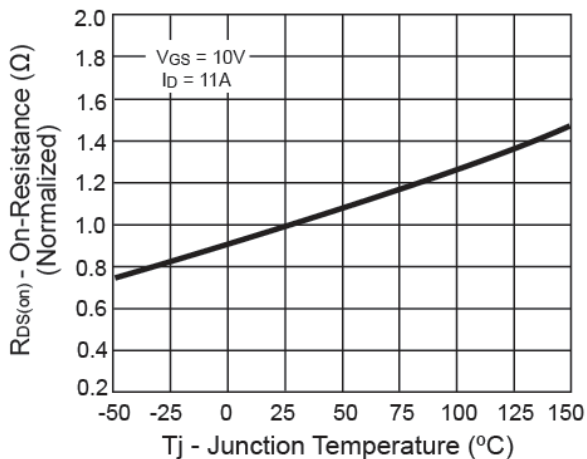
**On-Resistance vs. Drain Current**



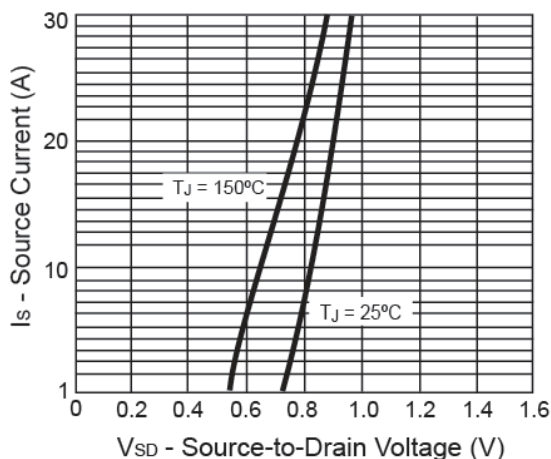
**Gate Charge**



**On-Resistance vs. Junction Temperature**

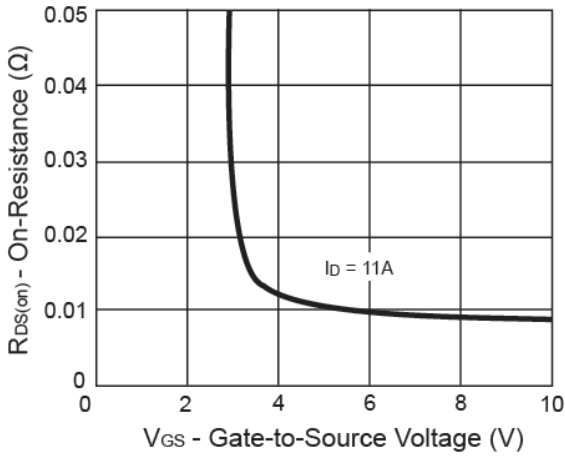


**Source-Drain Diode Forward Voltage**

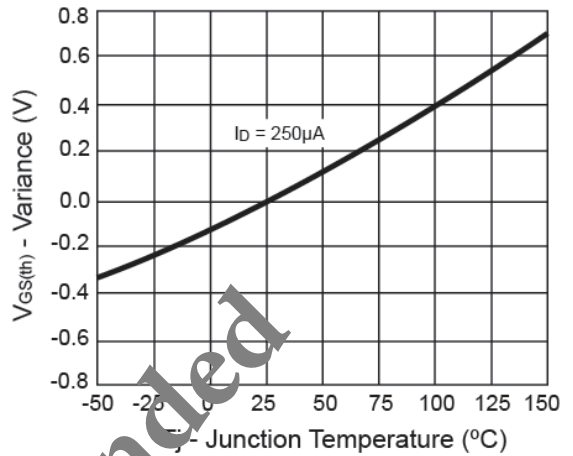


**Electrical Characteristics Curve**

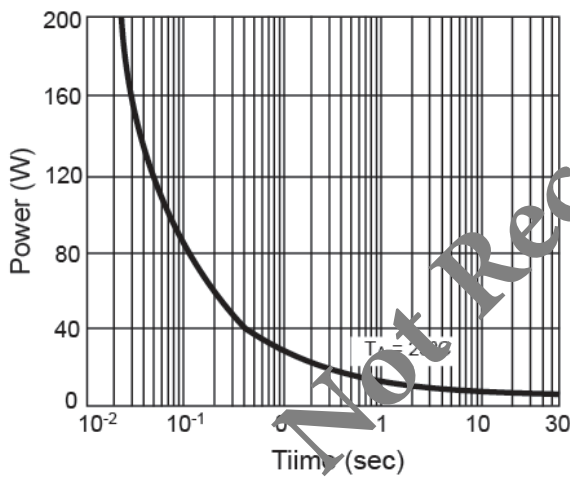
**On-Resistance vs. Gate-Source Voltage**



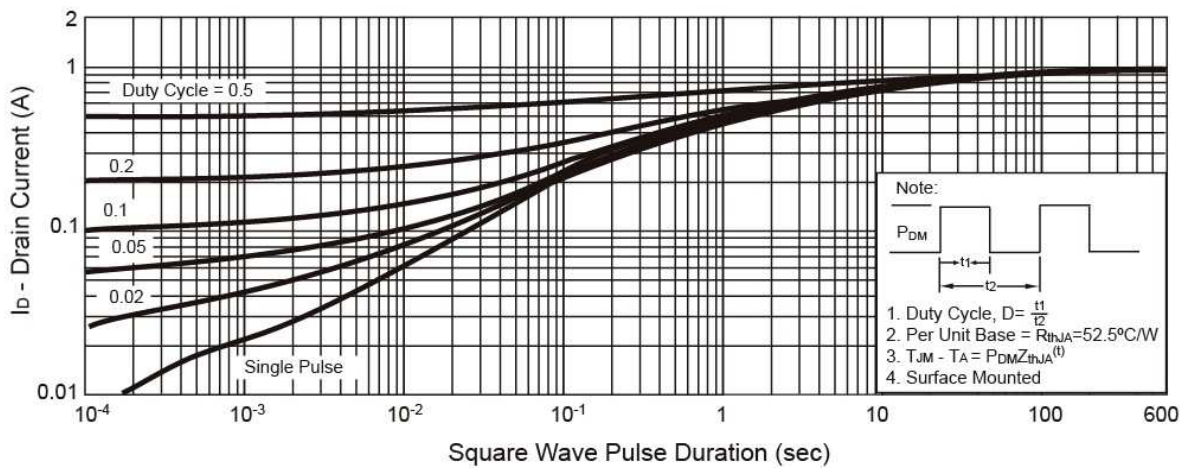
**Threshold Voltage**



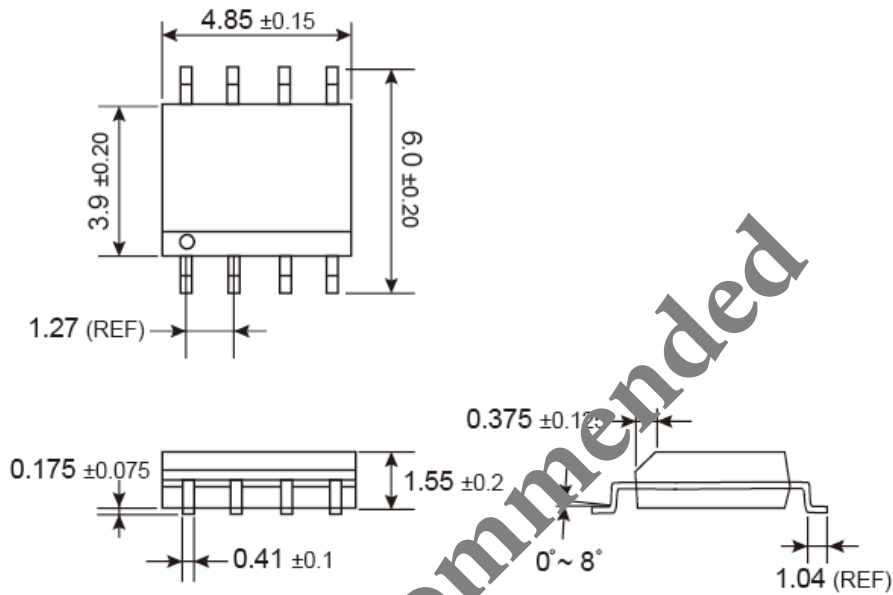
**Single Pulse Power**



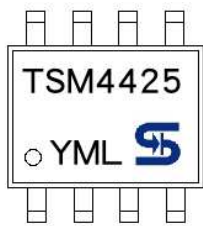
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**SOP-8 Mechanical Drawing**



**Marking Diagram**



Not Recommended

- Y = Year Code
- M = Month Code for Halogen Free Product
  - O =Jan    P =Feb    Q =Mar    R =Apr
  - S =May    T =Jun    U =Jul    V =Aug
  - W =Sep    X =Oct    Y =Nov    Z =Dec
- L = Lot Code



# TSM4425

## 30V P-Channel MOSFET

**Not Recommended**

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