Product introduction

SN74LVC1G04 is a non gate integrated circuit, which can realize the mathematical logic operation of Y=A. It is designed with advanced CMOS technology, which has the characteristics of low power consumption and high output driving ability. The chip can work normally when the voltage of VCC is between 1.65v and 5.5V. And 74lvc1g04 has a variety of small package shapes, which can be widely used in high-end precision instruments, miniaturized low-power handheld devices, and artificial intelligence and other fields.

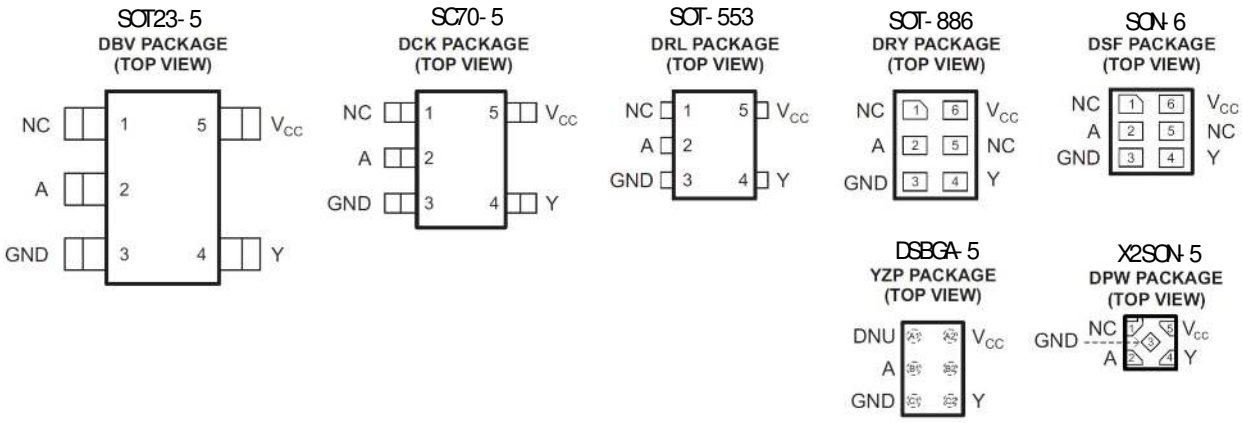
Product features

- Low input current: typical value 0.1uA
- Low static power consumption: typical value 0.1uA
- High output:VCC=4.5V, greater than32MA
- Wide operating voltage range: 1.65v to 5.5V
- Package form: DBV/DCK/DRL/YZP/ DRY/DSF/ DPW

Product use

- Portable audio interface
- digital television
- Wireless headset, smart watch, etc
- Blu ray player and home theater
- Solid state drive
- Intelligent wearable devices

Package form and pin function definition



	Pin				
name	DBV/DCK/DRL	DRY/DSF	YZP	DPW	explain
NC	1	1,5	A1, B2	1	Empty feet
A	2	2	B1	2	input
GND	3	3	C1	3	Power ground
Y	4	4	C2	4	output
VCC	5	6	A2	5	Power supply positive

Note: NC--Empty feet, no internal connection line

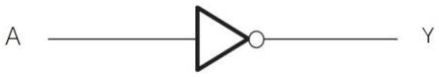
Limit parameter

parameter	Symbol	Limit value	Company
working voltage	V_{cc}	6.5	V
input	V_{IN}	-0.5~6.5	V
Output voltage (1)	V_{OUT}	-0.5~6.5	V
Single pin output current	I_{out}	25	mA
VCC or GND current	I_{cc}	50	mA
Storage temperature	T_{stg}	-65-150	℃
Pin welding temperature	T_L	260,10s	℃
working temperature	T_A	-40-105	℃

Note: 1. When VCC = 0V, the limit voltage that the output can withstand

2. The limit value of any parameter can not be exceeded. If the limit value is exceeded, it may cause physical damage such as product deterioration;At the same time, the chip can not be guaranteed to work normally when it is close to the limit parameters.

Principle logic diagram



truth table

Inputs	Output
A	Y
L	H
H	L

Working conditions

project	Symbol	Test conditions	minimum value	Typical value	Maximum	Company
working voltage	V_{CC}	-	1.65	-	5.5	V
Input high level voltage	V_{IH}	V_{CC} =1.65V~1.95V	0.65* V_{CC}	-	-	V
		V_{CC} =2.3V~2.7V	1.7V	-	-	
		V_{CC} =3V~5.5V	0.7* V_{CC}	-	-	
Input high level voltage	V_{IH}	V_{CC} =1.65V~1.95V	-	-	0.35* V_{CC}	V
		V_{CC} =2.3V~2.7V	-	-	0.7	
		V_{CC} =3V~5.5V	-	-	0.3* V_{CC}	
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	-	0	-	V_{CC}	V
High level output current	I_{OH}	V_{CC} =1.65V	-	-	-4	mA
		V_{CC} =2.3V	-	-	-8	
		V_{CC} =3V	-	-	-16	
		V_{CC} =4.5V	-	-	-32	
Low level output current	I_{OL}	V_{CC} =1.65V	-	-	4	mA
		V_{CC} =2.3V	-	-	8	
		V_{CC} =3V	-	-	16	
		V_{CC} =4.5V	-	-	32	

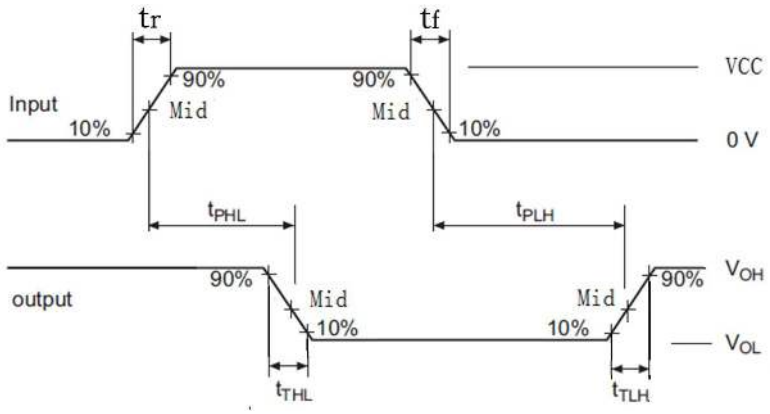
■ electrical properties

DC electrical characteristics: T_A=25℃

project	Symbol		Test conditions	V_{CC}	Typical value	Maximum	Company
High level load voltage	V_{OH}		I_{OH} =-100uA	1.65V~5.5V	1.64	-	V
			I_{OH} =-4 mA	1.65V	1.47	-	
			I_{OH} =-8 mA	2.3V	2.15	-	
			I_{OH} =-16 mA	3V	2.73	-	
			I_{OH} =-32 mA	4.5V	4.0		
Low level load voltage	V_{OL}		I_{OH} =100uA	1.65V~5.5V	0.01	-	V
			I_{OH} =4 mA	1.65V	0.11	-	
			I_{OH} =8 mA	2.3V	0.11	-	
			I_{OH} =16 mA	3V	0.2	-	
			I_{OH} =32 mA	4.5V	0.35	-	
Input current	I_I	A	VI = 5.5V or GND	0~5.5V	0.01	±5	uA
Turn off current	I_{OFF}	V_I	V_I=5.5V	0	0.01	±10	uA
		V_O	V_O=5.5V	0	0.01	±10	
Working current	I_{CC}		V_I=5.5V, I_O=0	1.65V~5.5V	0.01	10	uA
			V_I=GND , I_O=0		0.01	10	
Working current variation	ΔI_{CC}		A=V_{CC} -0.6V	3V~5.5V	25	-	uA

AC electrical characteristics: TA = 25 ℃ V_{CC}= 5.0V, TR =≤ 20ns, see test method.

project	Symbol	Test conditions	minimum value	Typical value	Maximum	Company
Maximum transmission delay time a, B to y	t_{PHL}	C_L=15pF	-	10	-	ns
	t_{PLH}	C_L=15pF	-	10	-	ns

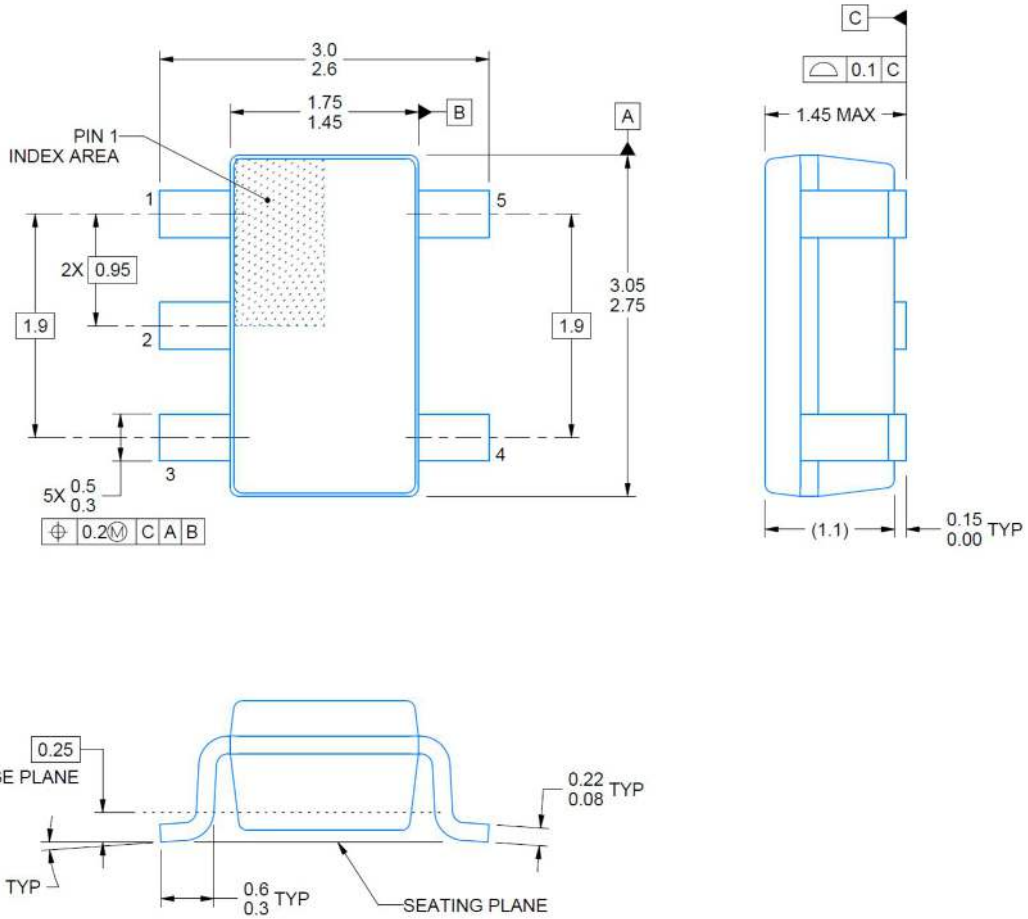


Note: 1. CL capacitor is an external chip capacitor (0603), which is connected close to the output pin, and the capacitance ground is close to the chip GND;2. Input: port input level, f = 500KHz, d = 50%;tr=tf≤20ns;
3. Output: y-end output test.

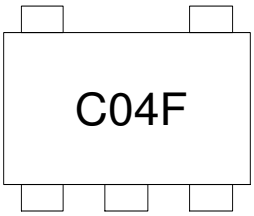
■ Encapsulation information

Unit: mm / in

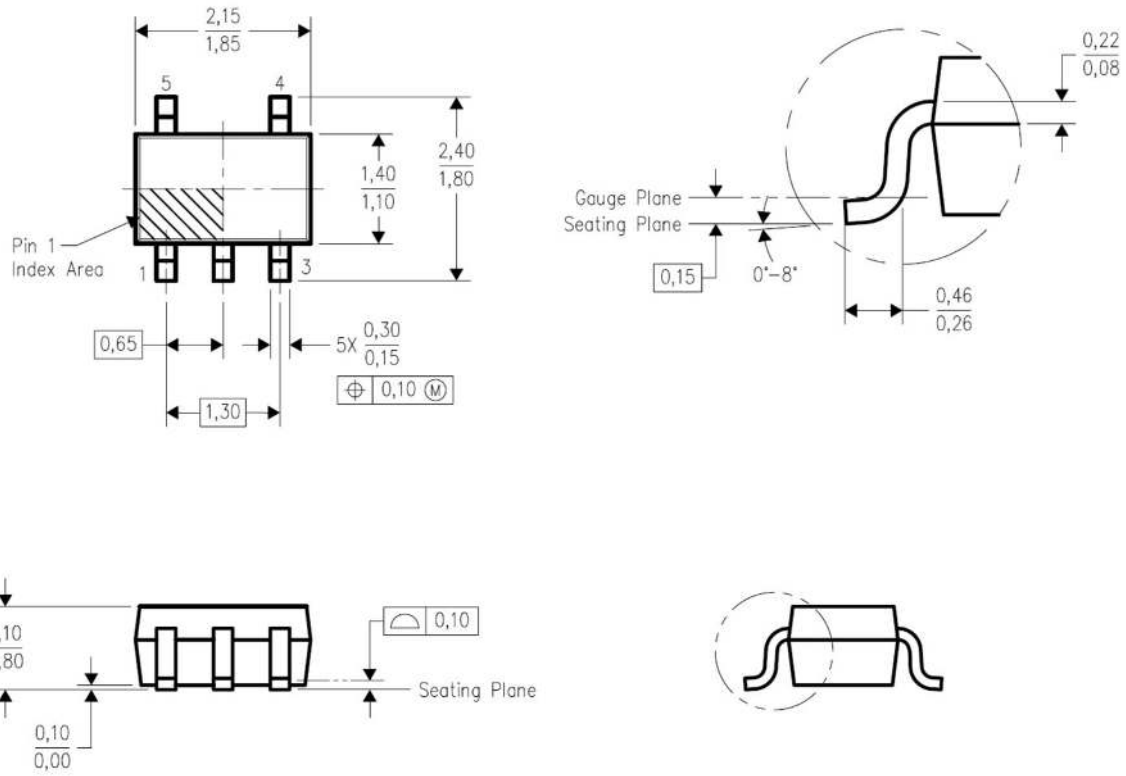
DBV(SOT23-5)



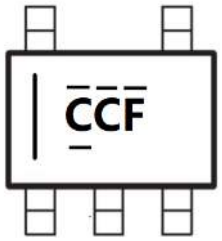
■ Marking



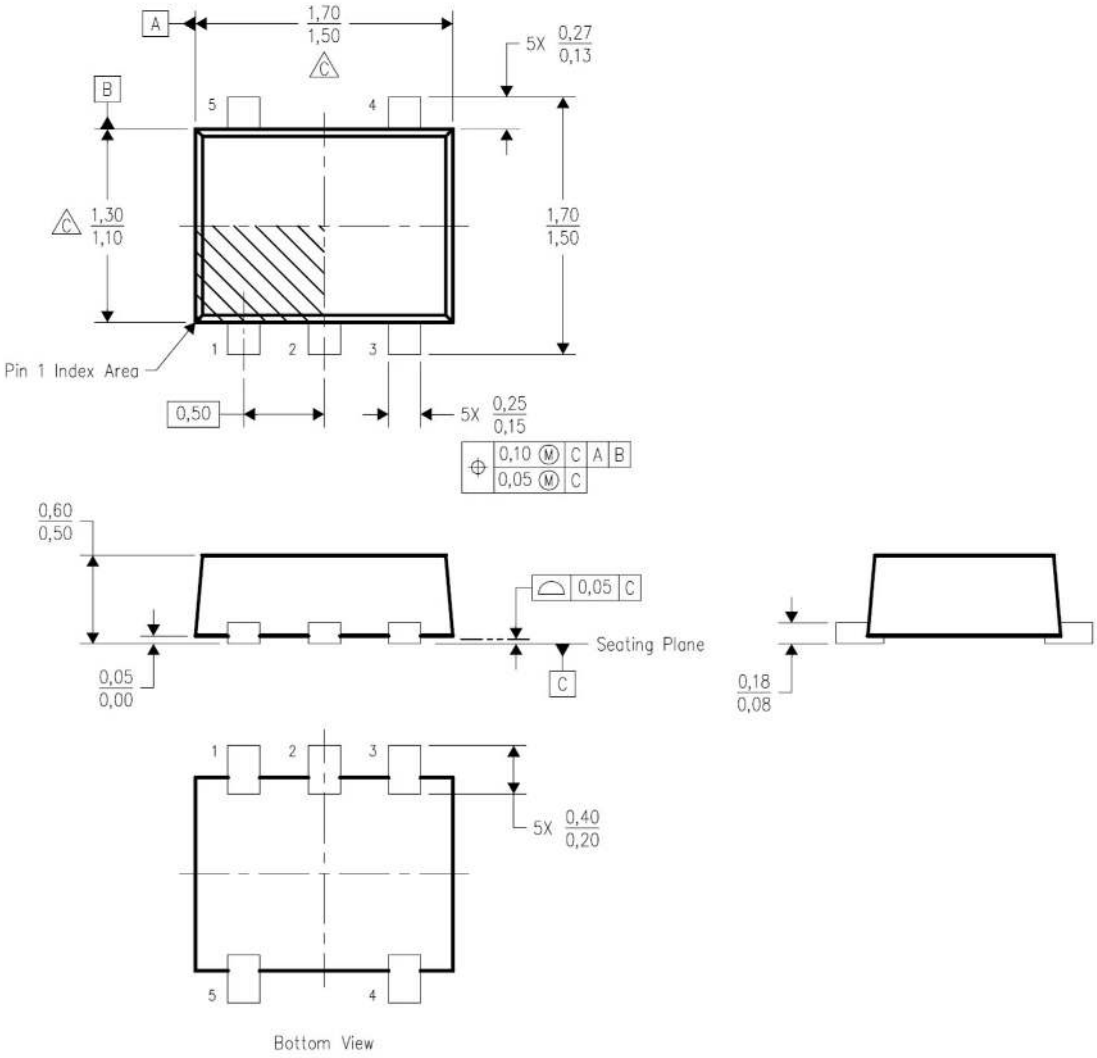
DCK(SC70-5)



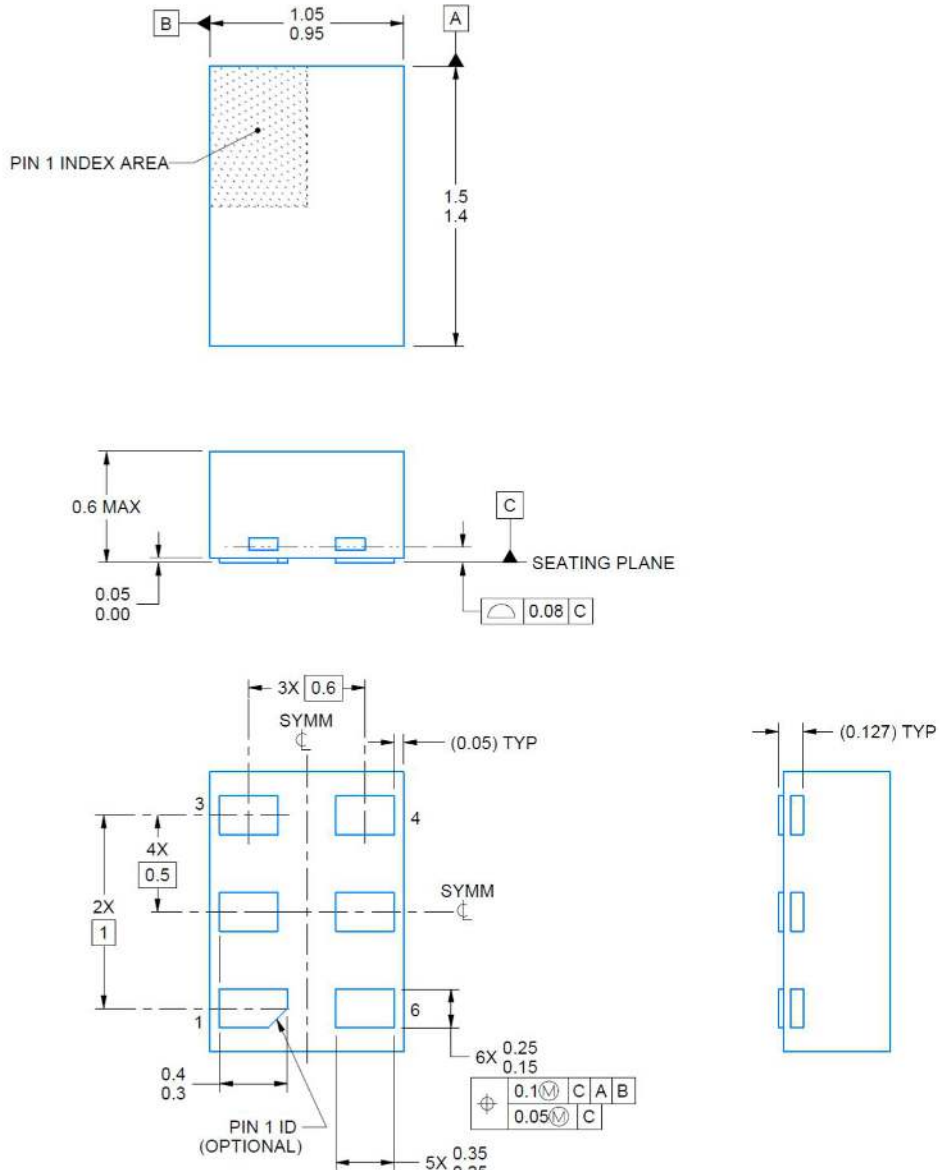
■ Marking



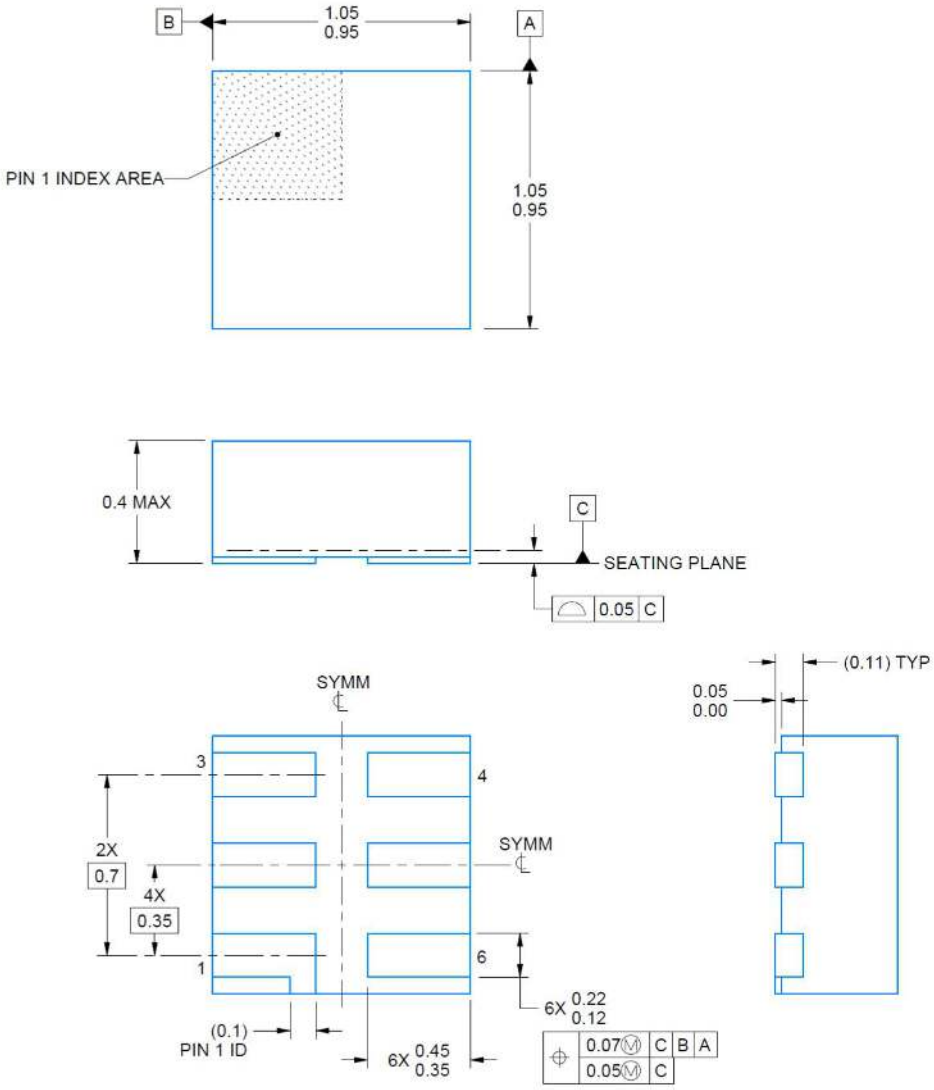
DRL (SOT-553)


A
1,70
1,50
C
5X 0,27
0,13
B
5
4
C 1,30
1,10
1,70
1,50
1
2
3
Pin 1 Index Area
0,50
5X 0,25
0,15
0,10 M C A B
0,05 M C
0,60
0,50
0,05 C
Seating Plane
C
0,05
0,00
0,18
0,08
1
2
3
5X 0,40
0,20
5
4
Bottom View

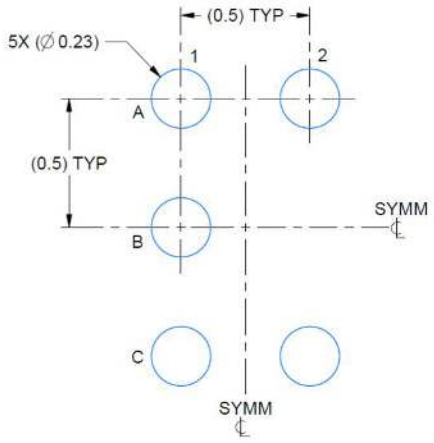
DRY(SOT-886)


B
1.05
0.95
A
PIN 1 INDEX AREA
1.5
1.4
0.6 MAX
C
SEATING PLANE
0.05
0.00
0.08 C
3X 0.6
SYMM
(0.05) TYP
(0.127) TYP
3
4
4X
0.5
SYMM
2X
1
1
6
6X 0.25
0.15
0.1 M C A B
0.05 M C
0.4
0.3
PIN 1 ID
(OPTIONAL)
5X 0.35

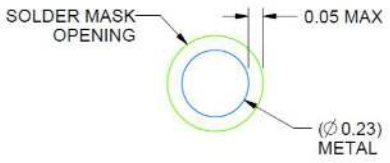
DSF(SON-6)


B
1.05
0.95
A
PIN 1 INDEX AREA
1.05
0.95
0.4 MAX
C
SEATING PLANE
0.05 C
SYMM
(0.11) TYP
0.05
0.00
3
4
2X
0.7
4X
0.35
SYMM
1
6
6X 0.22
0.12
(0.1)
PIN 1 ID
6X 0.45
0.35
0.07 M C B A
0.05 M C

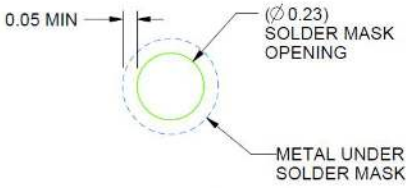
YZP(DSBGA-5)



LAND PATTERN EXAMPLE
SCALE:40X

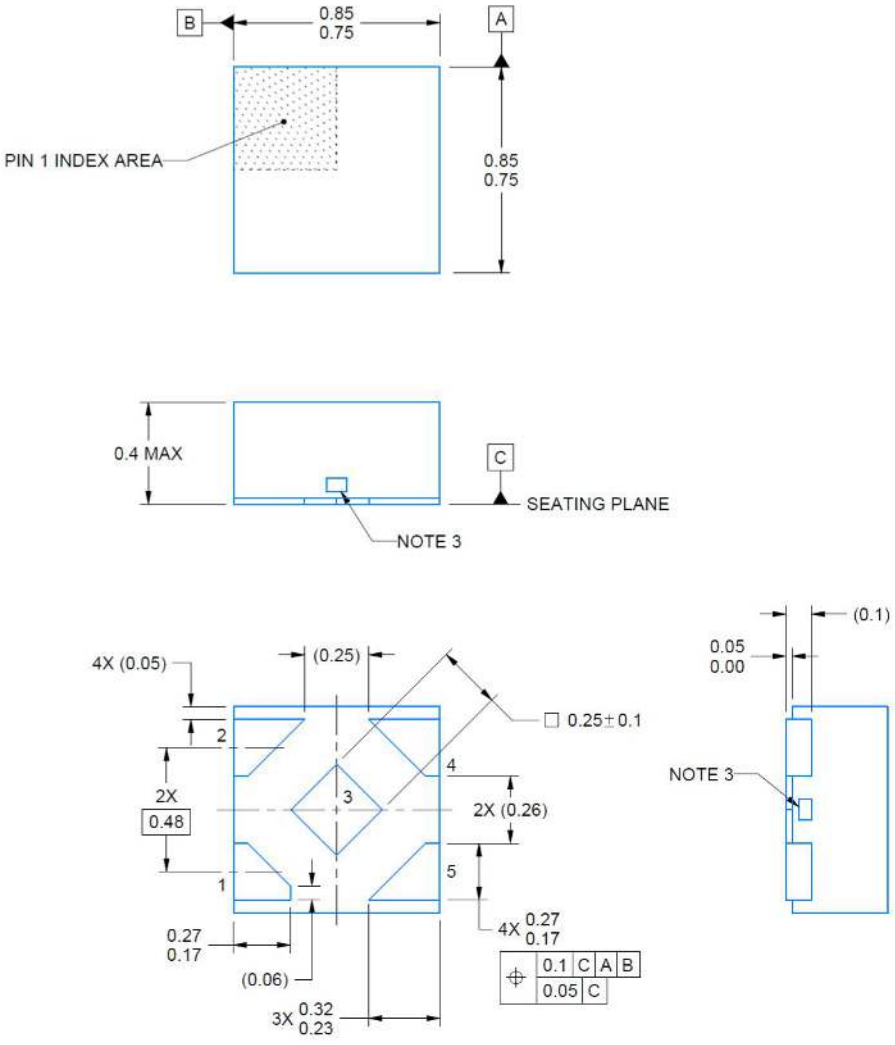


NON-SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

DPW(X2SON-4)


B
0.85
0.75
A
PIN 1 INDEX AREA
0.85
0.75
0.4 MAX
C
SEATING PLANE
NOTE 3
4X (0.05)
(0.25)
0.25±0.1
2
2X
0.48
1
3
4
2X (0.26)
5
4X 0.27
0.17
0.27
0.17
(0.06)
3X 0.32
0.23
0.1 C A B
0.05 C
(0.1)
0.05
0.00
NOTE 3