Automotive MOSFET

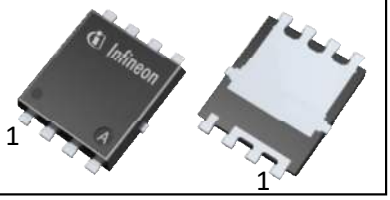
OptiMOS™-5 Power-Transistor

RoHS

Infineon Automotive Quality

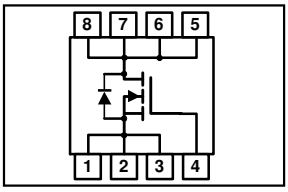
AEC Qualified

PG-TDSON-8-33



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested



Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	60	V
$R_{DS(on)}$	7.3	mΩ
I_D (chip limited)	60	A

Type	Package	Marking
IAUC60N06S5L073	PG-TDSON-8-33	5N06L073

Table of Contents

Maximum ratings

at Tj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, Chip limitation[1,2)]	60	A
		V_{GS}=10V, DC current	60	
		T_a=85 °C, V_{GS}=10 V, R_{thJA} on 2s2p[2,4)]	15	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C, t_p= 100 µs	168	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=30 A	40	mJ
Avalanche current, single pulse	I_{AS}	–	60	A
Gate source voltage	V_{GS}	–	±16	V
Power dissipation	P_{tot}	T_C=25 °C	52	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	2.9	K/W
Thermal resistance, junction - ambient[4)]	R_{thJA}	–	–	24.8	–	

Electrical characteristics

at Tj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=19 µA	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	–	–	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=100 °C[2)]	–	–	100	
Gate-source leakage current	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=30 A	–	8.2	9.8	mΩ
		V_{GS}=10 V, I_D=30 A	–	6.0	7.3	
Gate resistance[2)]	R_G	–	–	1.3	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	–	1273	1655	pF
Output capacitance	C_{oss}		–	277	360	
Reverse transfer capacitance	C_{rss}		–	14	21	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, R_G=3.5 Ω	–	2.8	–	ns
Rise time	t_r		–	2.3	–	
Turn-off delay time	$t_{d(off)}$		–	8.4	–	
Fall time	t_f		–	4.8	–	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=30 A, V_{GS}=0 to 10 V	–	4.2	5.5	nC
Gate to drain charge	Q_{gd}		–	2.8	4.2	
Gate charge total	Q_g		–	17.4	22.6	
Gate plateau voltage	$V_{plateau}$		–	3.3	–	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25 °C	–	–	60	A
Diode pulse current[2]	$I_{S,pulse}$	T_C=25 °C, t_p= 100 µs	–	–	168	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=30 A, T_j=25 °C	–	0.8	1.1	V
Reverse recovery time[2]	t_{rr}	V_R=30 V, I_F=50 A, di_F/dt =100 A/µs	–	28	–	ns
Reverse recovery charge[2]	Q_{rr}		–	17.0	–	nC

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

[2] The parameter is not subject to production testing – specified by design.

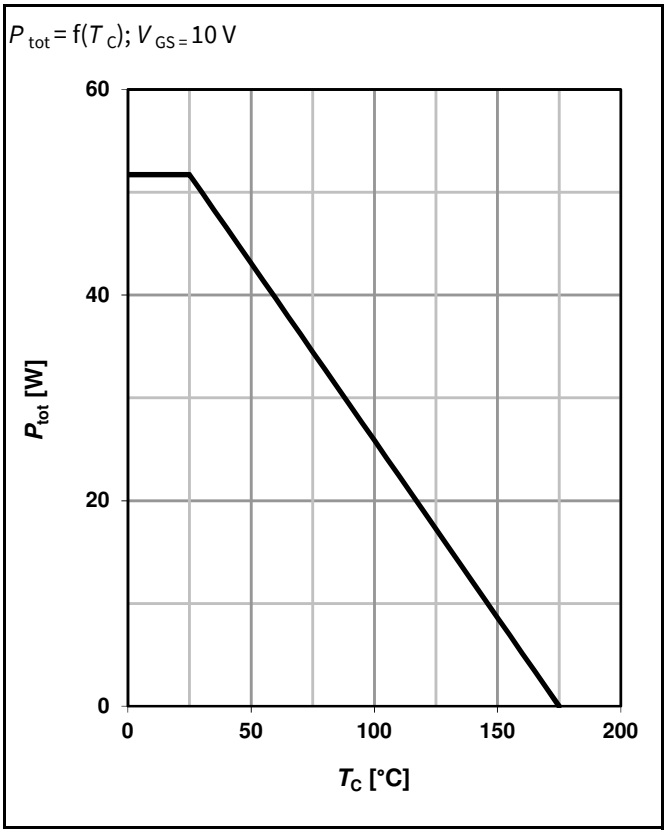
[3] Current is limited by the package.

[4] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

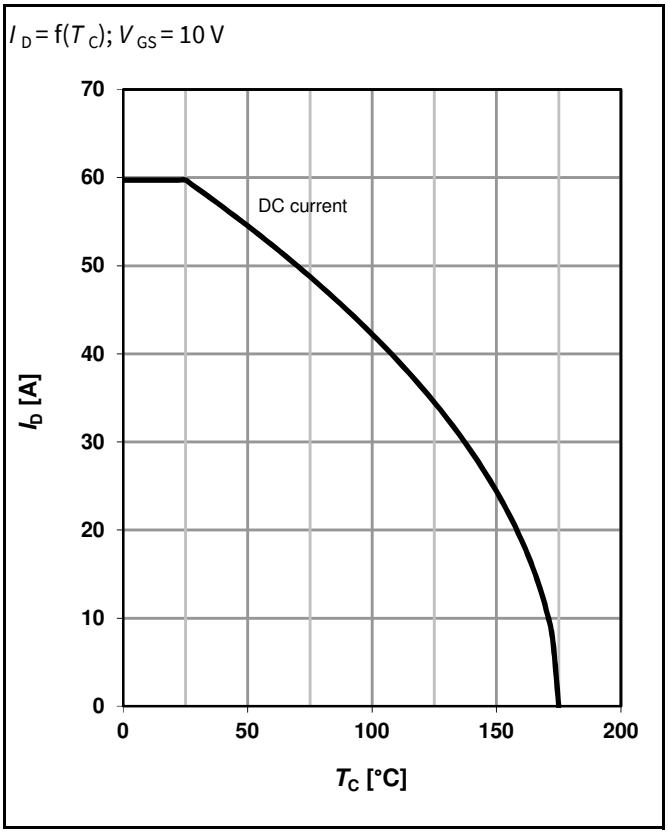
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} = 10$ V



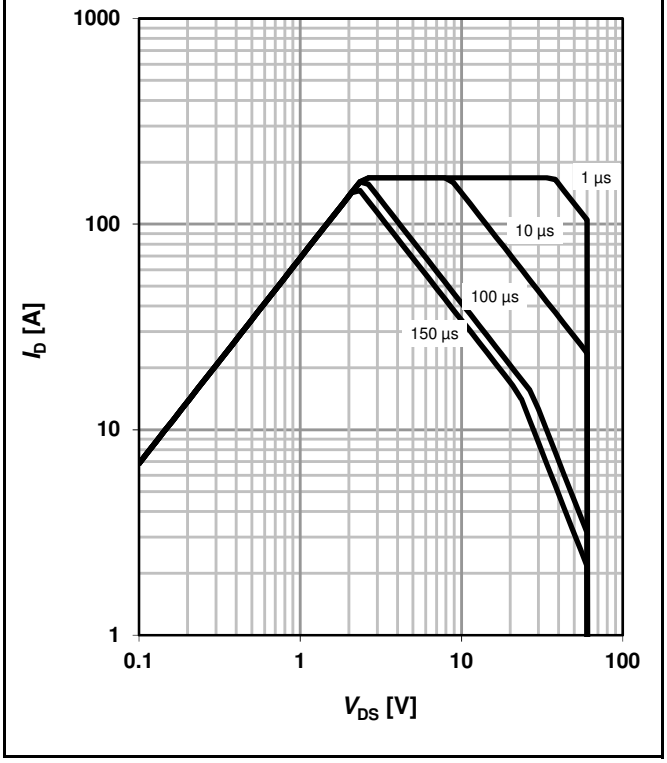
2 Drain current

$I_D = f(T_C)$; $V_{GS} = 10$ V



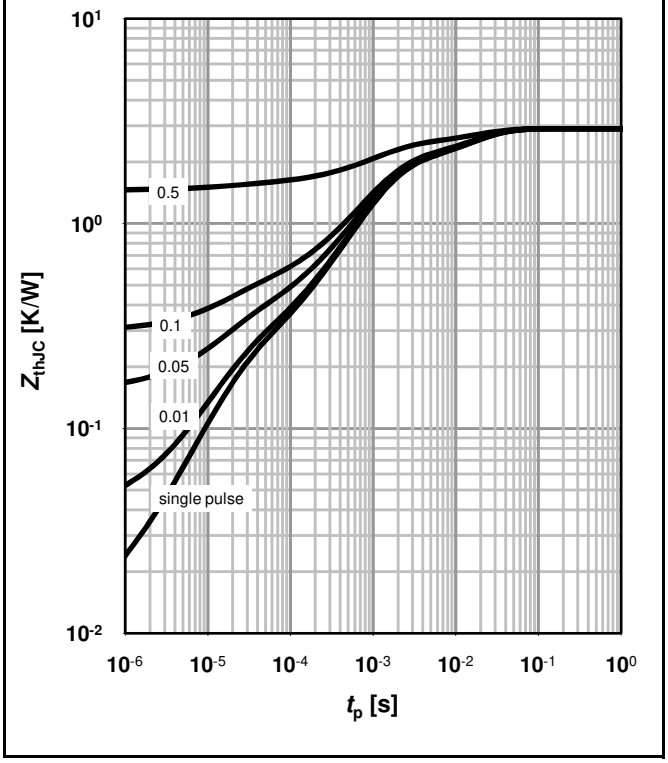
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



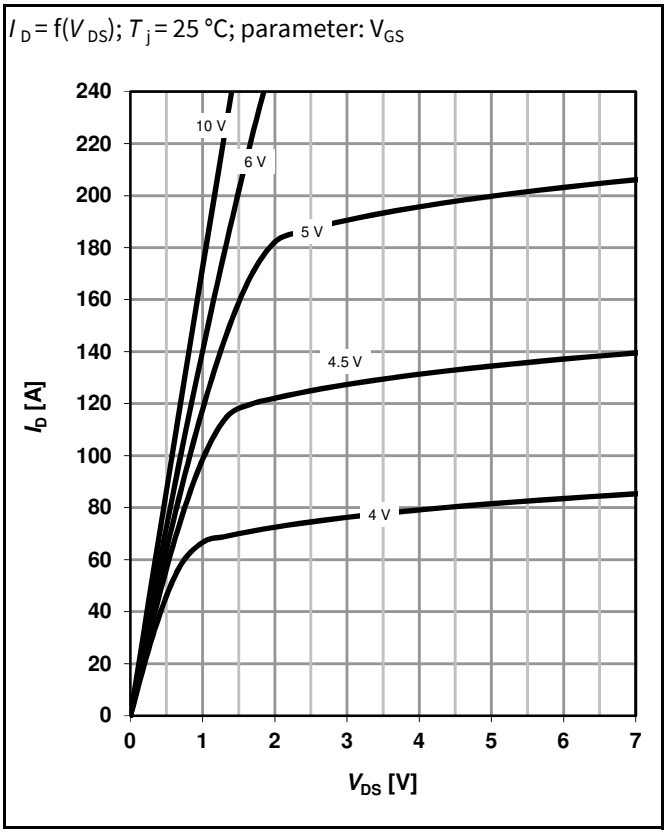
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D=t_p/T$



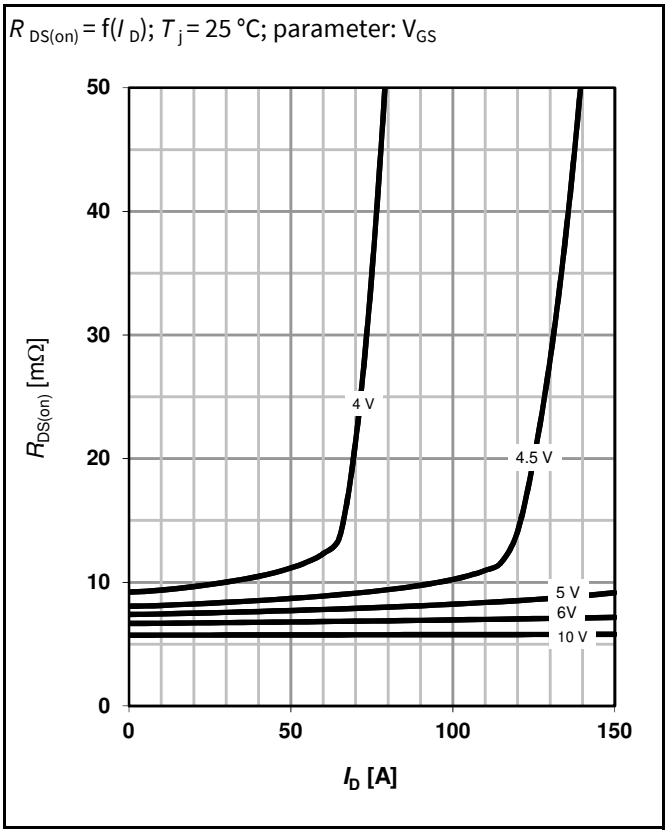
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



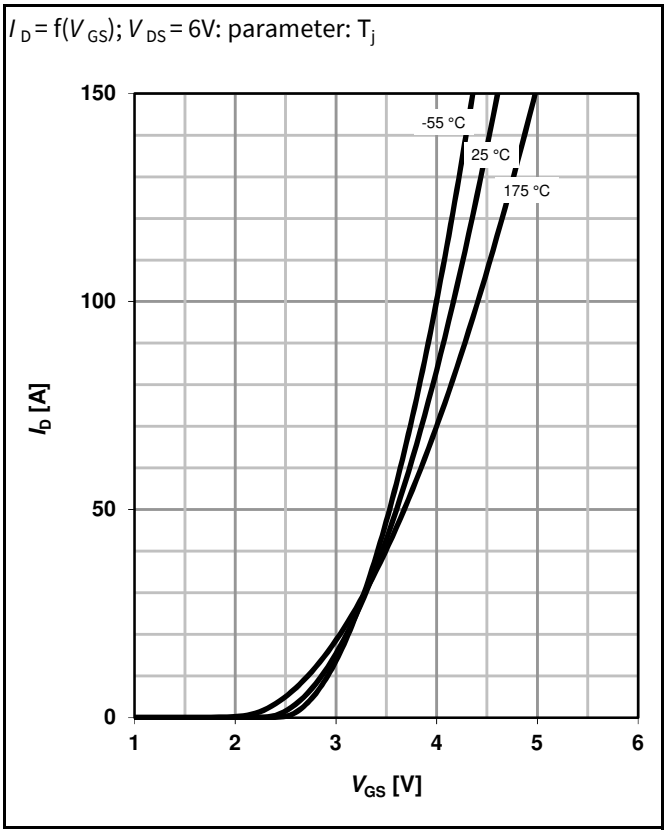
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



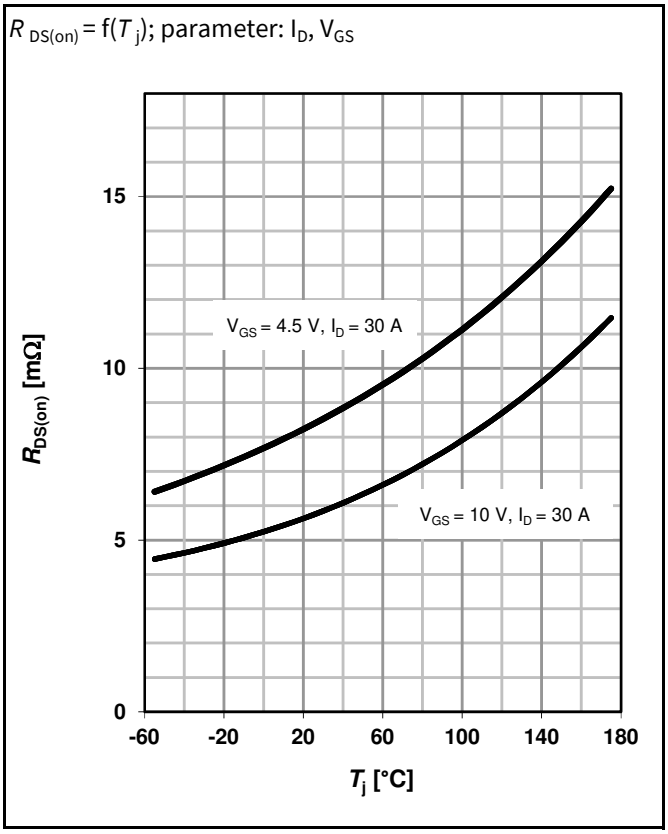
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V: parameter: T_j



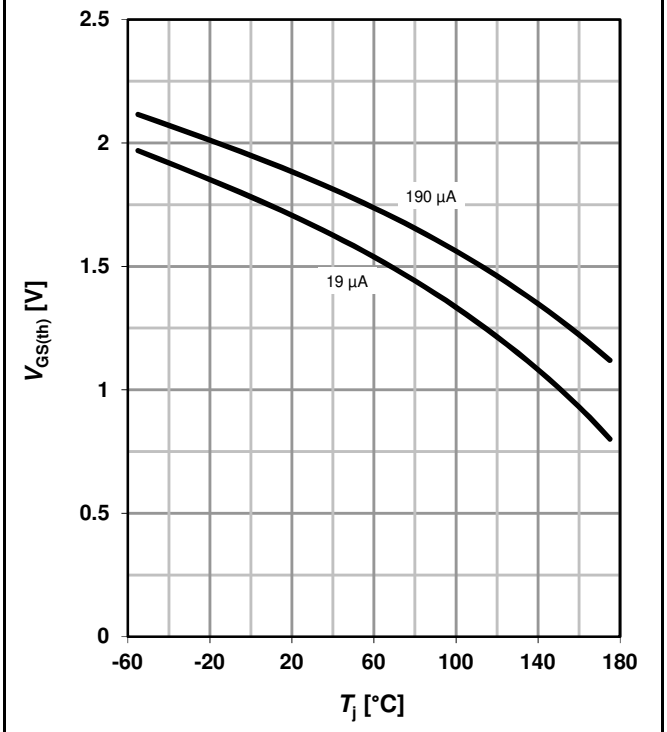
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



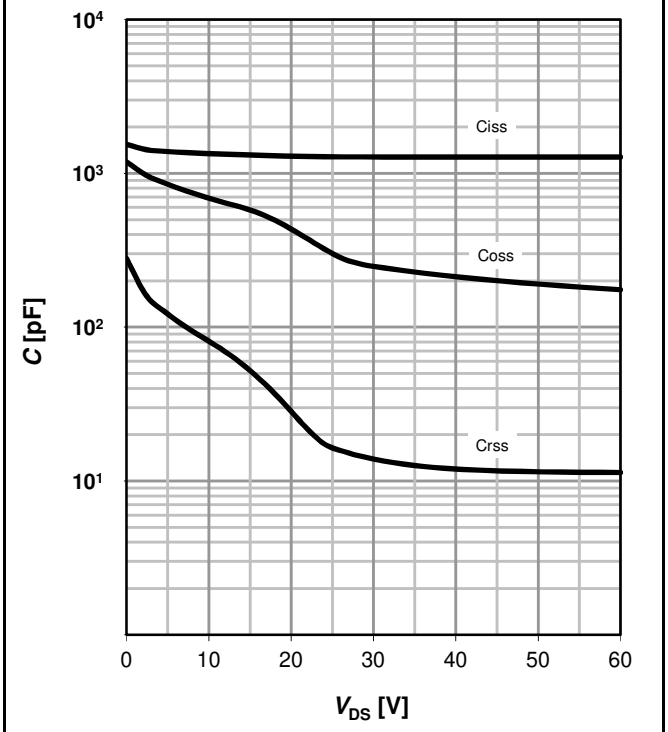
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



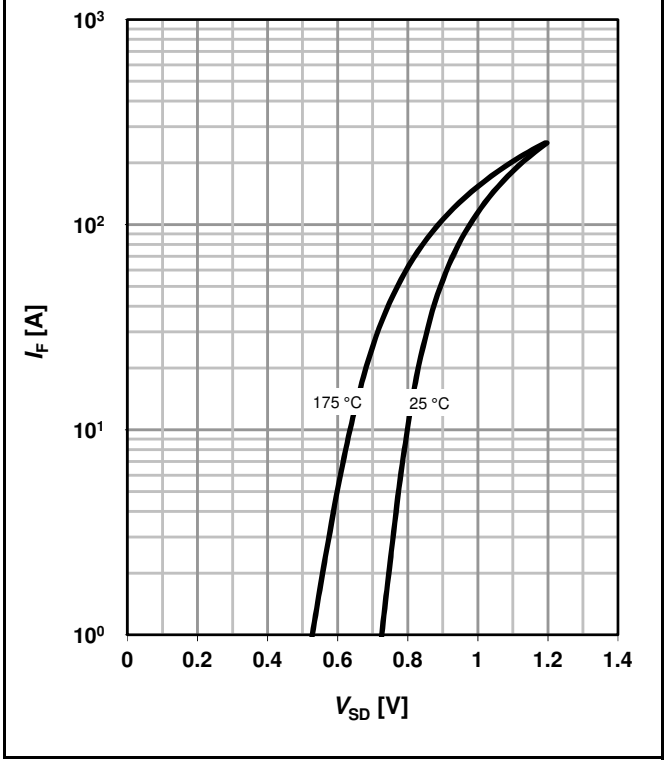
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



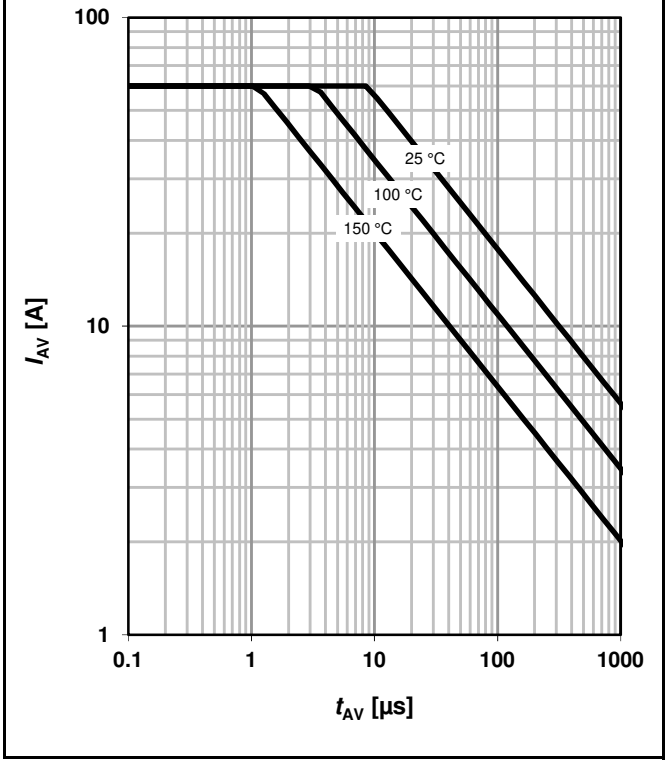
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



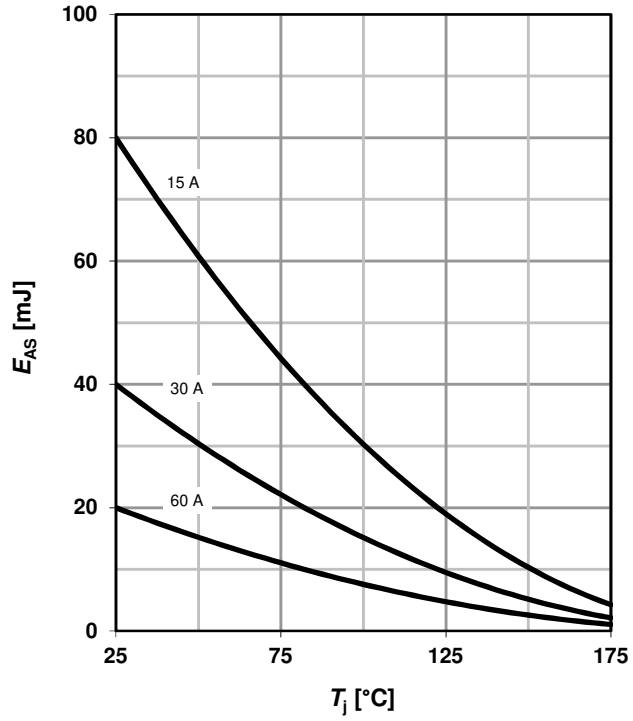
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



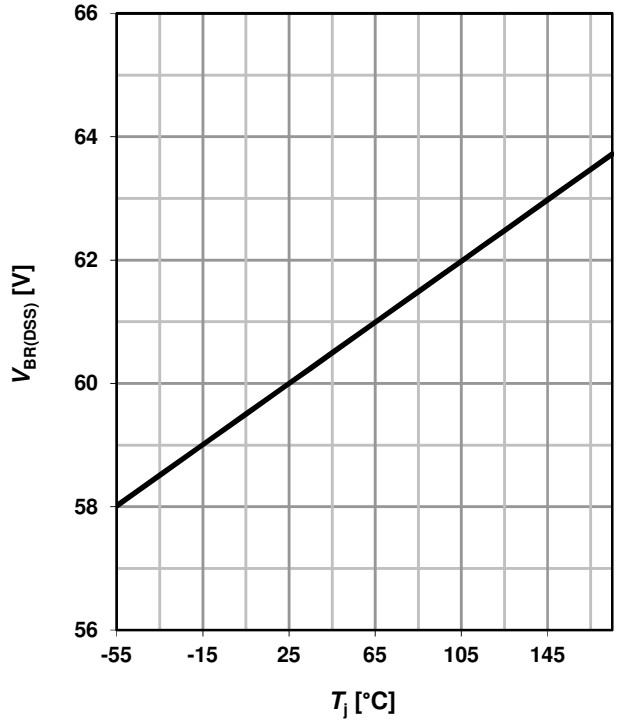
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



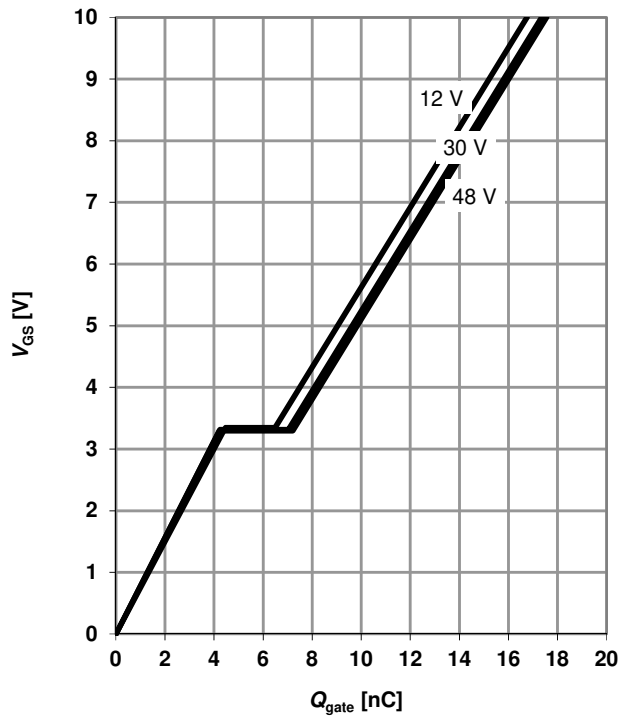
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; I_{D_typ} = 1 mA

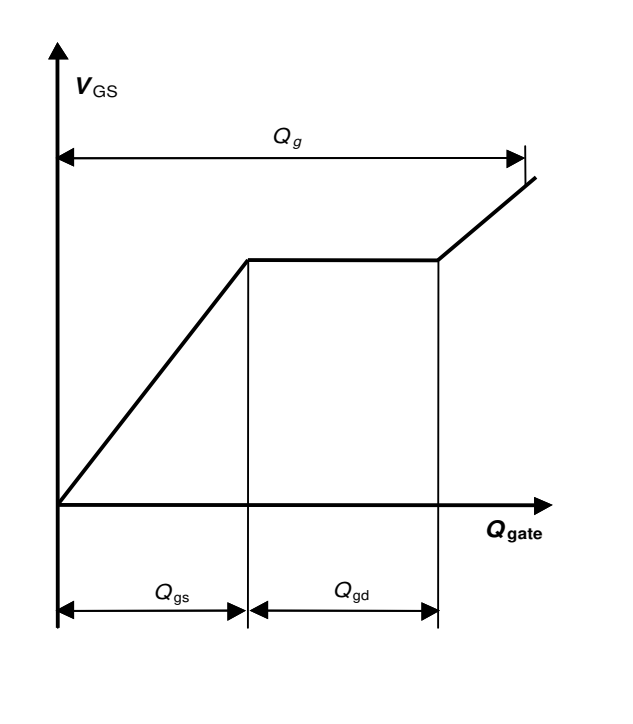


15 Typ. gate charge

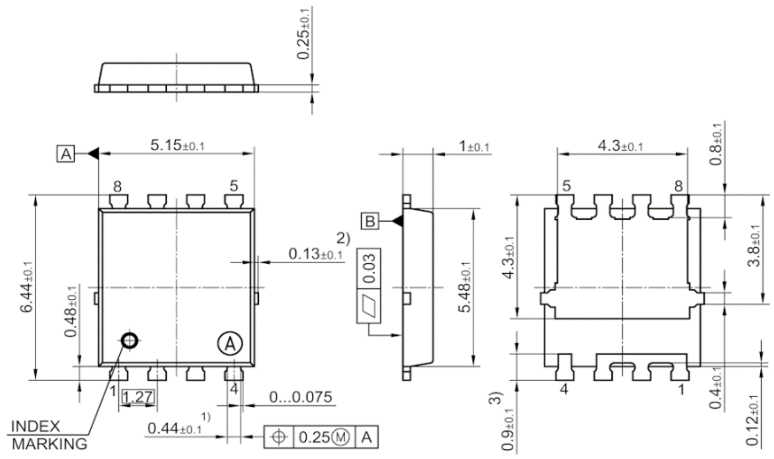
$V_{GS} = f(Q_{gate})$; I_D = 30 A pulsed; parameter: V_{DD}



16 Gate charge waveforms

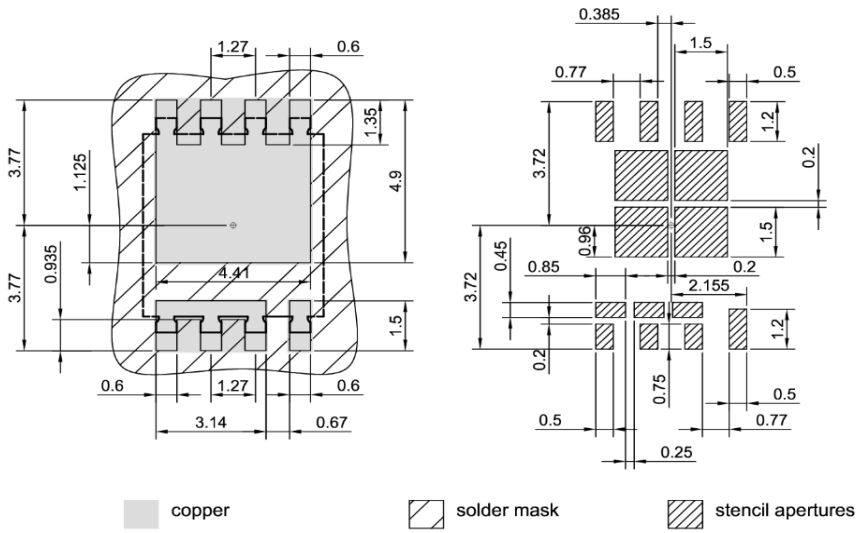


Package Outline



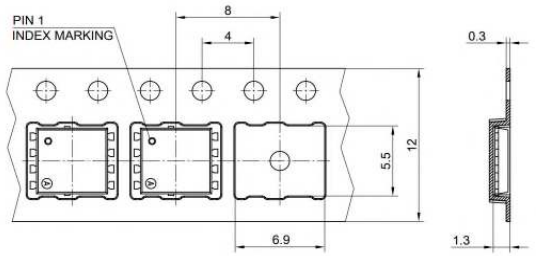
1) EXCLUDE MOLD FLASH
2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4)ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

Footprint



All dimensions are in units mm

Packaging



ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

Revision History

Revision	Date	Changes
Revision 1.0	04.05.2021	final data sheet
Revision 1.1	01.10.2021	normal level -> logic level (page 1)
Revision 1.2	27.01.2022	update image for pin layout (page 1)

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