4-CH OVER-VOLTAGE PROTECTION FOR CC/DIFF PINS ON USB TYPE-C

NEW PRODUCT

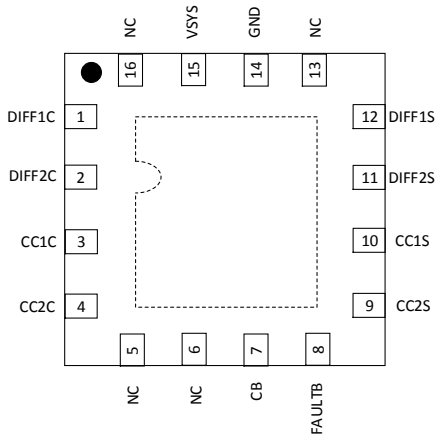
Description

The DPO2039DABQ-13 provides 4 channels of over-voltage protection over the CC1/2 & DIFF1/2 pins which are connected to the USB Type-C connector. The 4 channels are divided into two pairs, one pair of channels protect the CC1 and CC2 pins from being shorted to the V_{BUS}, one pair of channels protect the DIFF1 and DIFF2 pins from being shorted to the V_{BUS}. Whenever the voltage threshold set for any of the two pairs of channels is reached, the exception condition becomes valid and the low-active flag FAULTB is subsequently asserted.

This device is designed to draw its operating voltage primarily from the system power, V_{SYS}, which is either the always-ON 3.3/5V existed within the system or the 1-cell battery inside the mobile system. Under the circumstance when the battery inside a mobile system is fully depleted, DPO2039DABQ-13 can obtain power from the external peripheral system connected to the USB Type-C connector. The DPO2039DABQ-13 is housed in the low-profile and space-saving U-QFN3030-16 (Type B) package which is manufactured with environmental-friendly material.

Pin Assignments

(Top View)



U-QFN3030-16 (Type B)

Features

- Operating Voltage Range: 2.7V to 5.5V
- 4-Channel Over-Voltage Protection with Auto-Recovery
- IEC 61000-4-2 ESD Protection over CCxC and DIFFxC Pins
- $R_{DS(ON)}$ of OVP MOSFET for CC-Pin Protection: 300mΩ Typical
- $R_{DS(ON)}$ of OVP MOSFET for DIFF-Pin Protection: 5Ω Typical
- C_{IN} of OVP MOSFET for CC-Pin Protection: 50pF
- C_{IN} of OVP MOSFET for DIFF-Pin Protection: 5pF
- Built-In Over-Temperature Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DPO2039DABQ-13 is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- Notebook/Desktop/AIO PCs, Tablets, Mobile Phones
- VR/AR Headsets
- Docking Stations, Universal & Multimedia Hubs
- FPTVs, PC Monitors
- Set-Top-Boxes, Residential Gateways, Storage Devices
- Universal AC/DC Chargers/Adapters

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Application Circuit

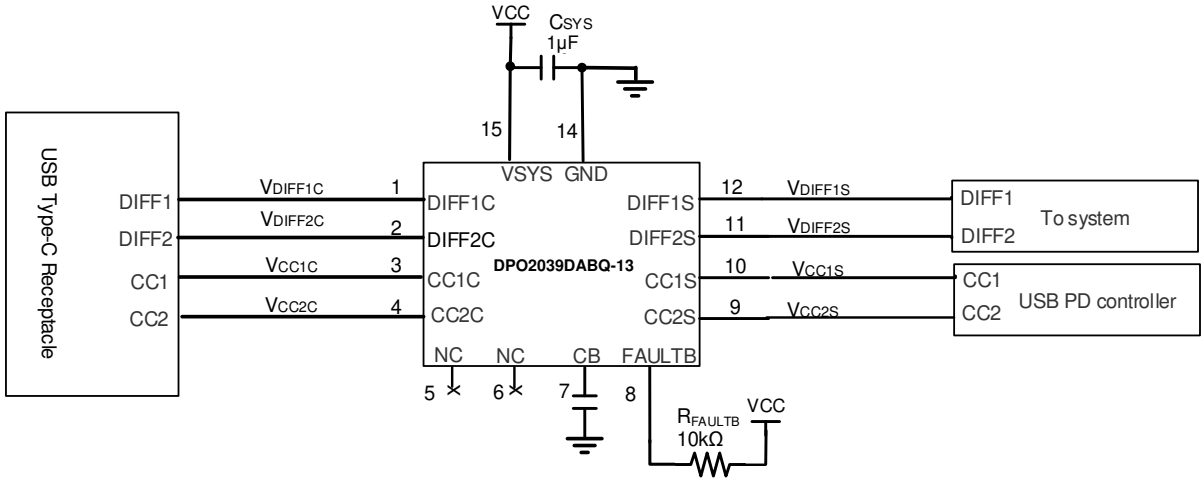

Figure 1. Typical Application Circuit

Pin Descriptions

Pin Number	Pin Name	Function
1	DIFF1C	DIFF1 connector side. This shall be connected to the DIFF1 pin of the USB Type-C connector.
2	DIFF2C	DIFF2 connector side. This shall be connected to the DIFF2 pin of the USB Type-C connector.
3	CC1C	CC1 connector side. This shall be connected to the CC1 pin of the USB Type-C connector.
4	CC2C	CC2 connector side. This shall be connected to the CC2 pin of the USB Type-C connector.
7	CB	Pin for ESD support capacitor. Place a 0.1µF capacitor on this pin to ground.
8	FAULTB	Fault status. This is an active-low open-drain output.
9	CC2S	CC2 system side. This shall be connected to the CC2 pin of the component to be protected.
10	CC1S	CC1 system side. This shall be connected to the CC1 pin of the component to be protected.
11	DIFF2S	DIFF2 system side. This shall be connected to the DIFF2 pin of the component to be protected.
12	DIFF1S	DIFF1 system side. This shall be connected to the DIFF1 pin of the component to be protected.
5, 6, 13, 16	NC	No connection.
14	GND	Ground.
15	VSYS	Power Input. This shall be connected to the 2.7 to 5.5V power source inside the system.
—	EP	Exposed pad. This shall be connected to ground.

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Functional Block Diagram

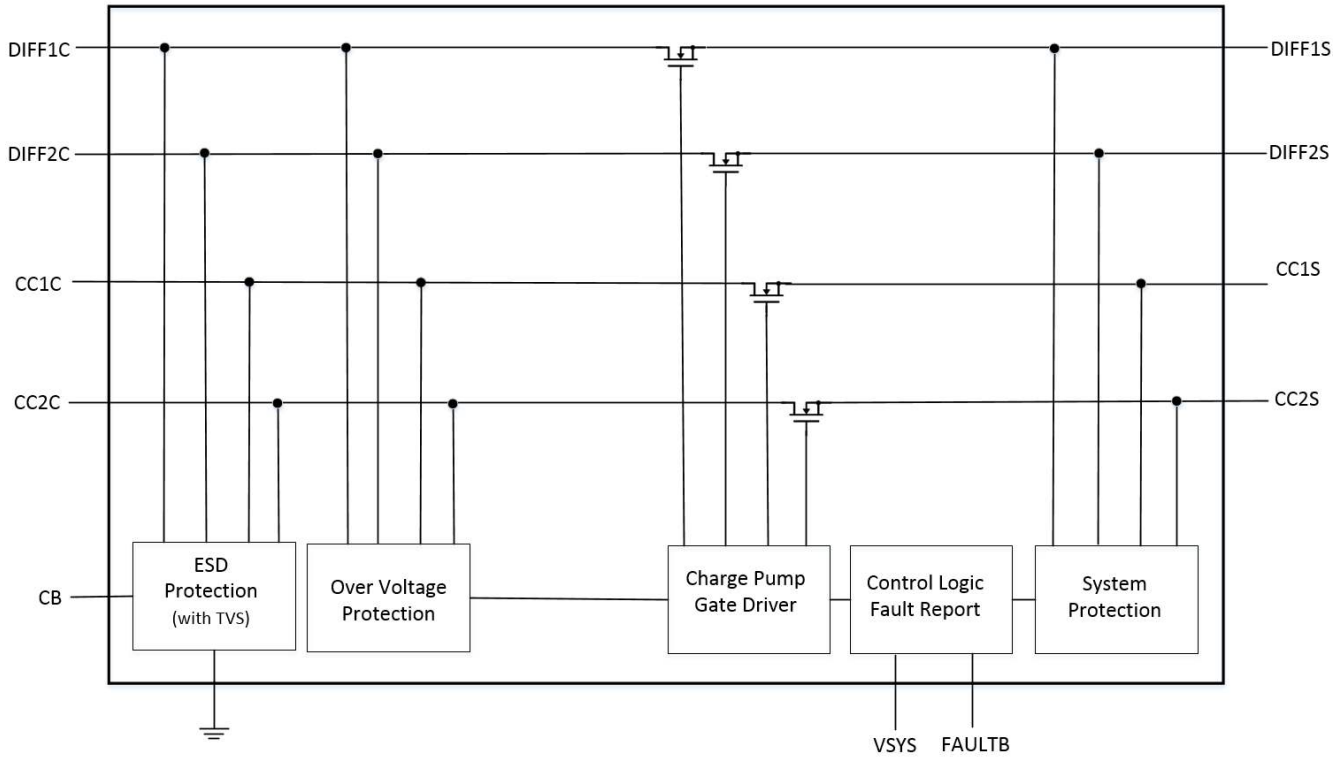

Figure 2. Internal Functional Blocks

Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified) (Note 4)

Symbol	Parameter	Rating	Unit
V_{VSYS}	Voltage Range of VSYS Pin	-0.3 to 6.0	V
V_{FAULTB}	Voltage Range of FAULTB Pin	-0.3 to 6.0	V
V_{CB}	Voltage Range of CB Pin	-0.3 to 24	V
V_{DIFFxS}, V_{CCxS}	Voltage Range of DIFF1S, DIFF2S, CC1S, CC2S Pins	-0.3 to 6.0	V
V_{DIFFxC}, V_{CCxC}	Voltage Range of DIFF1C, DIFF2C, CC1C, CC2C Pins	-0.3 to 24.0	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_L	Lead Temperature	+260	°C
T_{STG}	Storage Temperature	-65 to +150	°C
ESD	Human Body Model (HBM), JESD22-A114	±2.0	kV
	Charge Device Model (CDM), JESD22-C101	±0.5	

Note: 4. These are stress ratings only. Operation outside the absolute maximum ratings can cause device failure. Operation at the absolute maximum rating for extended periods can reduce device reliability.

Package Thermal Data (@ T_A = +25°C, unless otherwise specified) (Note 5)

Symbol	Parameter	Rating	Unit
P_D	Power Dissipation	1.75	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	73	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	12.7	°C/W

Note: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1" × 1" copper pad layout.

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Recommended Operating Conditions (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{VSYS}	Input Supply Voltage at VSYS Pin	2.7	5.5	V
V_{FAULTB}	Power Rail for Pull-Up on FAULTB Pin	2.7	5.5	V
V_{CB}	Voltage across CB Pin	0	5.5	V
V_{CCxC}, V_{CCxS}	I/O Voltage at CC1C, CC2C, CC1S, CC2S Pins	0	5.5	V
V_{DIFFxC}, V_{DIFFxS}	I/O Voltage at DIFF1C, DIFF2C, DIFF1S, DIFF2S Pins	0	4.2	V
I_{VCCX}	Output Current Flowing into CCxS and out of CCxC, with $V_{CCxS} - V_{CCxC} \leq$ 250mV	—	600	mA

Electrical Characteristics (@ T_A = +25°C, V_{VSYS} = 4.2V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CC OVP Switches						
$R_{DS(ON)\_CC}$	On Resistance of CC OVP FETs	V_{CCxC} = 5.5V, $T_A \leq$ +85°C	—	300	450	mΩ
		V_{CCxC} = 5.5V, $T_A \leq$ +105°C	—	300	480	mΩ
$R_{DS(ONFLAT)\_CC}$	On Resistance Flatness of CC OVP FETs	V_{CCxC} = 0.1 to 1.2V	—	—	5	mΩ
C_{ON_CC}	Equivalent ON Capacitance	Capacitance from CCxC or CCxS to GND when device is powered, (V_{CCxC} / V_{CCxS}) = 0V to 1.2V	—	50	—	pF
$V_{TH\_OVP\_CCxC}$	OVP Threshold on CCxC Signal	—	5.6	6	6.25	V
$V_{TH\_OVP\_HYS\_CCxC}$	OVP Hysteresis on CCxC Signal	—	—	140	—	mV
BW_{ON_CC} (Note 6)	CC Line ON Bandwidth Single Ended (-3dB)	Measured from CCxC to CCxS, 50Ω system, V_{CM} = 0.1V to 1.2V	—	200	—	MHz
$V_{SHT\_CCxC\_MAX}$ (Note 6)	Short-to-VBUS Tolerance on the CCxC Pins	Hot-plug CCxC with a 1 meter USB Type-C cable, place a 30Ω load on CCxS	—	—	24	V
$V_{SHT\_CCxS\_CL}$ (Note 6)	Short-to-VBUS Clamping Voltage on the CCxS Pins	Hot-plug CCxC with a 1 meter USB Type-C cable, place a 30Ω load on CCxS. Hot plug voltage V_{CCxC} = 24V	—	7	—	V
DIFF OVP Switches						
$R_{DS(ON)\_DIFF}$	On Resistance of DIFF OVP FETs	V_{DIFFxC} = 3.6V, T_A = +85°C	—	5	—	Ω
		V_{DIFFxC} = 3.6V, T_A = +105°C	—	5	—	Ω
$R_{DS(ONFLAT)\_DIFF}$	On Resistance Flatness of DIFF OVP FETs	V_{DIFFxC} = 0.1 to 3.6V	—	—	1	Ω
C_{ON_DIFF}	Equivalent ON Capacitance	Capacitance from DIFFxC or DIFFxS to GND when device is powered. V_{DIFFxC} / V_{DIFFxS} = 0V to 3.6V	—	5	—	pF
$V_{TH\_OVP\_DIFFxC}$	OVP Threshold on DIFFxC Signals	—	4.15	4.5	4.75	V
$V_{TH\_OVP\_HYS\_DIFFxC}$	OVP Hysteresis on DIFFxC Signals	—	—	110	—	mV
BW_{ON_DIFF} (Note 6)	DIFF line ON Bandwidth Single Ended (-3dB)	Measured from DIFFxC to DIFFxS, 50Ω system, V_{CM} = 0.1V to 3.6V	—	1000	—	MHz
$V_{SHTBUS\_DIFFxC\_MAX}$ (Note 6)	Short-to-VBUS Tolerance on the DIFFxC Pins	Hot-plug DIFFxC with a 1 meter USB Type-C cable, place a 40Ω in series with 150nF to GND on DIFFxS pin	—	—	24	V
$V_{SHTBUS\_DIFFxS\_CL}$ (Note 6)	Short-to-VBUS Clamping Voltage on the DIFFxS Pins	Hot-plug DIFFxC with a 1 meter USB Type-C cable, place a 40Ω in series with 100nF to GND on DIFFxS pin. Hot plug voltage V_{DIFFxC} = 24V, V_{VSYS} = 3.3V	—	7	—	V
X_{TALK_DIFFx} (Note 6)	Crosstalk between DIFFx Lines	Measure crosstalk at f = 1MHz, from DIFF1S to DIFF2C or DIFF2 to DIFF1C. V_{CM1} = 3.6V, V_{CM2} = 0.3V, terminate open sides to 50Ω	—	-80	—	dB

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Electrical Characteristics (@ T_A = +25°C, V_{VSYS} = 4.2V, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply and Leakage Current						
V_{UVLO}	V_{VSYS} under Voltage Lockout	V_{VSYS} steps up from 2V until CC or DIFF FETs turn ON	2.15	2.4	2.55	V
V_{UVLO_HSYS}	V_{VSYS} UVLO Hysteresis	V_{VSYS} steps down from 2.5V until CC or DIFF FETs turn off. Measure difference between rising and falling UVLO to calculate	—	200	—	mV
I_{VSYS_ON}	V_{VSYS} Supply Current	—	—	190	—	µA
I_{LEAK_CCxC}	Leakage current for CCxC when device is powered	V_{CCxC} = 3.6V	—	—	30	µA
I_{LEAK_DIFFxC}	Leakage current for DIFFxC when device is powered	V_{DIFFxC} = 3.6V	—	—	35	µA
I_{LEAK_CCxS}	Leakage current for CCxS when device is powered	V_{CCx} = 3.6V	—	—	30	µA
I_{LEAK_DIFFxS}	Leakage current for DIFFxS when device is powered	V_{DIFFx} = 3.6V	—	—	35	µA
$I_{LEAK\_OVP\_CCxC}$	Leakage current into CCxC pins when device is in OVP	V_{VSYS} = 0V, V_{CCxC} = 22V, V_{CCxS} = 0V	—	—	150	µA
		V_{VSYS} = 4.2V, V_{CCxC} = 22V, V_{CCxS} = 0V	—	—	150	µA
$I_{LEAK\_OVP\_DIFFxC}$	Leakage current into DIFFxC pins when device is in OVP	V_{VSYS} = 0V, V_{DIFFxC} = 22V, V_{DIFFxS} = 0V	—	—	200	µA
		V_{VSYS} = 4.2V, V_{DIFFxC} = 22V, V_{DIFFxS} = 0V	—	—	200	µA
$I_{LEAK\_OVP\_CCxS}$	Leakage current out of CCxS pins when device is in OVP	V_{VSYS} = 0V, V_{CCxC} = 22V, V_{CCxS} = 0V	—	—	1	µA
		V_{VSYS} = 4.2V, V_{CCxC} = 22V, V_{CCxS} = 0V	—	—	1	µA
$I_{LEAK\_OVP\_DIFFxS}$	Leakage current out of DIFFxS pins when device is in OVP	V_{VSYS} = 0V, V_{DIFFxC} = 22V, V_{DIFFxS} = 0V	—	—	1	µA
		V_{VSYS} = 4.2V, V_{DIFFxC} = 22V, V_{DIFFxS} = 0V	—	—	1	µA
FAULTB Pin						
V_{FAULTB}	Active-Low Output Voltage of FAULTB Pin	I_{OL} = 8mA	—	—	0.4	V
I_{LEAK_FAULB}	FAULTB Leakage Current	V_{FAULTB} = 4.2V	—	—	1	µA
$t_{FAULTB\_ASSERTION}$	FAULTB Assertion Time	—	—	—	300	µs
$t_{FAULTB\_DEASSERTION}$	FAULTB Deassertion Time	—	—	4	—	ms
Timing Requirements						
t_{ON}	Time from Crossing Rising V_{VSYS} UVLO until CC/DIFF OVP FETs are on	—	—	—	2.5	ms
$t_{OVP\_RESPONSE\_CC}$	OVP Response Time on the CC Pins, Time from OVP Asserted until OVP FETs Turnoff	—	—	100	—	ns
$t_{OVP\_RESPONSE\_DIFF}$	OVP Response Time on the DIFF Pins, Time from OVP Asserted until OVP FETs Turnoff	—	—	100	—	ns
$t_{OVP\_RESPONSE\_CC\_1}$	OVP Recovery Time on the CC Pins. Once an OVP has occurred, the minimum duration until CC FETs turn back on if OVP has been removed already	—	26	32	38	ms
$t_{OVP\_RESPONSE\_DIFF\_1}$	OVP Recovery Time on the DIFF Pins. Once an OVP has occurred, the minimum duration until DIFF FETs turn back on if OVP has been removed already	—	26	32	38	ms
$t_{OVP\_RESPONSE\_CC\_2}$	OVP Recovery Time on the CC Pins. Time from OVP removal until CC FETs turn back on, if device has been in OVP > 40ms	—	—	1	—	ms
$t_{OVP\_RESPONSE\_DIFF\_2}$	OVP Recovery Time on the DIFF Pins. Time from OVP removal until DIFF FETs turn back on, if device has been in OVP > 40ms	—	—	1	—	ms
Thermal Shutdown and Hysteresis						
T_{SHDN}	Thermal Shut Down Threshold	—	—	+150	—	°C
T_{HSYS}	Thermal Shut Down Hysteresis	—	—	+20	—	°C

Note: 6. Guaranteed by bench characterization

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Performance Characteristics (@ T_A = +25°C, unless otherwise specified.)

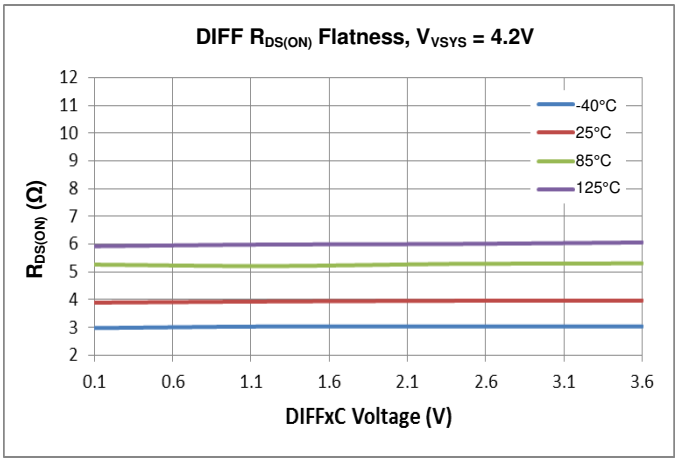

Figure 3. DIFF $R_{DS(ON)}$ Flatness

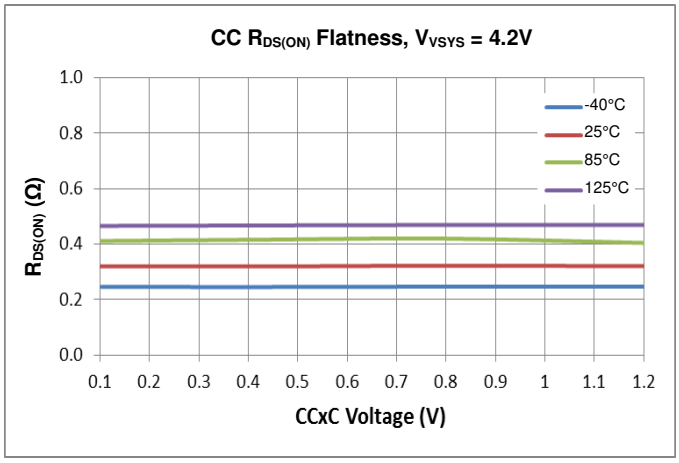

Figure 4. CC $R_{DS(ON)}$ Flatness

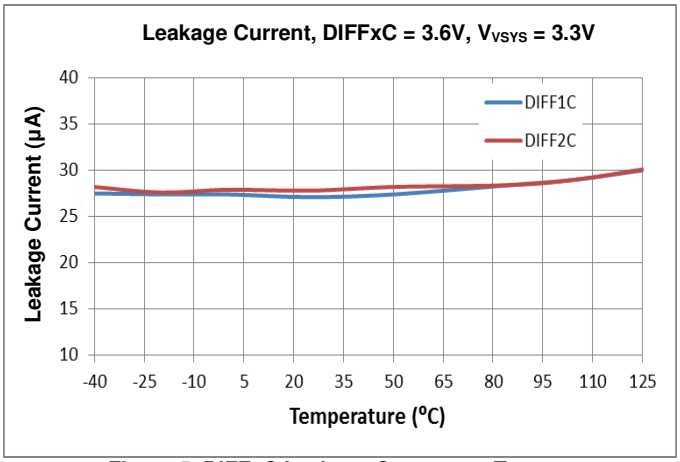

Figure 5. DIFFxC Leakage Current vs. Temperature

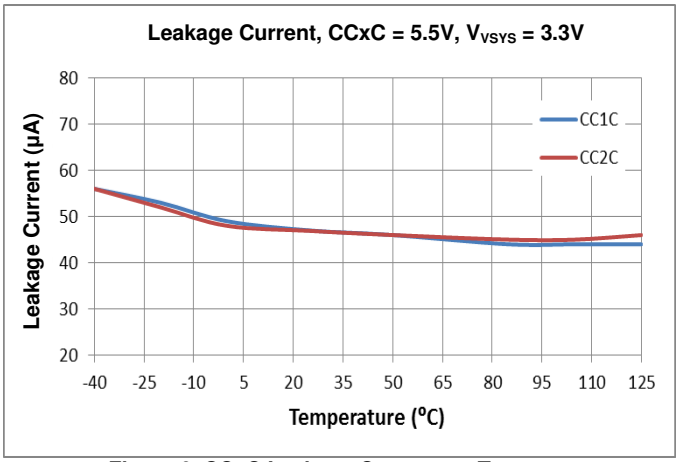

Figure 6. CCxC Leakage Current vs. Temperature

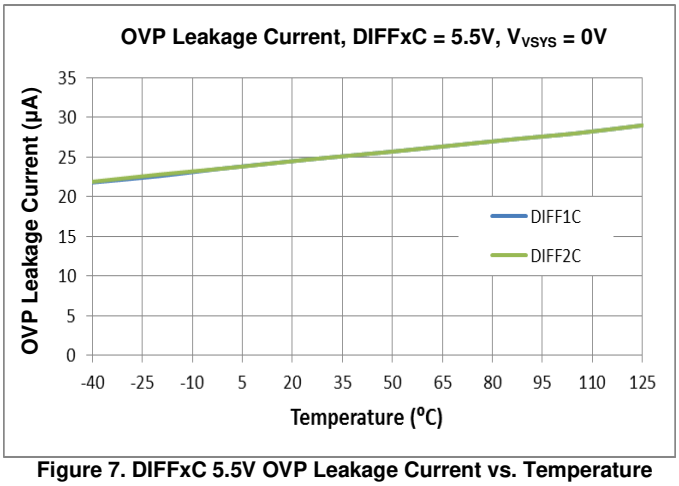

Figure 7. DIFFxC 5.5V OVP Leakage Current vs. Temperature

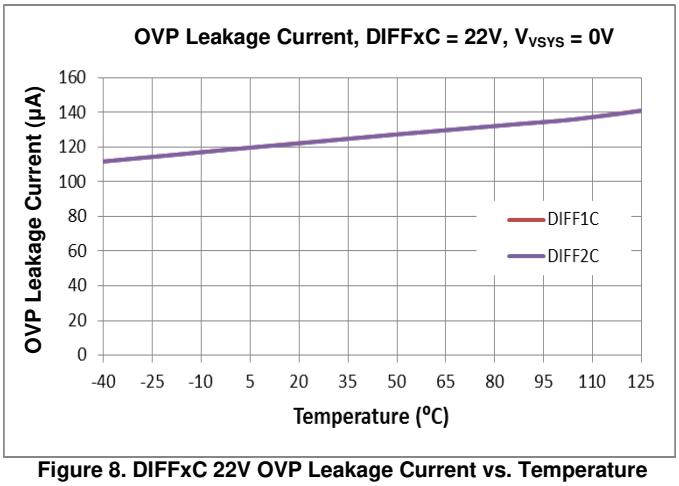

Figure 8. DIFFxC 22V OVP Leakage Current vs. Temperature

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Performance Characteristics (@ T_A = +25°C, unless otherwise specified.) (continued)

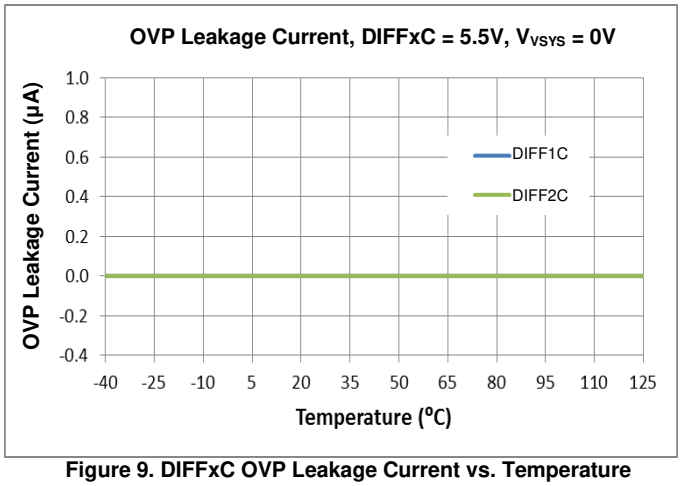

Figure 9. DIFFxC OVP Leakage Current vs. Temperature

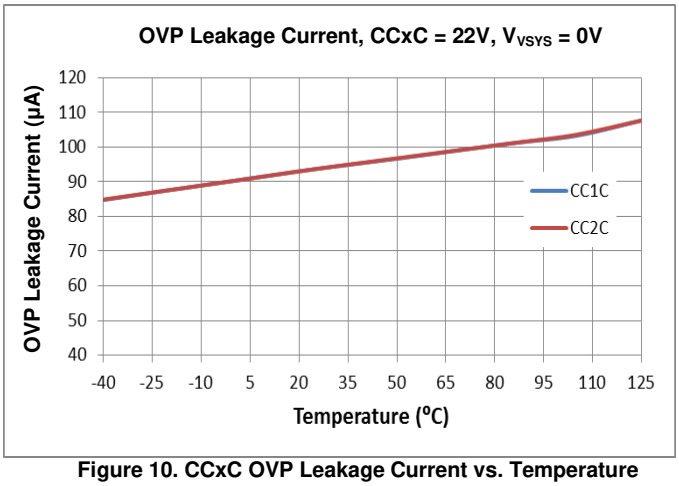

Figure 10. CCxC OVP Leakage Current vs. Temperature

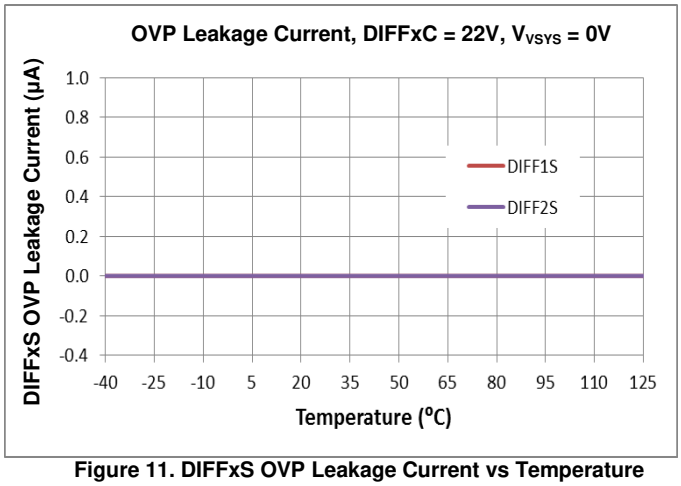

Figure 11. DIFFxS OVP Leakage Current vs Temperature

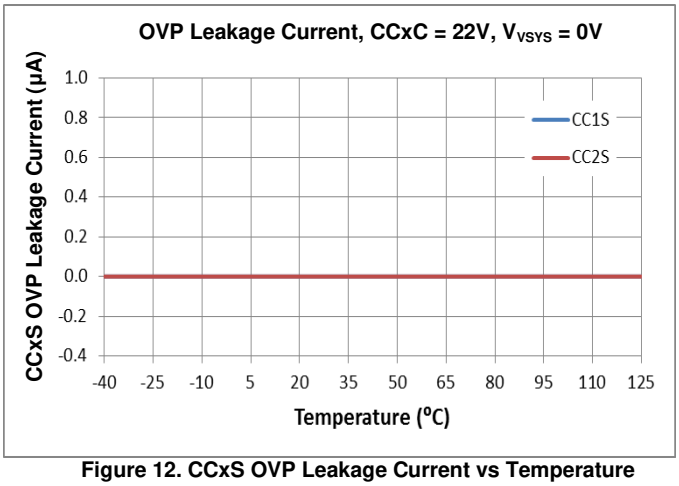

Figure 12. CCxS OVP Leakage Current vs Temperature

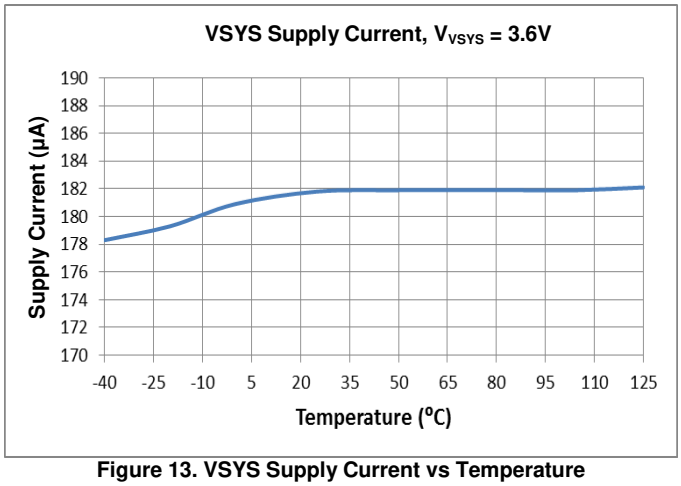

Figure 13. VSYS Supply Current vs Temperature

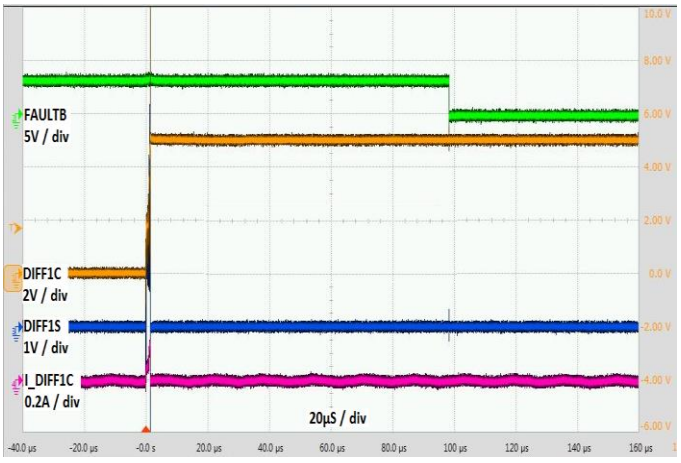

Figure 14. DIFF1C Short to 5V V_{BUS}

NEW PRODUCT

Performance Characteristics (@ T_A = +25°C, unless otherwise specified.) (continued)

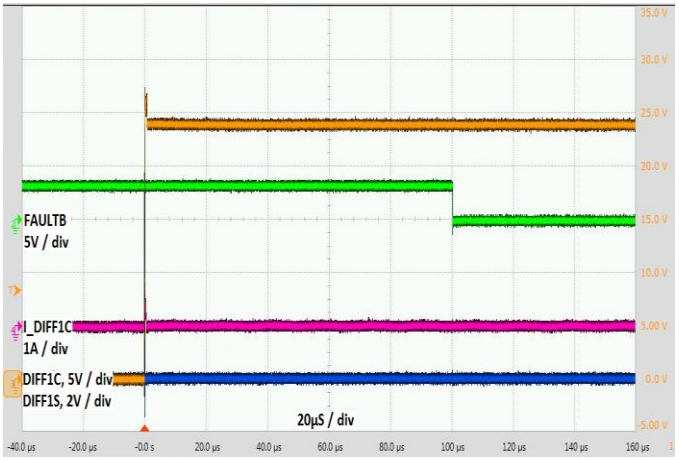

Figure 15. DIFF1C Short to 24V V_{BUS}

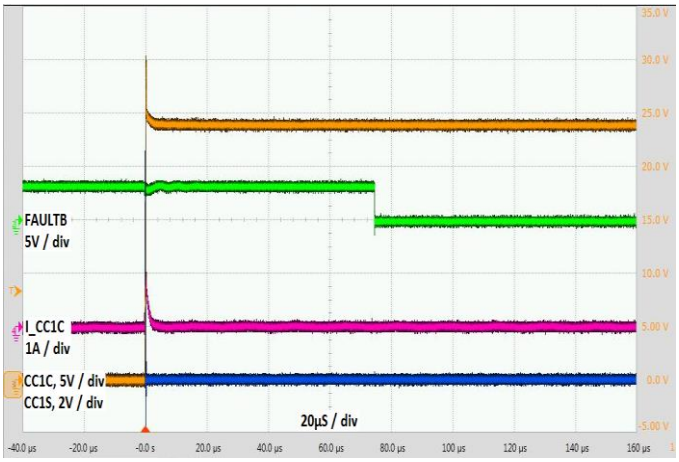

Figure 16. CC1C Short to 24V V_{BUS}

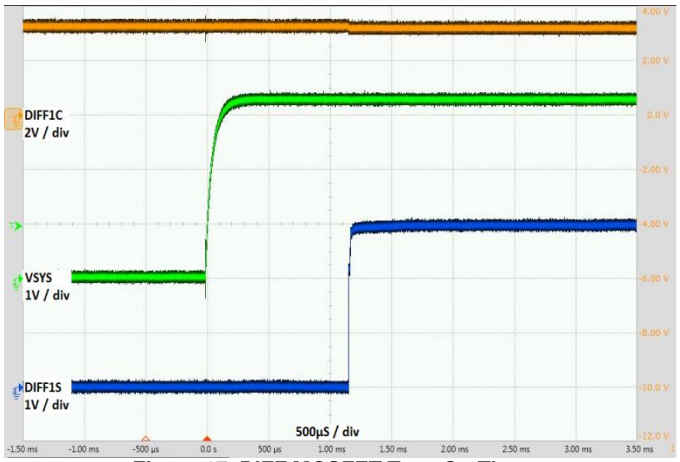

Figure 17. DIFF MOSFET Turn-On Time

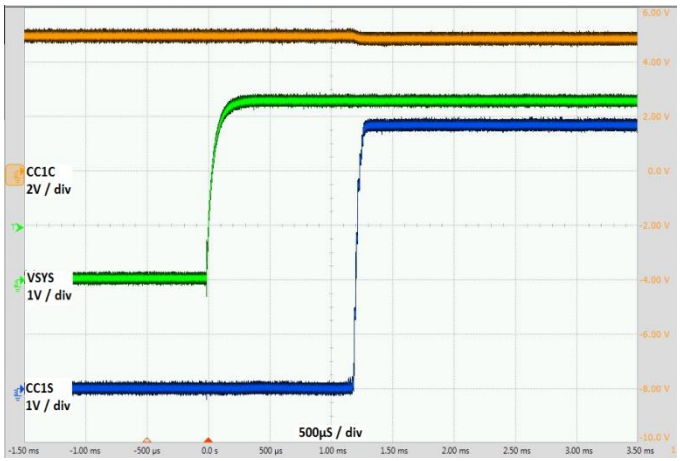

Figure 18. CC MOSFET Turn-On Time

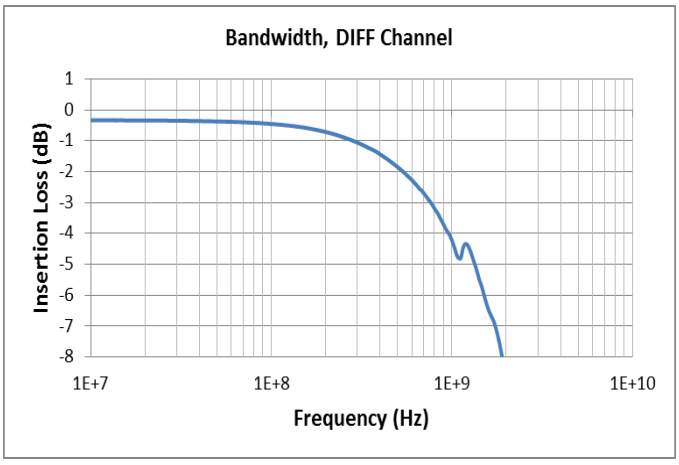

Figure 19. DIFF Channel Bandwidth

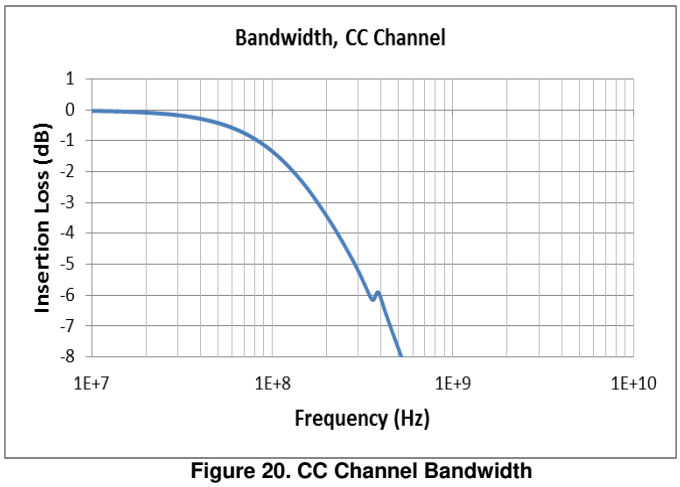

Figure 20. CC Channel Bandwidth

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Performance Characteristics (@ T_A = +25°C, unless otherwise specified.) (continued)

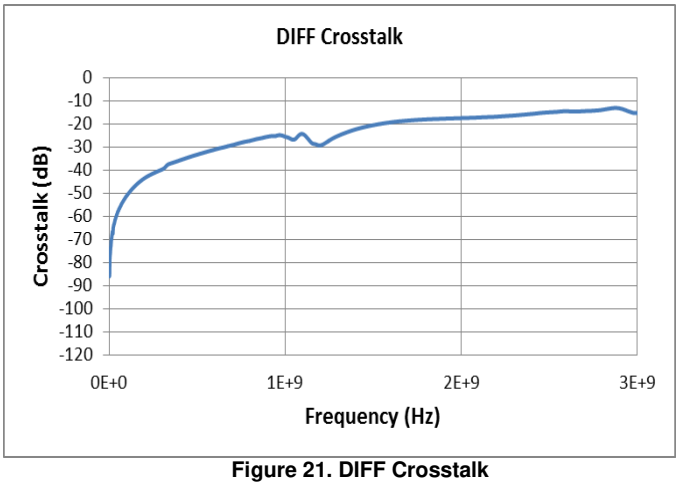

Figure 21. DIFF Crosstalk

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Application Information

General Description

The DPO2039DABQ-13 is a USB port protection device designed to work with USB Type-C connector, cable and USB PD to form a system that enables signal management and power delivery in a compact package. It provides short to VBUS protection for the CC and DIFF pins over the USB Type-C connector.

Short to VBUS Protection

The DPO2039DABQ-13 is a 4-channel uni-directional power switch with over-voltage protection. This is used to prevent the components inside a system which adopts the USB Type-C connector from being damaged by unexpected hazard. On the USB Type-C connector, the CC and DIFF pins are located in the close proximity of the VBUS pin. If ever the CC and/or the DIFF lines are short to the VBUS line either at the USB-C connector or at the cable end, the components (mostly ICs manufactured on the various sub-micron process nodes) behind the USB Type-C connector can easily be damaged by the resulting EOS. The damage, if occurred, is likely non-recoverable especially given that the voltage level on the VBUS line can go up to 20V or slightly higher. The DPO2039DABQ-13 integrates four series over-voltage FETs to protect the system side CC and DIFF lines. When either line on the Type-C connector side CC1C, CC2C, DIFF1C or DIFF2C is shorted to VBUS line, the DPO2039DABQ-13 will turn off the over-voltage FETs in less than 100ns window to isolate the system side CC and DIFF lines from the over-voltage connector side. When shorted to VBUS line is detected, the open-drain FAULTB will output low to indicate a fault condition.

Signal Operation Range

Table 1 and Table 2 show the signal operation range and output status:

0V to UVLO (Invalid)	0V to 5.85V	OFF
	5.85V to 20V	OFF
2.7V to 5.5V (Valid)	0V to 5.85V	ON
	5.85V to 20V	OFF: FAULTB Asserted (OVP detected)

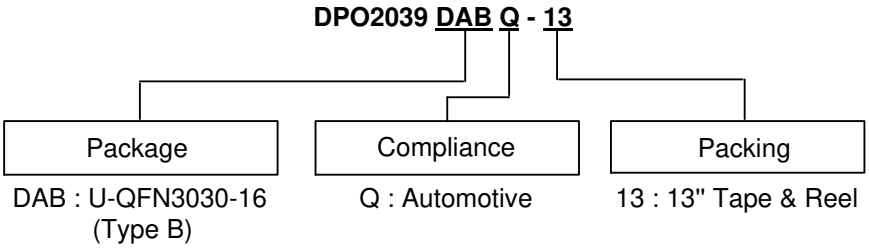
Table 1. Signal Operation Range for CCx

0V to UVLO (Invalid)	0V to 4.35V	OFF
	4.35V to 20V	OFF
2.7V to 5.5V (Valid)	0V to 4.35V	ON
	4.35V to 20V	OFF: FAULTB Asserted (OVP detected)

Table 2. Signal Operation Range for DIFFx

NEW PRODUCT

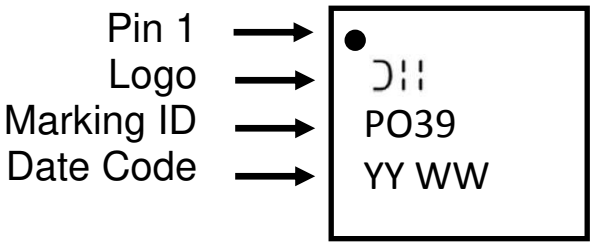
Ordering Information (Note 7)



Part Number	Marking ID	Reel Size (inches)	Tape Width (mm)	13" Tape and Reel	
				Quantity	Part Number Suffix
DPO2039DABQ-13	PO39	13	8	3,000/Tape & Reel	-13

Note: 7. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



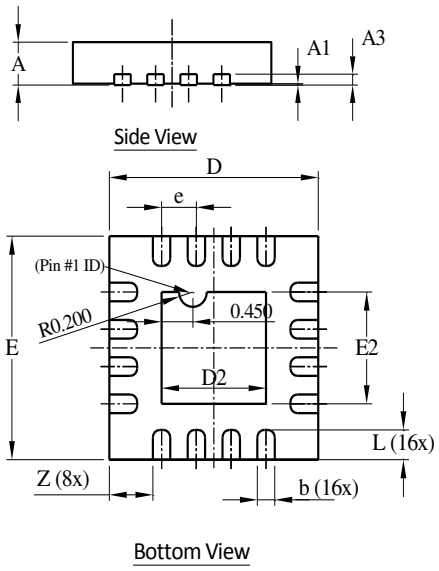
YY: Year
WW: Week 01 to 53

NEW PRODUCT

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN3030-16 (Type B)

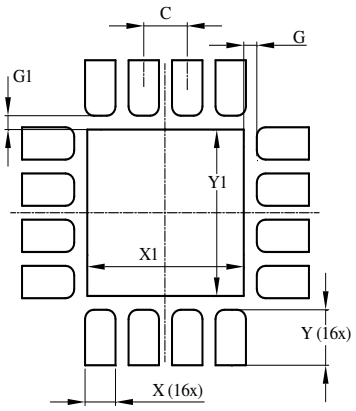


U-QFN3030-16 Type B			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.18	0.28	0.23
D	2.95	3.05	3.00
D2	1.40	1.60	1.50
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	-	-	0.50
L	0.35	0.45	0.40
Z	-	-	0.625
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN3030-16 (Type B)



Dimensions	Value (in mm)
C	0.500
G	0.150
G1	0.150
X	0.350
X1	1.800
Y	0.600
Y1	1.800

NEW PRODUCT

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