19-3889; Rev 1; 1/06

MAXIM

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

General Description

The MAX1365/MAX1367 low-power, 4.5- and 3.5-digit, panel meters feature an integrated sigma-delta analog-to-digital converter (ADC), LED display drivers, voltage digital-to-analog converter (DAC), and a 4–20mA (or 0 to 16mA) current driver.

The MAX1365/MAX1367's analog input voltage range is programmable to either ±2V or ±200mV. The MAX1367 drives a 3.5-digit (±1999 count) display and the MAX1365 drives a 4.5-digit (±19,999 count) display. The ADC output directly drives the LED display as well as the voltage DAC, which in turn drives the 4–20mA (or 0 to 16mA) current-loop output.

In normal operation, the 0 to 16mA/4–20mA current-loop output follows the ±2V or ±200mV analog input to drive remote panel-meter displays, data loggers, and other industrial controllers. For added flexibility, the MAX1365/MAX1367 allow direct access to the DAC output and the V/I converter input.

The sigma-delta ADC does not require external precision integrating capacitors, autozero capacitors, crystal oscillators, charge pumps, or other circuitry commonly required in dual-slope ADC panel-meter circuits. On-chip analog input and reference buffers allow direct interface with high-impedance signal sources. Excellent common-mode rejection and digital filtering provide greater than 100dB rejection of simultaneous 50Hz and 60Hz line noise. Other features include data hold, peak detection, and overrange/underrange detection.

The MAX1365/MAX1367 require a 2.7V to 5.25V supply, a 4.75V to 5.25V V/I supply, and a 7V to 30V loop supply. They are available in a space-saving (7mm x 7mm), 48-pin TQFP package and operate over the extended (-40°C to +85°C) temperature range.

Applications

Automated Test Equipment

Data-Acquisition Systems

Digital Multimeters

Digital Panel Meters

Digital Voltmeters

Industrial Process Control

Pin Configuration appears at end of datasheet.

Typical Operating Circuits appear at end of datasheet.

Features

- **Stand-Alone, Digital Panel Meter**
  - **20-Bit Sigma-Delta ADC**
    - **4.5-Digit Resolution (±19,999 Count, MAX1365)**
    - **3.5-Digit Resolution (±1999 Count, MAX1367)**
  - **No Integrating/Autozeroing Capacitors**
  - **100MΩ Input Impedance**
  - **±200mV or ±2.000V Input Range**
- **LED Display**
  - **Common-Cathode 7-Segment LED Driver**
  - **Programmable LED Current (0 to 20mA)**
  - **2.5Hz Update Rate**
- **Output DAC and Current Driver**
  - **±15-Bit DAC with 14-Bit Linear V/I Converter**
  - **Selectable 0 to 16mA or 4–20mA Current Output**
  - **Unipolar/Bipolar Modes**
  - **±50µA Zero Scale, ±40ppmFS/°C (typ)**
  - **±0.5% Gain Error, ±25ppmFS/°C (typ)**
  - **Separate 7V to 30V Supply for Current-Loop Output**
- **2.7V to 5.25V ADC/DAC Supply**
- **4.75V to 5.25V V/I Converter Supply**
- **Internal 2.048V Reference or External Reference**
- **48-Pin, 7mm x 7mm TQFP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1365ECM	-40°C to +85°C	48 TQFP
MAX1367ECM	-40°C to +85°C	48 TQFP

Selector Guide

PART	RESOLUTION (DIGITS)	PKG CODE
MAX1365ECM	4.5	C48-6
MAX1367ECM	3.5	C48-6

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

ABSOLUTE MAXIMUM RATINGS

AV_{DD}, DV_{DD} .....-0.3V to +6.0V
AIN+, AIN-, REF+, REF-.....V_{NEGV} to (AV_{DD} + 0.3V)
REG_FORCE, CMP, DAC_VDD, DACVOUT, CONV_IN, 4-20OUT.....-0.3V to (AV_{DD} + 0.3V)
EN_BPM, EN_I, REFSELE, DACDATA_SEL, INTREF, RANGE, $\overline{DPSET1}$, DPSET2, HOLD, PEAK, DPON, $\overline{CS\_DAC}$.....-0.3V to (DV_{DD} + 0.3V)
NEGV .....-2.6V to (AV_{DD} + 0.3V)
LED_EN.....-0.3V to (DV_{DD} + 0.3V)
SET.....-0.3V to (AV_{DD} + 0.3V)
REG_AMP, REG_VDD .....-0.3V to +6.0V
LEDV.....-0.3V to +6.0V
LEDG .....-0.3V to +0.3V
GND_DAC .....-0.3V to +0.3V
GND_V/I.....-0.3V to +0.3V
SEG_ to LEDG.....-0.3V to (V_{LEDV} + 0.3V)
DIG_ to LEDG.....-0.3V to (V_{LEDV} + 0.3V)
REF_DAC .....-0.3V to (AV_{DD} + 0.3V)
DIG_ Sink Current 300mA
DIG_ Source Current.....50mA
SEG_ Sink Current 50mA
SEG_ Source Current.....50mA
Maximum Current Input into Any Other Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 22.7mW/°C above +70°C).....1818.2mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, V_{LEDV} = +2.7V to +5.25V, LEDG = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), 4-20OUT = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ACCURACY						
Noise-Free Resolution		MAX1365	-19,999		+19,999	Counts
		MAX1367	-1999		+1999	
Integral Nonlinearity (Note 1)	INL	2.000V range		±1		Counts
		200mV range		±1		
Range Change Ratio		(V_{AIN+} - V_{AIN-} = 0.100V) on 200mV range; (V_{AIN+} - V_{AIN-} = 0.100V) on 2.0V range		10:1		Ratio
Rollover Error		V_{AIN+} - V_{AIN-} = full scale		±1		Counts
Output Noise				10		μV_{P-P}
Offset Error (Zero Input Reading)		V_{AIN+} - V_{AIN-} = 0 (Note 2)	-0		+0	Counts
Gain Error		(Note 3)	-0.5		+0.5	%FSR
Offset Drift (Zero Reading Drift)		V_{AIN+} - V_{AIN-} = 0 (Note 4)		0.1		µV/°C
Gain Drift				±1		ppm/°C
INPUT CONVERSION RATE						
Update Rate				5		Hz
ANALOG INPUTS (AIN+, AIN-) (bypass to GND with 0.1µF or greater capacitors)						
AIN Input Voltage Range (Note 5)		RANGE = GND	-2.0		+2.0	V
		RANGE = DV_{DD}	-0.2		+0.2	
AIN Absolute Input Voltage Range to GND			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		50Hz and 60Hz ±2%		100		dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, V_{LEDV} = +2.7V to +5.25V, LEDG = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), 4-20OUT = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Average Dynamic Input Current			-20		+20	nA
INTERNAL REFERENCE (REF- = GND, INTREF = DV_{DD})						
REF Input Voltage	V_{REF}		2.007	2.048	2.089	V
REF Output Short-Circuit Current				1		mA
REF Output Temperature Coefficient	TC_{VREF}			40		ppm/°C
Load Regulation		I_{SOURCE} = 0 to 300µA, I_{SINK} = 0 to 30µA		6		µV/µA
Line Regulation				50		µV/V
Noise Voltage		0.1Hz to 10Hz		25		$µV_{P-P}$
		10Hz to 10kHz		400		
EXTERNAL REFERENCE (INTREF = GND)						
REF Input Voltage		Differential (V_{REF+} - V_{REF-})		2.048		V
Absolute REF+, REF- Input Voltage to GND (V_{REF+} Must Be Greater Than V_{REF-})			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		50Hz and 60Hz ±2%		100		dB
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA
CHARGE PUMP						
Output Voltage	NEGV	C_{NEGV} = 0.1µF to GND	-2.60	-2.42	-2.30	V
DIGITAL INPUTS (INTREF, RANGE, PEAK, HOLD, DPSET1, DPSET2)						
Input Current	I_{IN}	V_{IN} = 0 or DV_{DD}	-10		+10	µA
Input Low Voltage	V_{INL}				0.3 x DV_{DD}	V
Input High Voltage	V_{INH}		0.7 x DV_{DD}			V
Input Hysteresis	V_{HYS}	DV_{DD} = 3V		200		mV

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, V_{LEDV} = +2.7V to +5.25V, LEDG = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), 4-20OUT = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC POWER SUPPLY (Note 7)						
AV_{DD} Voltage	AV_{DD}		2.70		5.25	V
DV_{DD} Voltage	DV_{DD}		2.70		5.25	V
Power-Supply Rejection AV_{DD}	PSR_A	(Note 8)		80		dB
Power-Supply Rejection DV_{DD}	PSR_D	(Note 8)		100		dB
AV_{DD} Current (Note 9)	I_{AVDD}				640	µA
		Standby mode			305	
DV_{DD} Current (Note 9)	I_{DVDD}	DV_{DD} = +5.25V			320	µA
		DV_{DD} = +3.3V			180	
		Standby mode			20	
DAC POWER SUPPLY						
DAC Supply Voltage	V_{DAC_VDD}		2.70		5.25	V
DAC Supply Current				0.10	0.21	mA
LINEAR REGULATOR AND V/I CONVERTER POWER REQUIREMENTS						
REG_AMP Supply Voltage	V_{REG_AMP}		4.75		5.25	V
REG_AMP Supply Current				0.19	0.30	mA
REG_VDD Supply Voltage	V_{REG_VDD}			5.20		V
REG_VDD Supply Current		Includes 20mA programmed current		25.2	27.4	mA
LED DRIVERS						
LED Supply Voltage	V_{LEDV}		2.70		5.25	V
LED Shutdown Supply Current	I_{SHDN}				10	µA
LED Supply Current	I_{LEDV}			176	180	mA
Display Scan Rate	f_{OSC}	MAX1365		512		Hz
		MAX1367		640		
Segment Current Slew Rate	$I_{SEG}/\Delta t$			25		mA/µs
DIG_ Voltage Low	V_{DIG}			0.178	0.300	V
Segment-Drive Source-Current Matching	ΔI_{SEG}			3	±12	%
Segment-Drive Source Current	I_{SEG}	V_{LEDV} - V_{SEG} = 0.6V, R_{SET} = 25kΩ	15.0	21.5	25.5	mA
LED Drivers Bias Current		From AV_{DD}		120		µA
Interdigit Blanking Time				4		µs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, V_{LEDV} = +2.7V to +5.25V, LEDG = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), 4-20OUT = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUT ACCURACY						
Zero-Scale Error		4–20mA or 0 to 16mA mode, T_A = +25°C			±50	µA
Zero-Scale Error Tempco				±40		ppmFS/°C
Gain Error		4–20mA or 0 to 16mA mode, T_A = +25°C			±0.5	%FS
Gain-Error Tempco				±25		ppmFS/°C
Span Linearity				±2	±4	µA
Power-Supply Rejection	PSR	V_{EXT} = 7V to 30V		4		µA/V
Signal Path Noise		10pF to GND on 4-20OUT		2.0		$µA_{RMS}$
4–20mA Current Limit		Limited to 12.5 x V_{REF} / 1.28kΩ		20		mA

Note 1: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after nulling the gain error and offset error.

Note 2: Offset calibrated.

Note 3: Offset nulled.

Note 4: Drift error is eliminated by recalibration at the new temperature.

Note 5: The input voltage range for the analog inputs is given with respect to the voltage on the negative input of the differential pair.

Note 6: V_{AIN+} or V_{AIN-} = -2.2V to +2.2V. V_{REF+} or V_{REF-} = -2.2V to +2.2V. All input structures are identical. Production tested on AIN+ and REF+ only. V_{REF+} must always be greater than V_{REF-}.

Note 7: Power-supply currents are measured with all digital inputs at either GND or DV_{DD}.

Note 8: Measured at DC by changing the power-supply voltage from 2.7V to 5.25V and measuring the effect on the conversion error with external reference. PSRR at 50Hz and 60Hz exceeds 120dB with filter notches at 50Hz and 60Hz (Figure 1).

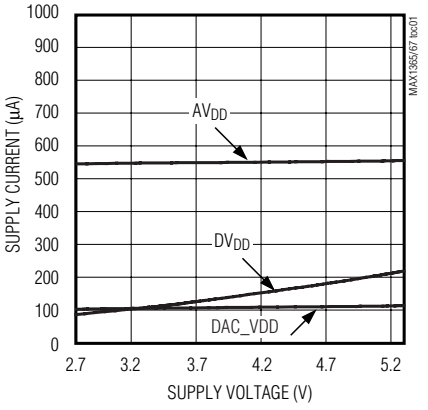
Note 9: LED drivers are disabled.

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

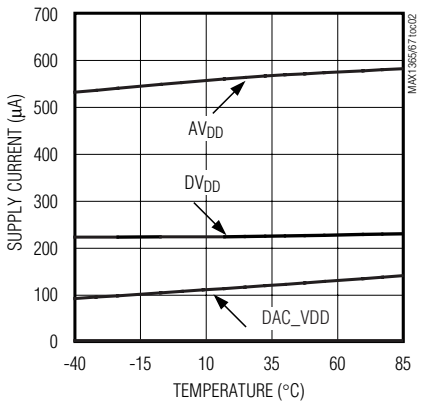
Typical Operating Characteristics

(A_{VDD} = D_{VDD} = +5V, V_{DAC_VDD} = +5.0V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, C_{REF+} = C_{REF-} = 0.1µF, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. T_A = +25°C, unless otherwise noted.)

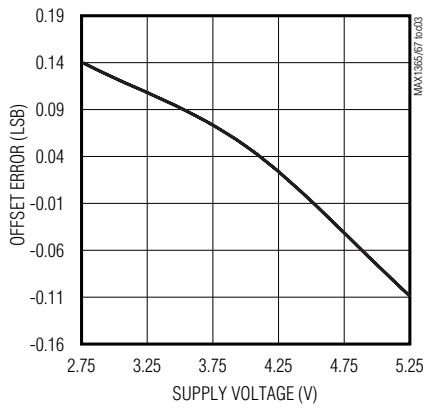
SUPPLY CURRENT vs. SUPPLY VOLTAGE



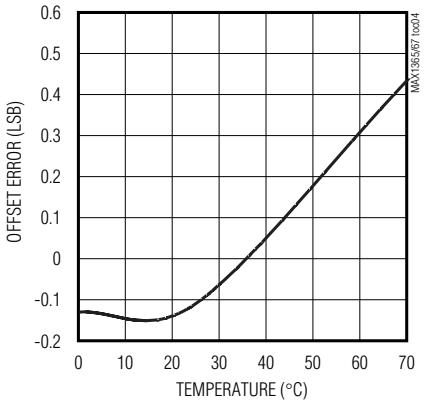
SUPPLY CURRENT vs. TEMPERATURE



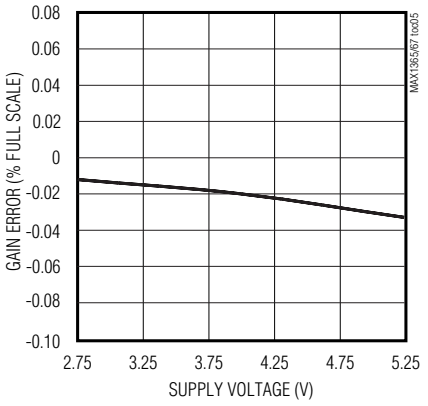
MAX1365 OFFSET ERROR vs. SUPPLY VOLTAGE



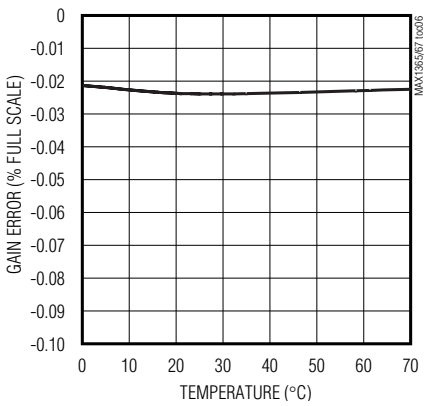
MAX1365 OFFSET ERROR vs. TEMPERATURE



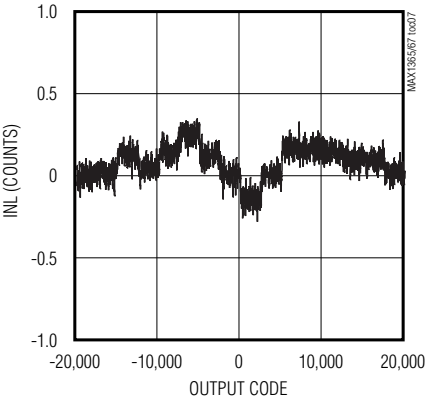
MAX1365 GAIN ERROR vs. SUPPLY VOLTAGE



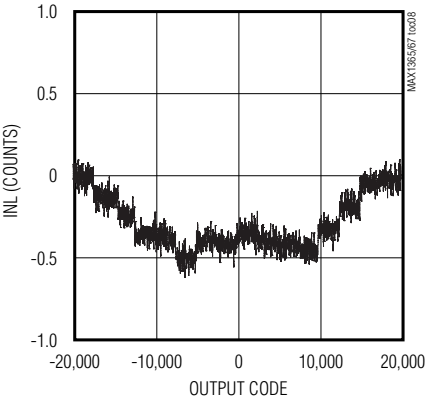
MAX1365 GAIN ERROR vs. TEMPERATURE



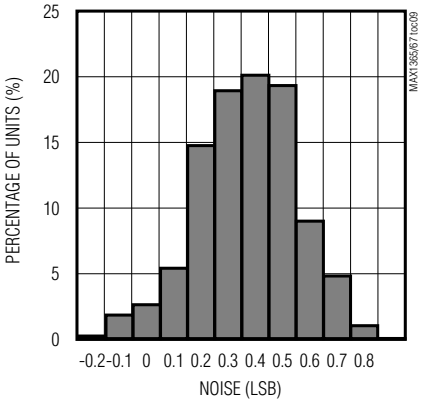
MAX1365 INL (±200mV INPUT RANGE) vs. OUTPUT CODE



MAX1365 INL (±2V INPUT RANGE) vs. OUTPUT CODE



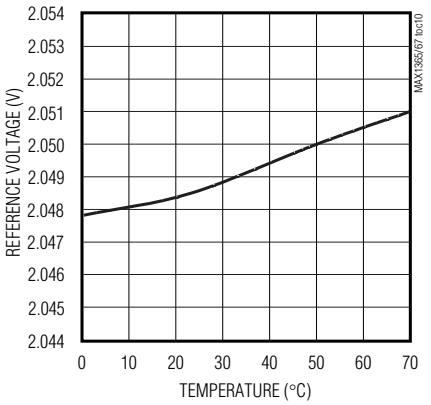
NOISE DISTRIBUTION



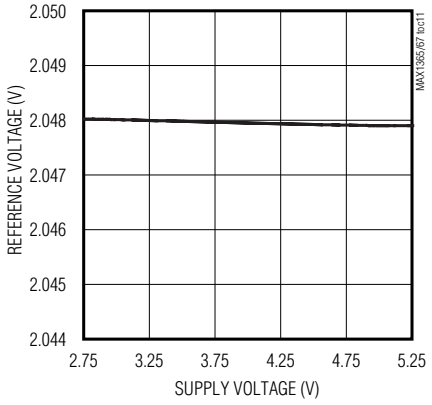
Typical Operating Characteristics (continued)

(A_{VDD} = D_{VDD} = +5V, V_{DAC_VDD} = +5.0V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, C_{REF+} = C_{REF-} = 0.1µF, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. T_A = +25°C, unless otherwise noted.)

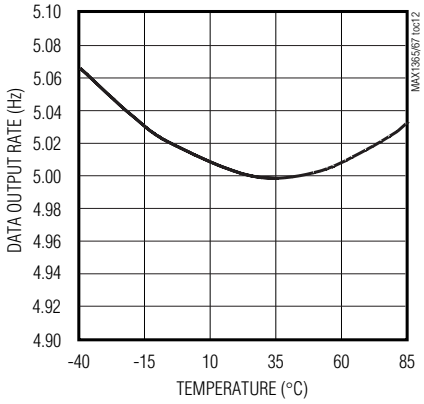
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



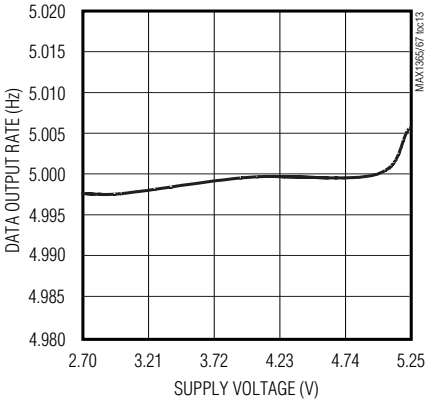
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



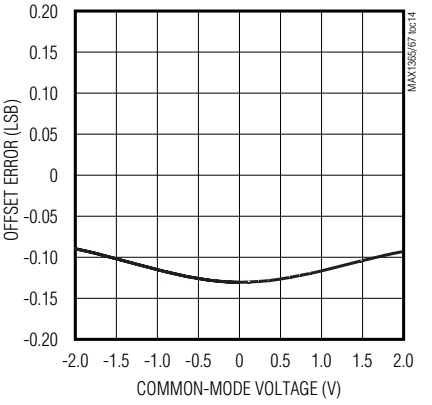
DATA OUTPUT RATE vs. TEMPERATURE



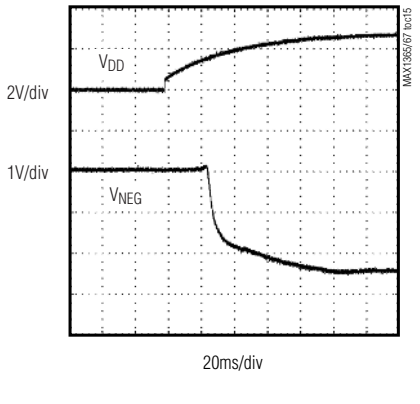
DATA OUTPUT RATE vs. SUPPLY VOLTAGE



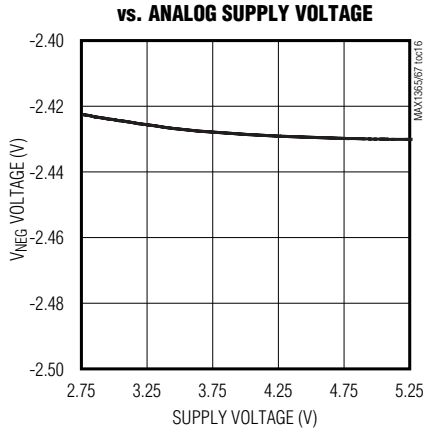
OFFSET ERROR vs. COMMON-MODE VOLTAGE



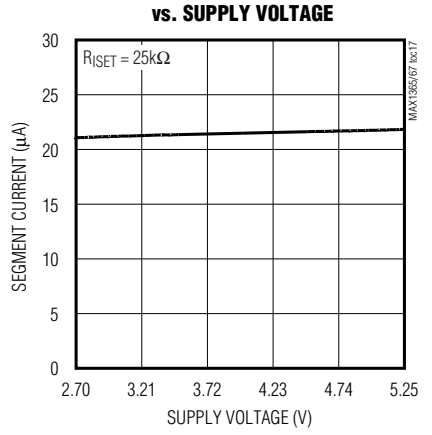
V_{NEG} STARTUP SCOPE SHOT



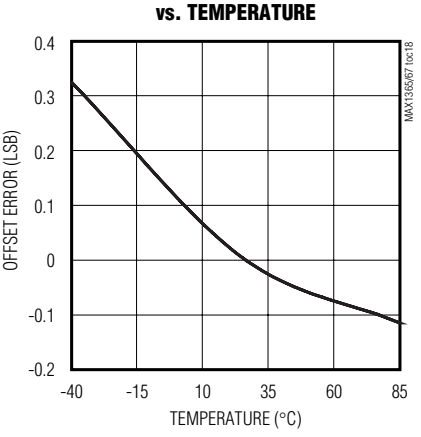
CHARGE-PUMP OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



SEGMENT CURRENT vs. SUPPLY VOLTAGE



DAC ZERO-CODE OFFSET ERROR vs. TEMPERATURE



Typical Operating Characteristics (continued)

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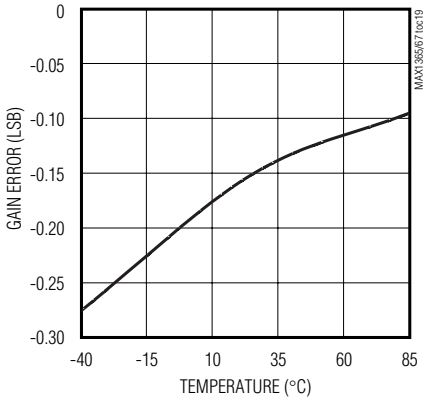
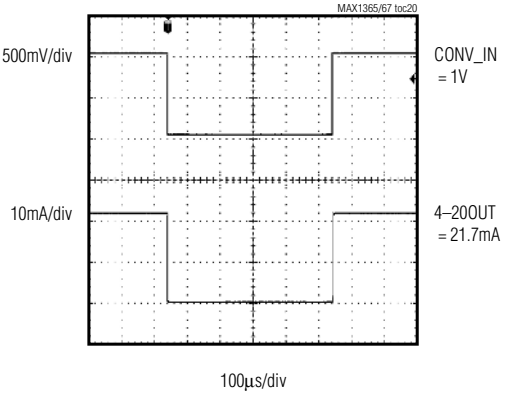
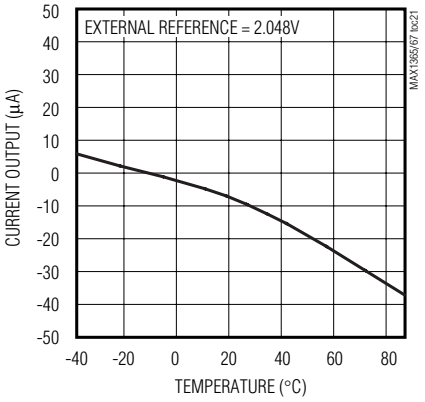
DAC GAIN ERROR vs. TEMPERATURE



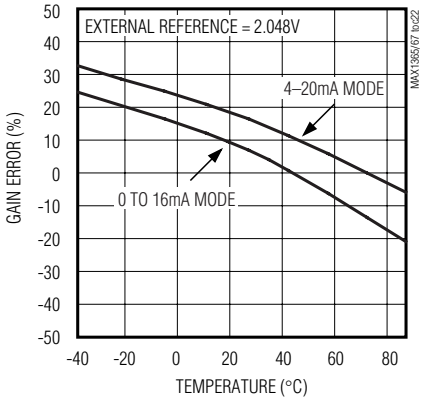
STEP RESPONSE



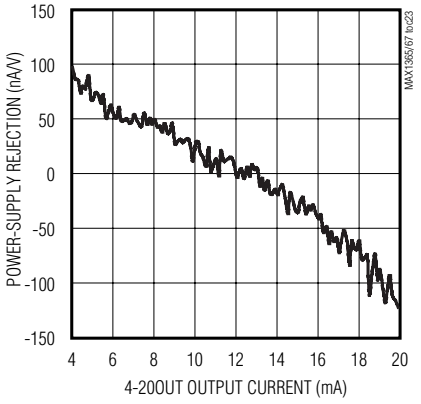
4–20OUT ZERO-SCALE ERROR vs. TEMPERATURE



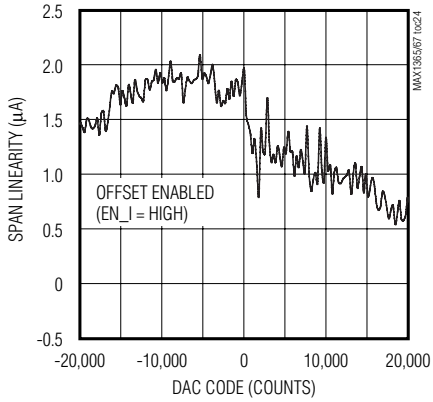
4–20OUT GAIN ERROR vs. TEMPERATURE



POWER-SUPPLY REJECTION vs. CURRENT OUTPUT (4-20OUT)



4–20OUT vs. DAC CODE (4–20OUT SPAN LINEARITY)



Pin Description

PIN	NAME	FUNCTION
1	AIN+	Positive Analog Input. Positive side of fully differential analog input. Bypass AIN+ to GND with a 0.1µF or greater capacitor.
2	AIN-	Negative Analog Input. Negative side of fully differential analog input. Bypass AIN- to GND with a 0.1µF or greater capacitor.
3	GND	Ground. Connect to star ground.
4	AV_{DD}	Analog Positive Supply Voltage. Connect AV_{DD} to a +2.7V to +5.25V power supply. Bypass AV_{DD} to GND with a 0.1µF capacitor.
5	DV_{DD}	Digital Positive Supply Voltage. Connect DV_{DD} to a +2.7V to +5.25V power supply. Bypass DV_{DD} to GND with a 0.1µF capacitor.
6	SET	Segment Current Set. Connect to ground through a resistor to set the segment current. See Table 7 for segment-current selection.
7	REG_VDD	V/I Converter Regulated Supply Output (5.2V typ)
8	REG_FORCE	REG_VDD Control. Drives the gate of external depletion-mode FET.
9	REG_AMP	Regulator/Reference Buffer Supply. Connect to a 4.75V to 5.25V power supply.
10	CMP	Regulator Compensation Node. Connect a 0.1µF capacitor from CMP to REG_FORCE.
11	DAC_VDD	DAC Analog Supply. Connect DAC_VDD to a +2.7V to +5.25V power supply.
12	DACVOUT	DAC Voltage Output. DAC output impedance is typically 6.2kΩ.
13	CONV_IN	V/I Converter Input
14	4-20OUT	4–20mA (0 to 16mA) Current-Loop Output. Referenced to GND.
15	GND_DAC	DAC Analog Ground. Connect to star ground.
16	GND_V/I	V/I Converter Analog Ground. Connect to star ground.
17	REF_DAC	V-to-I Converter/DAC Reference Input. Connect a voltage source for external reference operation or leave floating for internal reference. Bypass REF_DAC with a 0.1µF capacitor to GND for either internal or external reference operation.
18	EN_BPM	Active-High V/I-Converter Bipolar-Mode Enable. Set high for bipolar mode. Set low for unipolar mode.
19	EN_I	Active-High V/I-Converter 4mA Offset Enable. Set low for 0 to 16mA output. Set high for 4–20mA.
20	REFSELE	DAC External Reference Selection. Set low for internal reference. Set high for external reference. Leave REF_DAC unconnected when REFSELE is low.
21	DACDATA_SEL	DAC Data-Source Select. Connect to logic high for the MAX1365/MAX1367.
22	$\overline{CS\_DAC}$	DAC Chip Select. Connect to logic high for the MAX1365/MAX1367.
23	INTREF	ADC Reference Selection. Set INTREF high to select the internal ADC reference. Set INTREF low to select external ADC reference.
24	RANGE	ADC Range Select. Set RANGE low for ±2V analog input voltage range. Set RANGE high for ±200mV analog input voltage range.
25	PEAK	Peak Logic Input. Connect PEAK to DV_{DD} to display the highest ADC value on the LED. Connect PEAK to GND to disable the PEAK function (see Table 1).

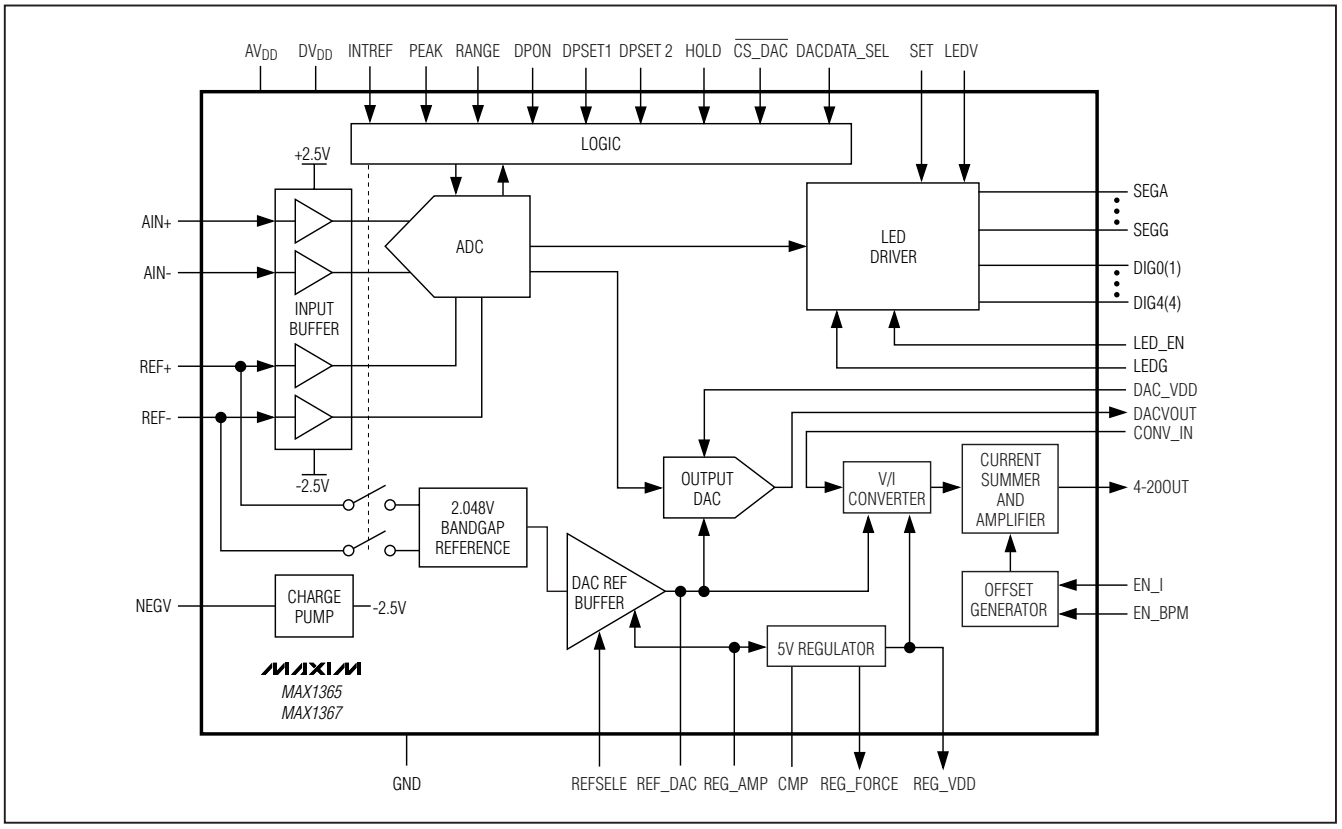
Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Pin Description (continued)

PIN	NAME	FUNCTION
26	HOLD	Hold Logic Input. Connect HOLD to DV_{DD} to hold the current ADC value on the LED. Connect HOLD to GND to update the LED at a rate of 2.5Hz and disable the hold function. Placing the device into hold mode initiates an offset mismatch calibration. Assert HOLD high for a minimum of 2s to ensure the completion of offset mismatch calibration (see Table 1).
27	DPSET2	Display Decimal-Point Logic-Input 2. Controls the decimal point of the LED. See the *Decimal-Point Control* section.
28	DPSET1	Display Decimal-Point Logic-Input 1. Controls the decimal point of the LED. See the *Decimal-Point Control* section.
29	LEDG	LED Segment-Drivers Ground
30	DIG0	Digit 0 Driver Out (Connected to GLED for the MAX1367)
31	DIG1	Digit 1 Driver Out
32	DIG2	Digit 2 Driver Out
33	DIG3	Digit 3 Driver Out
34	DIG4	Digit 4 Driver Out
35	SEGA	Segment A Driver
36	SEGB	Segment B Driver
37	LEDV	LED-Display Segment-Driver Supply. Connect to a +2.7V to +5.25V supply. Bypass with a 0.1µF capacitor to LEDG.
38	SEGC	Segment C Driver
39	SEGD	Segment D Driver
40	SEGE	Segment E Driver
41	SEGF	Segment F Driver
42	SEGG	Segment G Driver
43	SEGDP	Segment DP Driver
44	LED_EN	Active-High LED Enable. The MAX1365/MAX1367 display driver turns off when LED_EN is low. The MAX1365/MAX1367 LED-display driver turns on when LED_EN is high.
45	NEGV	-2.5V Charge-Pump Voltage Output. Connect a 0.1µF capacitor to GND.
46	DPON	Decimal-Point Enable Input. Controls the decimal point of the LED. See the *Decimal-Point Control* section. Connect DPON to DV_{DD} to enable the decimal point.
47	REF-	ADC Negative Reference Voltage Input. For internal reference operation, connect REF- to GND. For external reference operation, bypass REF- to GND with a 0.1µF capacitor and set V_{REF-} from -2.2V to +2.2V ($V_{REF+} > V_{REF-}$).
48	REF+	ADC Positive Reference Voltage Input. For internal reference operation, connect a 4.7µF capacitor from REF+ to GND. For external reference operation, bypass REF+ to GND with a 0.1µF capacitor and set V_{REF+} from -2.2V to +2.2V ($V_{REF+} > V_{REF-}$).

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Functional Diagram



Detailed Description

The MAX1365/MAX1367 low-power, highly integrated ADCs with LED drivers convert a ±2V differential input voltage (one count is equal to 100µV for the MAX1365 and 1mV for the MAX1367) with a sigma-delta ADC and output the result to an LED display. An additional ±200mV input range (one count is equal to 10µV for the MAX1365 and 100µV for the MAX1367) is available to measure small signals with finer resolution.

In addition to displaying the results on an LED display, these devices feature a DAC and V-to-I converter for 4–20mA (or 0 to 16mA) current output that proportionally follows the ADC input. The MAX1365/MAX1367 use an external depletion-mode NMOS transistor to regulate 7V to 30V for the V/I converter. Use the 4–20mA (or 0 to 16mA) output to drive a remote display, data logger, PLC input, or other 4–20mA devices in a current loop.

The MAX1365/MAX1367 include a 2.048V reference, internal charge pump, and a high-accuracy on-chip oscillator. The devices feature on-chip buffers for the differential input signal and external-reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal offset-calibration and offer > 100dB of 50Hz and 60Hz line-noise rejection. Other features include data hold and peak detection and overrange/underrange detection.

Analog Input Protection

The MAX1365/MAX1367 provide internal protection diodes that limit the analog input range on AIN+, AIN-, REF+, and REF- from NEGV to (AV_{DD} + 0.3V). If the analog input exceeds this range, limit the input current to 10mA.

Internal Analog Input/Reference Buffers

The MAX1365/MAX1367 analog input/reference buffers allow the use of high-impedance signal sources. The input buffers' common-mode input range allows the analog inputs and the reference to range from -2.2V to +2.2V.

Modulator

The MAX1365/MAX1367 perform analog-to-digital conversions using a single-bit, 3rd-order, sigma-delta modulator. The sigma-delta modulator converts the input

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

signal into a digital pulse train whose average duty cycle represents the digitized signal information. The modulator quantizes the input signal at a much higher sample rate than the bandwidth of the input. The MAX1365/MAX1367 modulator provides 3rd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise. A single-bit data stream is then presented to the digital filter to remove the frequency-shaped quantization noise.

Digital Filtering

The MAX1365/MAX1367 contain an on-chip digital low-pass filter that processes the data stream from the modulator using a $SINC^4$ response:

$$\left(\frac{\sin(x)}{x}\right)^4$$

The $SINC^4$ filter has a settling time of four output data periods (4 x 200ms). The MAX1365/MAX1367 have 25% overrange capability built into the modulator and digital filter. The digital filter is optimized for the f_{CLK} equal to 4.9152MHz. The frequency response of the $SINC^4$ filter is calculated as follows:

$$H(z)=\left[\frac{1(1-Z^{-N})}{N_{(1-Z^{-1})}}\right]^4$$

$$H(f)=\frac{1}{N}\left[\frac{\sin\left(N\pi\frac{f}{f_m}\right)}{\sin\left(\frac{\pi f}{f_m}\right)}\right]^4$$

where N is the oversampling ratio, and f_m = N x output data rate = 5Hz.

Filter Characteristics

Figure 1 shows the filter frequency response. The $SINC^4$ characteristic -3dB cutoff frequency is 0.228 times the first notch frequency (5Hz). The oversampling ratio (OSR) for the MAX1367 is 128 and the OSR for the MAX1365 is 1024. The output data rate for the digital filter corresponds to the positioning of the first notch of the filter's frequency response. The notches of the $SINC^4$ filter are repeated at multiples of the first notch frequency. The $SINC^4$ filter provides an attenuation of better than 100dB at these notches. For example, 50Hz is equal to 10 times the first notch frequency and 60Hz is equal to 12 times the first notch frequency. For large step changes at the input, allow a settling time of 800ms before valid data is read.

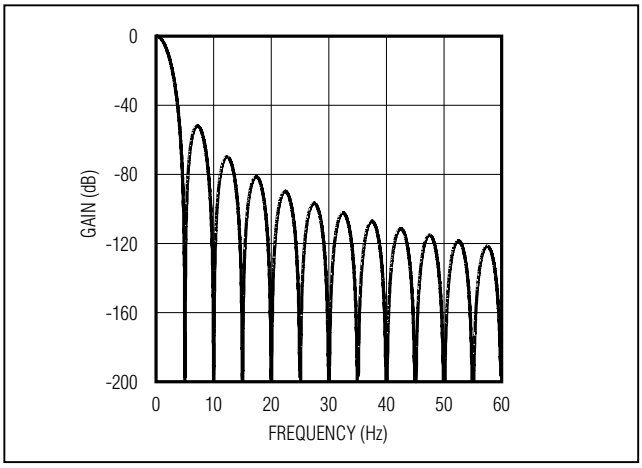


Figure 1. Frequency Response of the $SINC^4$ Filter (Notch at 60Hz)

Internal Clock

The MAX1365/MAX1367 contain an internal oscillator. Using the internal oscillator saves board space by removing the need for an external clock source. The oscillator is optimized to give 50Hz and 60Hz power-supply and common-mode rejection.

Charge Pump

The MAX1365/MAX1367 contain an internal charge pump to provide the negative supply voltage for the internal analog input/reference buffers. The bipolar input range of the analog input/reference buffers allows this device to accept negative inputs with high source impedances. Connect a 0.1µF capacitor from NEGV to GND.

LED Driver (Table 1)

The MAX1365 has a 4.5-digit common-cathode display driver, and the MAX1367 has a 3.5-digit common-cathode display driver. In addition, the LED drivers of the MAX1365/MAX1367 feature peak-detection and data-hold circuitry.

Figures 2 and 3 show the connection schemes for a standard seven-segment LED display. The LED update rate is 2.5Hz. Figure 4 shows a typical common-cathode configuration for two digits. In common-cathode configuration, the cathodes of all LEDs in a digit are connected together. Each segment driver of the MAX1365/MAX1367 connects to its corresponding LED's anodes. For example, segment driver SEGA connects to all LED segments designated as A. Similar configurations are used for other segment drivers.

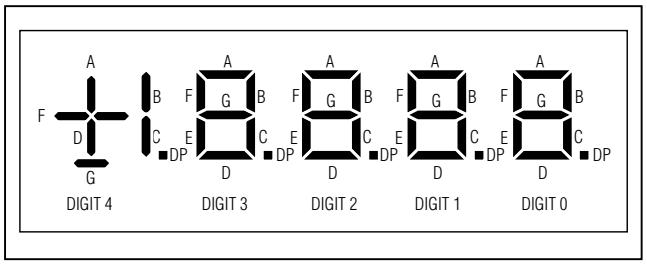


Figure 2. Segment Connection for the MAX1365 (4.5 Digits)

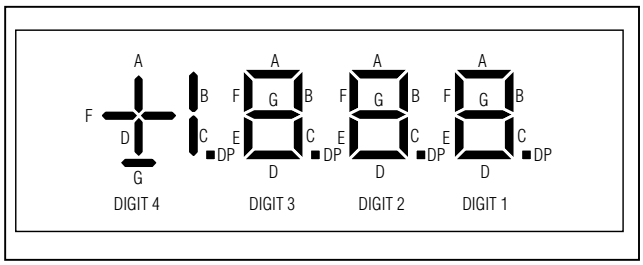


Figure 3. Segment Connection for the MAX1367 (3.5 Digits)

The MAX1365/MAX1367 use a multiplexing scheme to drive one digit at a time. The scan rate is fast enough to make the digits appear to be lit. Figure 5 shows the data-timing diagram for the MAX1365/MAX1367 where T is the display scan period (typically around 1/512Hz or 1.9531ms). T_{ON} in Figure 5 denotes the amount of time each digit is on and is calculated as follows:

$$T_{ON} = \frac{T}{5} = \frac{1.95312ms}{5} = 390.60\mu s$$

Decimal-Point Control

The MAX1365/MAX1367 allow for full decimal-point control and feature leading-zero suppression.

Use the DPON, DPSET1, and DPSET2 bits in the control register to set the value of the decimal point (Tables 2 and 3). The MAX1365/MAX1367 overrange and underrange display is shown in Table 4.

Leading-Zero Suppression

The MAX1365/MAX1367 include a leading-zero suppression circuitry to turn off unnecessary zeros. For example, when DPSET1 and DPSET2 = [0,0], 0.0 is displayed instead of 000.0 (MAX1365). This feature saves a substantial amount of power by not lighting unnecessary LEDs.

Interdigit Blanking

The MAX1365/MAX1367 also include an interdigit-blanking circuitry. Without this feature, it is possible to see a faint digit next to a digit that is completely on. The interdigit-blanking circuitry prevents ghosting over into the next digit for a short period of time. The typical interdigit blanking time is 4µs.

Table 1. LED Priority Table

HOLD	PEAK	DISPLAY VALUES FORM
1	X	Hold value
0	1	Peak value
0	0	Latest ADC result

X = Don't care.

Table 2. Decimal-Point Control Table—MAX1365

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
0	0	0	18888	0
0	0	1	18888	0
0	1	0	18888	0
0	1	1	18888	0
1	0	0	1888.8	0.0
1	0	1	188.88	0.00
1	1	0	18.888	0.000
1	1	1	1.8888	0.0000

Table 3. Decimal-Point Control Table—MAX1367

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
1	0	0	1888.	0.
1	0	1	188.8	0.0
1	1	0	18.88	0.00
1	1	1	1.888	0.000

Table 4. LED During Overrange and Underrange Conditions

CONDITION	MAX1367	MAX1365
Overrange	1---	1----
Underrange	-1---	-1----

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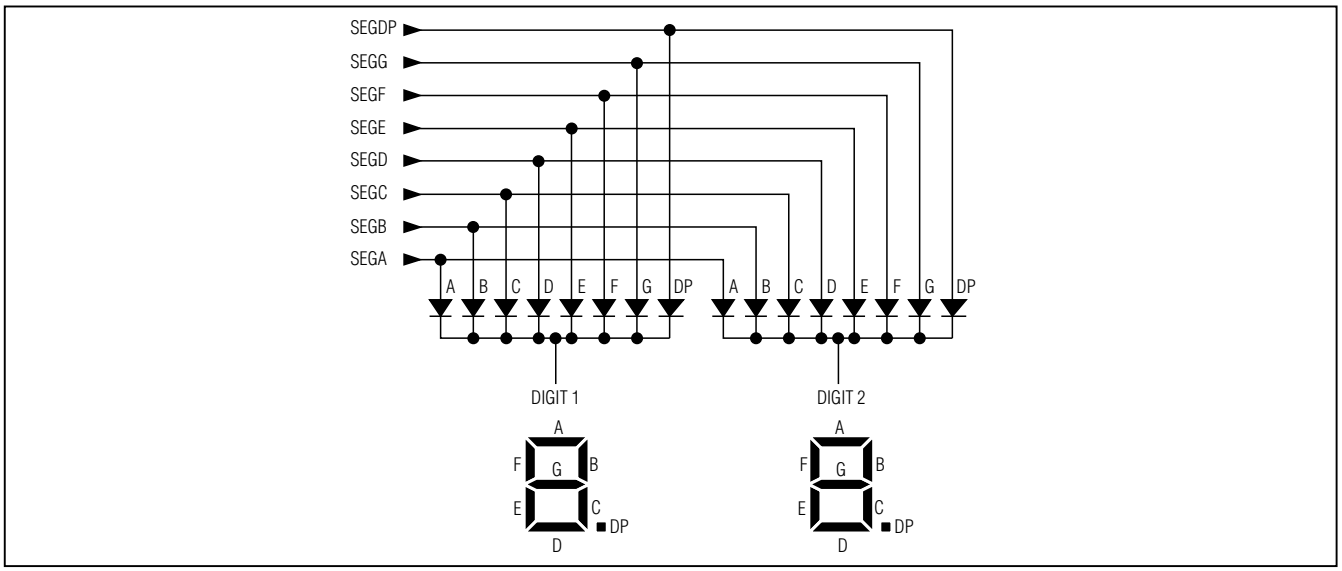

Figure 4. 2-Digit Common-Cathode Configuration

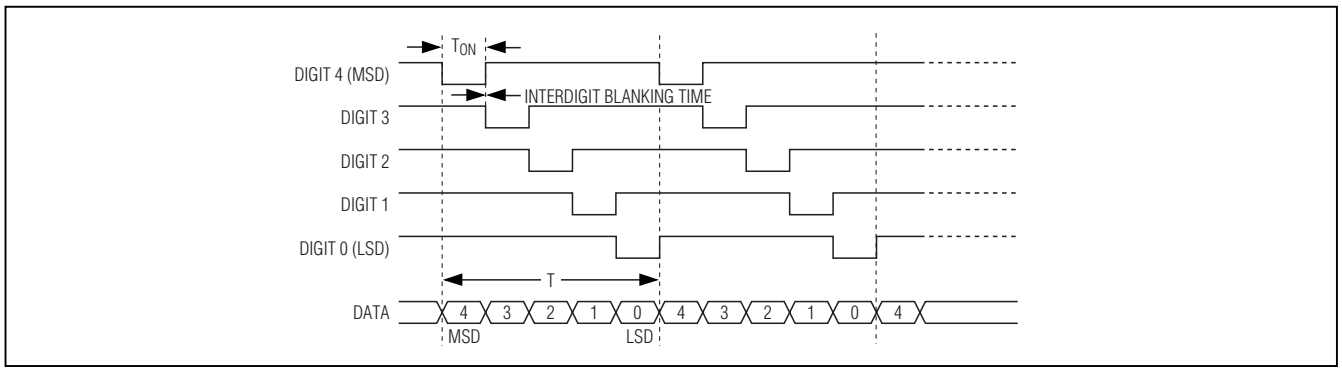

Figure 5. LED Voltage Waveform

Current Output

The MAX1365/MAX1367 feature a 4–20mA (0 to 16mA) current output for driving remote panel meters, data loggers, and process controllers in industrial applications. The DAC output is proportional to the input of the ADC and LED display. In the simplest configuration, connect DAC_VOUT directly to CONV_IN to have the current output (4–20mA or 0 to 16mA) follow the analog inputs.

Custom signal conditioning can be inserted between DAC_VOUT and CONV_IN, or CONV_IN can be driven independently by a voltage source if desired. See Figures 11–14 for the transfer functions of the DAC and V/I converter.

Note: The MAX1365/MAX1367 expect a 6kΩ (typ) source impedance from the external voltage source driving CONV_IN.

Current Offset

Set EN_I high for a current span of 4–20mA. Set EN_I low for a current span of 0 to 16mA. See Table 5 for current output.

Unipolar Mode

Set EN_BPM low to engage unipolar operation. In unipolar mode, the current output at 4-20OUT (4–20mA or 0 to 16mA) maps the analog input voltage (0 to 2V or 0 to 200mV). Negative voltages at the analog input result in a 4mA or 0mA output, depending on the EN_I setting. See Table 5 for current output. See Figures 12 and 13.

Table 5. Current Output Table

ANALOG INPUT	CURRENT OUTPUT (mA)			
	UNIPOLAR MODE (EN_I = LOW)	UNIPOLAR MODE (EN_I = HIGH)	BIPOLAR MODE (EN_I = LOW)	BIPOLAR MODE (EN_I = HIGH)
Negative Full Scale	0	4	0	4
0V	0	4	8	12
Positive Full Scale	16	20	16	20

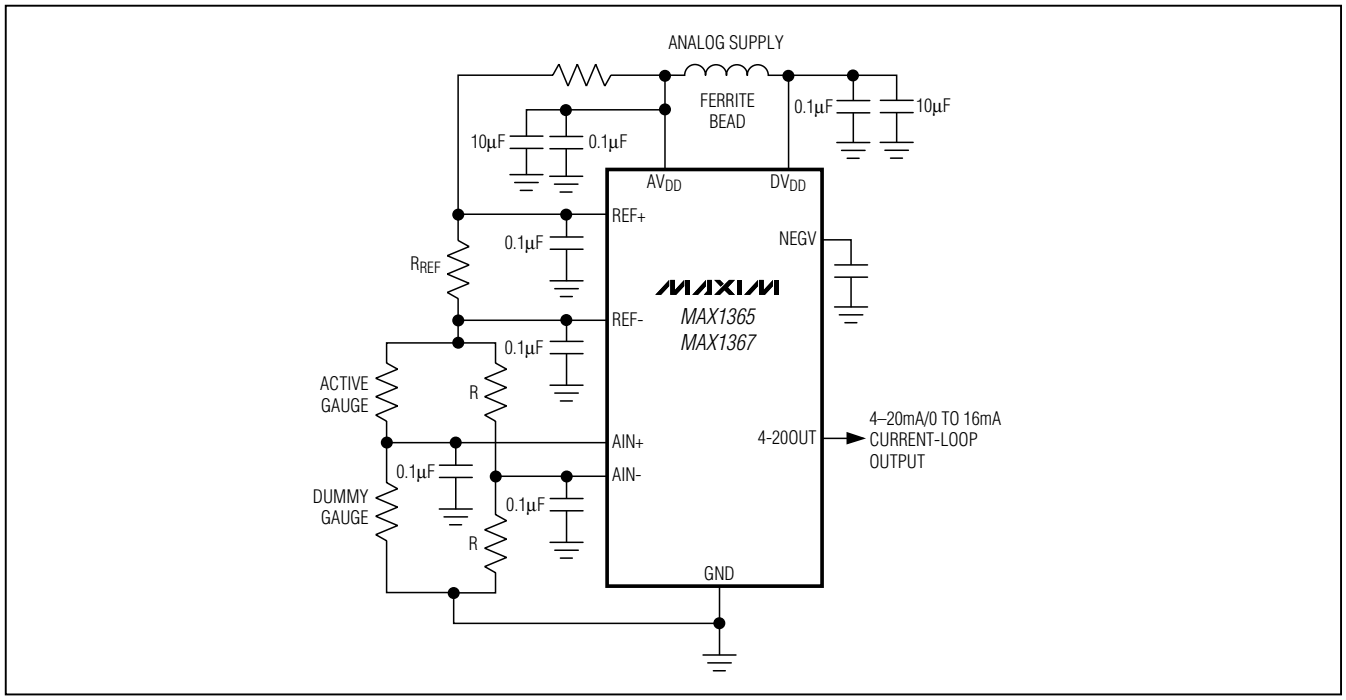

Figure 6. Strain-Gauge Application with the MAX1365/MAX1367

Bipolar Mode

Set EN_BPM high to engage bipolar operation. In bipolar mode, the current output at 4–20OUT (4–20mA or 0 to 16mA) maps the analog input voltage (±2V or ±200mV). In bipolar mode, a 0V analog input maps to midscale (12mA). See Table 5 for current output (see Figures 12 and 13).

5.2V Linear Regulator with Compensation

The MAX1365/MAX1367 feature a 5.2V linear regulator. The 5.2V regulator consists of an op amp and connections to an external depletion-mode FET. The 5.2V regulator regulates the loop voltage that powers the voltage-to-current converter and the rest of the transmitter circuitry. The regulator output voltage is available at REG_VDD and is given by the equation:

$$V_{REG\_VDD} = 2.54 \times V_{REF+}$$

The FET breakdown and saturation voltages determine the usable range of loop voltages (V_{EXT}). The external FET parameters such as V_{GS} (off), I_{DSS}, and transconductance must be chosen so that the op amp output on the REG_FORCE pin can control the FET operating point while swinging in the range from VREG_AMP to REG_VDD. See the *Selecting Depletion-Mode FET* section in the *Applications Information* section.

Connect a 0.1µF capacitor between CMP and REG_FORCE to ensure stable operation of the regulator.

Applications Information

Power-On Reset

At power-on, the digital filter and modulator circuits reset. The MAX1365 allows 6s for the reference to stabilize before performing enhanced offset calibration.

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During these 6s, the MAX1365 displays 1.2V to 1.5V when a stable reference is detected. If a valid reference is not found, the MAX1365 times out after 6s and begins enhanced offset calibration. Enhanced offset calibration typically lasts 2s. The MAX1365 begins converting after enhanced offset calibration.

Reference

ADC Reference

The MAX1365/MAX1367 reference sets the full-scale range of the ADC transfer function. With a nominal 2.048V reference, the ADC full-scale range is ±2V with RANGE = GND. With RANGE = DV_{DD}, the full-scale range is ±200mV. A decreased reference voltage decreases full-scale range (see the *Transfer Functions* section).

The ADC of the MAX1365/MAX1367 can accept either an external reference or an internal reference (INTREF). The INTREF logic selects the reference mode. For internal-reference operation, set INTREF to DV_{DD}, connect REF- to GND, and bypass REF+ to GND with a 4.7µF capacitor. The internal reference provides a nominal 2.048V source between REF+ and GND. The internal-reference temperature coefficient is typically 40ppm/°C.

For external-reference operation, set INTREF to GND. REF+ and REF- are fully differential. For a valid external-reference input, VREF+ must be greater than VREF-. Bypass REF+ and REF- with a 0.1µF or greater capacitor to GND in external-reference mode.

Figure 6 shows the MAX1365/MAX1367 operating with an external differential reference. In this figure, REF- is connected to the top of the strain gauge and REF+ is connected to the midpoint of the resistor-divider of the supply.

DAC Reference

The DAC of the MAX1365/MAX1367 accept either an external reference or an internal reference. The REFSELE enables or disables the internal reference. For external-reference operation, disable the DAC reference buffer by setting REFSELE to DV_{DD} and connect a voltage source to REF_DAC.

For internal-reference operation, enable the DAC reference buffer by setting REFSELE to GND. In this mode, leave REFDAC floating.

In either internal or external reference operation, bypass REF_DAC with a 0.1µF capacitor to GND. Choose a reference with output impedance (load regulation equivalent) of 100mΩ or less, such as the MAX6126. For best performance, use an external reference source for the ADC and DAC.

DAC Operation

For the MAX1365/MAX1367, a voltage proportional to the ADC input is available at DACVOUT. Connect DACVOUT to CONV_IN for normal operation. See Figure 11 for the DAC transfer function.

Offset Calibration

The MAX1365/MAX1367 offer on-chip offset calibration. The device offset calibrates during every conversion cycle.

Enhanced Offset Calibration

Enhanced offset calibration is a more accurate calibration method that is needed in the case of the ±200mV range and 4.5-digit resolution. In addition to enhanced offset calibration at power-up, the MAX1365/MAX1367 perform enhanced calibration on demand by connecting HOLD to AV_{DD} for > 2s.

Peak

The MAX1365/MAX1367 feature peak-detection circuitry. When activated, the devices display only the highest voltage measured to the LED. First, the current ADC result is displayed. The new ADC conversion result is compared to the current result. If the new value is larger than the previous peak value, the new value is displayed. If the new value is less than the previous peak value, the display remains unchanged. Connect PEAK to GND to clear the peak value and disable the peak function. See Table 1 for LED Display priority.

Hold

The MAX1365/MAX1367 feature data-hold circuitry. When activated, the device holds the current reading on the LED.

Strain-Gauge Measurement

Connect the differential inputs of the MAX1365/MAX1367 to the bridge network of the strain gauge. In Figure 6, the analog supply voltage powers the bridge network and the MAX1365/MAX1367, along with the reference voltage. The MAX1365/MAX1367 handle an analog input voltage range of ±200mV and ±2V full scale. The analog/reference inputs of the parts allow the analog input range to have an absolute value of anywhere between -2.2V and +2.2V.

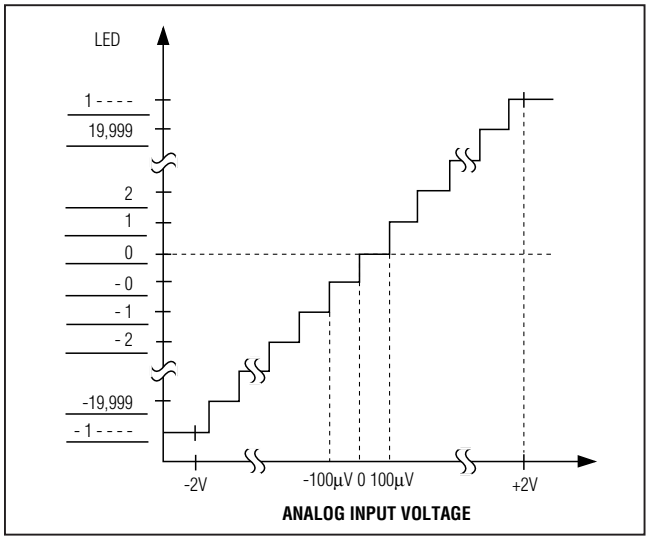

Figure 7. MAX1365 Transfer Function—±2V Range

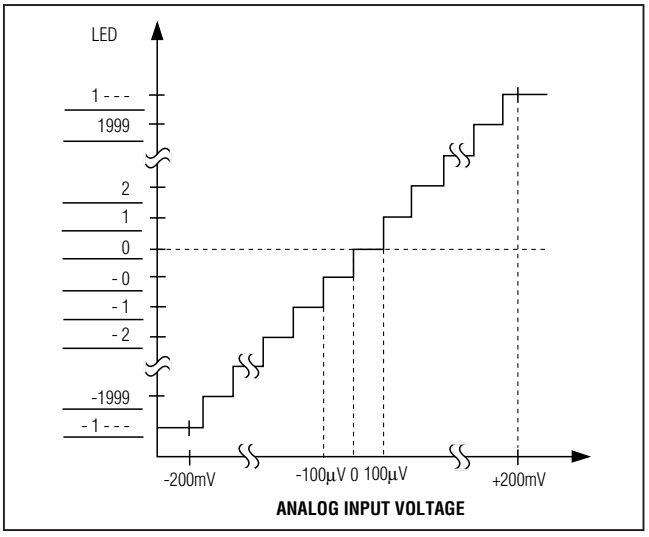

Figure 9. MAX1367 Transfer Function—±200mV Range

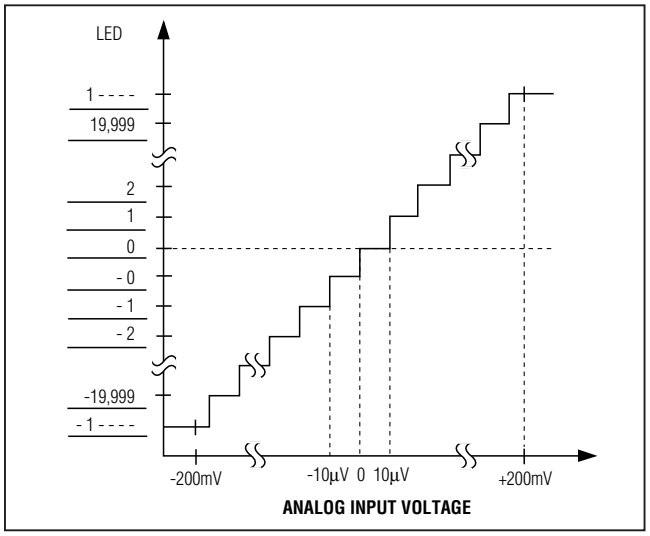

Figure 8. MAX1365 Transfer Function—±200mV Range

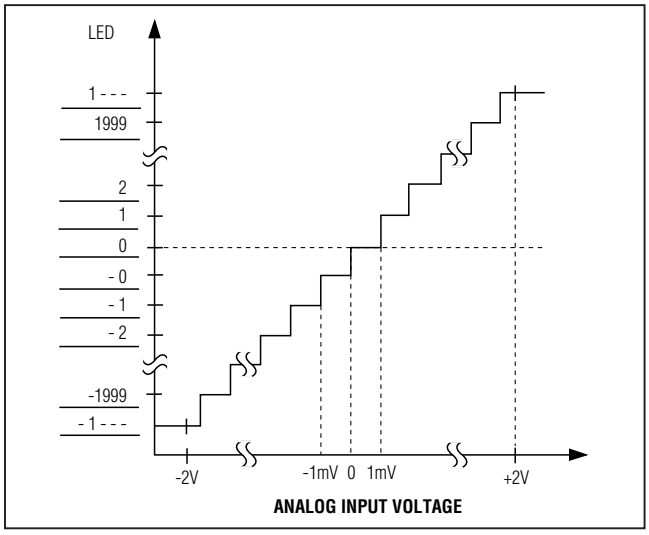

Figure 10. MAX1367 Transfer Function—±2V Range

Transfer Functions

ADC Transfer Functions

Figures 7–10 show the transfer functions of the MAX1365/MAX1367. The output data is stored in the ADC data register in two's complement.

The transfer function for the MAX1365 with AIN+ - AIN- ≥ 0 and RANGE = GND is:

$$(1)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right)$$

The transfer function for the MAX1365 with AIN+ - AIN- < 0 and RANGE = GND is:

$$(2)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) + 1$$

The transfer function for the MAX1367 with AIN+ - AIN- ≥ 0 and RANGE = GND is:

$$(3)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right)$$

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

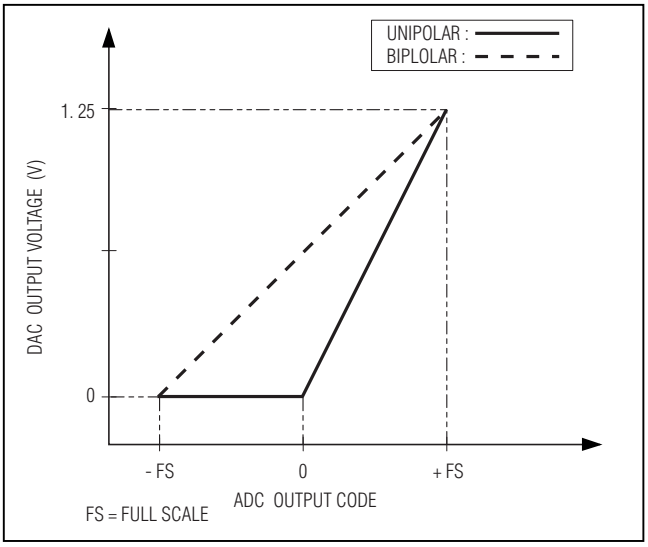

Figure 11. DAC Output Voltage vs. ADC Output Code

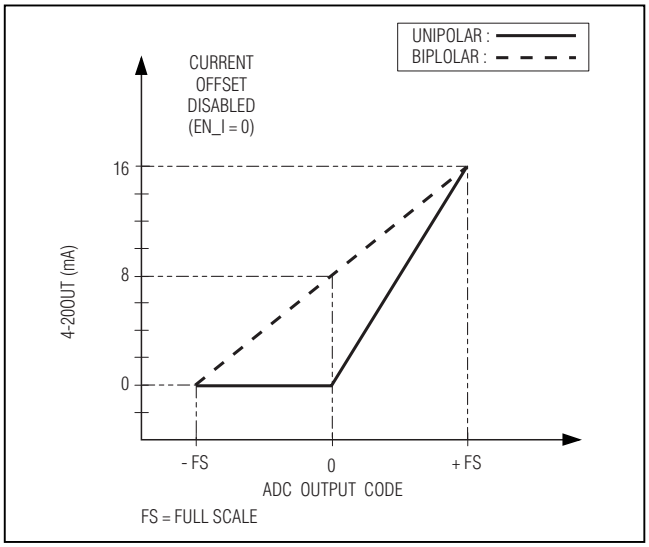

Figure 13. Output Current (4-20OUT) vs. ADC Output Code (Current Offset Disabled)

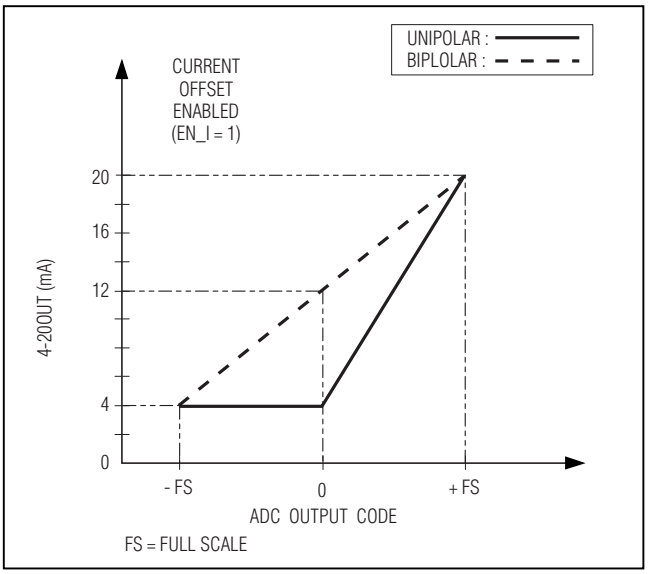

Figure 12. Output Current (4-20OUT) vs. ADC Output Code (Current Offset Enabled)

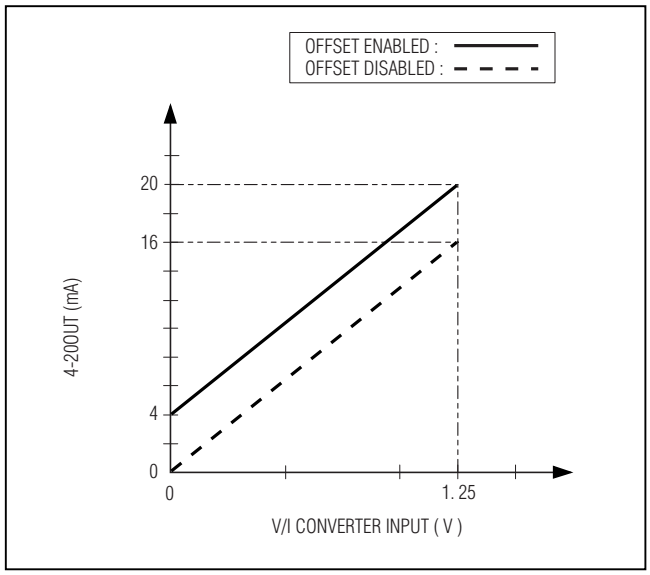

Figure 14. 4-20OUT Output Current vs. V/I Converter Input Voltage

The transfer function for the MAX1367 with AIN+ - AIN- < 0 and RANGE = GND is:

$$(4)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) + 1$$

The transfer function for the MAX1365 with AIN+ - AIN- ≥ 0 and RANGE = DV_{DD} is:

$$(5)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10$$

The transfer function for the MAX1365 with AIN+ - AIN- < 0 and RANGE = DV_{DD} is:

$$(6)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10 + 1$$

The transfer function for the MAX1367 with AIN+ - AIN- ≥ 0 and RANGE = DV_{DD} is:

$$(7)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10$$

The transfer function for the MAX1367 with AIN+ - AIN- < 0 and RANGE = DV_{DD} is:

$$(8)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10 + 1$$

DAC Transfer Functions

Figure 11 shows the DAC transfer function for the MAX1365/MAX1367 in unipolar and bipolar modes.

The transfer function for the DAC in the MAX1365/MAX1367 unipolar mode is:

$$V_{DACVOUT} = \frac{N}{32{,}768 - 1} \times V_{REF}$$

where N = two's complement ADC output code.

In unipolar mode, $V_{DACVOUT}$ is equal to 0V for all two's complement ADC codes less than zero (see Figure 12).

The transfer function for the DAC in the MAX1365/MAX1367 in bipolar mode is:

$$V_{DACVOUT} = \frac{N + 19{,}999}{65{,}536} \times V_{REF}$$

where N = two's complement ADC output.

Voltage-to-Current Transfer Function

Figures 12 and 13 show the MAX1365/MAX1367 transfer function of the output current (4-20OUT) versus the ADC input code.

The transfer function for the MAX1365/MAX1367 with the current offset enabled (EN_I is high) is:

$$IOUT \cong \frac{16mA}{1.25} \times V_{CONV\_IN} + 4mA$$

The transfer function for the MAX1365/MAX1367 with the current offset disabled (EN_I is low) is:

$$IOUT \cong \frac{16mA}{1.25} \times V_{CONV\_IN}$$

Note: The input at V_{CONV_IN} expects a source impedance of typically 6kΩ when driving V_{CONV_IN} externally.

Supplies, Layout, and Bypassing

Power up AV_{DD} and DV_{DD} before applying an analog input and external-reference voltage to the device. If this is not possible, limit the current into these inputs to 50mA. When the analog and digital supplies come from the same source, isolate the digital supply from the analog supply with a low-value resistor (10Ω) or ferrite bead. For best performance, ground the MAX1365/MAX1367 to the analog ground plane of the circuit board. Avoid running digital lines under the device as this can couple noise onto the IC. Run the analog ground plane under the MAX1365/MAX1367 to minimize coupling of digital noise. Make the power-supply lines to the MAX1365/MAX1367 as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line. Shield fast-switching signals, such as clocks, with digital ground to avoid radiating noise to other sections of the board. Avoid running clock signals near the analog inputs. Avoid crossover of digital and analog signals. Running traces that are on opposite sides of the board at right angles to each other reduces feedthrough effects. Good decoupling is important when using high-resolution ADCs. Decouple the supplies with 0.1µF ceramic capacitors to GND. Place these components as close to the device as possible to achieve the best decoupling.

Selecting Segment Current

A resistor from ISET to ground sets the current for each LED segment. See Table 6 for more detail. Use the following formula to set the segment current:

$$I_{SEG} = \left(\frac{1.20V}{R_{ISET}}\right) \times 450$$

R_{ISET} values below 25kΩ increase the I_{SEG}. However, the internal current-limit circuit limits the I_{SEG} to less than 30mA. At higher I_{SEG} values, proper operation of the device is not guaranteed. In addition, the power dissipated may exceed the package power-dissipation limit.

Choosing Supply Voltage to Minimize Power Dissipation

The MAX1365/MAX1367 drive a peak current of 25.5mA into LEDs with a 2.2V forward voltage drop when operated from a supply voltage of at least 3.0V. Therefore, the minimum voltage drop across the internal LED drivers is 0.8V (3.0V - 2.2V = 0.8V). The MAX1365/MAX1367 sink when the outputs are operating and the LED segment drivers are at full current (8 x 25.5mA = 204mA). For a 3.3V supply, the MAX1365/MAX1367 dissipate 224.4mW ((3.3V - 2.2V) x 204 = 224.4mW). If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly.

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

However, if the LEDs used have a higher forward voltage drop than 2.2V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.8V headroom. For a LEDV supply voltage of 2.7V, the maximum LED forward voltage is 1.9V to ensure 0.8V driver headroom. The voltage drop across the drivers with a nominal +5V supply (5.0V - 2.2V = 2.8V) is almost three times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.2V = 1.1V). Therefore, the driver's power dissipation increases three times. The power dissipation in the part causes the junction temperature to rise accordingly. In the high ambient temperature case, the total junction temperature may be very high (> +125°C). At higher junction temperatures, the ADC performance degrades. To ensure the dissipation limit for the MAX1365/MAX1367 is not exceeded and the ADC performance is not degraded; a diode can be inserted between the power supply and LEDV.

Selecting Depletion-Mode FET

An external depletion-mode FET (DMOS) works in conjunction with the regulator circuit to supply the V/I converter with loop power. REG_FORCE regulates the gate of the DMOS so that the drain voltage is 5.2V (typ) and allows the 4–20mA (0 to 16mA) loop to be directly powered from a 7V to 30V supply. DMOS I_{DS} consists of the current output at 4-20OUT, a 4mA offset current, and 1mA (typ) consumed by the V/I converter.

For offset-enabled mode (EN_I = 1):

$$I_{DS} = I_{4\text{-}20OUT} + 4mA + 1mA$$

where I_{DS} is the current in the DMOS.

For offset-disabled mode (EN_I = 0):

$$I_{DS} = I_{4\text{-}20OUT} + 1mA$$

where I_{DS} is the current in the DMOS.

Table 7 provides the FET characteristics for selecting an external DMOS transistor. The DN25D FET transistor from Supertex meets all the requirements of Table 7. Other suitable transistors include ND2020L and ND2410L from Siliconix.

Connect a 0.1µF capacitor between CMP and REG_FORCE to ensure stable regulator compensation.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1365/MAX1367 is measured using the end-point method.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of ±1 LSB. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Rollover Error

Rollover error is defined as the absolute-value difference between a near positive full-scale reading and near negative full-scale reading. Rollover error is tested by applying a full-scale positive voltage, swapping AIN+ and AIN-, and adding the results.

Zero-Input Reading

Ideally, with AIN+ connected to AIN-, the MAX1365/MAX1367 LED displays zero. Zero-input reading is the measured deviation from the ideal zero and the actual measured point.

Gain Error

Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point.

Common-Mode Rejection (CMR)

CMR is the ability of a device to reject a signal that is common to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels.

Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)

Normal-mode rejection is a measure of how much output changes when 50Hz and 60Hz signals are injected into only one of the differential inputs. The MAX1365/MAX1367 sigma-delta converter uses its internal digital filter to provide normal-mode rejection to both 50Hz and 60Hz power-line frequencies simultaneously.

Power-Supply Rejection (PSR)—ADC

PSR is a measure of the data converter's level of immunity to power-supply fluctuations. PSR assumes that the converter's linearity is unaffected by changes in the power-supply voltage. Power-supply rejection ratio (PSRR) is the ratio of the input signal change to the change in the converter output. PSRR is typically measured in dB.

Power-Supply Rejection—V/I Converter

PSR is a measure of the data converter's level of immunity to power-supply fluctuations. PSR assumes that the converter's linearity is unaffected by changes in the power-supply voltage.

Note: The V/I converter current output (4–20mA) power-supply rejection is with respect to the 7V to 30V loop supply.

Table 6. Segment-Current Selection

R_{SET} (kΩ)	I_{SEG} (mA)
25	21.6
50	10.8
100	5.4
500	1.1
> 2500	LED driver disabled

Table 7. FET Characteristics

FET TYPE	N-CHANNEL DEPLETION MODE
I_{DS}	30mA
BV_{DS}	(V_{EXT}* - REG_VDD) min
$V_{PINCHOFF}$	REG_VDD max
Power dissipation	30mA x (V_{EXT} - REG_VDD) min

*V_{EXT} is the 7V to 30V loop voltage.

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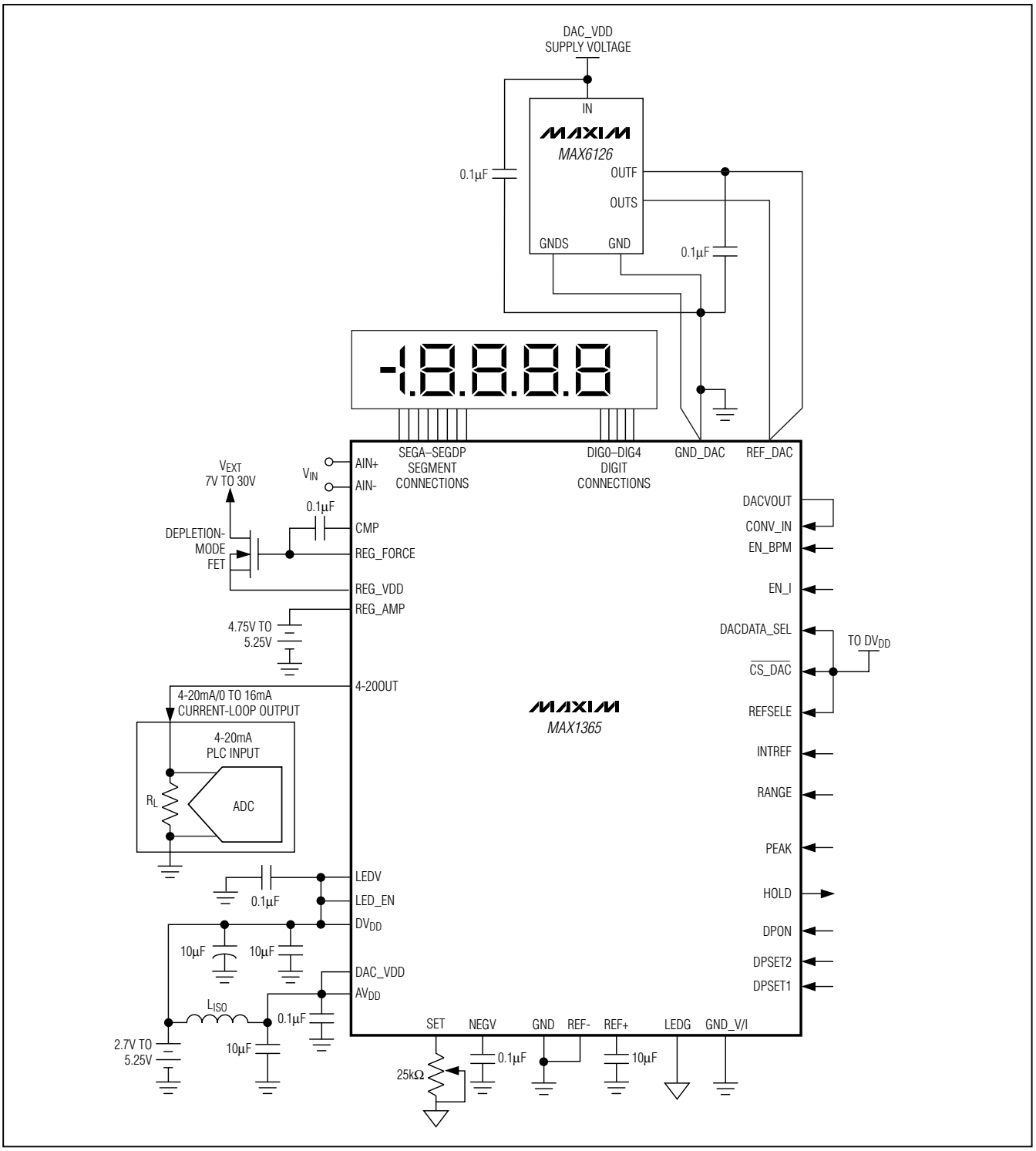
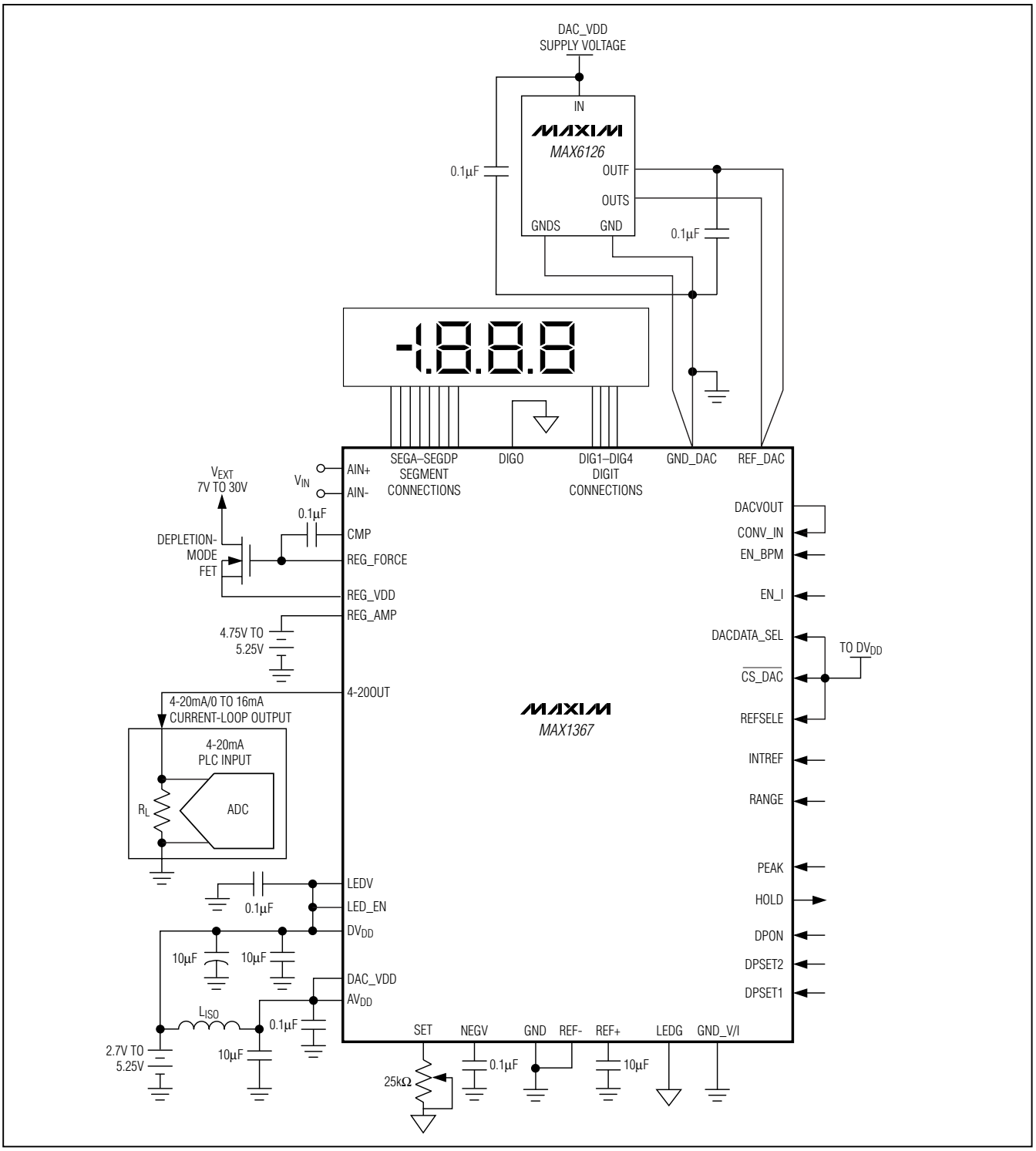
MAX1365 Typical Operating Circuit

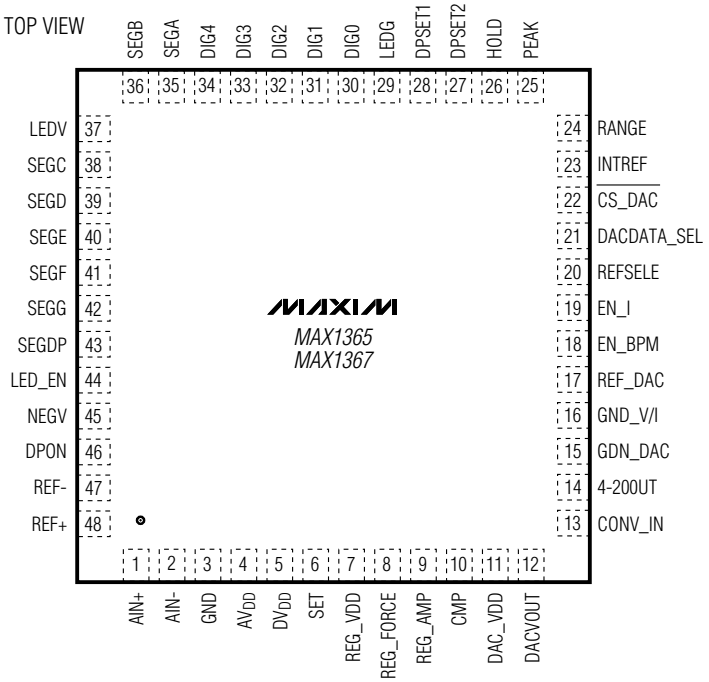


MAX1367 Typical Operating Circuit



Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Pin Configuration



TQFP

Chip Information

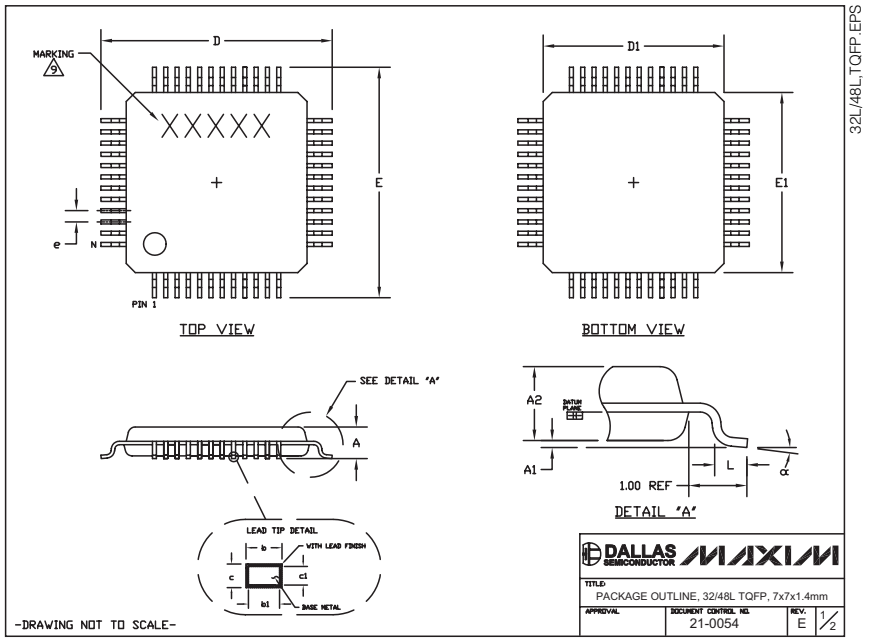
TRANSISTOR COUNT: 83,463

PROCESS: CMOS

Stand-Alone, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E_1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 32/48L TQFP, 7x7x1.4mm

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