

# Spread Spectrum Clock Generator

## MB88154A

### MB88154A-101/102/103/111/112/113

#### ■ DESCRIPTION

MB88154A is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates input frequency as Middle Centered and down spread which modulates so as not to exceed input frequency.

#### ■ FEATURE

- Input frequency : 16.6 MHz to 80 MHz
- Output frequency: 16.6 MHz to 80 MHz (One time input frequency)
- Modulation rate can select from  $\pm 0.5%$ ,  $\pm 1.0%$ ,  $\pm 1.5%$  or  $- 1.0%$ ,  $- 2.0%$ ,  $- 3.0%$ . (For center spread / down spread.)
- Equipped with crystal oscillation circuit: Range of oscillation 16.6 MHz to 48 MHz
- The external clock can be input: 16.6 MHz to 80 MHz
- Modulation clock output duty : 40% to 60%
- Modulation clock cycle-cycle jitter : Less than 100 ps
- Low current consumption by CMOS process : 5.0 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V  $\pm$  0.3 V
- Operating temperature :  $- 40$  °C to  $+85$  °C
- Package : SOP 8-pin

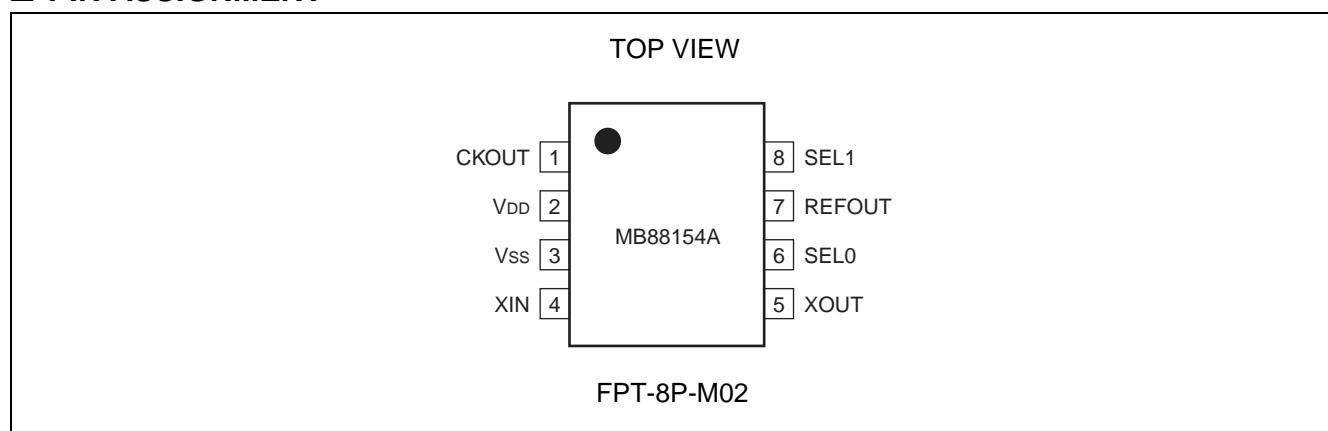
# MB88154A

## ■ PRODUCT LINEUP

MB88154A has two kinds of input frequency, and three kinds of modulation type (center/down spread), total six line-ups.

| Product      | Input/Output frequency | Modulation type |
|--------------|------------------------|-----------------|
| MB88154A-101 | 50 MHz to 80 MHz       | Down spread     |
| MB88154A-102 | 33 MHz to 67 MHz       |                 |
| MB88154A-103 | 16.6 MHz to 40 MHz     |                 |
| MB88154A-111 | 50 MHz to 80 MHz       | Center spread   |
| MB88154A-112 | 33 MHz to 67 MHz       |                 |
| MB88154A-113 | 16.6 MHz to 40 MHz     |                 |

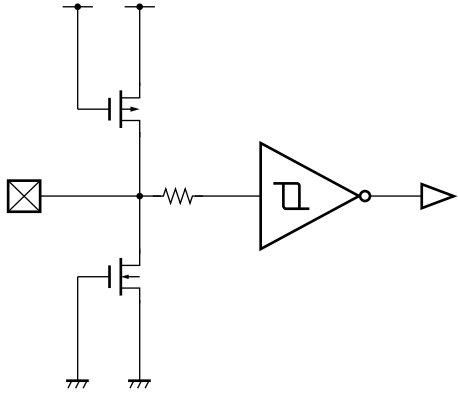
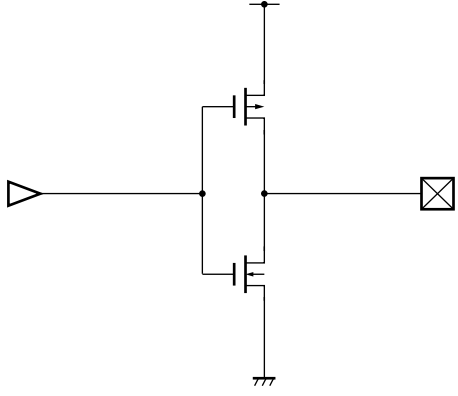
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

| Pin name        | I/O | Pin no. | Description                                      |
|-----------------|-----|---------|--|
| CKOUT           | O   | 1       | Modulated clock output pin                       |
| V <sub>DD</sub> | —   | 2       | Power supply voltage pin                         |
| V <sub>SS</sub> | —   | 3       | GND pin  |
| XIN             | I   | 4       | Crystal resonator connection pin/clock input pin |
| XOUT            | O   | 5       | Crystal resonator connection pin                 |
| SEL0            | I   | 6       | Modulation rate setting pin                      |
| REFOUT          | O   | 7       | Non-modulated clock output pin                   |
| SEL1            | I   | 8       | Modulation rate setting pin                      |

## ■ I/O CIRCUIT TYPE

| Pin             | Circuit type   | Remarks   |
|-----------------|--|---|
| SEL0<br>SEL1    |   | CMOS hysteresis input   |
| CKOUT<br>REFOUT |  | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• <math>I_{OL} = 3 \text{ mA}</math></li> </ul> |

Note : For XIN and XOUT pins, refer to “■ OSCILLATION CIRCUIT”

## ■ HANDLING DEVICES

### Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than  $V_{DD}$  or a voltage lower than  $V_{SS}$  is applied to an input or output pin or (b) a voltage higher than the rating is applied between  $V_{DD}$  pin and  $V_{SS}$  pin. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

### Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

### The attention when the external clock is used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.

Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

### Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

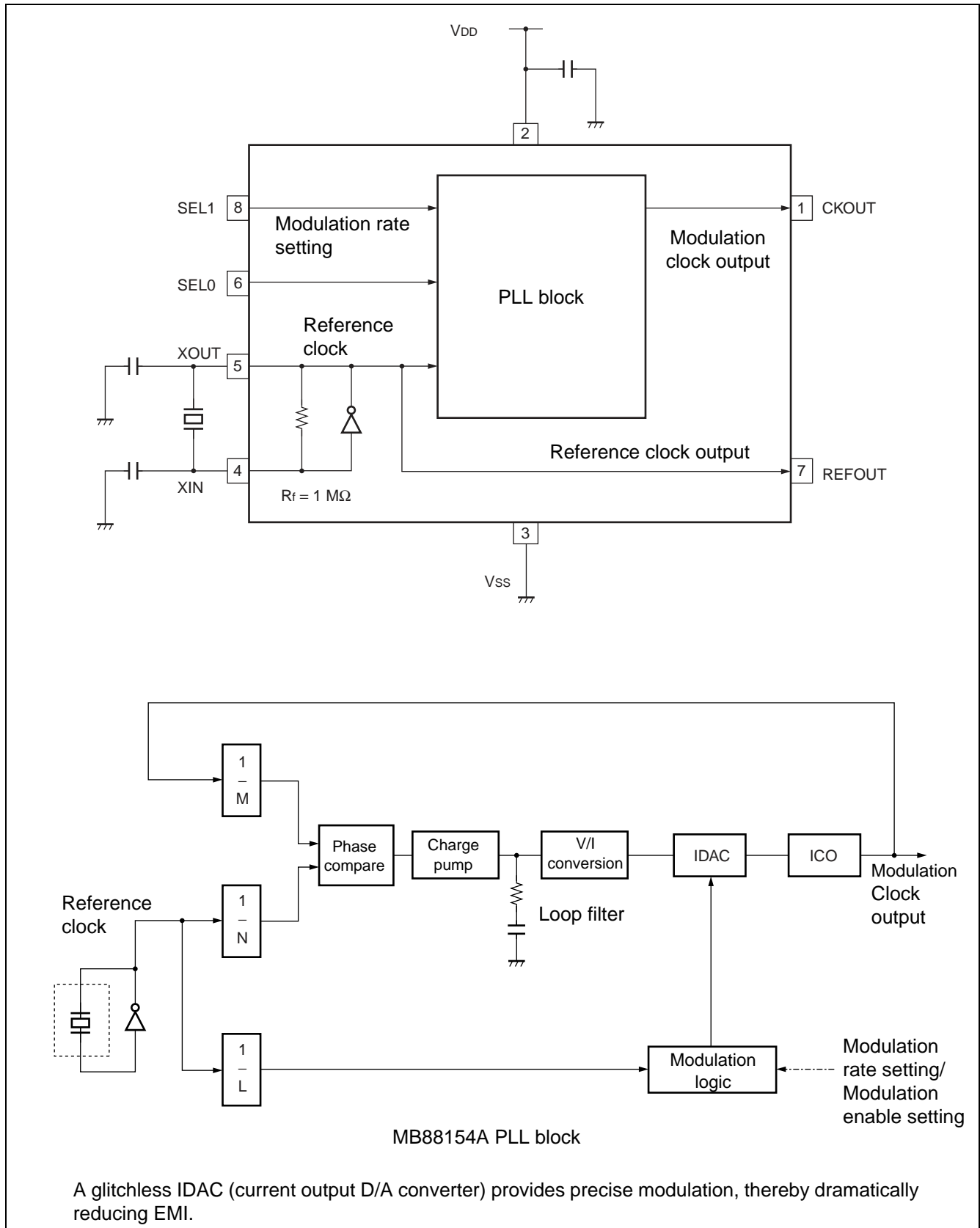
We recommend connecting electrolytic capacitor (about 10  $\mu\text{F}$ ) and the ceramic capacitor (about 0.01  $\mu\text{F}$ ) in parallel between  $V_{SS}$  pin and  $V_{DD}$  pin near the device, as a bypass capacitor.

### Oscillation circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

## ■ BLOCK DIAGRAM



## ■ PIN SETTING

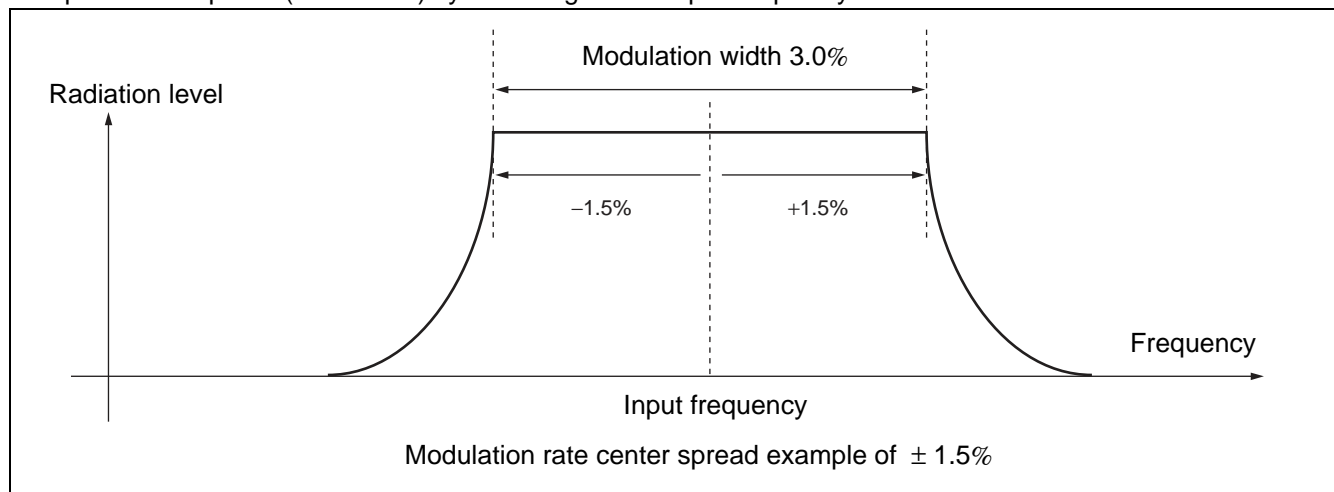
### SEL 0, SEL 1 Modulation rate setting

| SEL1 | SEL0 | Modulation rate                          |  |
|------|------|--|--|
|      |      | MB88154A-101, MB88154A-102, MB88154A-103 | MB88154A-111, MB88154A-112, MB88154A-113 |
|      |      | Down spread                              | Center spread                            |
| L    | L    | - 1.0%                                   | ± 0.5%                                   |
| L    | H    | - 2.0%                                   | ± 1.0%                                   |
| H    | L    | - 3.0%                                   | ± 1.5%                                   |
| H    | H    | No spread                                | No spread                                |

- Notes :
- The modulation rate can be changed at the level of the pin. Spectrum does not spread when “H” level is set to SEL0 and SEL1 pins. The clock with low jitter can be obtained.
  - When changing the modulation rate setting, the stabilization wait time for the modulation clock is required. The stabilization wait time for the modulation clock take the maximum value of “■ ELECTRICAL CHARACTERISTICS • AC Characteristics Lock-Up time”.

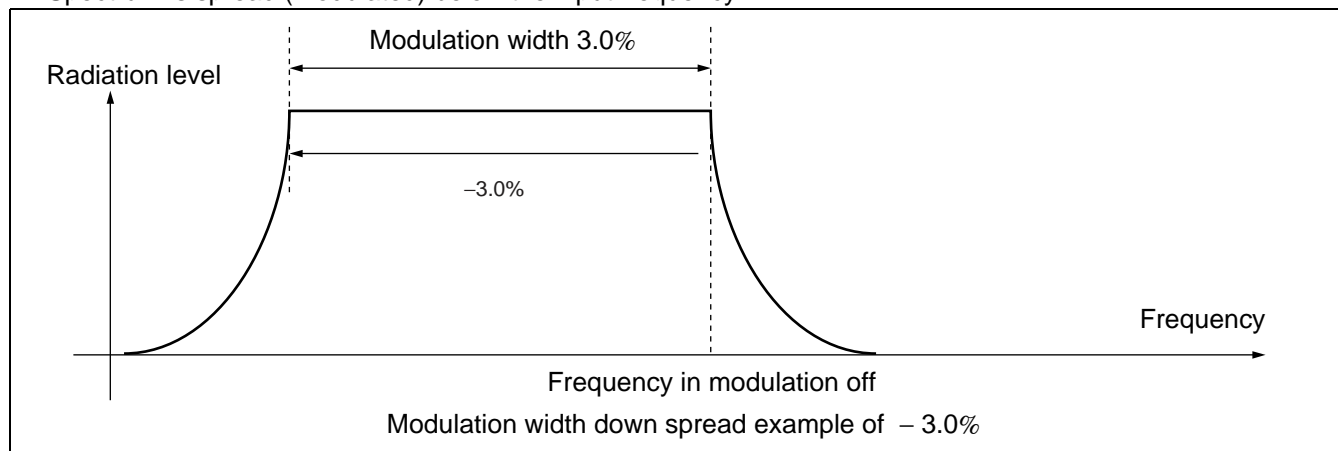
#### • Center spread

Spectrum is spread (modulated) by centering on the input frequency.



#### • Down spread

Spectrum is spread (modulated) below the input frequency.

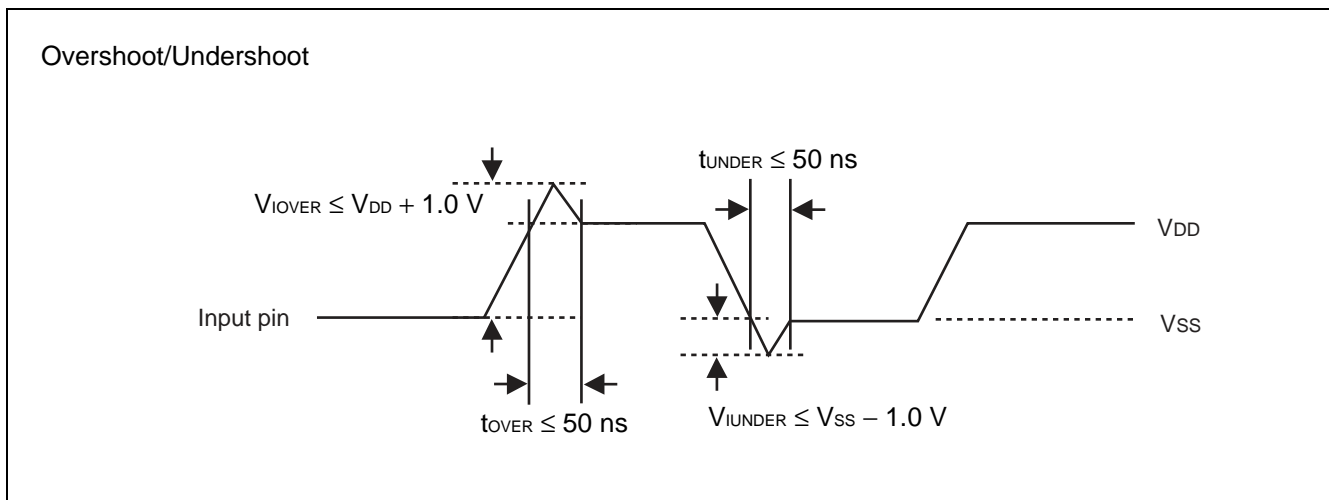


## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter                      | Symbol       | Rating                                   |   | Unit |
|--------------------------------|--------------|--|---|------|
|                                |              | Min                                      | Max                                     |      |
| Power supply voltage*          | $V_{DD}$     | - 0.5                                    | + 4.0                                   | V    |
| Input voltage*                 | $V_I$        | $V_{SS} - 0.5$                           | $V_{DD} + 0.5$                          | V    |
| Output voltage*                | $V_O$        | $V_{SS} - 0.5$                           | $V_{DD} + 0.5$                          | V    |
| Storage temperature            | $T_{ST}$     | - 55                                     | + 125                                   | °C   |
| Operation junction temperature | $T_J$        | - 40                                     | + 125                                   | °C   |
| Output current                 | $I_o$        | - 14                                     | + 14                                    | mA   |
| Overshoot                      | $V_{IOVER}$  | —  | $V_{DD} + 1.0$ ( $t_{OVER} \leq 50$ ns) | V    |
| Undershoot                     | $V_{IUNDER}$ | $V_{SS} - 1.0$ ( $t_{UNDER} \leq 50$ ns) | —                                       | V    |

\* : The parameter is based on  $V_{SS} = 0.0$  V.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



## RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0.0 V)

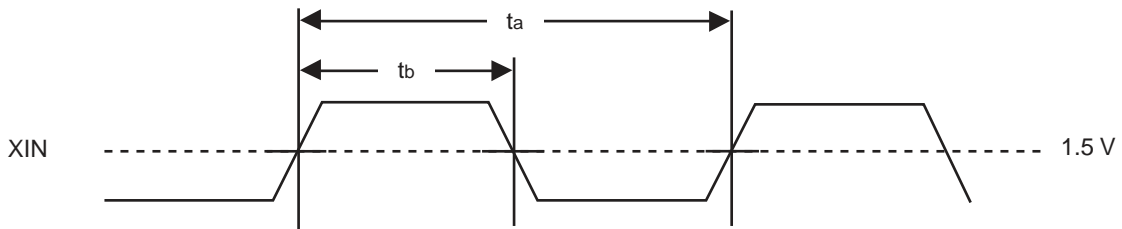
| Parameter                | Symbol           | Pin                   | Conditions                          | Value                              |     |                        | Unit |
|--------------------------|------------------|-----------------------|-------------------------------------|------------------------------------|-----|------------------------|------|
|                          |                  |                       |                                     | Min                                | Typ | Max                    |      |
| Power supply voltage     | V <sub>DD</sub>  | V <sub>DD</sub>       | —                                   | 3.0                                | 3.3 | 3.6                    | V    |
| “H” level input voltage  | V <sub>IH</sub>  | XIN,<br>SEL0,<br>SEL1 | —                                   | V <sub>DD</sub> × 0.80             | —   | V <sub>DD</sub> + 0.3  | V    |
| “L” level input voltage  | V <sub>IL</sub>  |                       | —                                   | V <sub>SS</sub>                    | —   | V <sub>DD</sub> × 0.20 | V    |
| Input clock duty cycle   | t <sub>DCI</sub> | XIN                   | 16.6 MHz to 80 MHz                  | 40                                 | 50  | 60                     | %    |
| Input clock through rate | SR <sub>IN</sub> | XIN                   | Input frequency<br>40 MHz to 80 MHz | 0.0475 ×<br>f <sub>in</sub> – 1.75 | —   | —                      | V/ns |
| Operating temperature    | T <sub>a</sub>   | —                     | —                                   | – 40                               | —   | + 85                   | °C   |

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

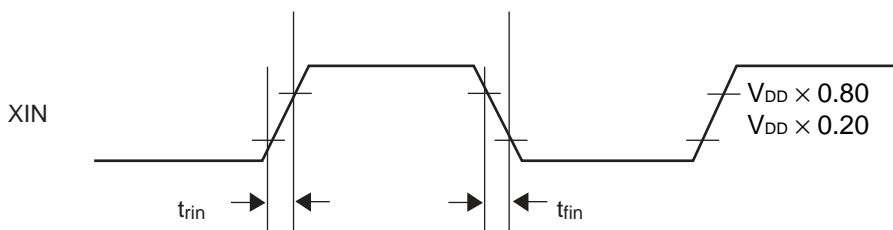
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle (t<sub>DCI</sub> = t<sub>b</sub>/t<sub>a</sub>)



Input clock through rate (SR<sub>IN</sub>)



Note : SR<sub>IN</sub> = (V<sub>DD</sub> × 0.80 – V<sub>DD</sub> × 0.20) / t<sub>rin</sub>, SR<sub>IN</sub> = (V<sub>DD</sub> × 0.80 – V<sub>DD</sub> × 0.20) / t<sub>fin</sub>



## ■ ELECTRICAL CHARACTERISTICS

- DC Characteristics

( $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

| Parameter            | Symbol   | Pin             | Conditions   | Value          |     |          | Unit     |
|----------------------|----------|-----------------|--|----------------|-----|----------|----------|
|                      |          |                 |  | Min            | Typ | Max      |          |
| Power supply current | $I_{CC}$ | $V_{DD}$        | no load capacitance at 24 MHz output   | —              | 5.0 | 7.0      | mA       |
| Output voltage       | $V_{OH}$ | CKOUT, REFOUT   | “H” level output<br>$I_{OH} = -3\text{ mA}$  | $V_{DD} - 0.5$ | —   | $V_{DD}$ | V        |
|                      | $V_{OL}$ |                 | “L” level output<br>$I_{OL} = 3\text{ mA}$   | $V_{SS}$       | —   | 0.4      | V        |
| Output impedance     | $Z_o$    | CKOUT, REFOUT   | 16.6 MHz to 80 MHz   | —              | 70  | —        | $\Omega$ |
| Input capacitance    | $C_{IN}$ | XIN, SEL0, SEL1 | $T_a = +25\text{ }^\circ\text{C}$ ,<br>$V_{DD} = V_i = 0.0\text{ V}$ ,<br>$f = 1\text{ MHz}$ | —              | —   | 16       | pF       |

# MB88154A

- AC Characteristics

( $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

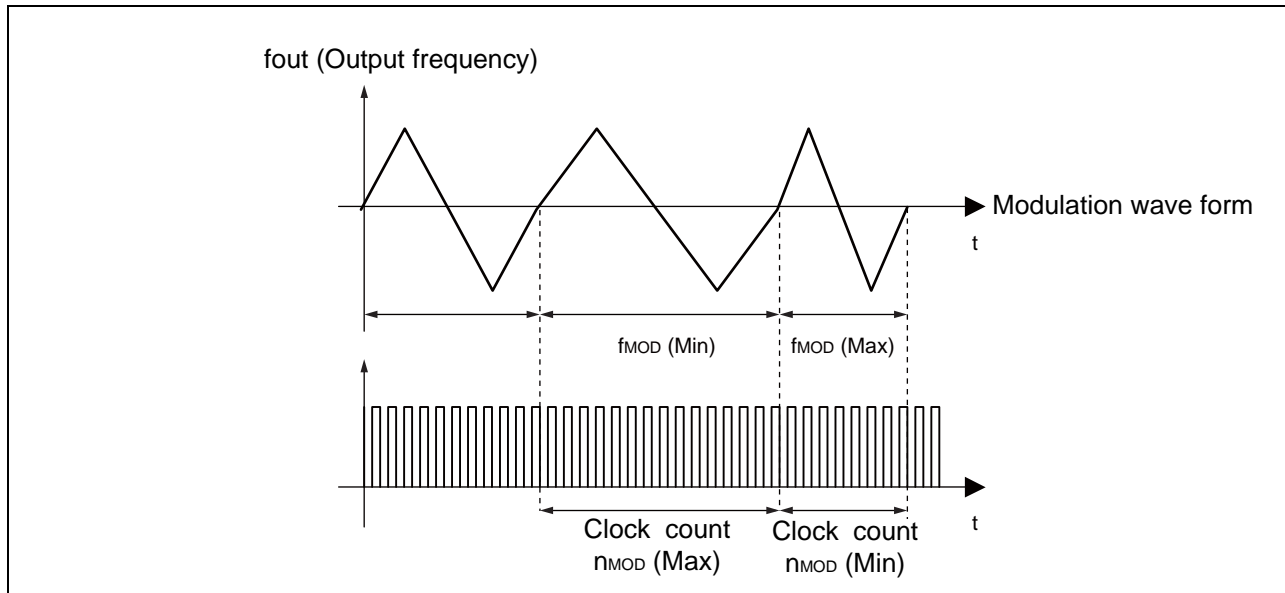
| Parameter  | Symbol                     | Pin              | Conditions   | Value                   |                         |                         | Unit          |
|--|----------------------------|------------------|--|-------------------------|-------------------------|-------------------------|---------------|
|  |                            |                  |  | Min                     | Typ                     | Max                     |               |
| Oscillation frequency  | $f_x$                      | XIN,<br>XOUT     | Fundamental oscillation  | 16.6                    | —                       | 40                      | MHz           |
|  |                            |                  | 3rd over-tone oscillation  | 40                      | —                       | 48                      |               |
| Input frequency  | $f_{in}$                   | XIN              | MB88154A-103/113   | 16.6                    | —                       | 40                      | MHz           |
|  |                            |                  | MB88154A-102/112   | 33                      | —                       | 67                      |               |
|  |                            |                  | MB88154A-101/111   | 50                      | —                       | 80                      |               |
| Output frequency   | $f_{OUT}$                  | CKOUT,<br>REFOUT | MB88154A-103/113   | 16.6                    | —                       | 40                      | MHz           |
|  |                            |                  | MB88154A-102/112   | 33                      | —                       | 67                      |               |
|  |                            |                  | MB88154A-101/111   | 50                      | —                       | 80                      |               |
| Output slew rate   | SR                         | CKOUT,<br>REFOUT | 0.4 V to 2.4 V<br>load capacitance 15 pF   | 0.3                     | —                       | 2.0                     | V/ns          |
| Output clock duty cycle  | $t_{DCC}$                  | CKOUT            | 1.5 V  | 40                      | —                       | 60                      | %             |
|  | $t_{DCR}$                  | REFOUT           | 1.5 V  | $t_{DCI} - 10^*$        | —                       | $t_{DCI} + 10^*$        | %             |
| Modulation frequency<br>(Number of input clocks<br>per modulation) | $f_{MOD}$<br>( $n_{MOD}$ ) | CKOUT            | MB88154A-103/113   | $f_{in}/2640$<br>(2640) | $f_{in}/2280$<br>(2280) | $f_{in}/1920$<br>(1920) | kHz<br>(clks) |
|  |                            |                  | MB88154A-102/112   | $f_{in}/4400$<br>(4400) | $f_{in}/3800$<br>(3800) | $f_{in}/3200$<br>(3200) |               |
|  |                            |                  | MB88154A-101/111   | $f_{in}/5280$<br>(5280) | $f_{in}/4560$<br>(4560) | $f_{in}/3840$<br>(3840) |               |
| Lock-Up time   | $t_{LK}$                   | CKOUT            | —  | —                       | 2                       | 5                       | ms            |
| Cycle-cycle jitter   | $t_{JC}$                   | CKOUT            | No load capacitance,<br>$T_a = +25\text{ }^\circ\text{C}$ ,<br>$V_{DD} = 3.3\text{ V}$ | —                       | —                       | 100                     | ps-rms        |

\* : Duty of the REFOUT output is guaranteed only for the following A and B because it depends on  $t_{DCI}$  of input clock duty.

A. Resonator : When resonator is connected with XIN and XOUT and oscillates normally.

B. External clock input : The input level is Full - swing ( $V_{SS} - V_{DD}$ ).

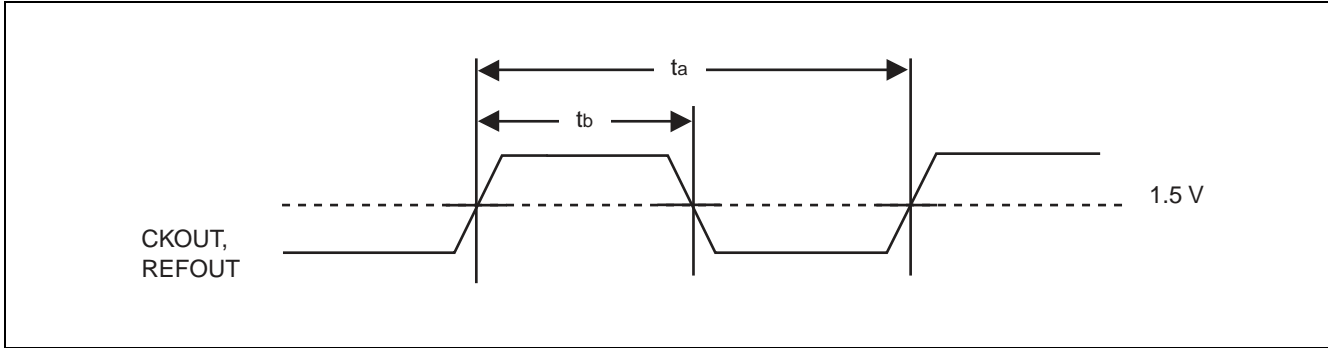
## <Definition of modulation frequency and number of input clocks per modulation>



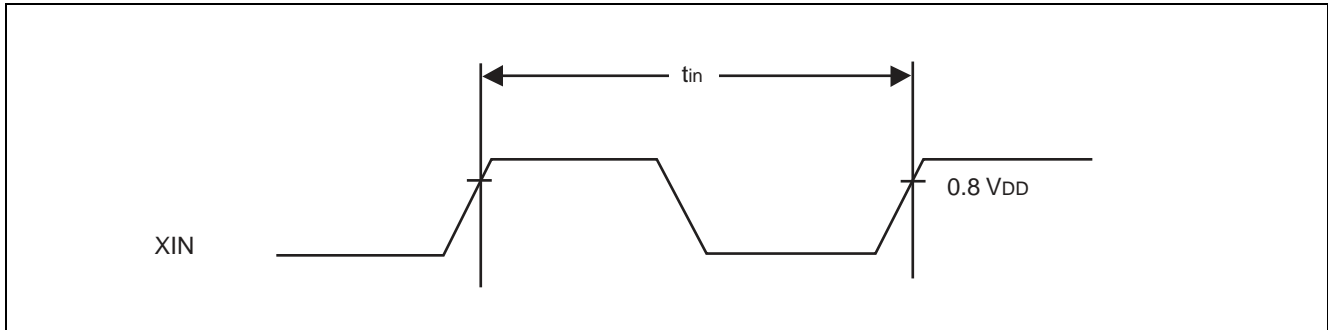
MB88154A contains the modulation period to realize the efficient EMI reduction.

The modulation period  $f_{MOD}$  depends on the input frequency and changes between  $f_{MOD} (Min)$  and  $f_{MOD} (Max)$ . Furthermore, the average value of  $f_{MOD}$  equals the typical value of the electrical characteristics.

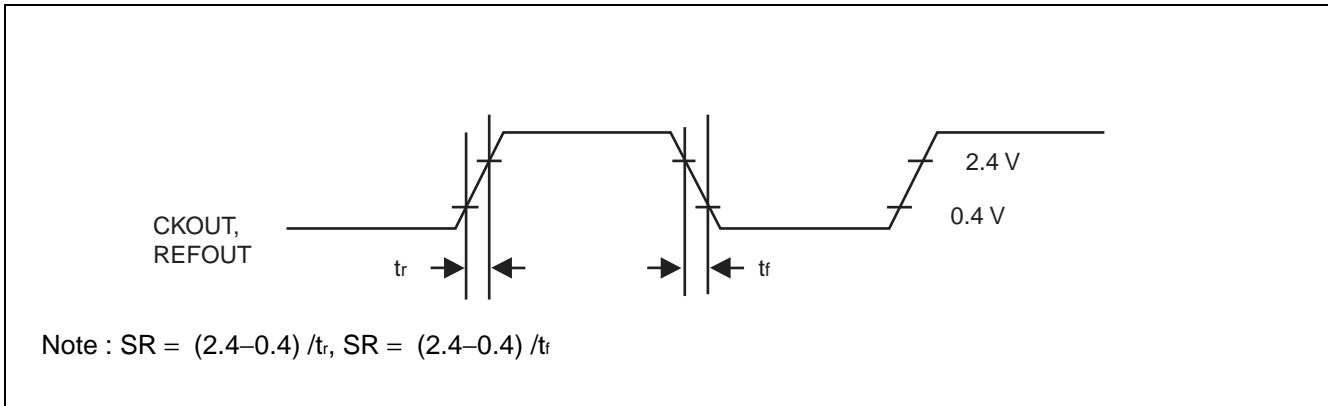
## ■ OUTPUT CLOCK DUTY CYCLE ( $t_{DCC}$ , $t_{DCR} = t_b/t_a$ )



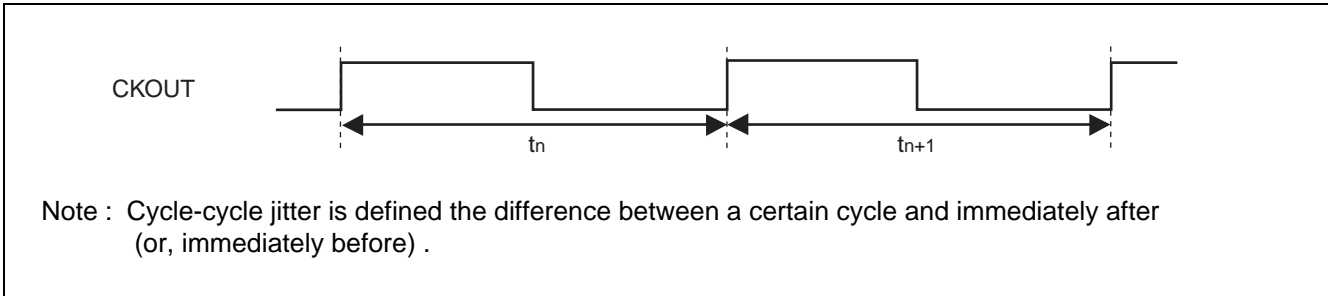
## ■ INPUT FREQUENCY ( $f_{in} = 1/t_{in}$ )



## ■ OUTPUT SLEW RATE (SR)

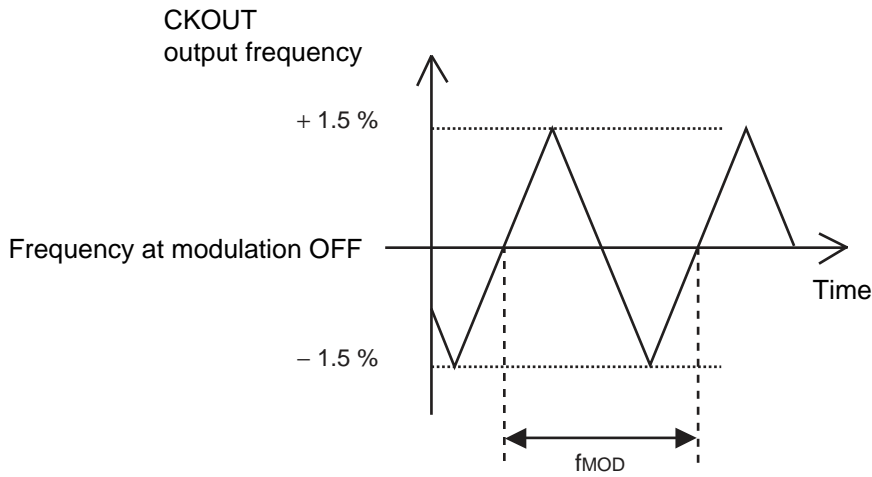


## ■ CYCLE-CYCLE JITTER ( $t_{JC} = | t_n - t_{n+1} |$ )

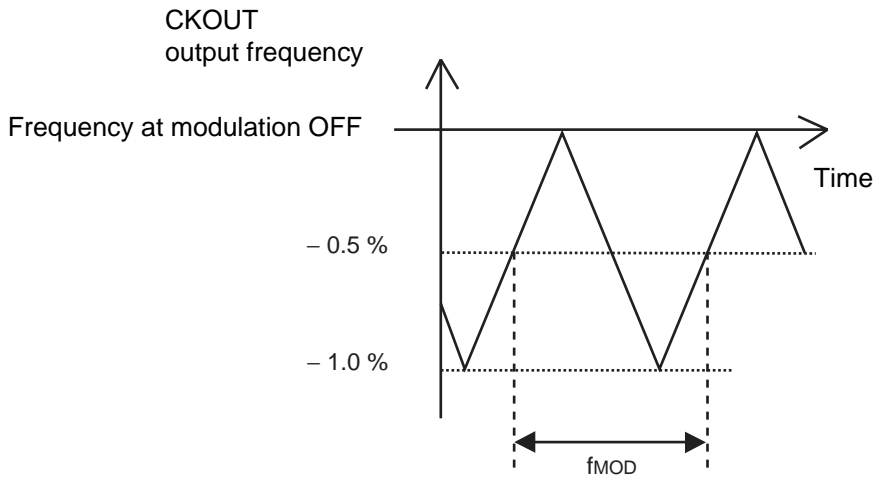


## MODULATION WAVEFORM

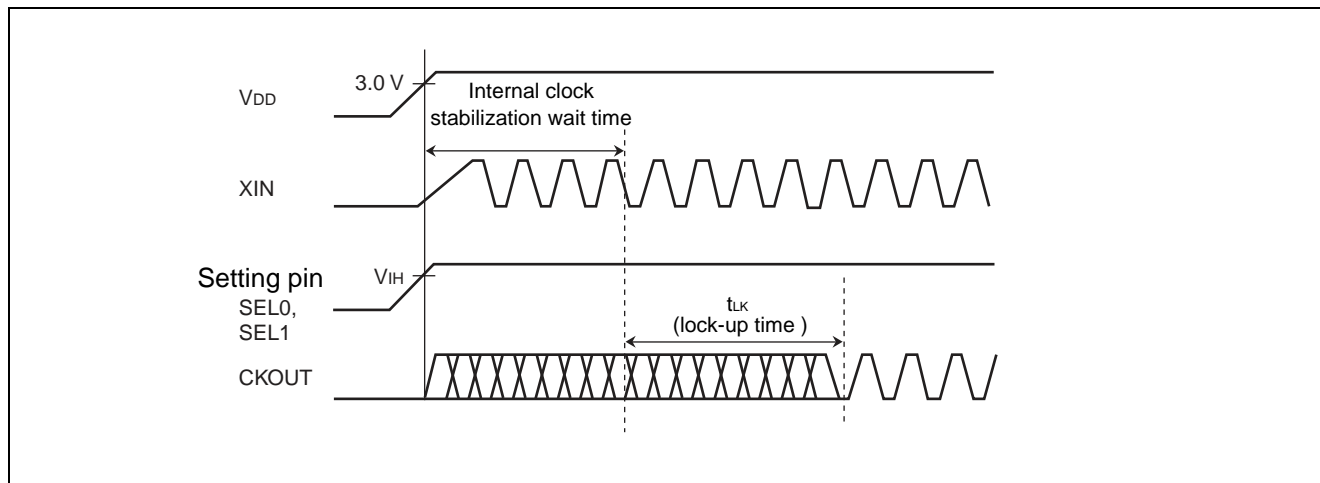
- $\pm 1.5\%$  modulation rate, Example of center spread



- $-1.0\%$  modulation rate, Example of down spread



## ■ LOCK-UP TIME



If the setting pin is fixed at the "H" or "L" level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) + (the lock-up time " $t_{LK}$ "). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.

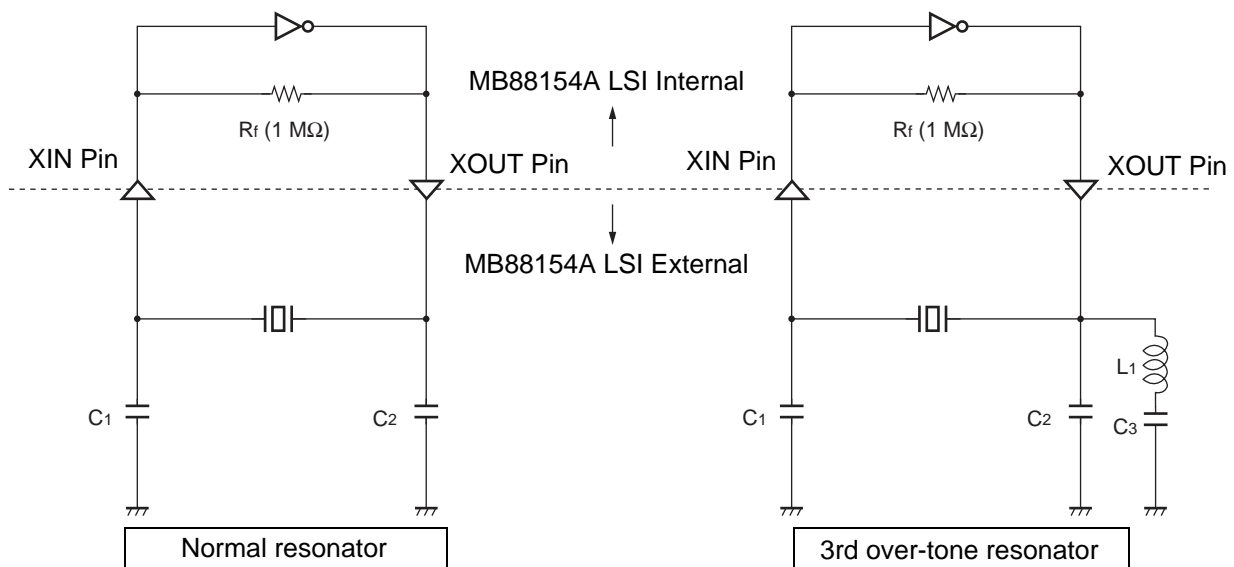
Note : When the pin setting is changed, the CKOUT pin output clock stabilization time is required. Until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.

## ■ OSCILLATION CIRCUIT

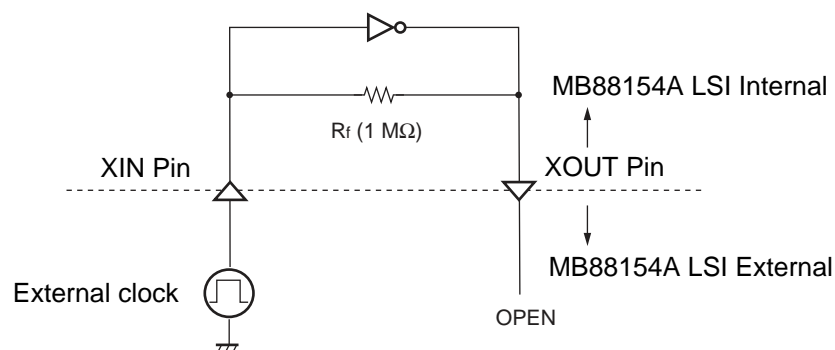
The left side of figures below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistance ( $R_f$ ). The value of capacity ( $C_1$  and  $C_2$ ) is required adjusting to the most suitable value of an individual resonator.

The right side of figures below shows the example of connecting for the 3rd over-tone resonator. The value of capacity ( $C_1$ ,  $C_2$  and  $C_3$ ) and inductance ( $L_1$ ) is needed adjusting to the most suitable value of an individual resonator. The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which use for the most suitable value. When an external clock is used (the resonator is not used), input the clock to XIN pin and do not connect anything with XOUT.

- When using a resonator

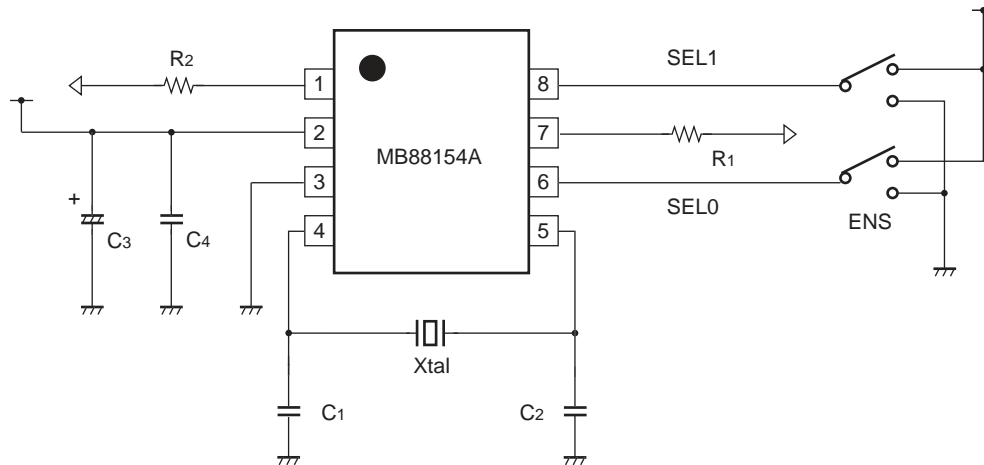


- When using an external clock



Note : Note that a jitter characteristic of an input clock may cause an affect a cycle-cycle jitter characteristic.

## ■ INTERCONNECTION CIRCUIT EXAMPLE



- C<sub>1</sub>, C<sub>2</sub> : Oscillation stabilization capacitance (refer to “■ OSCILLATION CIRCUIT”).
- C<sub>3</sub> : Capacitor of 10  $\mu$ F or higher
- C<sub>4</sub> : Capacitor about 0.01  $\mu$ F (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device.)
- R<sub>1</sub>, R<sub>2</sub> : Impedance matching resistor for board pattern

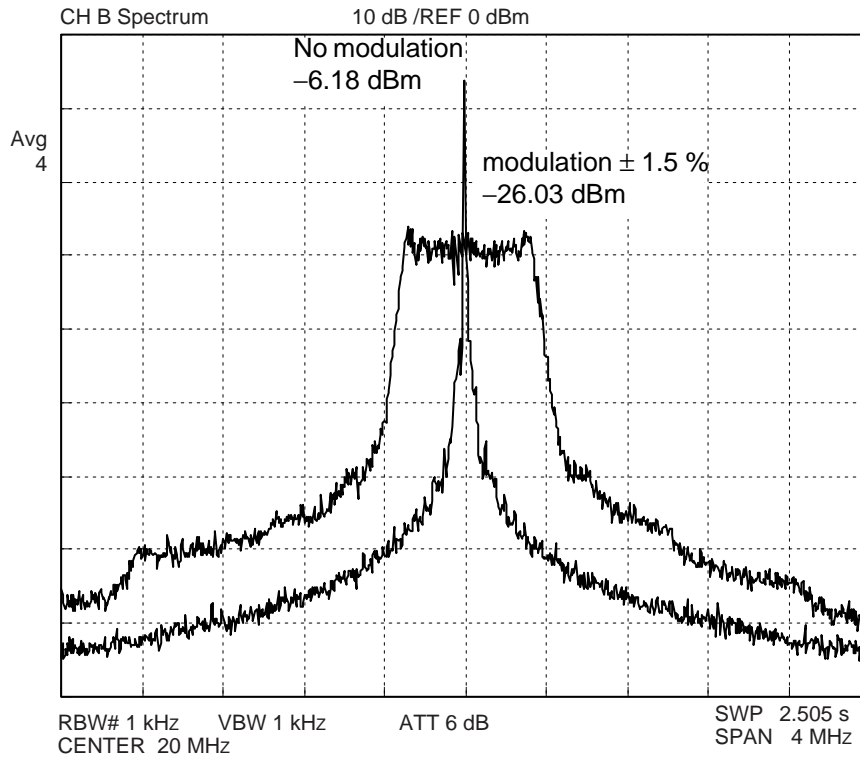


## ■ EXAMPLE CHARACTERISTICS

The condition of the examples of the characteristic is shown as follows: Input frequency = 20 MHz (Output frequency = 20 MHz : Using MB88154A-113), Power - supply voltage = 3.3 V, None load capacity.

Modulation rate =  $\pm 1.5\%$  (center spread)

Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for -6dB).

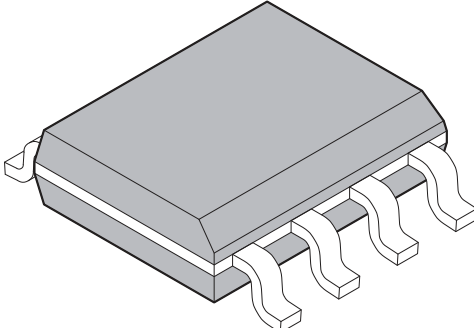


# MB88154A

## ■ ORDERING INFORMATION

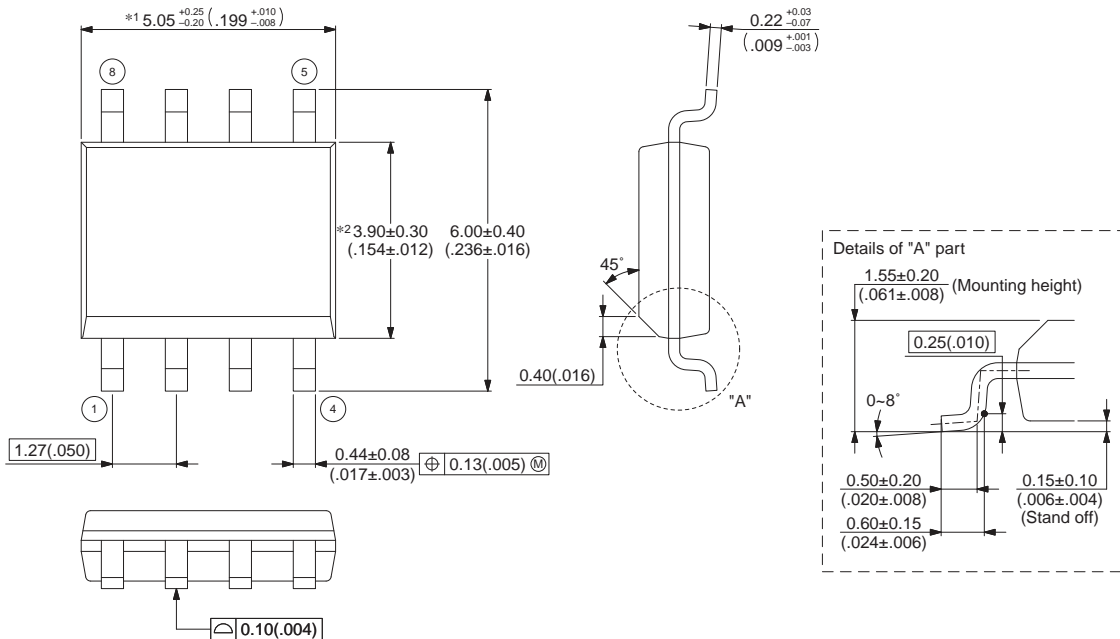
| Part number  | Input/Output frequency   | Modulation type                                    | Package                           | Remarks                    |
|--|--|--|-----------------------------------|----------------------------|
| MB88154APNF-G-101-JNE1<br>MB88154APNF-G-102-JNE1<br>MB88154APNF-G-103-JNE1<br>MB88154APNF-G-111-JNE1<br>MB88154APNF-G-112-JNE1<br>MB88154APNF-G-113-JNE1             | 50 MHz to 80 MHz<br>33 MHz to 67 MHz<br>16.6 MHz to 40 MHz<br>50 MHz to 80 MHz<br>33 MHz to 67 MHz<br>16.6 MHz to 40 MHz | Down<br>Down<br>Down<br>Center<br>Center<br>Center | 8-pin plastic SOP<br>(FPT-8P-M02) |                            |
| MB88154APNF-G-101-JNEFE1<br>MB88154APNF-G-102-JNEFE1<br>MB88154APNF-G-103-JNEFE1<br>MB88154APNF-G-111-JNEFE1<br>MB88154APNF-G-112-JNEFE1<br>MB88154APNF-G-113-JNEFE1 | 50 MHz to 80 MHz<br>33 MHz to 67 MHz<br>16.6 MHz to 40 MHz<br>50 MHz to 80 MHz<br>33 MHz to 67 MHz<br>16.6 MHz to 40 MHz | Down<br>Down<br>Down<br>Center<br>Center<br>Center | 8-pin plastic SOP<br>(FPT-8P-M02) | Emboss taping<br>(EF type) |
| MB88154APNF-G-101-JNERE1<br>MB88154APNF-G-102-JNERE1<br>MB88154APNF-G-103-JNERE1<br>MB88154APNF-G-111-JNERE1<br>MB88154APNF-G-112-JNERE1<br>MB88154APNF-G-113-JNERE1 | 50 MHz to 80 MHz<br>33 MHz to 67 MHz<br>16.6 MHz to 40 MHz<br>50 MHz to 80 MHz<br>33 MHz to 67 MHz<br>16.6 MHz to 40 MHz | Down<br>Down<br>Down<br>Center<br>Center<br>Center | 8-pin plastic SOP<br>(FPT-8P-M02) | Emboss taping<br>(ER type) |

## ■ PACKAGE DIMENSION

|  |                                |               |
|--|--------------------------------|---------------|
| <p style="text-align: center;">8-pin plastic SOP</p>  <p style="text-align: center;">(FPT-8P-M02)</p> | Lead pitch                     | 1.27 mm       |
|  | Package width × package length | 3.9 × 5.05 mm |
|  | Lead shape                     | Gullwing      |
|  | Sealing method                 | Plastic mold  |
|  | Mounting height                | 1.75 mm MAX   |
|  | Weight                         | 0.06 g        |
|  |                                |               |

8-pin plastic SOP  
(FPT-8P-M02)

Note 1) \*1 : These dimensions include resin protrusion.  
 Note 2) \*2 : These dimensions do not include resin protrusion.  
 Note 3) Pins width and pins thickness include plating thickness.  
 Note 4) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).  
 Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.  
<http://edevice.fujitsu.com/package/en-search/>

## FUJITSU MICROELECTRONICS LIMITED

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