1 FEATURES

MERUS™ multilevel switching technology

- 5-level voltage modulation for ultra-low idle power consumption: 52 mW @ 18 PVDD (LPC mode) without the need of complex dynamic rail-tracking systems
- Inductor-less application for reduced system cost without output power limitations
- Reduced EMI emissions compared to traditional 2 and 3 level class D audio amplifiers for fast time to market without compromises in audio performance or efficiency
- High efficiency at low output power: 79 %, 2×1 W, 8 Ω for extended battery life and easy thermal management in multichannel products even in idle state

Flexible configuration and application

- BTL rated output: 2×37 W, 18 V, 4 Ω, 10% THD
- PBTL rated output: 1×74 W, 18 V, 2 Ω, 10% THD
- PVDD voltage range: 10 V to 20 V
- High efficiency at low output power: 79 %, 2×1 W, 8 Ω
- Selectable power mode profiles: Low Power Consumption (LPC) or High Audio Performance (HAP)
- Short circuit protection: 6 A peak (BTL) / 12 A peak (PBTL)
- External closed-loop feedback for improved THD
- Integrated DSP with limiters and volume control
- Easy configuration over I2C-bus with up to 64 device addresses
- 8-bit auxiliary ADC for internal temp. / PVDD monitoring or sampling from external sources
- Configurable switching edge steepness and inter-chip PWM sync for multi-device systems.
- No external heatsink required

Audio performance

- Output noise: 52 µVrms (A-weighted, HAP mode)
- Dynamic range: 106 dB (A-weighted, HAP mode)
- THD+N: 0.05%, 5 W, 1 kHz

Audio I/O

- 3-wire digital audio interface (no MCLK required)
- 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz sample rates
- I2S and TDM formats supported
- Low input-to-output latency for echo cancellation
- Post-DSP I2S output for chaining / echo cancellation

2 TARGET APPLICATIONS

- Battery powered speakers
- Bluetooth/wireless/smart speakers and soundbars
- Conference speakers
- Multichannel/multi-room audio systems

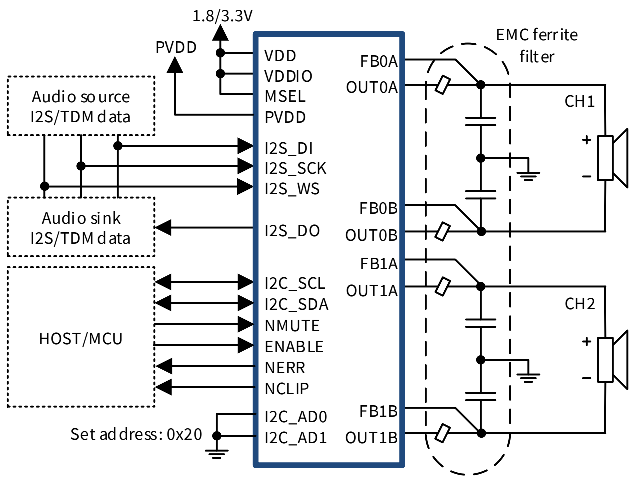
3 DESCRIPTION

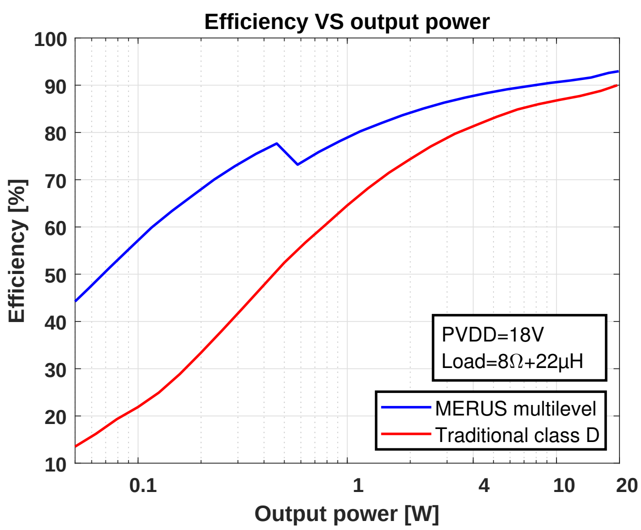
The MA2304PNS is a 2×37 W audio amplifier with I2S/TDM audio interface. It features the MERUS™ multilevel switching amplifier technology enabling unmatched power efficiency at both low and high output power. Multilevel switching also relaxes EMI and enables inductor-less applications with lower cost and no compromise in audio performance or efficiency. A high order internal feedback loop ensures low THD for excellent audio performance. The ultra-low idle power consumption is at least five times lower than the traditional class D audio amplifiers in the market, making MA2304PNS ideal for battery powered speaker applications with extended battery life and/or reduced battery cell cost. In mains-powered multichannel applications, the reduced and scalable EMI performance, enables otherwise impossible industrial designs, without the necessity for a heatsink or a traditional LC filter.

4 PRODUCT VALIDATION

Qualification standard: Standard

5 TYPICAL APPLICATION





6 Functional Application Block Diagram

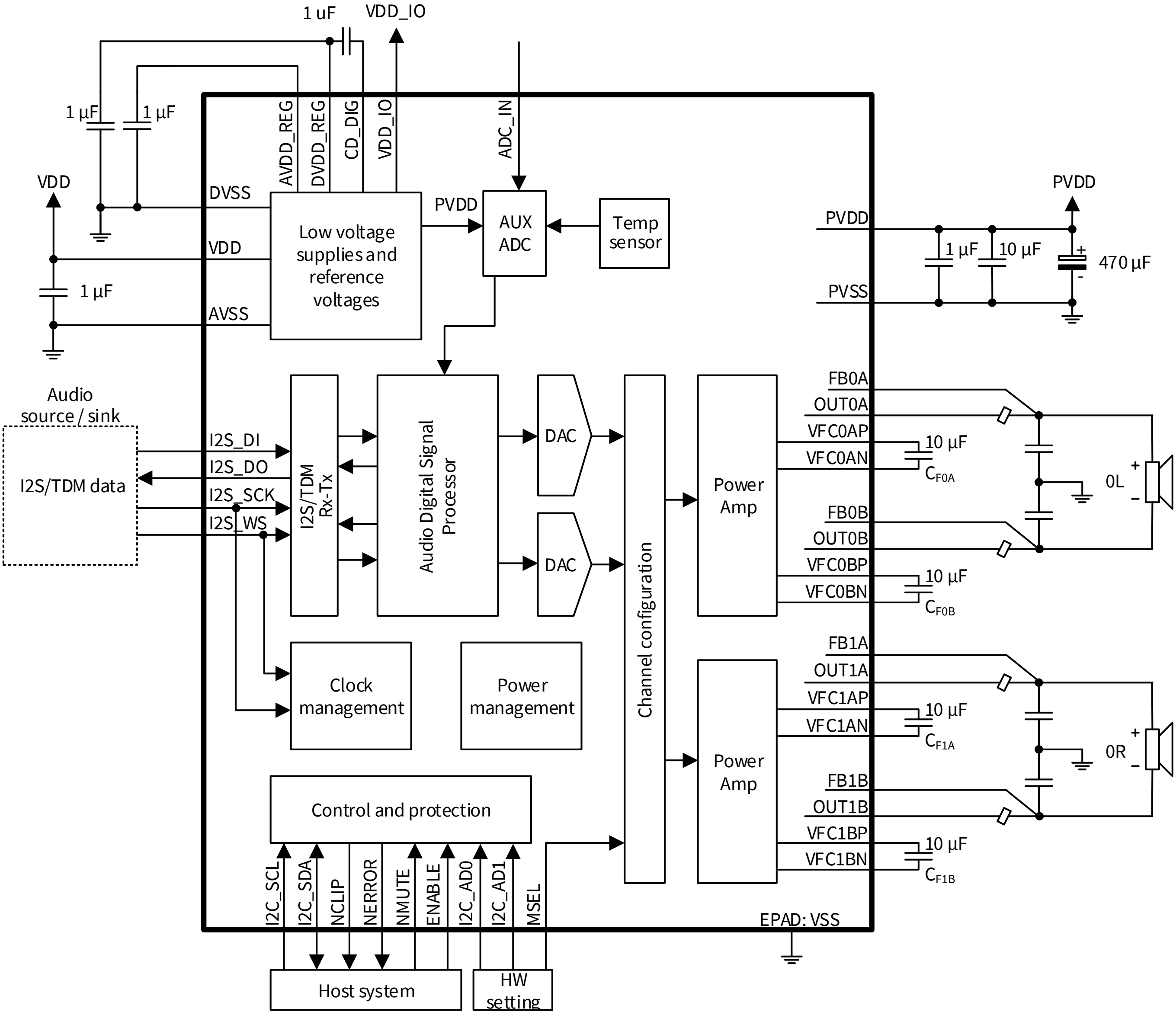


Figure 6.1: Functional Application Block Diagram

Contents

7 Device Comparison Table

Table 1: Device comparison

Device name	Functional variance
MA2304DNS	Fully configurable DSP, 10-20 V
MA2304PNS	Audio limiter and volume control only, 10-20 V

8 Pin Configuration

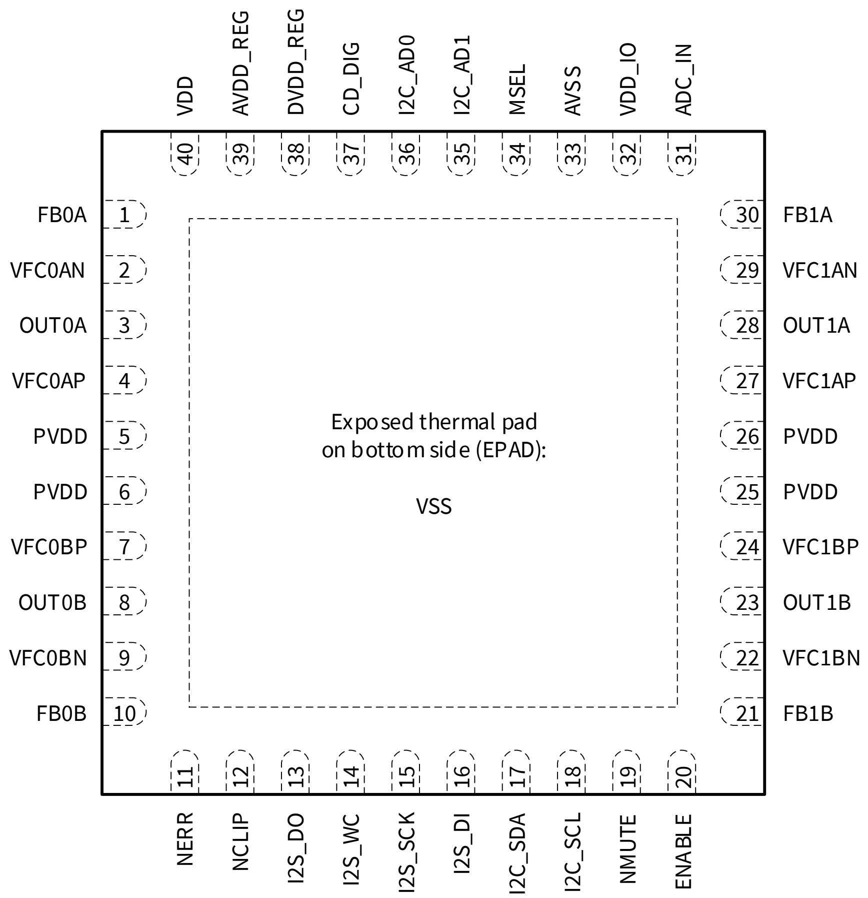


Figure 8.1: Package Overview - 6x6 mm QFN-40 pins

9 Pin List

Table 2: Pin List MA2304PNS

Pin Nr.	Name	Type	Description
1	FB0A	I	Output channel 0A post-ferrite feedback
2	VFC0AN	P	Negative side flying capacitor for channel 0A
3	OUT0A	O	Audio output channel 0A
4	VFC0AP	P	Positive side flying capacitor for channel 0A
5	PVDD	P	Power supply for power stage
6	PVDD	P	Power supply for power stage
7	VFC0BP	P	Positive side flying capacitor for channel 0B
8	OUT0B	O	Audio output channel 0B

9	VFC0BN	P	Negative side flying capacitor for channel 0B
10	FB0B	I	Output channel 0B post-ferrite feedback
11	NERR	O	Error indicator – open drain output. Use this pin as interrupt for host microcontroller to read error register.
12	NCLIP	I/O	Clipping indicator output (default) or PWM synchronization I/O
13	I2S_DO	O	I2S/TDM digital audio data output
14	I2S_WC	I	I2S/TDM digital audio word clock
15	I2S_SCK	I	I2S/TDM digital audio bit clock
16	I2S_DI	I	I2S/TDM digital audio data input
17	I2C_SDA	I/O	I2C bus serial clock
18	I2C_SCL	I/O	I2C bus serial data
19	NMUTE	I	Mutes audio output when pulled low
20	ENABLE	I	Enables device when pulled high. Pulling this pin low shuts down the device.
21	FB1B	I	Output channel 1B post-ferrite feedback
22	VFC1BN	P	Negative side flying capacitor for channel 1B
23	OUT1B	O	Audio output channel 1B
24	VFC1BP	P	Positive side flying capacitor for channel 1B
25	PVDD	P	Power supply for power stage
26	PVDD	P	Power supply for power stage
27	VFC1AP	P	Positive side flying capacitor for channel 1A
28	OUT1A	O	Audio output channel 1A
29	VFC1AN	P	Negative side flying capacitor for channel 1A
30	FB1A	I	Output channel 1a post-ferrite feedback
31	ADC_IN	I	Auxiliary ADC input
32	VDD_IO	P	Digital I/O supply. Used for external resistor pull-ups, e.g. for I2C bus.
33	AVSS	P	Ground for internal analog circuitry
34	MSEL	I	Hardware select for BTL (pull high) or PBTL (pull low)
35	I2C_AD1	I	I2C bus address pin 1. Use I2C_AD1 and I2C_AD0 to set I2C address: 00:0x20, 01:0x21, 10:0x22, 11:0x23.
36	I2C_AD0	I	I2C bus address pin 0
37	CD_DIG	P	Internal digital core supply charge-pump. Connect 1 µF between this pin and DVDD_REG.
38	DVDD_REG	P	Internal regulated supply decoupling. Connect 1 µF between this pin and ground.
39	AVDD_REG	P	Internal regulated supply decoupling. Connect 1 µF between this pin and ground.
40	VDD	P	External low voltage supply.
EPAD	VSS	P	Ground for internal digital circuitry and PVDD

10 Specifications

10.1 Absolute Maximum Ratings

NOTE: Usage outside the specifications stated in this table may cause permanent damage to the device and/or compromise reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
VDD	Low voltage supply	-0.3	5.5	V
PVDD	Power amp supply	-0.3	22	V
VDD_IO	Digital I/O supply	-0.3	5.5	V
V_{speak}	Speaker node output pins	-0.3	PVDD+2	V
V_{PIO}	IO and hardware setting pins (NERR, NCLIP, I2S_DO, I2S_WC, I2S_SCK, I2S_DI, I2C_SDA, I2C_SCL, NMUTE, ENABLE, MSEL, I2C_AD0, I2C_AD1)	-0.3	VDD_IO	V
V_{ADC}	ADC_IN pin	-0.3	1.5	V
T_{AMB}	Ambient operating temperature	-25.0	85	°C
T_J	Junction temperature	-25.0	150	°C
T_{STORE}	Storage temperature	-55.0	150	°C

10.2 ESD and Thermal Characteristics

Table 4: ESD and Thermal Characteristics

Parameter	Description	Min	Typ	Max	Unit
$V_{ESD,HB}$	ESD Human Body Model	-3000		+3000	V
$V_{ESD,CD}$	ESD Charged Device Model	-1000		+1000	V
$T_{\theta JA}$	Thermal resistance, Junction-to-Ambient, 4-layer PCB (EVAL_MA23xx)		28.9		°C/W
$T_{\theta JC}$	Thermal resistance, Junction-to-Case (EPAD)		1.9		°C/W

10.3 Recommended Operating Conditions

NOTE: Usage outside the recommended operating conditions stated in this table may cause the device to not behave properly. This can lead to interrupted audio playback, protection features being triggered etc. This applies to DC+AC values outside the min/max values.

Table 5: Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VDD	Low voltage supply (DC+AC ripple)	1.62	1.8	3.65	V
PVDD	Power amp supply (DC+AC ripple)	10.0	18	20	V
VDD_IO	Digital I/O supply (DC+AC ripple)	1.62	1.8	3.65	V
ILEQ	Minimum required equivalent load inductance per output pin for short circuit protection	0.5			µH

Refer to sections 11.5 and 11.5.4 for more details on supply voltages and their protection mechanisms.

10.4 Electrical Characteristics

Conditions (unless specified otherwise): PVDD=18 V, VDD/VDD_IO=3.3 V, Power Mode Profile: LPC, T_{AMB}=25 °C, Load: 4 ohm + 22 µH, PCB: EVAL_AUDIO_MA23xx (no output filter)

Table 6: Electrical characteristics.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
BTL Output Power						
$P_{COUT,BTL}$	Continuous Output Power p/ch[1]	Load=4Ω+22µH, sig=pink noise, CF=9dB; Thermal Warning triggered		12		W
		Load=4Ω+22µH, sig=pink noise, CF=9dB, Thermal Error triggered (device shuts down)		14		W
		Load=8Ω+22µH, sig=1 kHz sine, THD+N=1%		17		W
		Load=8Ω+22µH, sig=1 kHz sine, THD+N=10%		20		W
$P_{RMSOUT,BTL}$	RMS Output Power p/ch[1]	Load=4Ω+22µH, sig=1 kHz sine, THD+N=1%		30		W
		Load=4Ω+22µH, sig=1 kHz sine, THD+N=10%		37		W
$P_{IPOUT,BTL}$	Instantaneous Peak Output Power p/ch[1]	Load=4Ω+22µH, sig=1 kHz sine, THD+N=1%		60		W
$I_{OUT,BTL}$	Maximum Output Current p/ch[1]		6			A
$T_{CASE,BTL}$	Case temperature on board at 'Continuous Output Power p/ch'[2]	PCB=EVAL_AUDIO_MA23xx, Load=4Ω+22µH		113		°C
PBTL Output Power						
$P_{COUT,PBTL}$	Continuous Output Power p/ch[1]	Load=4Ω+22µH, sig=pink noise, CF=9dB, Thermal Warning triggered		24		W
		Load=4Ω+22µH, sig=pink noise, CF=9dB, Thermal Error triggered (device shuts down)		28		W
$P_{RMSOUT,PBTL}$	RMS Output Power p/ch[1]	Load=2Ω+22µH, sig=1kHz sine, THD+N=1%		60		W
		Load=2Ω+22µH, sig=1kHz sine, THD+N=10%		74		W
$P_{IPOUT,PBTL}$	Instantaneous Peak Output Power p/ch[1]	Load=2Ω+22µH, sig=1kHz sine, THD+N=1%		120		W
$I_{OUT,PBTL}$	Maximum Output Current p/ch[1]		12			A
$T_{CASE,PBTL}$	Case temperature on board at 'Continuous Output Power p/ch'[2]	PCB=EVAL_AUDIO_MA23xx, Load=2Ω+22µH		78		°C
Power stage						
η_{BTL}	Efficiency (BTL)[2]	POUT=2x100mW, Load=8Ω+22µH		57		%
		POUT=2x1W, Load=8Ω+22µH		79		%
		POUT=full scale, Load=8Ω+22µH		90		%
		POUT=2x100mW, Load=4Ω+22µH		54		%
		POUT=2x1W, Load=4Ω+22µH		73		%
		POUT=full scale, Load=4Ω+22µH		84		%
$R_{ON,BTL}$	Total on-resistance of the internal power stage (BTL)[1]	BTL on-resistance: 4x MOSFETS in series + bond wires		400		mΩ
$R_{ON,PBTL}$	Total on-resistance of the internal power stage (PBTL)[1]	PBTL on-resistance: 2x BTL power stages in parallel		200		mΩ
$f_{SW,FET}$	Internal MOSFET switching[1] frequency	LPC mode, low signal level		128		kHz
		LPC mode, high signal level		256		kHz

		HAP mode		256		kHz
$f_{SW,LOAD}$	Switching frequency seen[1] differentially by the load	LPC mode, low signal level		512		kHz
		LPC mode, high signal level		1024		kHz
		HAP mode		1024		kHz
Power Consumption						
P_{IDLE}	Total idle power consumption for VDD+PVDD+VDD_IO[1] (device enabled and unmuted)	PVDD=18V, LPC mode		52		mW
		PVDD=18V, HAP mode		70		mW
$I_{PVDD,IDLE}$	Quiescent/idle current, PVDD [1] (device enabled and unmuted)	PVDD=18V, LPC mode		2.2		mA
		PVDD=18V, HAP mode		3.2		mA
$I_{VDD,IDLE}$	Quiescent/idle current, VDD [1] (device enabled and unmuted)	VDD=3.3 V, LPC mode		3.5		mA
		VDD=1.8 V, LPCmode		3.5		mA
		VDD=3.3 V, HAP mode		3.6		mA
		VDD=1.8 V, HAP mode		3.6		mA
$I_{VDD\_IO,IDLE}$	Quiescent/idle current, VDD_IO[1]	VDD_IO = 3.3 V, No load on I2S_DO		2.3		µA
		VDD_IO = 1.8 V, No load on I2S_DO		2.3		µA
$P_{IDLE,STANDBY}$	Total power consumption in standby mode for VDD+PVDD+VDD_IO[1]	PVDD=18V, VDD=1.8V		2.8		mW
		PVDD=18V, VDD=3.3V		4.7		mW
Audio Performance/IO						
V_{NOISE}	Output integrated noise level	20-20kHz integrated noise, A-weighted, LPC mode		82		µV
		20-20kHz integrated noise, A-weighted, HAP mode		52		µV
DNR	Dynamic Range	-60dBFS method, LPC mode		102		dB
		-60dBFS method, HAP mode		106		dB
THD+N	Total Harmonic Distortion + Noise[1]	POUT=5W, sig=1kHz, Load=4Ω		0.05		%
V_{OS}	Output offset voltage for low pop/click-noise		-25	-/+ 3	25	mV
f_S	Supported I2S/TDM input sampling rates[1]			32 44.1 48 88.2 96 176.4 196		kHz
t_{PD}	Propagation delay from audio input to amplifier[1]	Sample rate = 48 kHz, DSP enabled running ROM code		146		µs
$I2S\_SCK_{MAX}$	Maximum supported bit clock on I2S_SCK pin[1]			25		MHz
$N_{CH,MAX,IN}$	Maximum supported input I2S/TDM channels[1]			16		
$N_{CH,MAX,OUT}$	Maximum supported output I2S/TDM channels[1]			2		
G	Amplifier gain in dB (Vrms/FS)[1]	pvdd_scale=11, PVDD=18 V		22.5		dB
		pvdd_scale=10, PVDD=15 V		21.2		dB
		pvdd_scale=01, PVDD=12 V		19		dB
		pvdd_scale=00, PVDD=10 V		16.5		dB
Enable/Mute						
T_{ENABLE}	Time from ENABLE=high until ready for I2C communication[1]			15		ms
T_{UNMUTE}	Unmute time delay until audio output[1]			30		ms

I2C serial control interface						
f_{SCL}	I2C clock frequency[1]	Standard Mode		100		kHz
		Fast Mode		400		kHz
V_{IL}	Logic low voltage[1]	Percentage of VDD_IO voltage		30		%
V_{IH}	Logic high voltage[1]	Percentage of VDD_IO voltage		70		%
t_r	SDA and SCL rise time[1]	Standard Mode			1000	ns
t_f	SDA and SCL fall time[1]	Standard Mode			300	ns
t_{HIGH}	SCL clock high[1]	Standard Mode	4			µs
t_{LOW}	SCL clock low[1]	Standard Mode	4.7			µs
$t_{SU;DAT}$	Data, setup[1]	Standard Mode	250			ns
$t_{HD;DAT}$	Data, hold[1]	Standard Mode	5			ns
t_{BUF}	Min. stop to start condition[1]	Standard Mode	4.7			µs
$R_{PU,FM}$	Pull-up resistor for SDA/SCL[1]	Fast Mode	1		4.7	kΩ
$R_{PU,SM}$	Pull-up resistor for SDA/SCL[1]	Standard Mode	1		5.6	kΩ
Protection						
$UVLO_{PVDD}$	PVDD undervoltage lock-out threshold (I2C interface functional)			6.5		V
OVP_{PVDD}	PVDD over-voltage error threshold	PVDD rising		21.5		V
$OVP_{PVDD,CLR}$	PVDD over-voltage error clear	PVDD falling while OVP error triggered	20			V
OTE_{TRIG}	Over-temperature error trigger	Temperature rising		145		°C
OTE_{CLR}	Over-temperature error clear	Temperature falling		140		°C
OTW_{TRIG}	Over-temperature warning trigger	Temperature rising		115		°C
OTW_{CLR}	Over-temperature warning clear	Temperature falling		110		°C

[1]Guaranteed by design simulation.
[2]Measured on EVAL_MA2304 evaluation kit PCB. Parameter may depend on application/layout/board stackup etc.

11 Functional description

11.1 MERUS™ Multilevel Switching

MERUS™ multilevel switching features several benefits in class D audio amplification compared to conventional 2-level switching:

- Ultra low power consumption
- Unmatched power efficiency
- Low electromagnetic emission
- Reduced system cost

This chapter aims to explain these benefits in more detail.

11.1.1 Multilevel Topology

The integrated power stage of the MA2304PNS is a MERUS™ multilevel switching topology. It consists of two half-bridges with each four power MOSFETs and a flying capacitor. An intermediate voltage supply is generated over the flying capacitor's terminals, which together with the switching scheme of the MOSFETs result in a 2-phase PWM output with three voltage levels (0V, ½PVDD and PVDD) rather than the conventional two. This doubles the effective switching frequency seen at the PWM output.

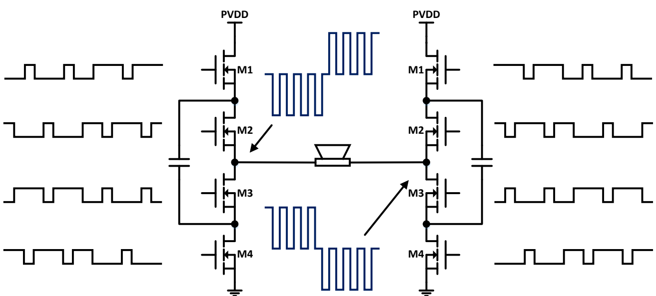


Figure 11.1: BTL/PBTL configuration of two 3-level half bridges

In MA2304PNS, two half-bridges are combined in a BTL/PBTL configuration (Figure 11.1) with a relative phase shift of 270°achieving a 5-level switching scheme across the load, effectively quadrupling the switching frequency seen at the load. This allows the internal MOSFETs to be driven with lower switching frequency, thus reducing power losses related to switching. Switching waveforms are shown in Figure 11.2.

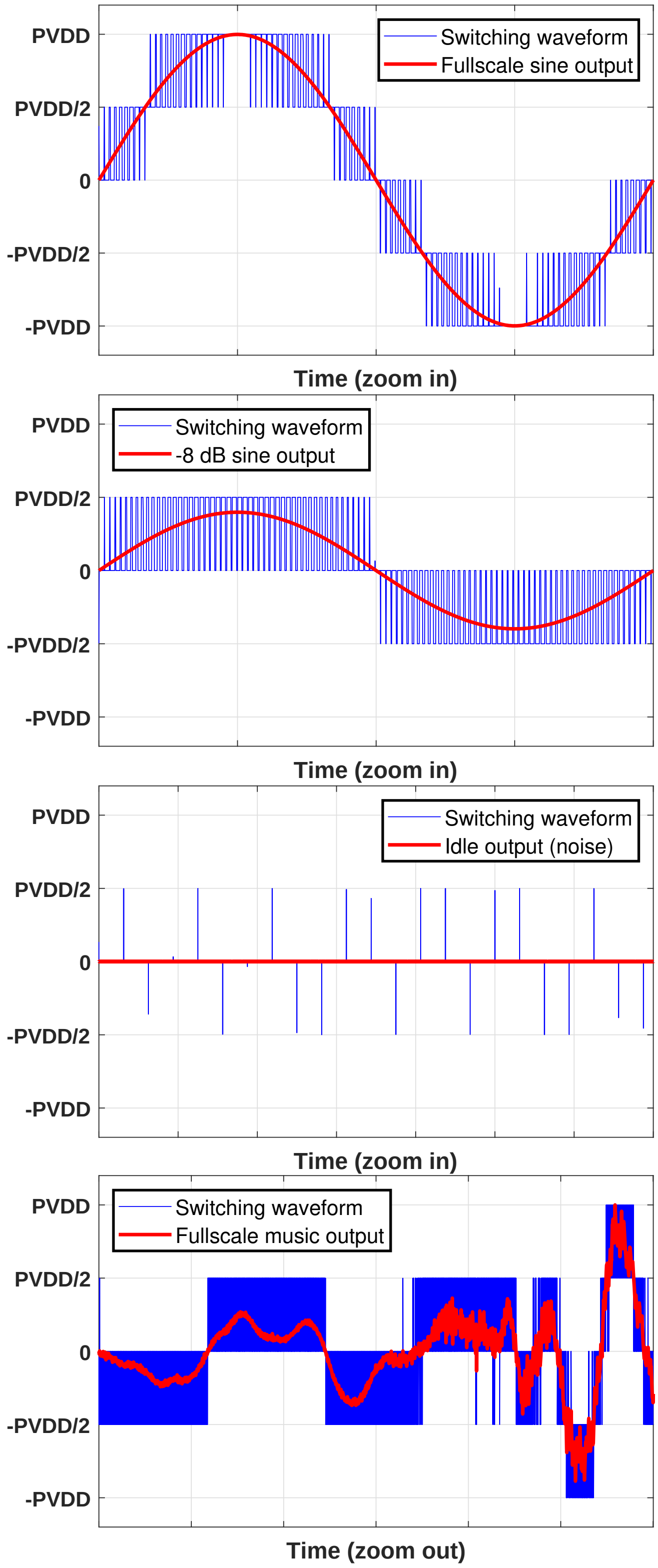


Figure 11.2: Multilevel switching with various signals.

11.1.2 Reduced Inductor Ripple Current

The multilevel topology reduces the voltage magnitude over the output filter inductor during switching, which in turn reduces the ripple current and relaxes filter inductor requirements. At idle operation where the output signal level is low, the MOSFETs are switched at 50 % duty cycle, resulting in near-zero ripple current. Hysteresis losses in the inductor core material are therefore also greatly reduced which improves overall power efficiency. From Figure 11.3 it is clear that 5-level switching provides greatly reduced ripple current over the entire duty cycle range compared to conventional 2-level switching. In fact, it is not even necessary to use a standard LC filter for electromagnetic interference (EMI) suppression. The MA2304PNS can even operate with a simple ferrite filter reducing both application cost and size. See Section 11.1.4 and 12 for more information.

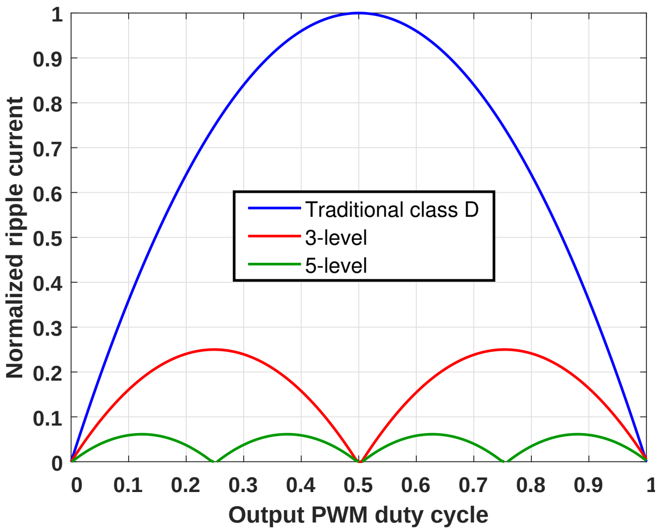


Figure 11.3: Ripple current comparison

11.1.3 Ultra Low Power Consumption with Music

MA2304PNS exhibits ultra low power consumption at low and mid output power, which is ensured by low MOSFET switching frequency, smaller voltage transitions when switching and near zero-ripple current. The low idle power consumption can make battery-powered applications last significantly longer or reduce the amount of battery cells required for a particular application.

Because of the low power consumption at lower output power levels, the MA2304PNS is ideal for real applications with dynamic signals like music/noise that exhibit a high signal peak-to-RMS ratio (crest factor). Power efficiency can be as high as 80 % at 1 W output power per channel, and because of the low power losses MA2304PNS may run without external heatsink in most applications. Figure 11.4 shows the difference in power efficiency between multilevel and traditional class D. From the figure it is clear that multilevel operation yields superior results for lower playback levels, which is the normal usage in common speaker products.

11.1.4 EMI Reduction

Complying with EMC regulations is a typical challenge with class D amplifiers due to the high power square wave output waveform. Traditional class D amplifiers have maximum current ripple in the output filter inductor at 50 % duty cycle (idle operation) which gives rise to high amount of common mode frequency content. However, MERUS™ multilevel operation exhibits minimal switching at idle which ensures minimal common mode emission at idle operation. The differential mode content at higher playback levels, when switching activity is stronger, is also significantly reduced as the transition between voltage levels is relatively small

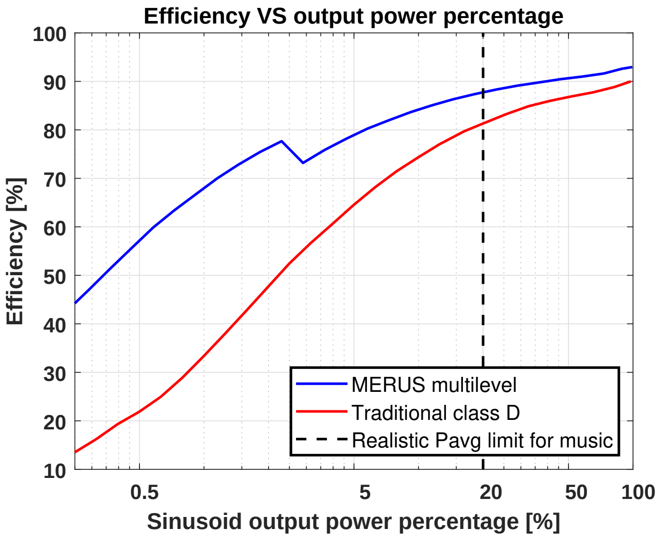


Figure 11.4: MERUS™ multilevel modulation efficiency compared to traditional 2-level modulation

for multilevel compared to traditional class D. In addition, MA2304PNS makes it possible to address EMC issues from a software perspective with its PWM synchronization feature as well as configurable switching edge steepness (slew rate), all to reduce EMI in applications with many devices, e.g. multi-channel amplifiers.

11.1.5 Power Mode Profiles (PMP)

The MA2304PNS features two selectable power mode profiles (PMP):

- Low Power Consumption (LPC) Mode
- High Audio Performance (HAP) Mode

LPC mode keeps efficiency as high as possible and minimizes idle losses by using a lower switching frequency for low output levels. HAP mode improves noise by using a higher switching frequency and therefore achieves a feedback loop with higher bandwidth. Switching frequency is dynamic for LPC mode and varies with output power with no audible artifacts. Table 7 shows the general properties of the two modes.

Table 7: Power Mode Profiles
*PVDD=18 V, VDD/VDD_IO=1.8 V, BTL, Load=8 Ω+22 µH, PCB=EVAL_AUDIO_MA23xx

Parameter	LPC	HAP
Idle consumption*	52 mW	70 mW
Efficiency 0.1 W*	57 %	47 %
Efficiency 1 W*	79 %	79 %
Efficiency 10 W*	93 %	93 %
FET switch. freq.	128-256 kHz	256 kHz
Switch. freq. at load.	512-1024 kHz	1024 kHz
THD+N, 1 kHz, 5 W	0.05 %	0.05 %
Noise, A-weighted	82 µV	52 µV
Dynamic Range	102 dB	106 dB

11.2 Modes of Operation

11.2.1 Normal Operation / Shutdown (ENABLE pin)

The ENABLE pin (20) controls the shutdown state of MA2304PNS. When ENABLE is low, the device is in shutdown mode. When ENABLE becomes high, the device exits shutdown state, boots up and enters normal operation. Refer to specifications for ENABLE timing.

11.2.2 Mute / Unmute (NMUTE pin)

NMUTE (19) controls muting of the amplifier output and is an active-low pin, i.e. if NMUTE=high the output will be unmuted. Muting is instantaneous, but unmuting is a timed function with a delay (refer to NMUTE timing)
Muting can also be performed with the mute_ch0/1 register for individual channels. Use mute_source to choose the source of muting: NMUTE pin or register setting.

In muted state, no audio content is present at the amplifier output, but there will be some switching activity to balance and pre-charge the flying capacitors. If no switching activity is desired the individual amplifier channels can be disabled with the disable_ch0/1 registers.

11.2.3 Standby

The device can be put in standby mode for lowest possible power consumption while still maintaining a functional I2C interface (to wake the device at a later point). Standby mode is controlled with the standby register.

11.3 BTL/PBTL Output Configurations

The amplifier output can be configured to operate in

- Bridge Tied Load (BTL)
- Parallel Bridge Tied Load (PBTL)

Table 8: BTL/PTBL properties

Parameter	PBTL	BTL
Min. current limit	12 A	6 A
Recommended load	2-4 Ω	4-8 Ω
MSEL pin tie-off	Ground	VDD_IO

The MSEL pin (34) controls the output configuration and must be set before the device powers up (when ENABLE=1). Alternatively, the mode_pbtl register can be used to configure the output after the device has powered up. The TBD_reg_ctrl register must also be set for the mode_pbtl register to take effect and override the hardware setting of the MSEL pin.

BTL is best suited for standard current, two-channel applications, e.g. stereo speaker pairs and 2-way systems. PTBL is a 1-channel configuration but with twice the output power/current capability, which can be useful for subwoofers and/or low impedance speakers. Refer to Figure 11.5 and 11.6 for configuration diagrams.

PBTL mode dynamically enables the second output based on the signal level so that idle power consumption can be as low as possible when high output power is not needed.

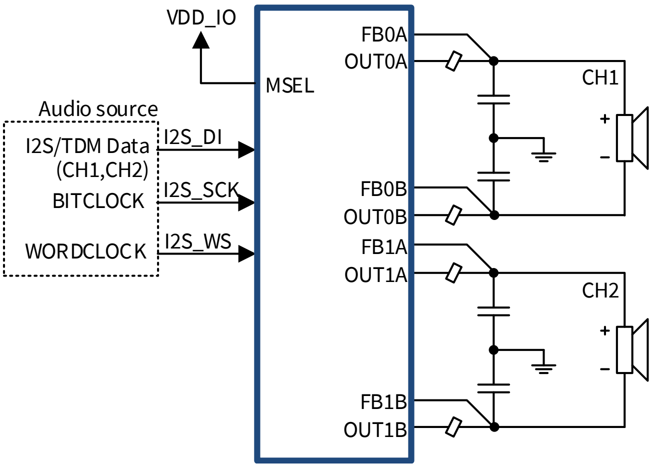


Figure 11.5: Bridge Tied Load (BTL) configuration

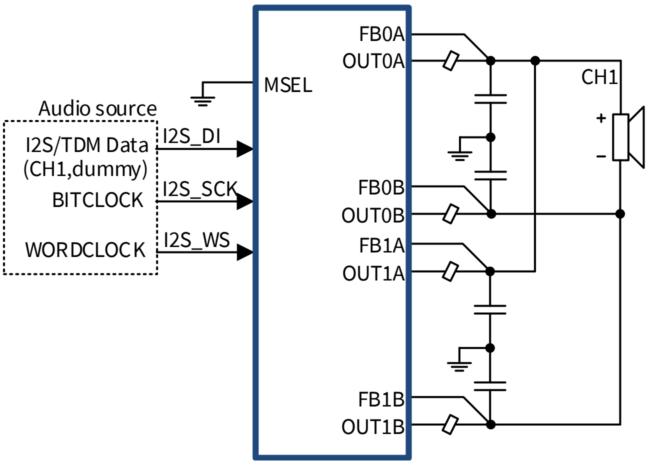


Figure 11.6: Bridge Tied Load (PBTL) configuration. Note: It is also possible to connect output pins A and B before the ferrite filter in order to use two ferrites in total instead of four.

11.4 Gain Configuration

MA2304PNS offers different gain configurations for matching full scale output with the desired PVDD voltage in an application. The gain is controlled with the pvdd_scale register. Reducing the amplifier gain to a lower value also reduces output noise. Gain frequency response is shown in Figure 13.28. Changing gain settings while the power stage is unmuted can result in significant pop/click and should be avoided. The table below shows the recommended pvdd scale setting for each different typical PVDD supply level. For a complete usable PVDD range in each pvdd scale setting refer to Figure 13.30 . Setting 11 and 10 can be used from 10V to 18V, setting 01 can be used from 10V to 16V and setting 00 can be used from 10V to 15V.

Table 9: Gain options for recommended (guideline) PVDD voltages.

pvdd_scale	Recommended PVDD
00	10 V
01	12 V
10	15 V
11 (default)	18 V

For additional noise characteristics as a function of gain and PVDD, please see Figure 13.29 and 13.30.

Note that the power stage cannot operate at full scale above 20 kHz. HAP mode is preferred if out-of-band operation is desired as its bandwidth is greater than LPC mode.

11.5 Protection

MA2304PNS offers a range of protection features to avoid damage to the device itself or attached speakers.

11.5.1 Errors and Error Handling (NERR pin)

The protection system in MA2304PNS monitors a range of parameters to check if min/max thresholds are exceeded. Exceeding the thresholds will trigger an error event in the protection system and the NERR pin (pin 11) will change from high to low. The NERR pin will only report errors correctly after the first PLL lock which requires clocks present on I2S_SCK and I2S_WC pins.

The NERR pin can be used as an interrupt flag for an external host control device, e.g. a system microcontroller. Alternatively, the err_pin register can be used to monitor the NERR pin as well. Once an error has been detected by the host, the error type can be identified by reading the error registers. Connect a 51 kΩ resistor from NERR to VDD_IO.

General device errors:

- Low temperature warning
- I2S input error
- PLL error
- PVDD over-voltage
- PVDD under-voltage
- Over-temperature error
- Over-temperature warning

The errors above can be read as individual bits in the following registers:

- errVect_now.errVector_all__0 (instantaneous)
- errVect_acc.errVector_all__0 (accumulated/sticky)

Individual channel errors:

- DC error
- Flying capacitor error
- Over-current error

The errors above can be read as individual bits in the following registers:

- errVect_acc.errVector_ch0 (Channel 0 accumulated / sticky errors)
- errVect_acc.errVector_ch1 (Channel 1 accumulated / sticky errors)

Clearing errors
Errors can be cleared by toggling the reg.errTrig_reset register from 0 to 1 and then back to 0.

Error handling:
It is generally recommended to use to accumulated error registers for error detection and handling. Normal error handling procedure:

- Disregard errors during start-up of the device defined by T_{ENABLE}.
- Clear errors immediately after start-up.
- Monitor accumulated error registers (general + channel) and take appropriate action if an error occurs.
- Clear error register(s) after action has been taken to again monitor for new errors.

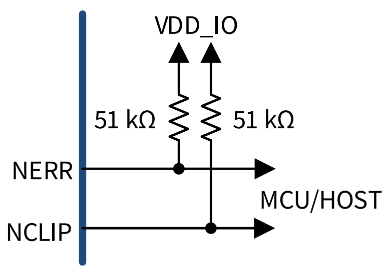


Figure 11.7: NERR/NCLIP schematic

11.5.2 Output DC Protection (DCP)

The amplifier output can detect if a DC voltage is present at the output terminals. If the output voltage stays above the DCP threshold for too long, corresponding to a 1 Hz sinusoid, the power stage will shut down, a DC error will be reported to the channel error register and the power stage will attempt to restart and resume operation. Each output channel is monitored separately.

11.5.3 Over-Current Protection (OCP)

Over-current (OC) events can be triggered by e.g. driving low impedance loads with high PVDD and shorting speaker terminals to each other or to ground. The current flowing in each internal MOSFET in the output stage is monitored. If the threshold is exceeded (refer to BTL threshold and PBTL threshold) the power stage will shut down, an OCP error will be reported to the error register and the power stage will attempt to restart and resume operation.

11.5.4 PVDD Over/Under-Voltage Protection

PVDD features over-voltage (OVP) and under-voltage (UVP) protection as well as under-voltage lockout (UVLO). Threshold voltages can be found in specifications. Refer to Figure 11.8 for an overview of the voltage protection on PVDD.

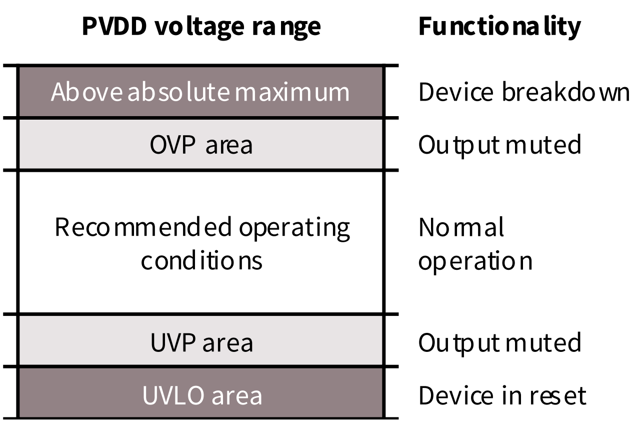


Figure 11.8: PVDD voltage protection overview

OVP protects the MOSFETs in the output power stage against permanent damage due to over-voltage. If PVDD voltage rises above OVP_{PVDD} the power stage will stop switching and the output will effectively be muted (overriding NMUTE pin). PVDD voltage must fall below $OVP_{PVDD,CLR}$ voltage before the device exits muted state. OVP will not protect the device against PVDD voltages rising above the absolute maximum value.

UVP behaves similarly and also mutes the output (without audio artifacts) by stopping all switching in the output power stage if PVDD voltage drops below the recommended operating conditions. In UVP state it is still possible to communicate with the device but mute is sustained. UVP should be considered a warning for low and/or unstable PVDD.

If PVDD is reduced further, falling below the $UVLO_{PVDD}$ threshold, the device shuts down. Power-on reset is applied when raising PVDD above the rising threshold again. When shut down, the device is not functional.

11.5.5 Over Temperature Protection (OTP)

An internal temperature sensor effectively safeguards the device against a thermally induced failure due to overloading and/or insufficient cooling. A high die temperature initially causes an Over Temperature Warning (OTW). During an OTW event, the device will continue to operate normally but if the temperature rises further, the device will reach Over Temperature Error (OTE). An OTE event will cause the device to stop all output switching activity in order to avoid permanent damage. The device will resume switching when the temperature has dropped sufficiently. Both OTW and OTE will report to the NERR pin and the error registers. Refer to specifications for OTE and OTW trigger and clear temperatures.

11.5.6 PLL Error and I2S Input Error

PLL error will occur in case of lost clock signals on the I2S_SCK and I2S_WC. The MA2304PNS relies on these clock signals to operate properly and if they are not present or faulty, the core will come to a halt state, reporting to the error system that the PLL is not locked. When the clock signals return, operation is resumed. In the event of bad audio input an error will also be reported to the error register on a separate bit.

11.5.7 Flying Capacitor Over/Under-Voltage Protection

The flying capacitors connected to the VFCxxx pins are essential for MERUS™ multilevel switching to function properly. During normal operation an internal voltage balancing circuit will generate a virtual PVDD/2 supply across the external flying capacitor. To protect the internal MOSFETs against permanent damage the MA2304PNS features over/under-voltage protection (OVP/UVP) in case of loop instability or flying capacitor balancing errors. The flying capacitor voltage is monitored and OVP/UVP is triggered if the voltage over the flying capacitors is deviating too far from PVDD/2. In this event, the output stage stops switching (output muted). When the flying capacitor voltage has again been balanced the device starts switching automatically (output unmuted).

Note that flying capacitor over/under-voltage protection will not trigger if the PVDD voltage is below 13 V. The reason is that the feature is designed to protect the internal MOSFETs against over-voltage conditions that could cause permanent damage to the IC, and at lower PVDD voltages the MOSFETs are no longer prone to this condition.

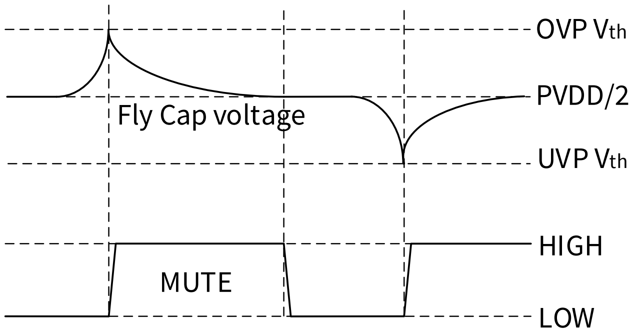


Figure 11.9: Flying capacitor protection behaviour

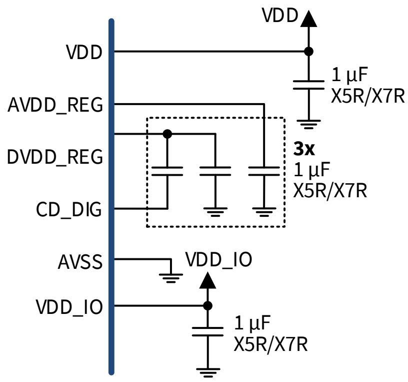


Figure 11.10: Decoupling/supply capacitor schematic with recommended specifications

11.5.8 NCLIP Pin

The NCLIP works as a clipping indicator and starts pulsing from high to low at higher levels and becomes constant low when near clipping. A system microcontroller can use this pin as an indicator to decrease volume/gain if desired when clipping occurs. Alternatively, the integrated DSP features a configurable output limiter that can be used to prevent clipping. Triggering NCLIP does not register as an error, but the clip_pin register can be used monitor the state of NCLIP. Connect a 51 kΩ resistor from NCLIP to VDD_IO as shown in Figure 11.7.

11.6 Power Supplies

11.6.1 Supplies for Internal Analog/Digital Circuitry (VDD/VDD_IO)

MA2304PNS generates its own internal analog/digital supplies from VDD with the use of external capacitors and the AVDD_REG, DVDD_REG and CD_DIG pins. AVSS is the ground reference pin for the internal analog circuitry. MA2304PNS is designed to work with common power supply voltages, 1.8 V / 3.3 V, which are typically found in applications powering the host device already. When VDD is power cycled, the MA2304PNS register settings are reset to default. All VDD decoupling capacitors should be placed as close as possible to the supply pins. The recommended capacitor specifications are shown in Figure 11.10.
VDD_IO is used for pull-up resistors to I/O pins on the south side of MA2304PNS (pins 11-18). These are NERR (11), NCLIP (12), I2S_DO (13), I2S_WC (14), I2S_SCK (15), I2S_DI (16), I2C_SDA (17), I2C_SCL (18), NMUTE (19) and ENABLE (20). Note that the serial audio data output pin I2S_DO is internally driven by the VDD_IO supply.

For simplicity, VDD_IO and VDD can be tied to the same low voltage supply in the application.

11.6.2 Flying Capacitors

The MA2304PNS power stage uses flying capacitors to generate a ½PVDD supply voltage for multilevel operation. Each output switch node pin OUTxx has a corresponding flying capacitor, with a positive and a negative terminal, VCFxxP and VCFxxN pins. The fly-cap pins are high power pins and care must be taken to reduce inductance/resistance in the PCB layout as the full output current will flow through pins/caps. Keep the flying capacitors as close to the device as possible with as short and wide PCB traces as possible. Refer to Section 12 for more information.

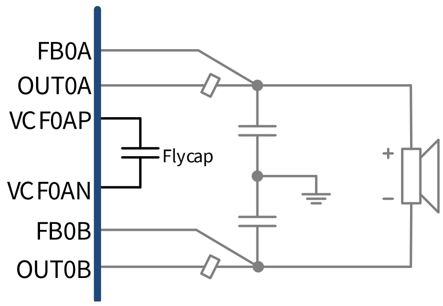


Figure 11.11: Flying capacitor schematic with recommended specifications

When choosing flying capacitors, it is necessary to keep capacitance derating vs. DC bias voltage in mind if multilayer ceramic capacitors (MLCC) are used. The fly-caps are constantly charged to ½PVDD, which will derate the expected capacitance. In general, high quality 10 µF 25V X5R/X7R 0805 MLCCs are recommended (example: C2012X5R1E106K125AB). The minimum effective capacitance should be 4.0 µF at ½PVDD for correct operation.

11.6.3 Power Stage Supply (PVDD)

PVDD supplies current to the output power stage to drive the load. A bulk decoupling capacitor is recommended on the PCB to keep the supply stable, e.g. aluminium electrolytic type capacitor. Capacitance value will depend on the application (lowest playback frequency, ripple voltage and maximum peak power requirements). In general, a 470 µF aluminium electrolytic capacitor will be sufficient for most applications.

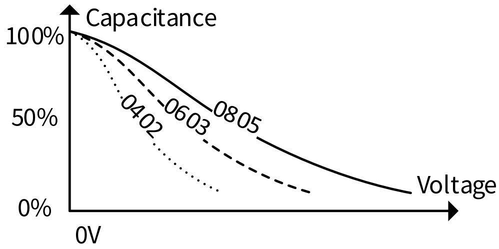


Figure 11.12: Typical derating for multi-layer ceramic capacitors (MLCC) with different package sizes

To decouple fast transitents, it can be beneficial to place two low ESR capacitors with smaller capacitance value, e.g. 1 µF and 10 µF, close to the PVDD pins on each opposing side of the MA2304PNS. Figure 11.13 shows the recommended PVDD decoupling schematic.

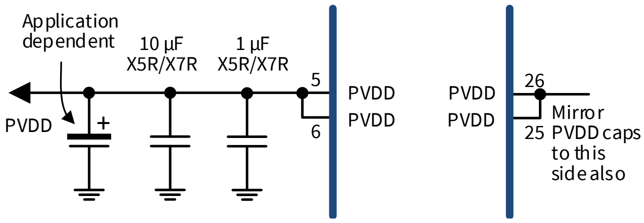


Figure 11.13: Typical derating for multi-layer ceramic capacitors (MLCC) with different package sizes

11.7 Clock System

MA2304PNS generates its own internal clock through a PLL in the presence of a serial audio bit clock (I2S_SCK) and a word clock (I2S_WC).

The frequency of the audio bit clock is auto-detected and clock frequencies up to 24.576 MHz are supported. The audio bit clock frequency will depend on sampling frequency, slot size (frame width) and the number of channels in the audio stream according to Equation 1.

$$f_{SCK} = f_s \cdot \mathrm{slot\_size} \cdot N_{CH} \leq 24.576\mathrm{MHz} \quad (1)$$

11.8 Audio Interface

11.8.1 Digital Serial Audio Input

MA2304PNS has a single serial data audio input port that consists of the pins I2S_WC (word clock), I2S_SCK (bit clock) and I2S_DI (data in). The input port supports two-channel I2S and multi-channel TDM audio formats with sampling rates of 32, 44.1, 48, 88.2, 96, 176.4 and 192 kHz with data-words of 16, 24 or 32 bits in length. The format alignment is configured in the data_alignment register. MA2304PNS is always configured as an audio sink device (receiver). TDM format is capable of up to 16 audio channels on a single data line, making it ideal for multi-channel applications with multiple ICs.

By default, the internal audio receiver in MA2304PNS will look for starting edge on the word clock and receive packages based on the package slot size (also known as frame width, see slot_size register), irrelevant of the frame midpoint transition on the word clock. This means that I2S (2-channel) and TDM (multichannel) are processed similarly by the receiver, the difference being the amount of slot size packages received between two starting edges of the word clock. For example, a 2-channel 32 bit I2S audio stream will have a 64 bit audio frame cycle between word clock starting edges, whereas a 4-channel 32 bit TDM audio stream will have 128 bit between starting edges (refer to audio data configuration examples in Figures 11.15 and 11.16). In this way, MA2304PNS can automatically detect if the format is 2-channel or multichannel (I2S/TDM) as long as slot_size, data_size (bit depth), data_alignment, sck_pol, ws_fs_rising and lsb_first registers are configured to match for both the external transmitter (source) and the MA2304PNS (sink).

To configure the input channel routing, refer to the tdm_input_map register.

11.8.2 Digital Serial Audio Output

MA2304PNS features a serial audio data output (pin 13: I2S_DO) with the same audio format properties as the serial audio input. To enable the audio output, the tx_enable register must be enabled. By default (refer to ROM code), the DSP output channels 1 and 2 (the signals received by the amplifier) are routed to I2S_DO, but this can be configured using the tdm_output_map0-15 registers.

11.8.3 Input-to-Output Audio Propagation Delay

MA2304PNS offers a very low propagation delay from audio input to amplified output, making it ideal for delay sensitive applications such as echo-cancelling speaker phones and conference equipment. Refer to specifications for more info.

11.9 Digital Signal Processor (DSP)

11.9.1 ROM Code / Static Memory

The MA2304PNS contains ROM code (static memory) with a preconfigured DSP program that includes volume control and peak limiters. The ROM code is applied to the DSP by default when MA2304PNS is reset.

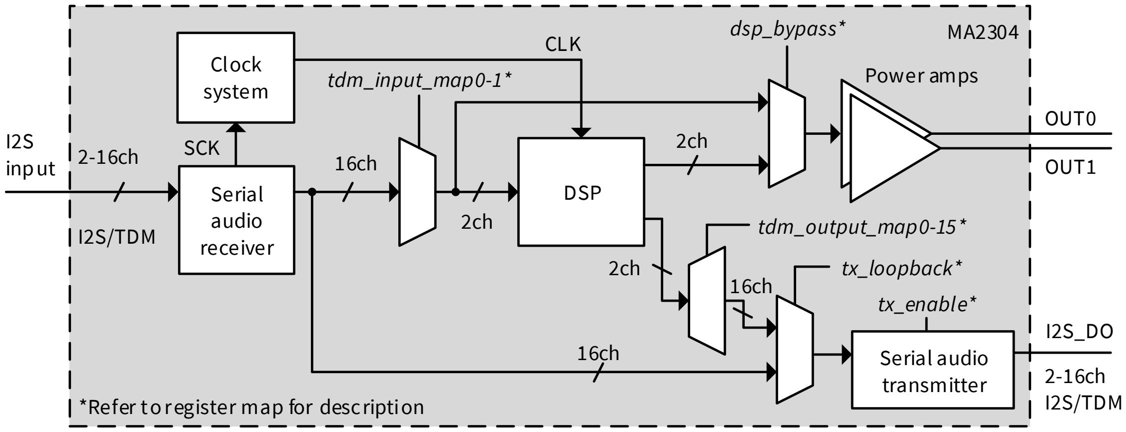


Figure 11.14: Audio routing

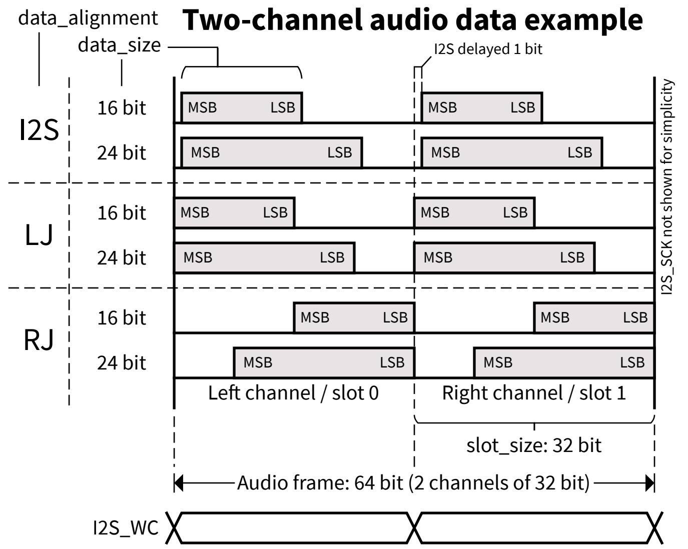


Figure 11.15: Audio data configuration/timing for two channels

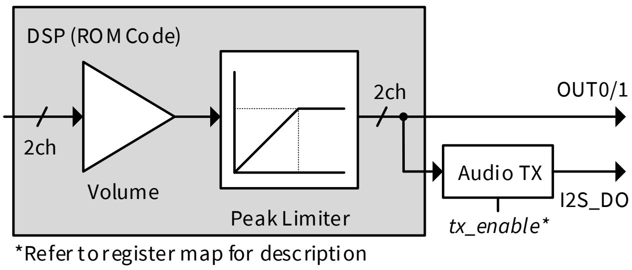


Figure 11.17: DSP ROM code

The ROM code can be disabled by disabling the DSP entirely in the dsp_enable register. Alternatively, the DSP can be bypassed with the dsp_bypass register. The output signal would be identical using either method, but the power consumption is slightly reduced by disabling the DSP instead of bypassing.

11.9.2 Volume Control

Volume can be controlled with the volume_ch register. The audio volume is not applied instantly but ramped to avoid audible click/pop artifacts. Volume ramping can be disabled by enabling the vol_instant register.

11.9.3 Peak Limiter (ROM Code)

The peak limiters in the ROM code can be configured with attack_ch, release_ch and threshold_ch registers, which control the attack and release times as well as the threshold for limiting. The attack and release times are sample rate dependent in the way that a higher register value should be chosen for higher sample rates to achieve an equivalent attack/release time.

11.10 Auxiliary ADC

MA2304PNS features an 8-bit auxiliary ADC. The ADC can sample from the power stage supply PVDD, the internal

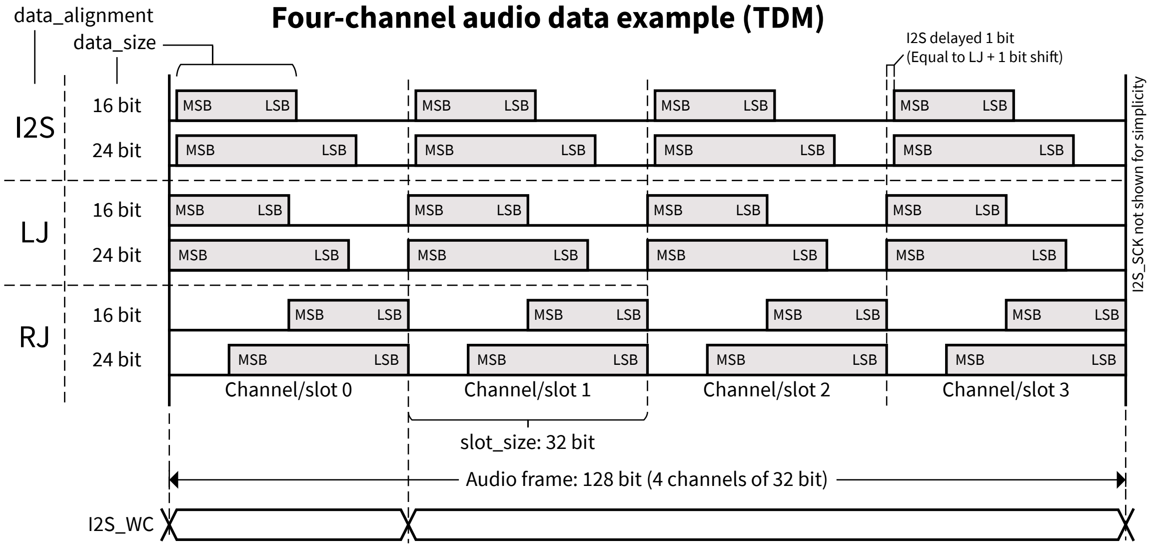


Figure 11.16: Audio data configuration/timing for four channels. Note that choosing 'I2S' in data_alignment for MA2304PNS does not restrict the data stream to only two channels. 'I2S' in data_alignment just refers to the data being aligned to the left and delayed by one bit.

temperature sensor or a voltage on the ADC_IN pin from an external source. The sampled data is available in registers pvdd_chip, temp_chip and adc_pin. The ADC_IN pin voltage range is 0 V (min) to 1 V (max).

The ADC can be useful for general purpose monitoring, e.g. keeping temperature below a specified point by adjusting volume if temperature readings become too high according to the application specification. The ADC is not designed for tasks with high precision.

11.11 I2C Serial Control Interface

MA2304PNS offers a serial control interface through the standard 2-wire I2C protocol using I2C_SDA (data) and I2C_SCL (clock) lines. An application host device may then access the register map to configure the MA2304PNS.

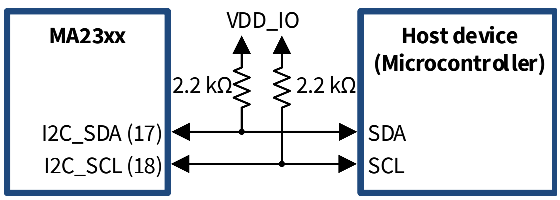


Figure 11.18: I2C serial control interface block diagram

MA2304PNS uses 16 bit register adresses for its internal register map (example: 0x0001). The SDA line is sampled on the rising edge of the SCL line and the I2C command is shifted/sampled with MSB first.

Communicating properly with the MA2304PNS to access a single register must contain the following I2C sequence:

Device address 7 bits + R/W bit	Register address 16 bits	Data 8 bits

Please see Section 11.11.2 and 11.11.3 for device addressing and write/read commands.

The SDA and SCL lines must be pulled high once per application to the voltage supplying VDD_IO through a resistor, e.g. 2.2 kΩ, to ensure correct I2C functionality. The minimum and maximum recommended pull-up resistor value is shown in specifications.

Please refer to the original I2C bus specification and user manual provided by NXP Semiconductors for more detailed information on I2C communication.

11.11.1 Device Address

Device addresses for I2C communication can be set by pulling the I2C_AD0 (pin 36) and I2C_AD1 (pin 35) pins to VDD_IO (high) or ground (low). This gives four unique device addresses for applications with up to eight BTL channels. The pin configuration on I2C_AD0 and I2C_AD1 are only read once during start-up of the device.

Table 10: Device addresses combinations

I2C address	I2C_AD1	I2C_AD0
0x20	Low	Low
0x21	Low	High
0x22	High	Low
0x23	High	High

If four device addresses are not sufficient, hardware resistor programming can be used for the I2C_AD0 and I2C_AD1 pins to enable up to 64 unique device addresses. The pins must be connected to ground through a resistor of a specific value as shown in Figure 11.19. Table 11 illustrates the combination of resistors to yield a specific address.

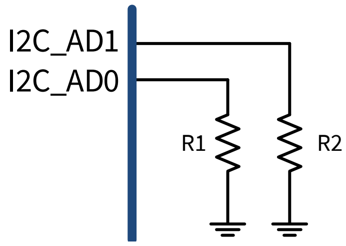


Figure 11.19: Resistor programming schematic

Table 11: Device addresses using resistor programming. Addresses are shown in decimal format

R2 / R1	150k	100k	68k	47k	33k	22k	15k	10k
150k	0	1	2	3	4	5	6	7
100k	8	9	10	11	12	13	14	15
68k	16	17	18	19	20	21	22	23
47k	24	25	26	27	28	29	30	31
33k	32	33	34	35	36	37	38	39
22k	40	41	42	43	44	45	46	47
15k	48	49	50	51	52	53	54	55
10k	56	57	58	59	60	61	62	63

11.11.2 I2C Write Operation

Each I2C transaction is initiated from an I2C transmitter by sending an I2C start condition followed by the 7-bit I2C device address and the read/write bit (bit 8, write=0).

If the transmitted I2C address matches the configured address of the device, the device will acknowledge the request by pulling the SDA line to ground (bit 9). The I2C transmitter samples the acknowledged bit from the device on the next rising edge of SCL.

To complete the write operation, the I2C transmitter must continue transmitting the address and at least one data byte. The device continues to acknowledge each byte received on the 9th SCL rising edge. Each additional data byte written to the device is written to the next address in the register bank.

The write transaction is terminated when the I2C transmitter sends a stop condition to the device (rising edge on SDA during SCL kept high).

Block writing large amounts of data is also supported.

Refer to Figure 11.20 for write sequence.

11.11.3 I2C Read Operation

To read data from the device register bank, the read transaction is started by the I2C transmitter, sending a write command to the I2C address (bit 8, write=1), followed by the device address to read from.

The device will acknowledge the two bytes and data can now be read from the device by sending a repeated start, followed by an I2C read command (bit 8, read=1).

The device will acknowledge the read request and start to drive the SDA bus with the bits from the requested register bank address.

If the user tries to read in a non-existing address, acknowledge will be sent anyway but read will be ignored internally (0x00 will be sent to the I2C read requester).

The read transaction continues until the I2C source does not acknowledge the 9th bit of the data read byte transaction and sends a stop condition (rising edge on SDA during SCL kept high).

Refer to Figure 11.20 for read sequence.

Read Operation without Write Start

To read data from the device register bank, the I2C source can send a read transaction without write command first, meaning an I2C read command consisting of a byte with the device I2C address and the R/W bit set. The device will acknowledge the read request and start to drive the SDA bus with the bits from the last requested register bank address+1.

11.12 EMI Mitigation

In addition to the inherently low EMI levels from the MERUS™ multilevel switching output, MA2304PNS features ways to mitigate EMI further, which can be useful for applications with multiple devices.

11.12.1 Configurable Switching Edge

Fast square wave switching transients usually increase the amount of unwanted high frequency EMI. The switching edge steepness (slew rate) can be controlled in the gd_dVdt register which can be used as a tool for tuning applications for EMI compliance. The compromise is efficiency, as slower transients will result in higher switching losses). Additional EMI suppression can be achieved by reducing the switching edge steepness (tested using the MA2304PNS EVK).

11.12.2 PWM Synchronization for EMI Reduction

In multi-channel systems with multiple MA2304PNS devices, it can be increasingly necessary to suppress EMI. The NCLIP pin (12) can be used as an input/output to synchronize PWM signals of multiple devices and allow them to be driven out of phase which can have an influence on EMI performance. PWM sync is configured according to Figure 11.23 as follows:

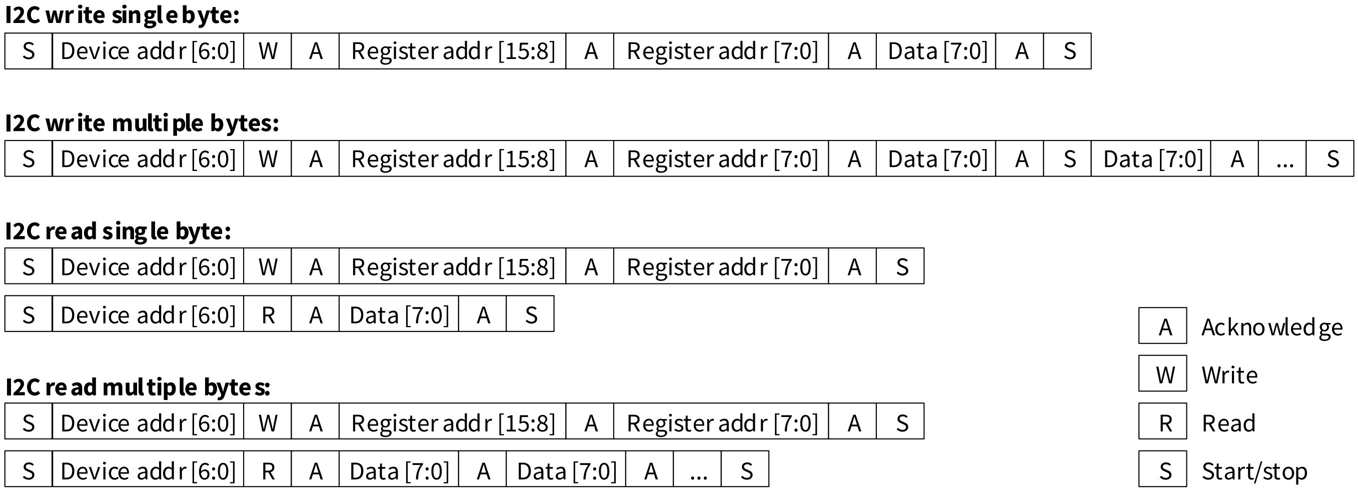


Figure 11.20: I2C write and read sequences

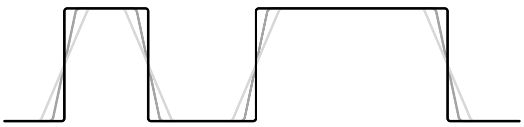


Figure 11.21: Configurable PWM switching edges to reduce high frequency EMI content

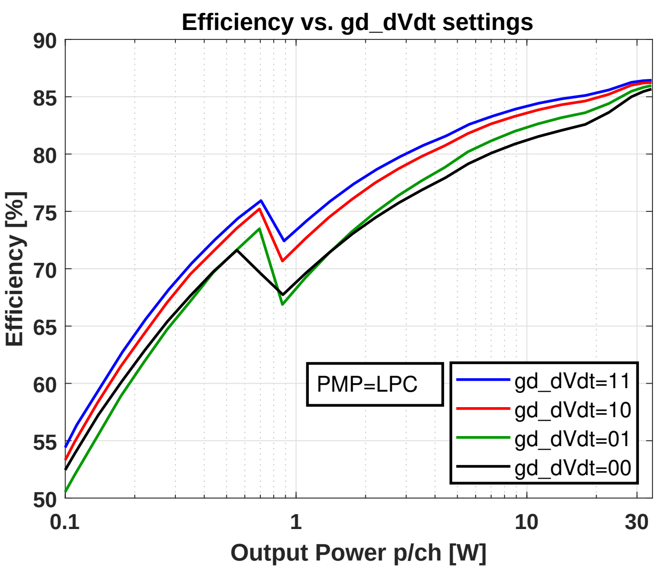


Figure 11.22: Efficiency for different gd_dVdt settings

1. Configure NCLIP pin to act as PWM input/output gpio_sync_zclip

2. Configure PWM source device by setting sync_out_enable

3. Configure PWM sink devices by setting sync_in_enable

4. Control PWM phase relationship in either source or sink devices by setting time lag in reg.pwm_phase

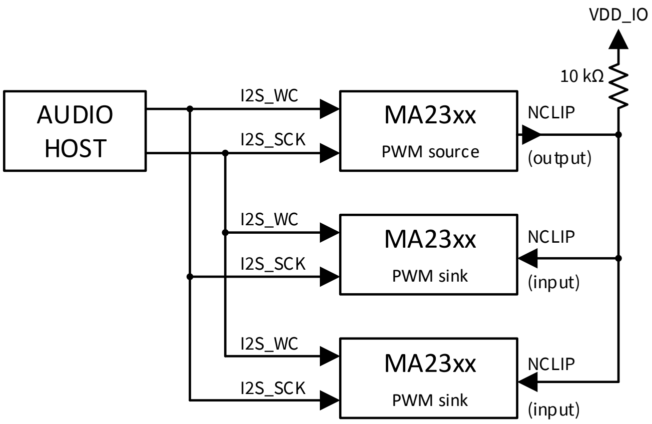


Figure 11.23: PWM synchronization for multiple MA2304PNS devices

NCLIP must be pulled up to VDD_IO through a 10 kΩ resistor. The clock signals I2S_SCK and I2S_WC in the audio stream must be the same for all devices.

11.13 Post-Ferrite Filter Feedback

MA2304PNS can include an output filter ferrite in the internal control loop to compensate for the non-linearities in the ferrite material and as such improve audio performance in terms of THD+N. This relaxes the requirements for high quality ferrites and can therefore minimize cost of the output filter.

The feedback pins (FBXA and FBXB) must always be connected for loop stability. If post-ferrite feedback is not desired, the feedback pins must be directly connected to the OUTXA and OUTXB pins, respectively as shown in Figure 11.25.

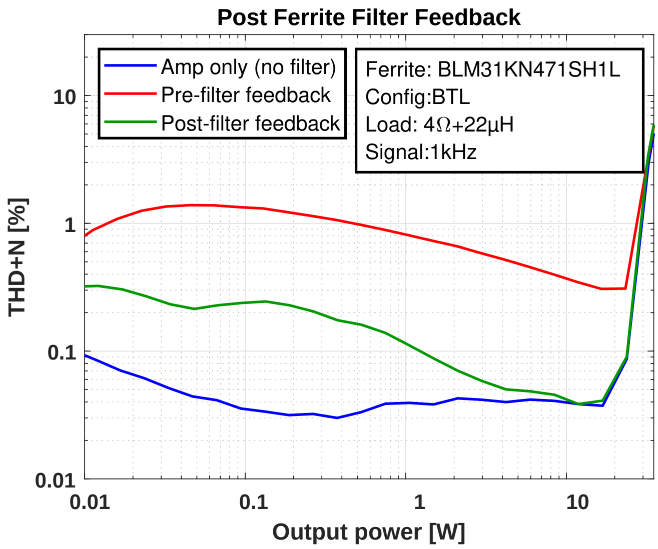


Figure 11.24: Example of the post-ferrite filter feedback effect on distortion characteristics

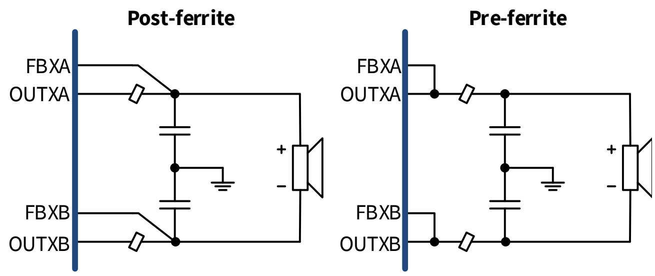


Figure 11.25: Post-ferrite filter feedback schematic

It is not recommended to use an LC filter with post-ferrite filter feedback because the phase introduced by the LC filter can cause loop instability. If an LC filter is desired in the application, pre-ferrite feedback should be used.

12 Application Information

12.1 EMC Ferrite Output Filter

The MA2304PNS allows for inductor-less operation while achieving EMI compliance. This is mainly due to the MERUS™ multilevel switching technology which reduces the magnitude of the switching waveform at all output levels. A simple and inexpensive ferrite-capacitor output filter can be used to suppress the emissions from the amplifier output. The filter schematic is shown in Figure 12.1 and recommended filter component values are shown in Table 12.

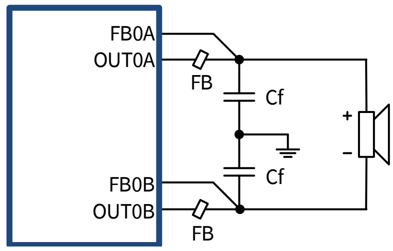


Figure 12.1: EMC ferrite output filter

Table 12: EMC ferrite filter recommendation

Ferrite	Capacitor
NFZ2MSD150SN10L	220 pF
NFZ2MSD301SZ10L	220 pF

PCB layout for the output filter should be tight and with the smallest possible current return path for optimal EMI performance. In an application, cables connected from speaker terminals to the PCB should be twisted if possible for the same reason.

12.1.1 Capacitor Value Impact on Power Consumption

The filter capacitor can have a significant impact on the MA2304PNS power consumption and must be of relatively low capacitance value, e.g. 100-220 pF for minimal impact. For a 220 pF capacitor on each output channel in a BTL configuration results in approximately 10-20 mW additional power consumption at idle operation. Higher capacitance values will increase power consumption further, but also provide a lower corner frequency with improved suppression of EMI. The capacitor value should be balanced for the target application, however, no more than 1 nF should be used.

Please refer to MA2304PNS application notes for more information and EMI measurement results.

12.1.2 Ferrite Filter Selection

The most important factor in EMI suppression is the output filter ferrite bead. Ferrite bead performance may vary greatly in terms of effective frequency region and suppression magnitude. This means that one ferrite part cannot necessarily replace another directly, and must be tested at an EMC lab for verification of compliance with regulations. An important characteristic is saturation current of ferrite material, which must comply with the maximum application output current in order to be effective at high output levels. Ferrites in 0805/1206 SMD packages will usually provide sufficient specifications. The NFZ-series from Murata yields good results, e.g. NFZ2MSD301SZ10L and NFZ2MSD150SN10L.

12.1.3 Ferrite Filter Stability Under Light Loads

Operating the MA2304PNS under very light output loads above 500 Ω can result in the amplifier's feedback loop becoming unstable, which can be a real scenario if the load is planned to be disconnected from time to time. If the load is planned to be disconnected during normal operation, it is recommended to use an RC damping network (snubber) similar to the damping network using an LC filter (Refer to Section 12.1.4). Starting point RC values can be R<500 Ω and C=22 nF but they need to be tuned to the specific application. The RC network will help maintain loop stability when the load is removed.

12.1.4 LC filter options

MA2304PNS can also operate with a LC filter for even higher EMI suppression. An LC filter can provide additional suppression of EMI, but will usually be higher cost and footprint size on board than a ferrite filter.

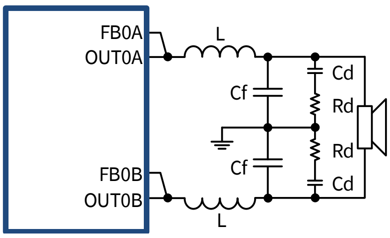


Table 13: LC filter schematic

The LC filter has to be carefully designed and tested to properly avoid instability with MA2304PNS. Stability issues can occur if the filter corner frequency is too low and non-sufficient EMI suppression may occur if the corner frequency is too high. The LC filter should consist of a filtering part (L and Cf) and a damping network (Cd and Rd) as shown in Figure 13. Typical recommended LC filter component values are shown in Table 14.

Table 14: Recommended LC filter component values

Design	L	Cf	Cd + Rd
#1	3.3 µH	470 pF	1 nF + 220 Ω
#2	4.7 µH	1 nF	10 nF + 100 Ω
#3	6.8 µH	10 nF	100 nF + 22 Ω
#4	10 µH	220 nF	1 µF + 10 Ω

Table 15 shows the difference in output noise (A-weighted) and idle power consumption as a function of the LC filter components and Power Mode Profile. All characteristics shown in the table are derived from the same device on the same board (EVK).

Please refer to MA2304PNS application notes for more information and EMI measurement results.

Table 15: Power and noise performance characteristics for recommended LC filter designs.
*Ref: Reference using no filter. Same device and board (EVK) was used to test all filter designs including reference.
**LPC mode was not applicable with high capacitance filter components.

Design	Idle power		Output noise	
	LPC	HAP	LPC	HAP
Ref*	49 mW	74 mW	90 µV	54 µV
#1	75 mW	106 mW	120 µV	60 µV
#2	76 mW	96 mW	101 µV	55 µV
#3	70 mW	82 mW	95 µV	54 µV
#4	N/A**	69 mW	N/A**	53 µV

12.2 Thermal Design

The MA2304PNS is designed to be used in applications without external heatsink. A well-designed 4-layer PCB can act as a heatsink. The bottom thermal pad (EPAD) of the IC package should be thermally well-connected to the top layer copper with as many vias as possible to the other layers. It is recommended to keep routed traces in the middle layers to a minimum, avoiding any routing at all if possible. Let the bottom layer only be used for routing traces between layers. Deadspace in all layers should be filled with copper connected to ground to maintain unhindered thermal flow away from the IC. Refer to Figure 12.8 for PCB layout reference.

Heat is generated primarily in the on-resistance of the internal MOSFETs, as well as the bond wires from the silicon to the IC pins, and will be dependent on load current. The losses due to heat will be more severe with lower load impedances, as conduction losses in the IC will dominate with increasing current. A comparison between load and output configuration (BTL/PBTL) is shown in Figure 13.12 and 13.13.

12.3 Start-up Procedure

The recommended procedure for proper start-up of the device:

1. Keep the device disabled and muted: ENABLE = 0, NMUTE = 0.
2. Ensure MSEL, AD0 and AD1 pins are configured correctly.
3. Enable VDD, VDD_IO and PVDD supplies and wait for them to become stable.
4. Ensure I2S bit clock and frame clock are present.
5. Enable device: ENABLE = 1.
6. Wait T_{ENABLE} until the device has started up in order to read the NERR pin status and start communicating with I2C.
7. Program/initialize the device via I2C (if needed)

8. Unmute device: NMUTE = 1. When NMUTE time has elapsed, the device is ready for audio playback.
9. The device is now in normal operation state (idle) and ready to play audio.

12.4 Procedure for handling discontinuous audio clock

In some applications the audio clocks may be stopped by the transmitter side from time to time, which will also halt the MA2304PNS audio playback. When the clocks return, MA2304PNS will continue operation once the PLL has locked again. MA2304PNS is designed to handle loss of clocks without any audio artifacts without muting. For optimal performance, it is recommended to follow this procedure:

1. The device is in normal operation and audio clocks are present.
2. Mute the device: NMUTE=0. Alternatively, put the device in standby mode.
3. Disable the audio clocks from the transmitting side. The device is now only operational through I2C. PLL error is reported to the error register internally.
4. When audio playback is required again, enable the audio clocks, wait for the PLL to lock and the device to be fully operational again (see timing for T_{ENABLE})
5. Unmute the device: NMUTE=1. Alternatively, put the device out of standby mode.
6. The device is now in normal operation again and ready to play audio.

12.5 Power-down Procedure

The recommended procedure for proper power-down described below:

1. The device is in normal operation state.
2. Mute device: NMUTE = 0.
3. Disable device: ENABLE = 0.
4. The device is now in power-down state.
5. (Optional: Bring down VDD, VDD_IO and PVDD supplies.)

12.6 Recommended Layout

The recommended application/PCB layout is shown in Figure 12.8:

- **Decoupling:** Decoupling capacitors for power supplies VDD, AVDD_REG, DVDD_REG, CD_DIG, PVDD and VDD_IO must be kept as close to the device as possible. The smallest value capacitors should be placed closest to the device to handle fast transients.
- **Fly-caps:** Flying capacitors for VFCxxx pins must be kept as close to the device as possible and care must be taken to keep the current loop tight and short to ensure multilevel switching stability.
- **PCB layers:** A PCB with four layers is recommended to achieve power output performance stated in the electrical characteristics. Via stitching/array between board layers is encouraged on the ground net (GND), especially below the bottom thermal pad of the device which uses the PCB as a heatsink to dissipate heat. In general, the unused copper (deadspace) in all layers should be connected to ground for optimal thermal and EMI performance. Avoid breaking up the ground planes with any routing traces in all layers as much as possible to ensure good thermal connection throughout all PCB layers.
- **Output filter:** The traces from the output to the filter should be kept as short as possible for optimal EMI performance.
- **RC filter on I2S:** Digital audio/control lines (I2S/I2C) can have an impact on EMI performance. It is suggested to implement a RC first order lowpass filter close to the source on these lines to slow the transients and hence avoiding high frequency EMI. Values for the resistor and capacitor in the lowpass filter will be application dependent, but a good starting point could be 33 Ω and 180 pF.
- **Output cables placement:** Keep output speaker terminals/cables on the opposite side of the PCB from PVDD for EMI reasons. Radiated emission from the output switching waveform can couple from the output cables to the PVDD traces/cables and influence conducted emission performance significantly.

12.7 Evaluation Board as Reference

The EVAL_AUDIO_MA2304PNS evaluation board can be used as reference when designing an application. The evaluation board layout has specifically been optimized to achieve best possible thermal performance without an external heatsink. Refer to Figures 12.2 through 12.7 and/or refer to design files on infineon.com

Figure 12.2: Evaluation board top side

Figure 12.3: Evaluation board bottom side

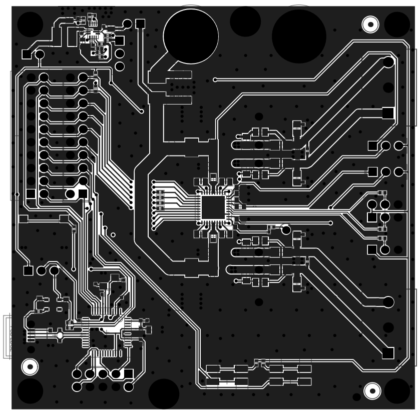


Figure 12.4: Top Layer

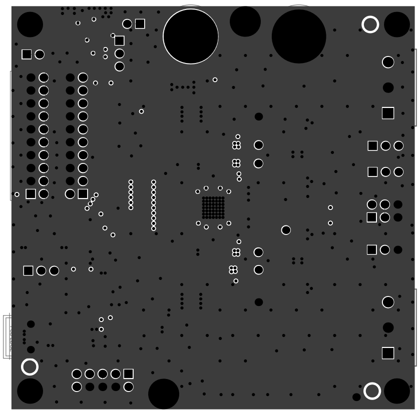


Figure 12.5: Mid Layer 1

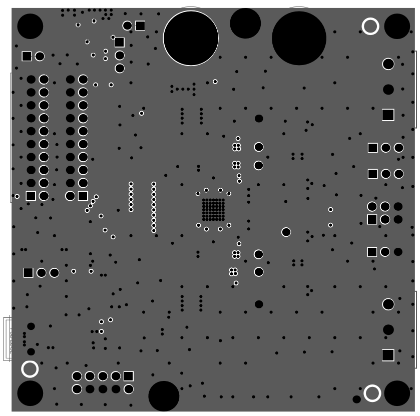


Figure 12.6: Mid Layer 2

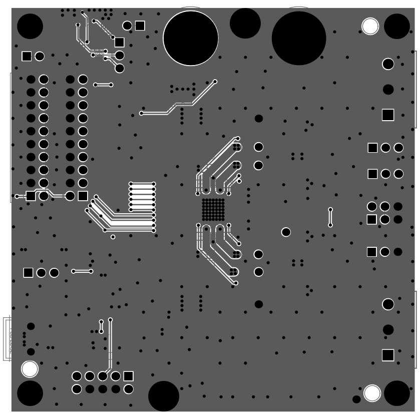


Figure 12.7: Bottom Layer

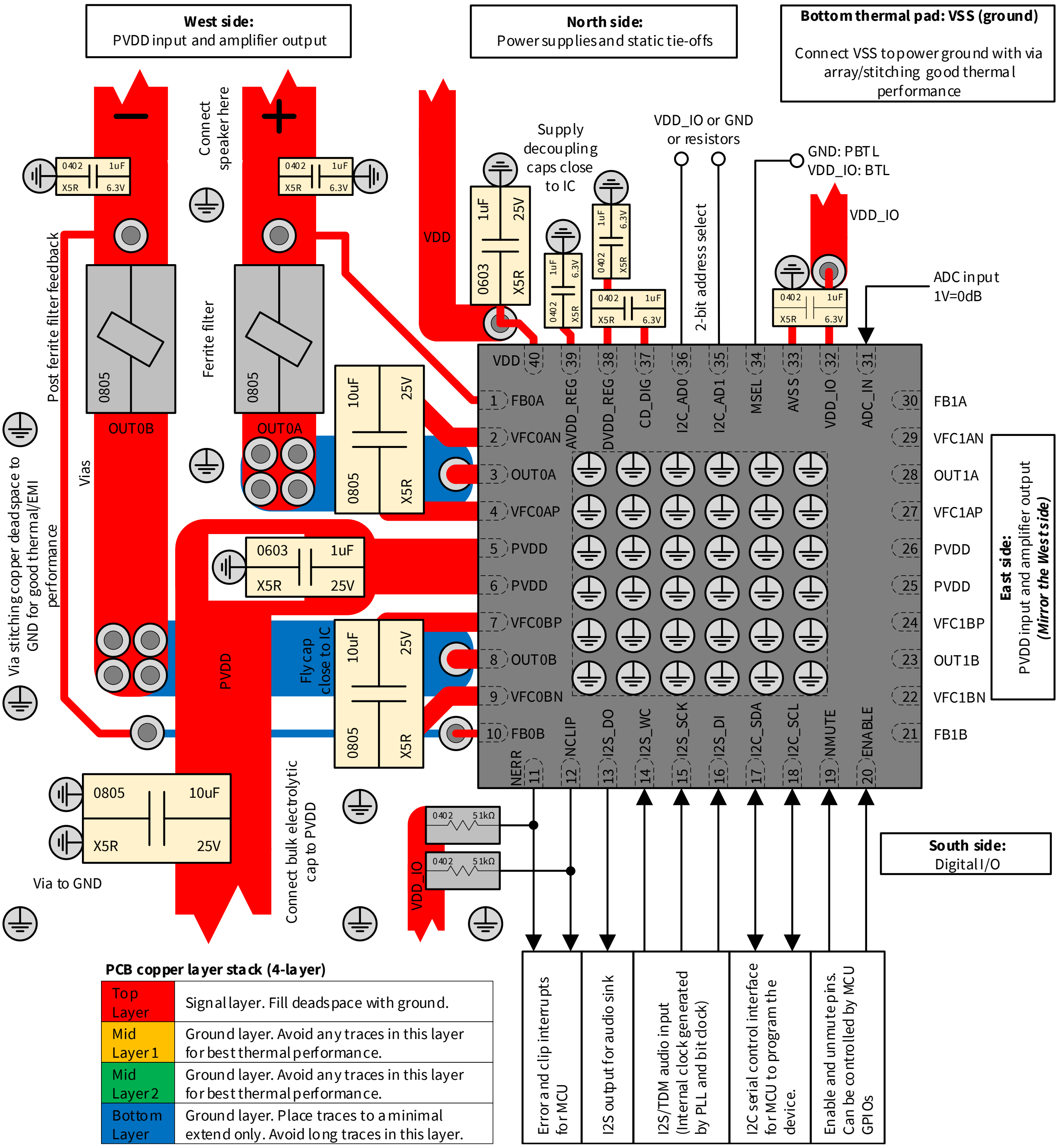


Figure 12.8: Recommended application/PCB layout for best performance

13 Typical Characteristics

Note that some characteristics are based on interpolated/averaged data.

13.1 Efficiency and power consumption

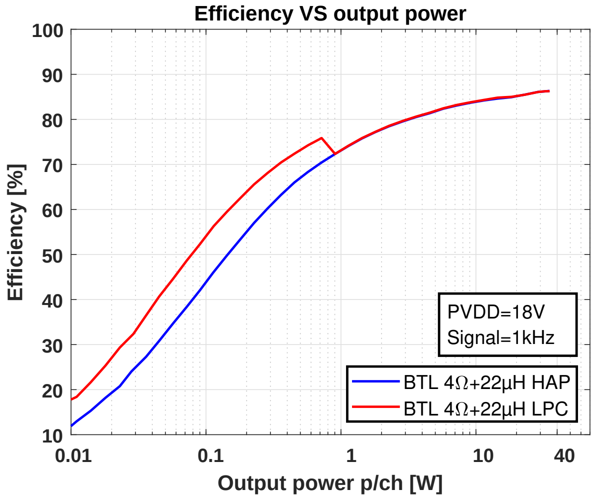


Figure 13.1

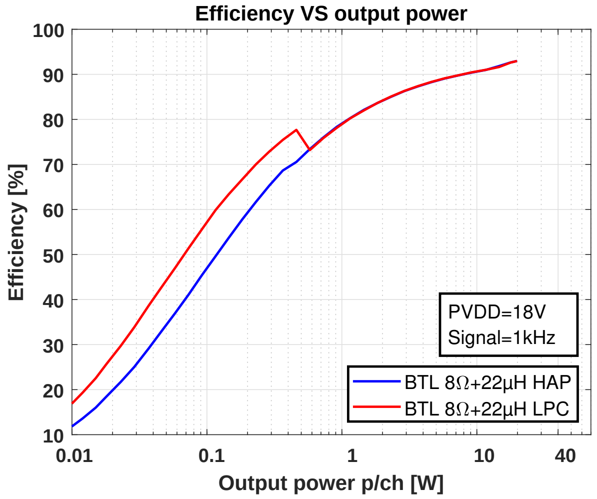


Figure 13.2

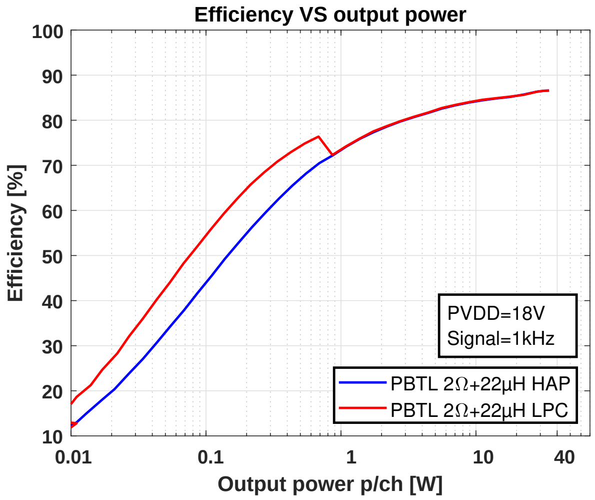


Figure 13.3

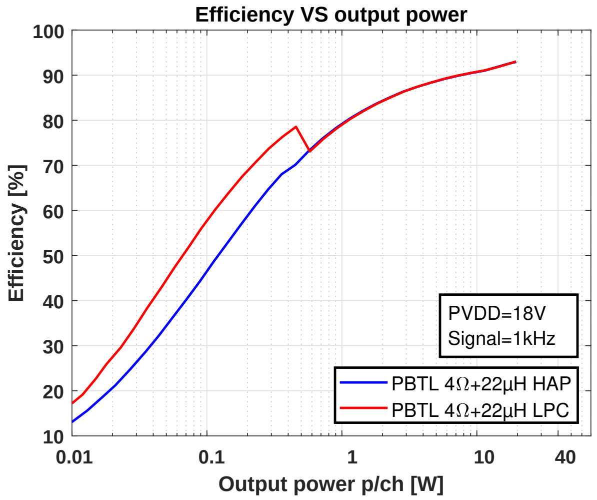


Figure 13.4

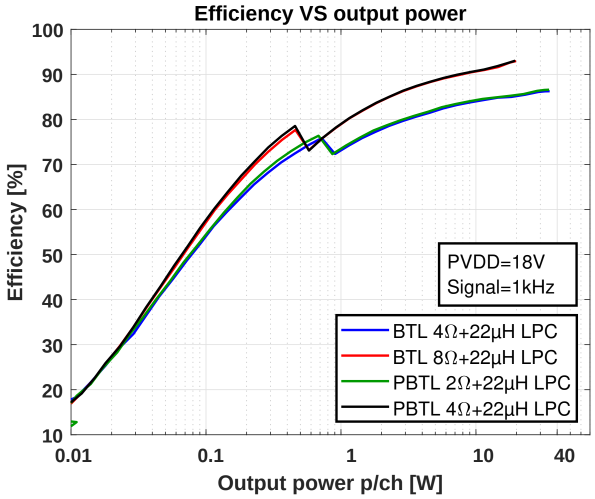


Figure 13.5

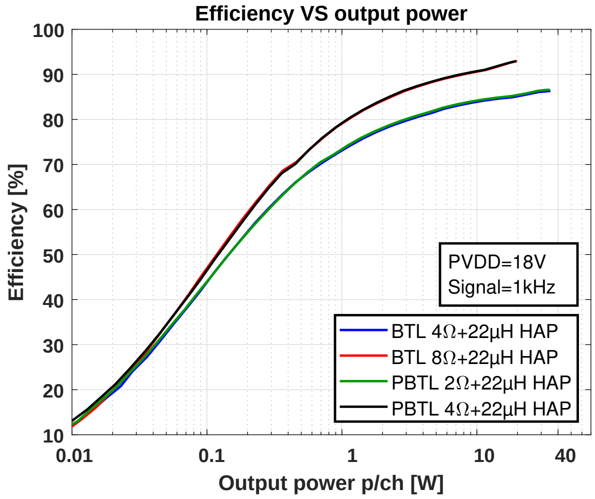


Figure 13.6

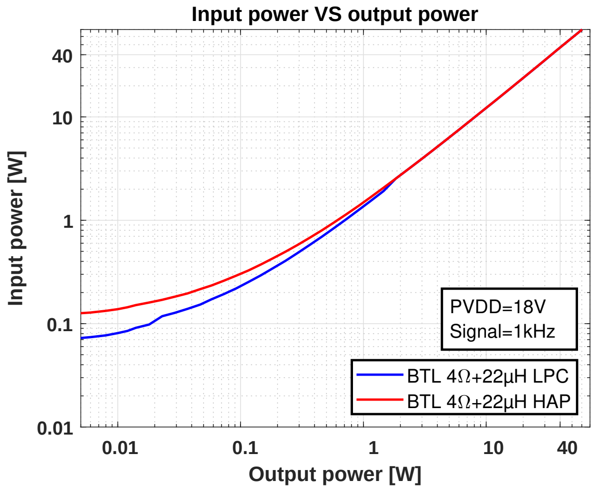


Figure 13.7

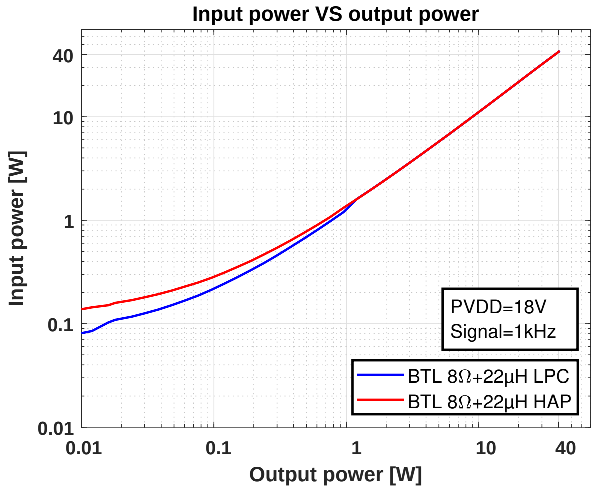


Figure 13.8

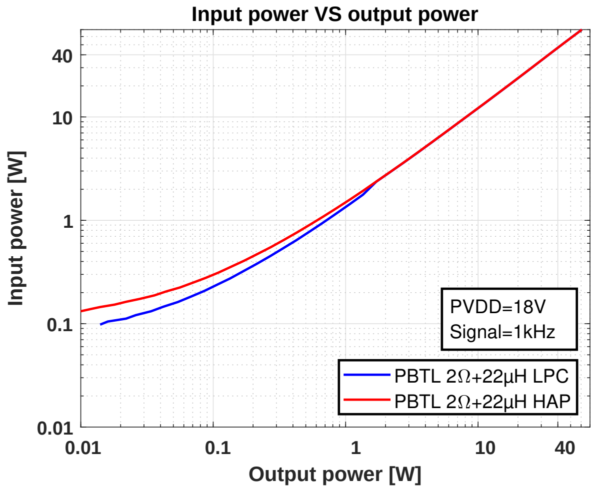


Figure 13.9

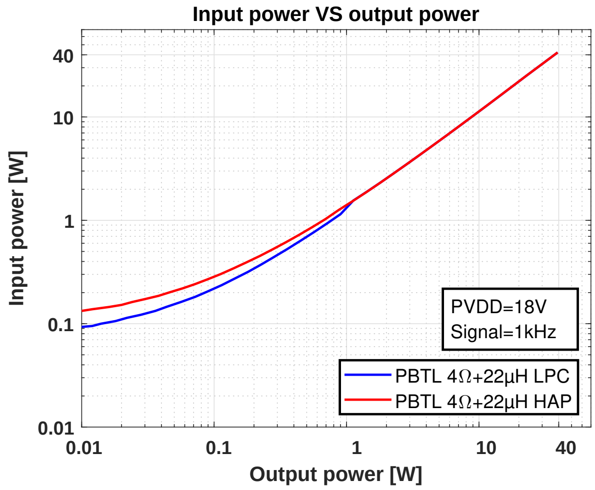


Figure 13.10

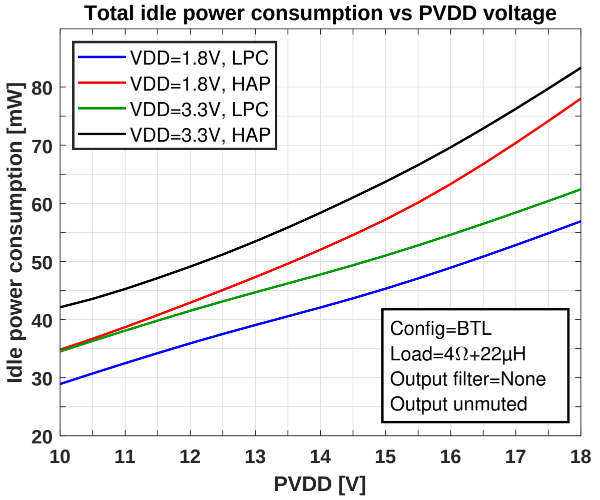

Total idle power consumption vs PVDD voltage
VDD=1.8V, LPC
VDD=1.8V, HAP
VDD=3.3V, LPC
VDD=3.3V, HAP
Config=BTL
Load=4Ω+22µH
Output filter=None
Output unmuted
Idle power consumption [mW]
PVDD [V]
20
30
40
50
60
70
80
10
11
12
13
14
15
16
17
18

Figure 13.11

13.2 Thermal performance

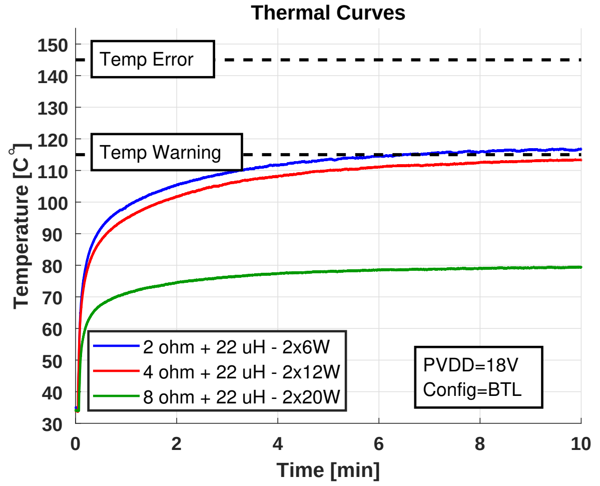


Figure 13.12

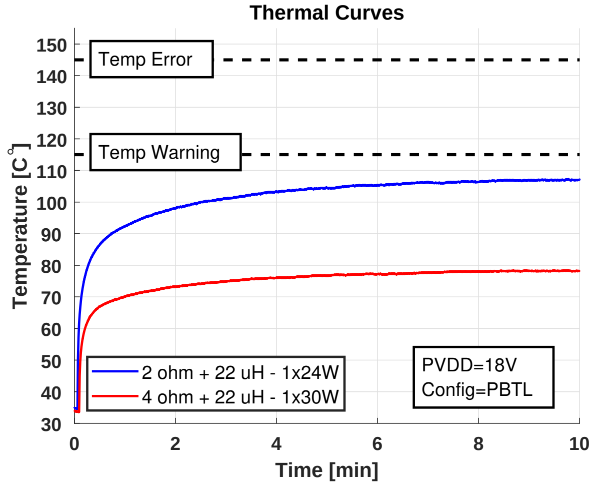


Figure 13.13

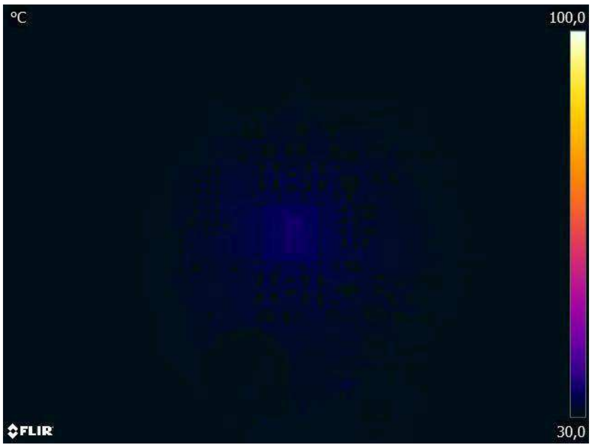


Figure 13.14: Thermal photo of EVAL_AUDIO_MA2304PNS at 2x1 W, 4 Ω

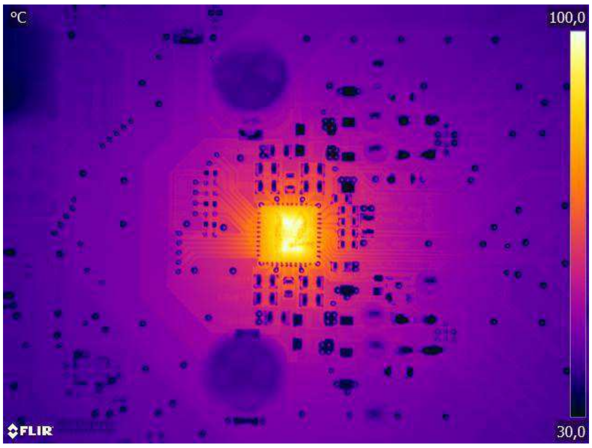


Figure 13.15: Thermal photo of EVAL_AUDIO_MA2304PNS EVK at 2x12 W, 4 Ω

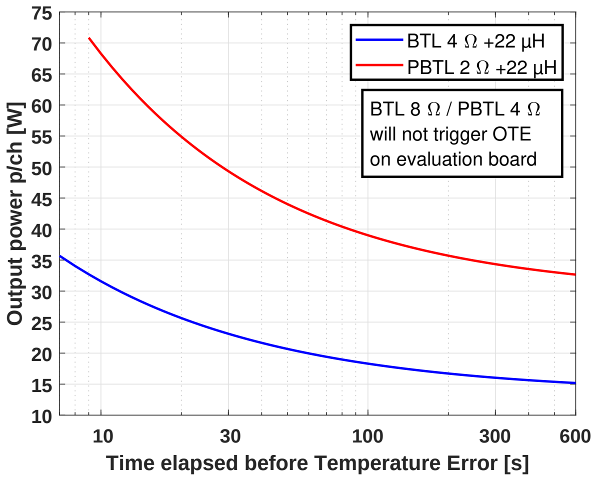


Figure 13.16

13.3 Audio performance

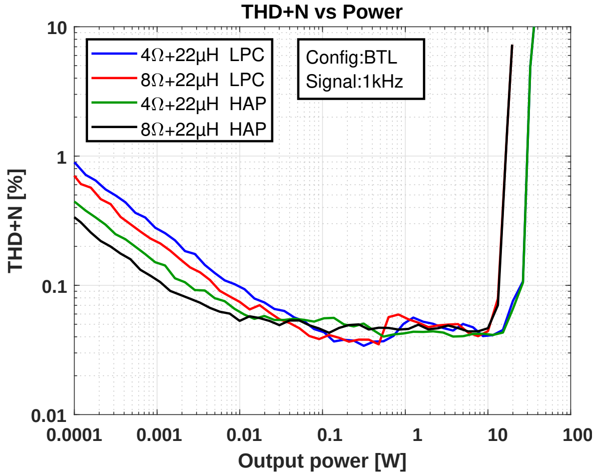


Figure 13.17

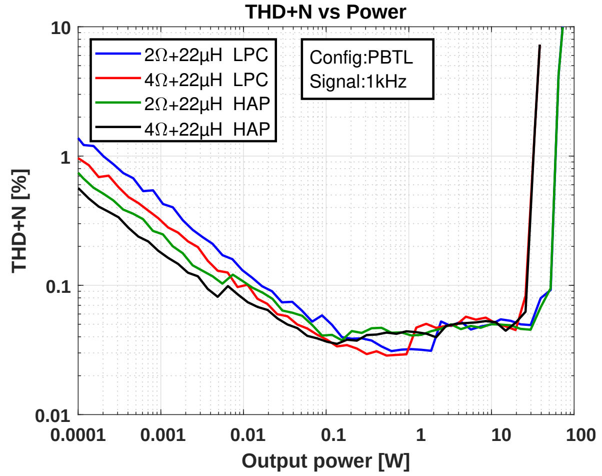


Figure 13.18

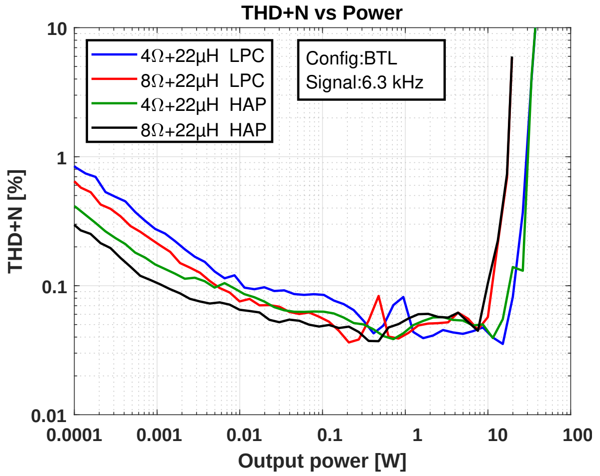


Figure 13.19

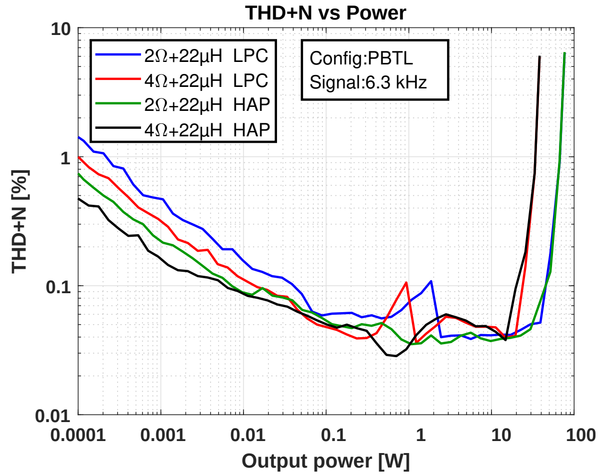


Figure 13.20

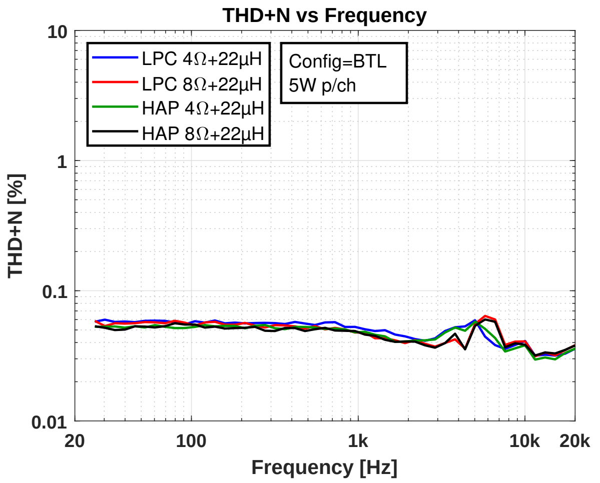


Figure 13.21

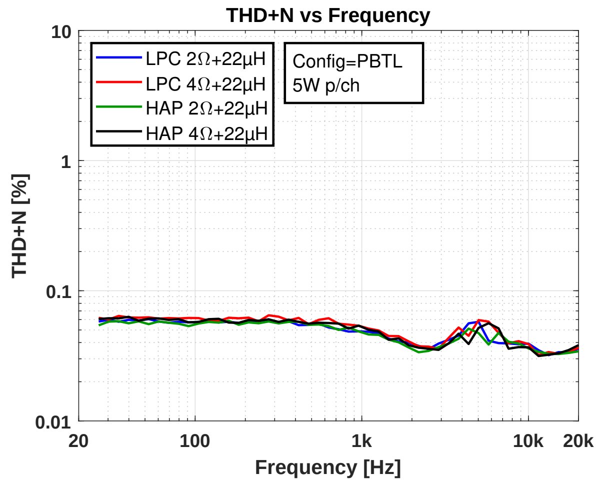


Figure 13.22

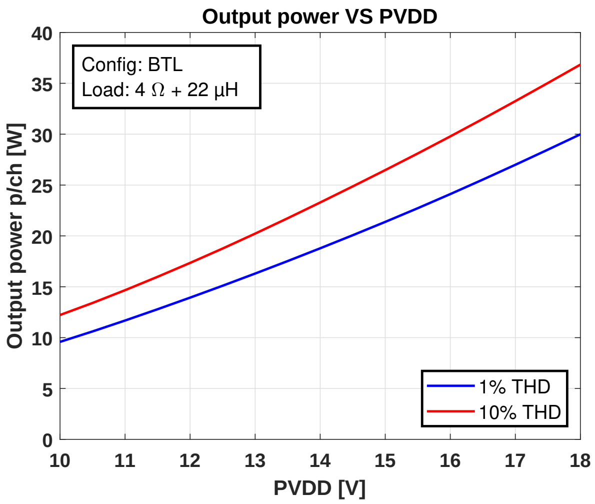


Figure 13.23

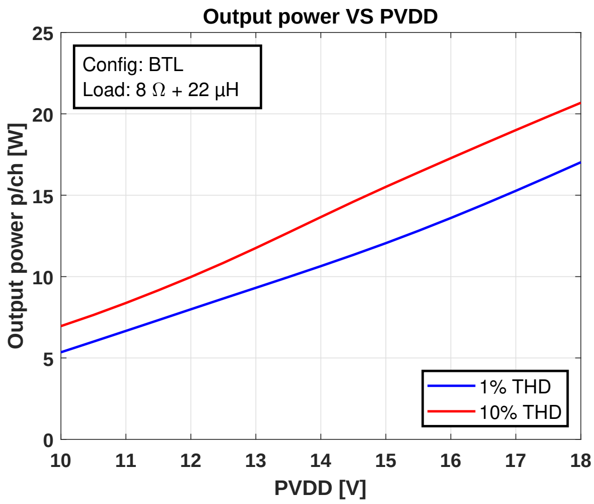


Figure 13.24

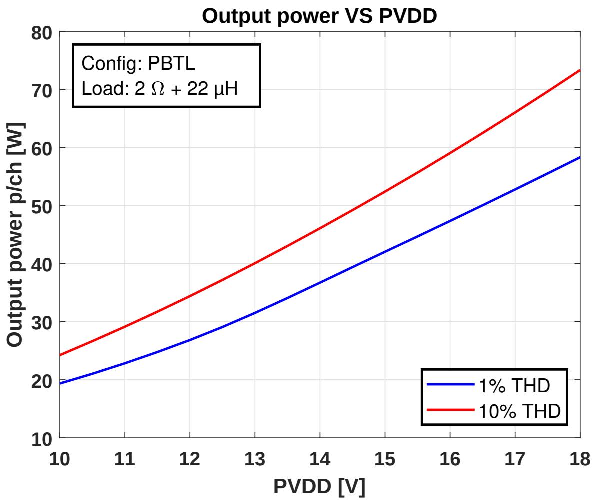


Figure 13.25

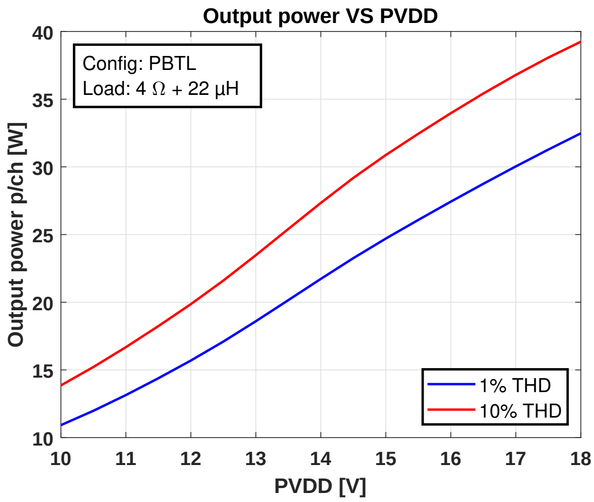


Figure 13.26

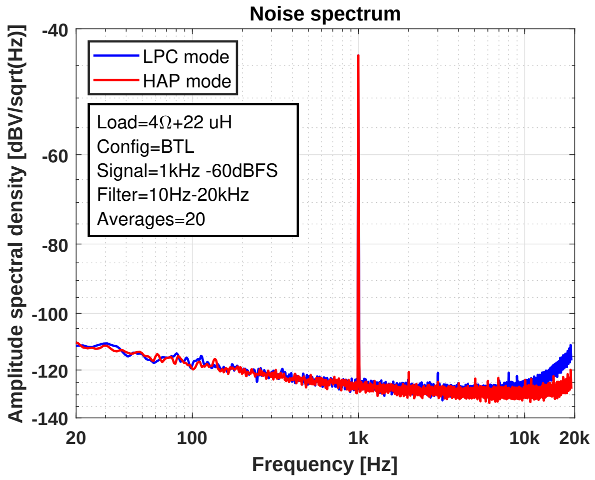


Figure 13.27

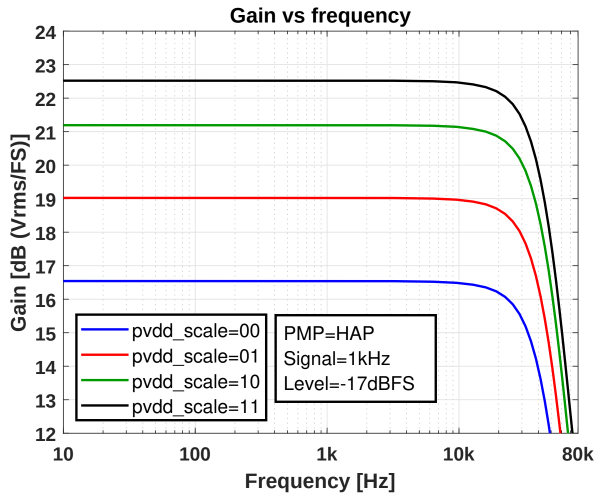


Figure 13.28

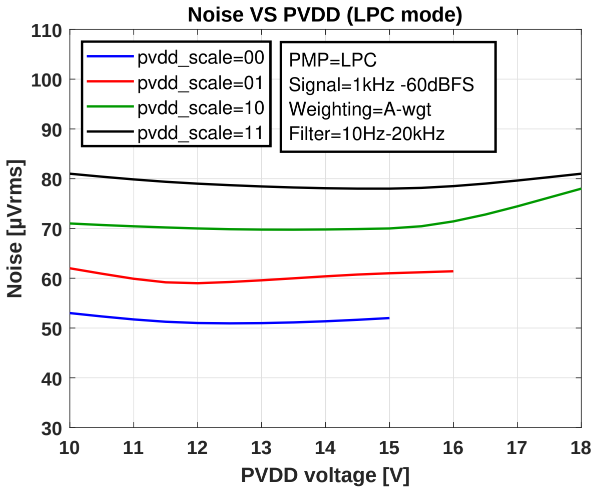


Figure 13.29

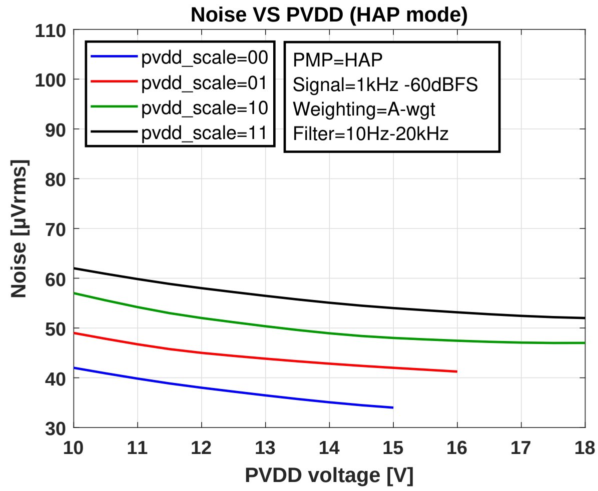


Figure 13.30

14 Register map

Legend:
Red: Bits in the register which correspond to the specific Name/Function.

pa					
Address	Reset	Name/Function	Bits	Value	Description
0x0000	0x32	PMP_select	2:0	00110010	Power Mode Profile selection 010: LPC mode 100: HAP mode
		mode_pbtl	3	00110010	Output channel configuration 0: BTL mode 1: PBTL mode
		pvdd_scale	5:4	00110010	Gain scaling. 00: Optimized for PVDD=10V 01: Optimized for PVDD=12V 10: Optimized for PVDD=15V 11: Optimized for PVDD=18V
		TBD_reg_ctrl	6	00110010	Override pin/hardware programmed settings with register stettings 0: Hardware settings are chosen 1: Register settings are chosen
0x0001	0x03	gd_dVdt	1:0	00000011	Gate drive strength (dV/dt) 00: Lowest 01: Low 10: High 11: Highest
0x0002	0x00	mute_ch0	0	00000000	Mute channel 0 (mute_source must be set first) 0: Unmute 1: Mute
		mute_ch1	1	00000000	Mute channel 1 (mute_source must be set first) 0: Unmute 1: Mute
		disable_ch0	2	00000000	0: Channel 0 is enabled 1: Channel 0 is disabled
		disable_ch1	3	00000000	0: Channel 1 is enabled 1: Channel 1 is disabled
		standby	4	00000000	0: Disable standby 1: Enable standby
		mute_source	5	00000000	Select source for the internal mute signal 0: NMUTE pin 1: mute_ch0/1 register settings
0x0003	0x20	volume_ch0	7:0	00100000	Channel 0 volume setting. Step size: -0.75 dB per register value increment. 0x00: +24 dB 0x01: +23.25 dB .. 0x1F: +0.75 dB 0x20: +0.00 dB (default) 0x21: -0.75 dB .. 0xFF: -167.25 dB
0x0004	0x20	volume_ch1	7:0	00100000	Channel 1 volume setting. See volume_ch0 for more information.
0x0005	0x00	dsp_enable	1	00000000	Enable digital audio processor (DSP) 0: DSP disabled 1: DSP enabled

		dsp_bypass	3	00000000	Audio routing bypasses DSP 0: Audio is routed through DSP 1: Audio is routed directly to amplifier
		vol_instant	0	00000000	Volume control ramp disable 0: Volume is ramped 1: Volume is applied instantly - no ramp
		gpio_sync_zclip	4	00000000	NCLIP pin function select 0: NCLIP is output pin indicating amp clipping 1: NCLIP pin is used for inter-IC PWM synchronization (use sync_in_enable and sync_out_enable registers to select if NCLIP is input/output)
0x0006	0x00	clip_pin	0	00000000	State of the clip signal driving the NCLIP pin (read-only) 0: No clipping 1: Clipping
		err_pin	1	00000000	State of the error signal driving the NERR pin 0: No error 1: Error
0x0007	0x00	adc_pin	7:0	00000000	ADC reading from ADC_IN pin spanning between 0 V (min) and 1 V (max)
0x0008	0x00	temp_chip	7:0	00000000	Read internal temperature sensor. Resolution is 1 °C per increment with 0x00=-50 °C
0x0009	0x00	pvdd_chip	7:0	00000000	Read internal PVDD sensor. Resolution is 125 mV per increment
0x000B	0x00	attack_ch1	4:0	00000000	Channel 1 attack time for peak limiter (ROM code). Sample rate dependent. At 48 kHz: 0x00: 0 ms/10 dB (default) 0x08: 1 ms/10 dB 0x09: 2 ms/10 dB 0x0A: 4 ms/10 dB 0x0B: 8 ms/10 dB 0x0C: 16 ms/10 dB 0x0D: 32 ms/10 dB 0x0E: 64 ms/10 dB 0x0F: 128 ms/10 dB
0x000A	0x00	attack_ch0	4:0	00000000	Channel 0 attack time for peak limiter (ROM code). See attack_ch0 for more information.
0x000C	0x12	release_ch0	4:0	00010010	Channel 0 release time for peak limiter (ROM code). Sample rate dependent. At 48 kHz: 0x0C: 16 ms/10 dB 0x0D: 32 ms/10 dB 0x0E: 64 ms/10 dB 0x0F: 128 ms/10 dB 0x10: 256 ms/10 dB 0x11: 512 ms/10 dB 0x12: 1024 ms/10 dB (default) 0x13: 2048 ms/10 dB
0x000D	0x12	release_ch1	4:0	00010010	Channel 1 release time for peak limiter (ROM code). See release_ch0 for more information.

0x000E	0x00	threshold_ch0	7:0	00000000	Channel 0 threshold for peak limiter (ROM code). Step size: -0.75 dB per register value increment. 0x00: +24 dB 0x01: +23.25 dB .. 0x1F: +0.75 dB 0x20: +0.00 dB (default) 0x21: -0.75 dB .. 0xFF: -167.25 dB
0x000F	0x00	threshold_ch1	7:0	00000000	Channel 1 threshold for peak limiter (ROM code). See threshold_ch0 for more information.

i2s_tdm

Address	Reset	Name/Function	Bits	Value	Description
0x0010	0x10	data_alignment	1:0	00010000	I2S/TDM data alignment 00: I2S 01: Left Justified 10: Right Justified
		sck_pol	4	00010000	I2S/TDM clock polarity 0: Data changes on rising edge of SCK 1: Data changes on falling edge of SCK
		slot_size	6:5	00010000	I2S/TDM channel slot size (frame width) 00: 32 bit 01: 24 bit 10: 16 bit
		ws_fs_rising	7	00010000	I2S/TDM word/frame clock polarity 0: Word/frame starts at falling edge 1: Frame starts at rising edge
		data_size	3:2	00010000	Data size / bit depth 00: 24 bit 01: 20 bit 10: 18 bit 11: 16 bit
0x0011	0x00	lsb_first	0	00000000	I2S/TDM word order 0: MSB is transmitted first 1: LSB is transmitted first
0x0012	0x00	tdm_input_map0	4:0	00000000	Select channel (0-16) in received I2S/TDM stream to pass on to DSP/amp channel 0. 00000: Channel 0 00001: Channel 1 .. 01110: Channel 14 01111: Channel 15
0x0013	0x01	tdm_input_map1	4:0	00000001	Select channel (0-16) in received I2S/TDM stream to pass on to DSP/amp channel 1. See tdm_input_map0 register description for more information.
0x0016	0x1A	tdm_output_map0	2:0	00011010	Audio channel transmitted to I2S_DO pin in slot 0 of I2S/TDM stream. 000: Zero 001: High-Z 010: DSP output channel 0 011: DSP output channel 1
		tdm_output_map1	5:3	00011010	Audio channel transmitted to I2S_DO pin in slot 1 of I2S/TDM stream. Setup is similar to tdm_output_map0.

0x0017	0x00	tdm_output_map2	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 2 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map3	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 3 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0018	0x00	tdm_output_map4	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 4 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map5	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 5 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0019	0x00	tdm_output_map6	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 6 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map7	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 7 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001A	0x00	tdm_output_map8	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 8 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map9	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 9 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001B	0x00	tdm_output_map10	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 10 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map11	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 11 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001C	0x00	tdm_output_map12	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 12 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map13	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 13 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x001D	0x00	tdm_output_map14	2:0	00000000	Audio channel transmitted to I2S_DO pin in slot 14 of I2S/TDM stream. Setup is similar to tdm_output_map0.
		tdm_output_map15	5:3	00000000	Audio channel transmitted to I2S_DO pin in slot 15 of I2S/TDM stream. Setup is similar to tdm_output_map0.
0x0026	0x0A	tx_loopback	0	00001010	Selects if transmitted audio data should be a copy of the received data. 0: I2S_DO is configured by tdm_output_map 1: I2S_DO is a copy of I2S_DI
		tx_enable	2	00001010	I2S/TDM transmitter enable 0: Disabled 1: Enabled
		rx_enable	1	00001010	I2S/TDM receiver enable (necessary to play audio) 0: Disabled 1: Enabled
		tx_strong_drive	3	00001010	Drive strength for I2S_DO pin 0: Normal 1: Strong

0x0027	0x04	sync_in_enable	0	00000100	Configure NCLIP pin as input for PWM synchronization 0: Disable 1: Enable
		sync_out_enable	1	00000100	Configure NCLIP pin as output (open-drain) for PWM synchronization. 0: Disable 1: Enable
		fast_sync	2	00000100	Select frequency of the PWM synchronization signal 0: Slow (fs/12288) 1: Fast (fs/12)
			pmc		
Address	Reset	Name/Function	Bits	Value	Description
0x00BD	0x00	PM_ch0	2:0	00000000	Current selected Power Mode for channel 0
		PM_ch1	5:3	00000000	Current selected Power Mode for channel 1
0x00BE	0x00	Mdetector_ch0	7:0	00000000	Channel 0 modulation index M detector output. If register value is 0, modulation index is 0.0 (minimum). If register value is 255, modulation index is 1.0 (full modulation)
0x00BF	0x00	Mdetector_ch1	7:0	00000000	Channel 1 modulation index M detector output. If register value is 0, modulation index is 0.0 (minimum). If register value is 255, modulation index is 1.0 (full modulation)
			prot_sys		
Address	Reset	Name/Function	Bits	Value	Description
0x0109	0x00	reg.errTrig_reset	1	00000000	Error register reset 0: Do not reset error trigger 1: Reset error trigger
0x011A	0x00	errVect_now.errVector_all__0	7:0	00000000	Instantaneous error vector 0. Bit 7: Low temperature warning Bit 6: I2S input error Bit 5: PLL not locked Bit 4: PVDD over-voltage Bit 3: Reserved Bit 2: PVDD under-voltage Bit 1: Over-temperature error Bit 0: Over-temperature warning
0x011C	0x00	errVect_acc.errVector_ch0	4:0	00000000	Accumulated channel 0 error vector. Bit 4: Reserved Bit 3: DC error Bit 2: Flying cap error Bit 1: Reserved Bit 0: Over-current protection
0x011D	0x00	errVect_acc.errVector_ch1	4:0	00000000	Accumulated channel 1 error vector. See description for errVect_acc.errVector_ch0
0x011E	0x00	errVect_acc.errVector_all__0	7:0	00000000	Accumulated error vector 0. Bit 7: Low temperature warning Bit 6: I2S input error Bit 5: PLL not locked Bit 4: PVDD over-voltage Bit 3: Reserved Bit 2: PVDD under-voltage Bit 1: Over-temperature error Bit 0: Over-temperature warning
			pa_hw		
Address	Reset	Name/Function	Bits	Value	Description

0x0142	0x03	otp.unmute_cnt	3:0	00000011	Unmute time delay from NMUTE=high to audio playback. 0011: 300 ms 1101: 30 ms (default)
0x015F	0x00	reg.pwm_phase	6:0	00000000	Time/phase delay of PWM signal in 22.5 degree increments. Used with PWM sync to change relative PWM phase of synchronized devices. 0000000: 0 deg 0000001: +22.5 deg ... 0001111: +337.5 deg 0010000: +360 deg (equivalent to 0 deg)

15 Package Information

Dimensions are in millimeter unless otherwise specified.

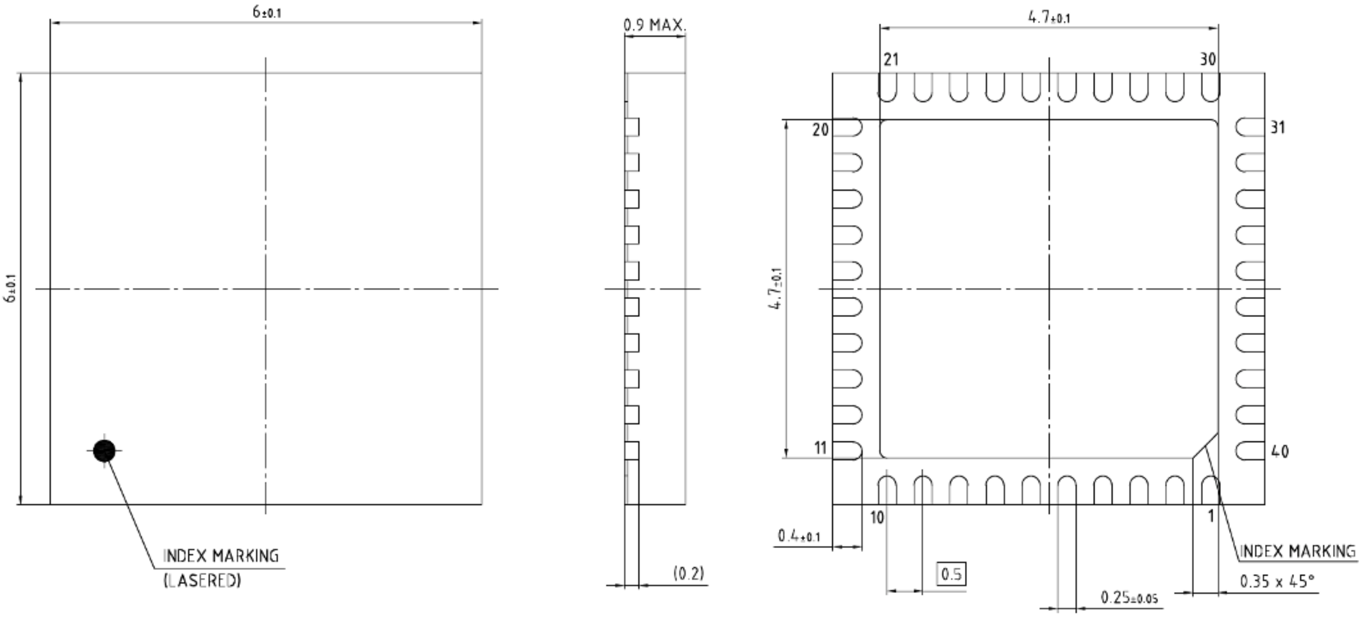


Figure 15.1: QFN pad-down 40-pin MA2304PNS package dimensions. Left: Top view. Middle: Side view. Right: Bottom view.

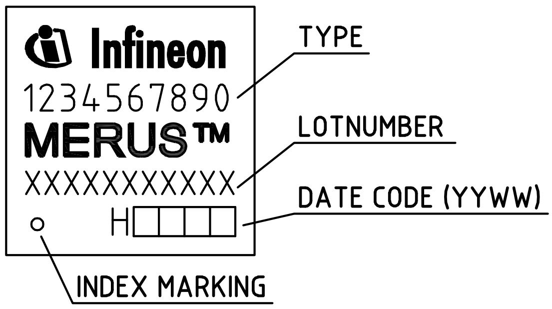


Figure 15.2: Package marking

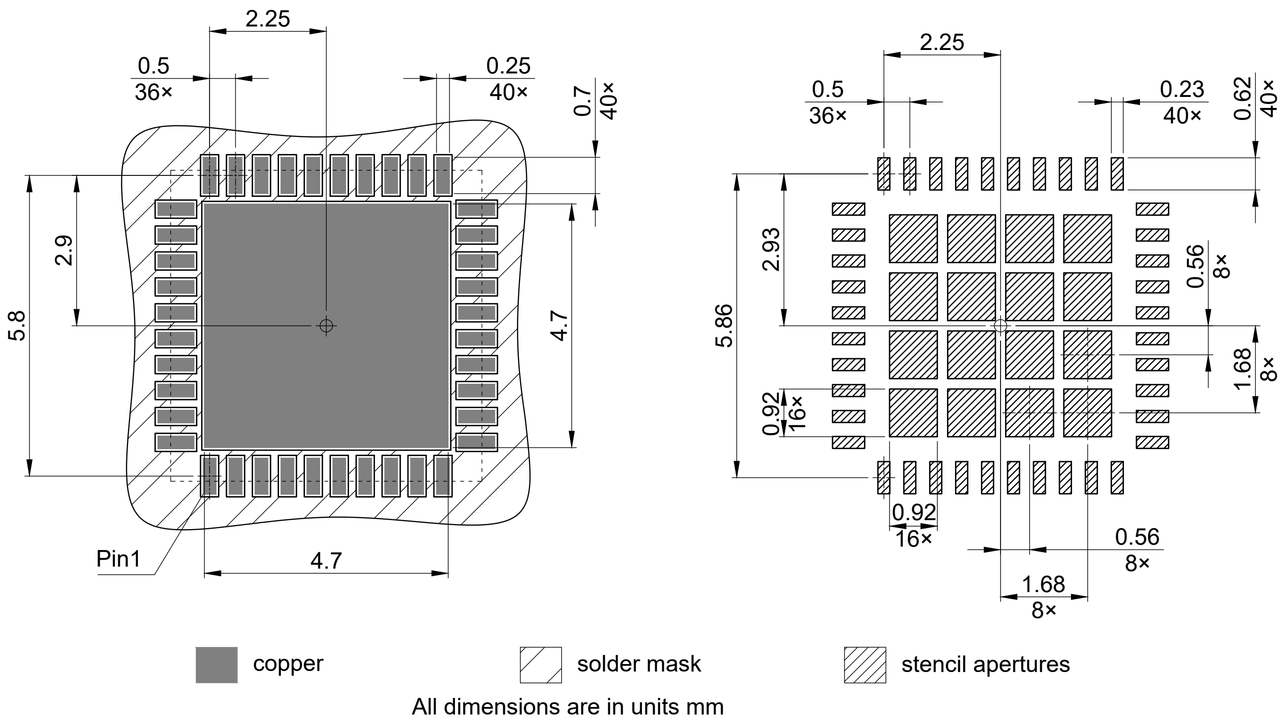
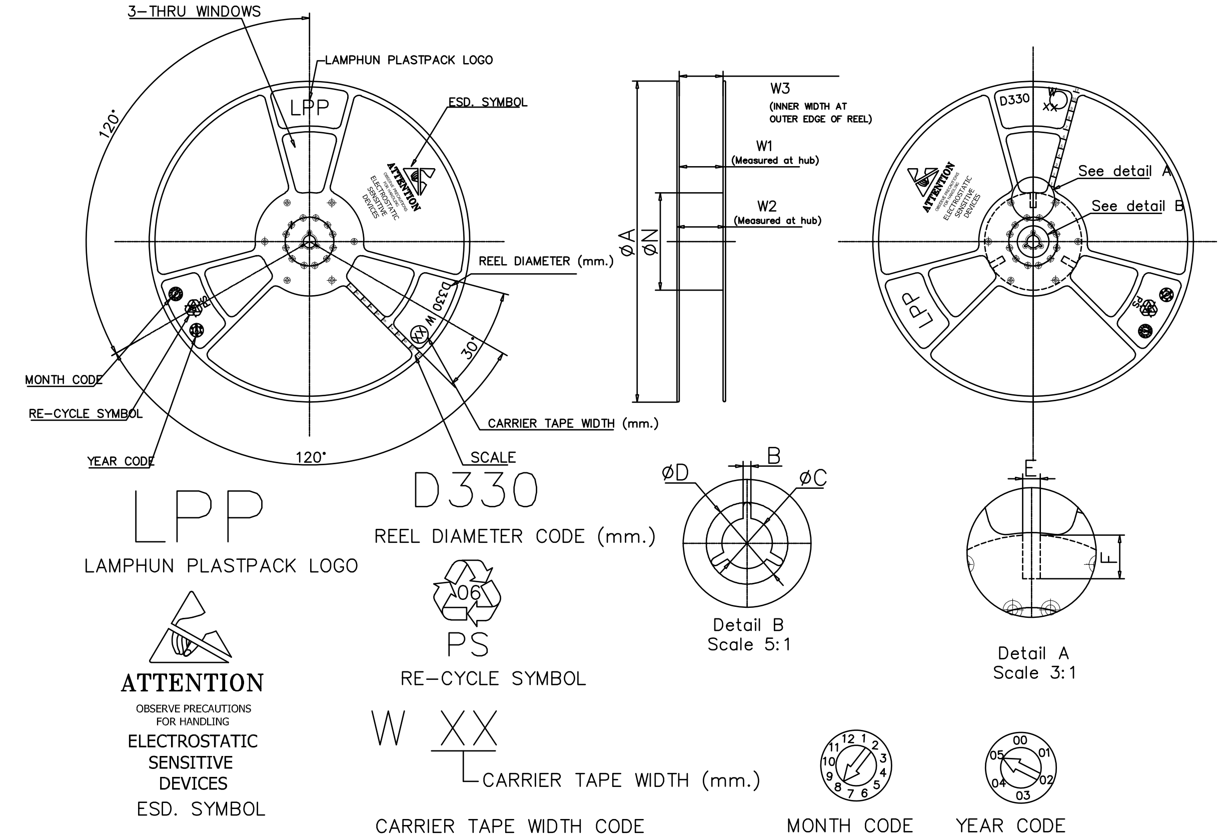


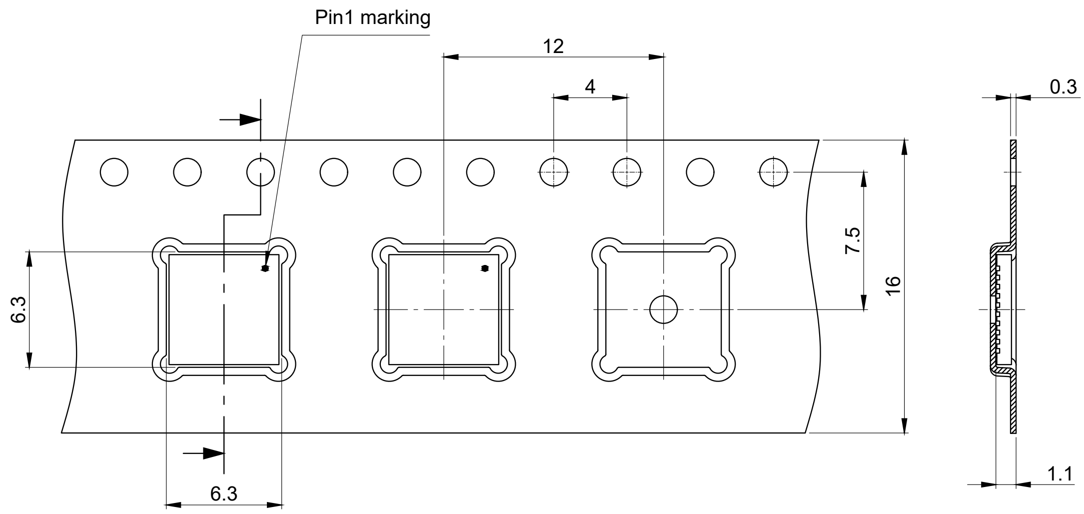
Figure 15.3: Recommended land pattern

16 Tape and Reel Information



PART NO.	CARRIER TAPE WIDTH	ØA (±2)	B (Min.)	ØC ($^{+0.50}_{-0.20}$)	ØD (Min.)	E (Min.)	Min.)	ØN (±2)	T (Min)	W1 ($^{+2.00}_{-0.00}$)	W2 (Max.)	W3 Min.	W3 Max
R13-16-04-E	16	330	1.50	13.00	20.20	2.50	10	100	2.40	16.40	22.40	16.35	19.40

Figure 16.1: Tape reel information



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 16.2: Carrier tape information

Revision History

MA2304PNS

Revision: 2022-08-23, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-07-06	Release of final version
2.1	2022-07-18	Add filter condition on electrical characteristics
2.2	2022-08-23	Add continuous output power data at 8 ohm load

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.