Integrated Circuit Systems, Inc.

ICS889831

LOW SKEW, 1-TO-4 DIFFERENTIAL LVPECL-TO-LVPECL/ECL FANOUT BUFFER

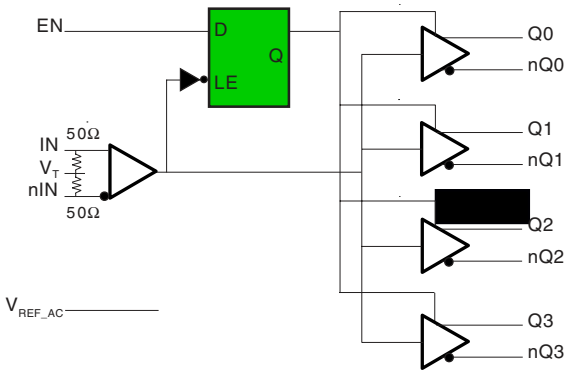
GENERAL DESCRIPTION

The ICS889831 is a high speed 1-to-4 Differential-to-LVPECL/ECL Fanout Buffer and is a member of the HiPerClockS™family of high performance clock solutions from ICS. The ICS889831 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin which may be useful for system test and debug purposes. The ICS889831 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

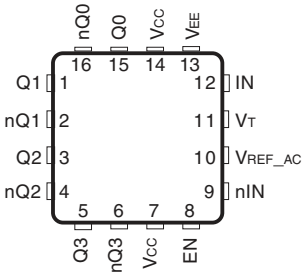
FEATURES

- 4 differential LVPECL/ECL outputs
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- 50Ω internal input termination to V_T
- Maximum output frequency: > 2.1GHz
- Output skew: 30ps (maximum)
- Part-to-part skew: 185ps (maximum)
- Additive phase jitter, RMS: 0.27ps (typical)
- Propagation delay: 570ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.5V ± 5%, 3.3V ± 5%, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.3V ± 5%, 2.5V ± 5%
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS889831
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q1, nQ1	Output		Differential output pair. LVPECL / ECL interface levels.
3, 4	Q2, nQ2	Output		Differential output pair. LVPECL / ECL interface levels.
5, 6	Q3, nQ3	Output		Differential output pair. LVPECL / ECL interface levels.
7, 14	V_{CC}	Power		Positive supply pins.
8	EN	Input	Pullup	Synchronizing clock enable. When LOW, Q outputs will go LOW and nQ outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V_{CC}/2V. Includes a 37kΩ pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal IN. LVTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential clock input. 50Ω internal input termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications.
11	V_T	Input		Termination input.
12	IN	Input		Non-inverting differential clock input. 50Ω internal input termination to V_T.
13	V_{EE}	Power		Negative supply pin.
15, 16	Q0, nQ0	Output		Differential output pair. LVPECL / ECL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Input	Outputs	
EN	**Q0:Q3**	**nQ0:nQ3**
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled

After EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

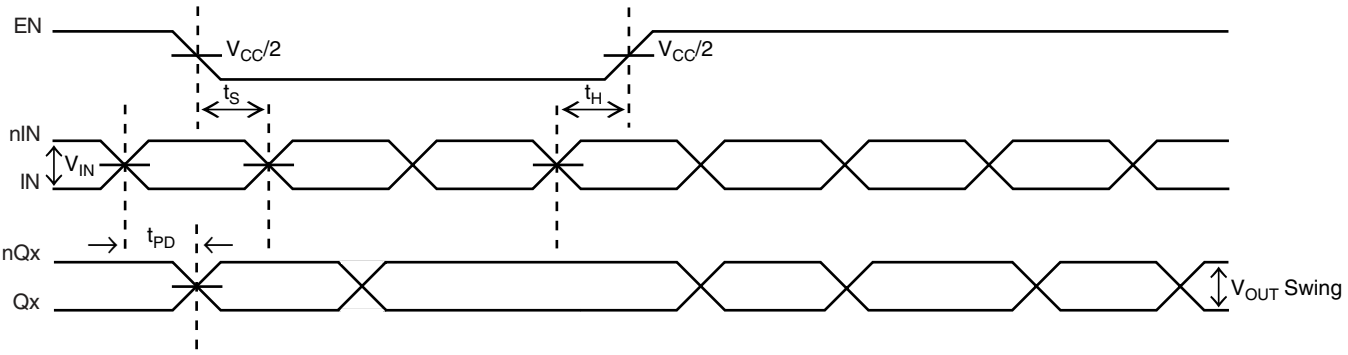


FIGURE 1. EN TIMING DIAGRAM

TABLE 3B. TRUTH TABLE

Inputs			Outputs	
IN	**nIN**	**EN**	**Q0:Q3**	**nQ0:nQ3**
0	1	1	0	1
1	0	1	1	0
X	X	0	0(1)	1(1)

NOTE 1: On next negative transition of the input signal (IN).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.5V ± 5%, 3.3V ± 5%; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				60	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 2.5V ± 5%, 3.3V ± 5%; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. DC CHARACTERISTICS, V_{CC} = 2.5V ± 5%, 3.3V ± 5%; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)	IN-to-VT	40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing			0.15		2.8	V
V_{REF_AC}	Reference Voltage			V_{CC} - 1.42	V_{CC} - 1.37	V_{CC} - 1.32	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		3.4	V
I_{IN}	Input Current; NOTE 1	(IN, nIN)				35	mA

NOTE 1: Guaranteed by design.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.465V; V_{EE} = 0V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.125	V_{CC} - 1.005	V_{CC} - 0.935	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 1.895	V_{CC} - 1.78	V_{CC} - 1.67	V
V_{OUT}	Output Voltage Swing		0.6		1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.2		2.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

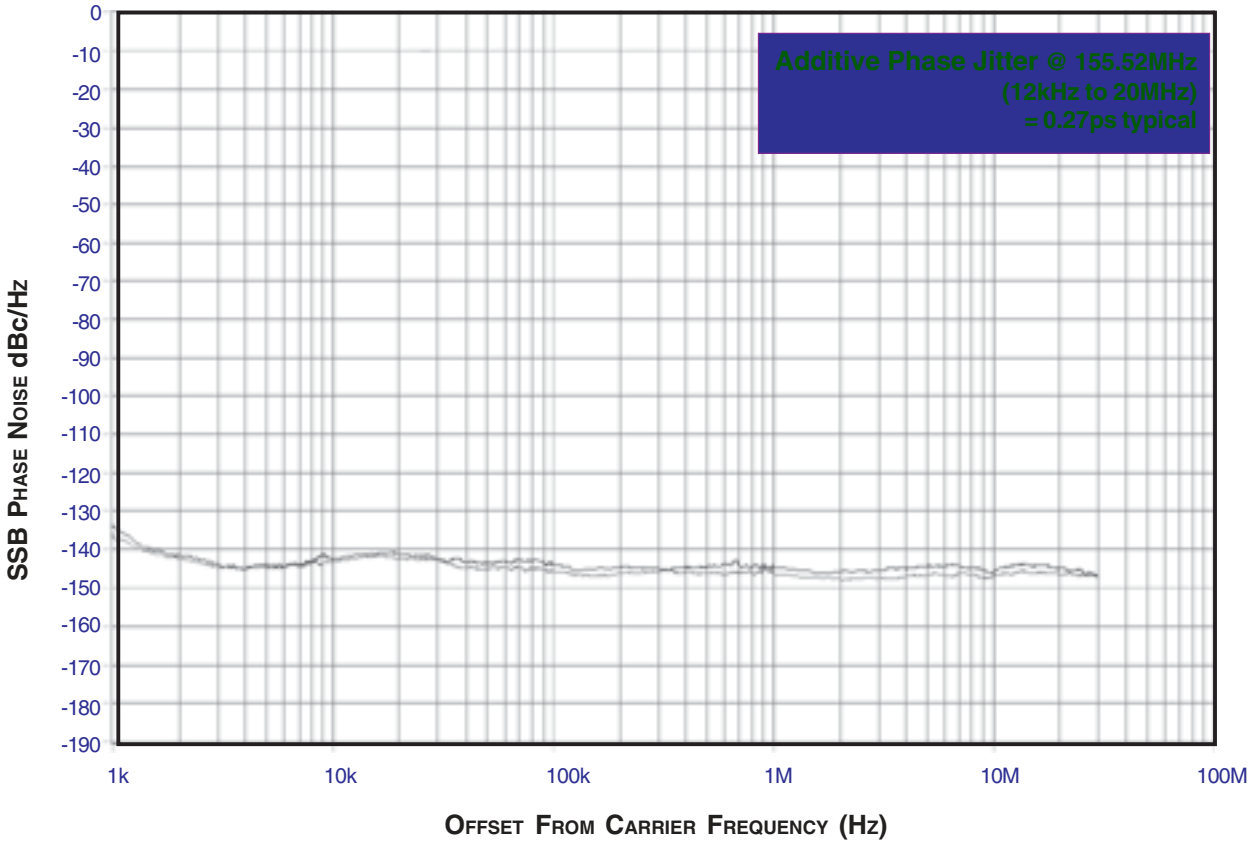
TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.3V ± 5%, -2.5V ± 5% OR V_{CC} = 2.5 ± 5%, 3.3V ± 5%; V_{EE} = 0V

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency		Output Swing ≥ 450mV	2.1			GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1		Input Swing: 100mV	300	435	570	ps
			Input Swing: 800mV	255	370	485	ps
*t*sk(o)	Output Skew; NOTE 2, 4					30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					185	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		155.52MHz, Integration Range: 12kHz - 20MHz		0.27		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	100		250	ps
t_S	Clock Enable Setup Time	EN to IN, nIN		300			ps
t_H	Clock Enable Hold Time	EN to IN, nIN		300			ps

All parameters characterized at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

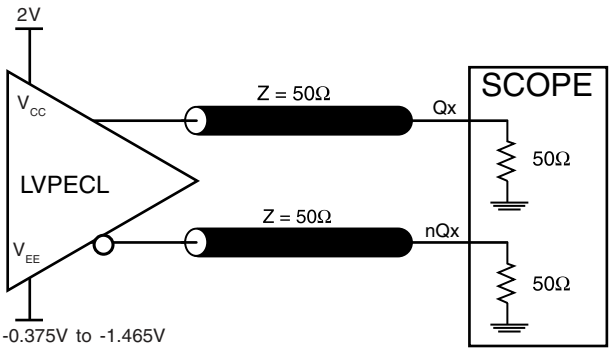
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

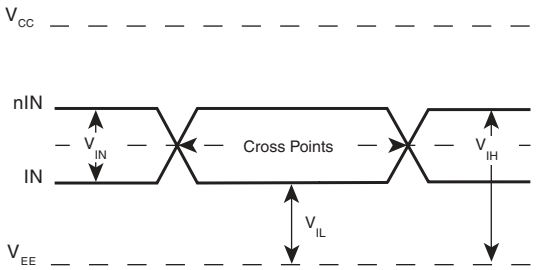


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

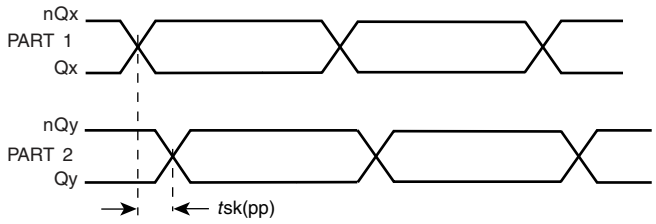
PARAMETER MEASUREMENT INFORMATION



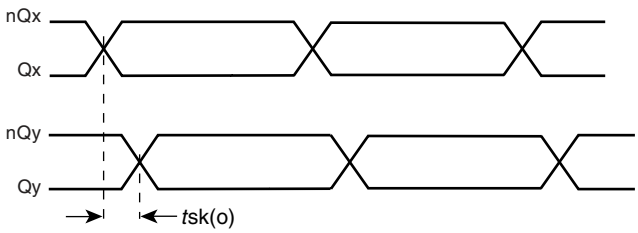
OUTPUT LOAD AC TEST CIRCUIT



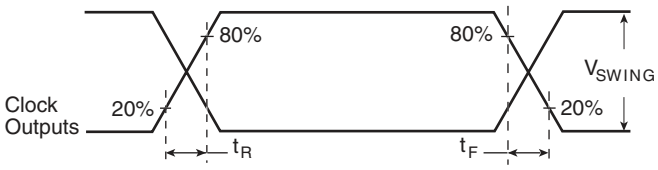
DIFFERENTIAL INPUT LEVEL



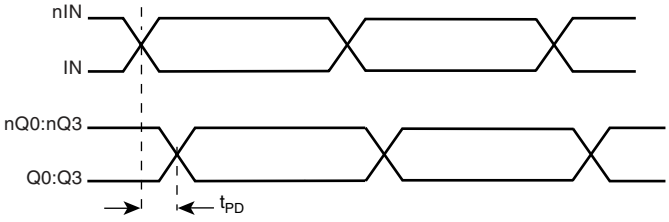
PART-TO-PART SKEW



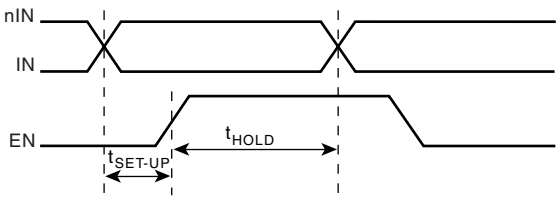
OUTPUT SKEW



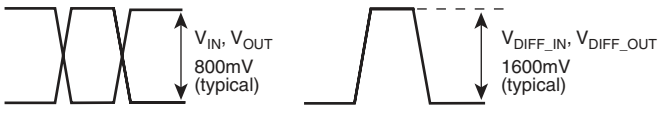
OUTPUT RISE/FALL TIME



PROPAGATION DELAY



SETUP & HOLD TIME



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING

APPLICATION INFORMATION

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

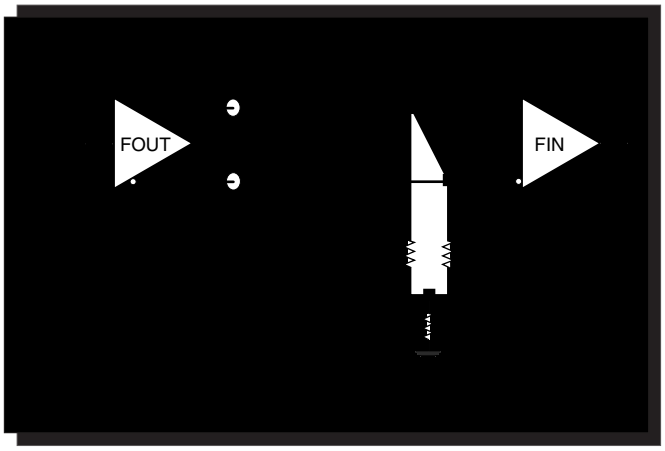


FIGURE 2A. LVPECL OUTPUT TERMINATION

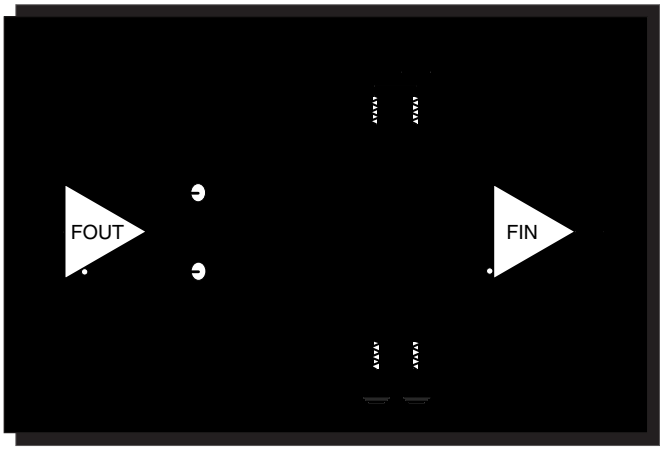


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

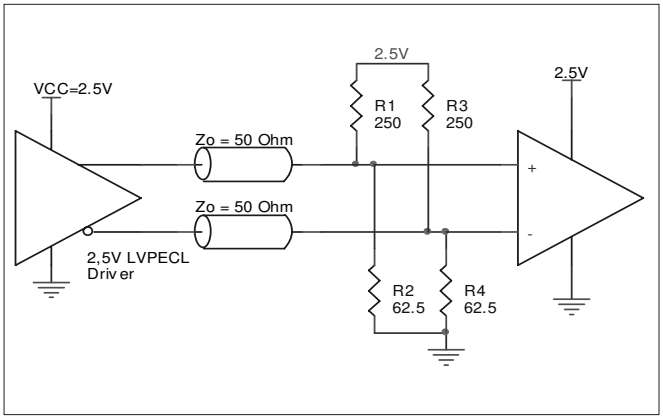


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

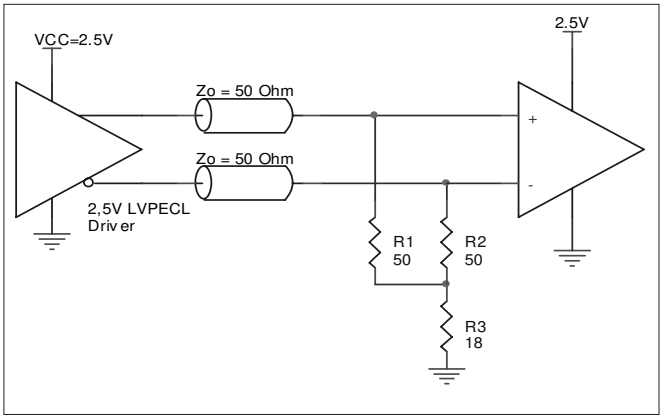


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

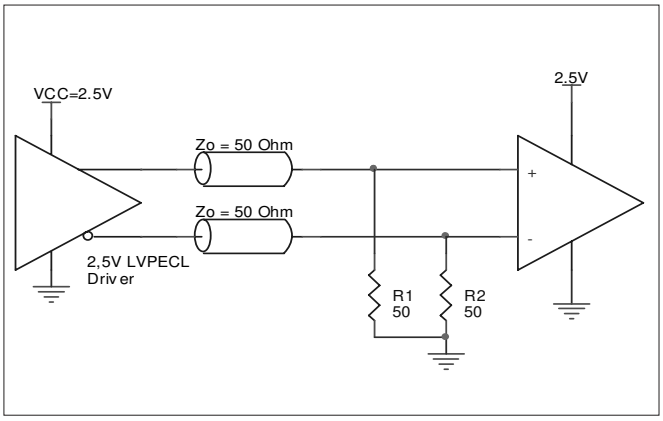


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

2.5V LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACES

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{OUT} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

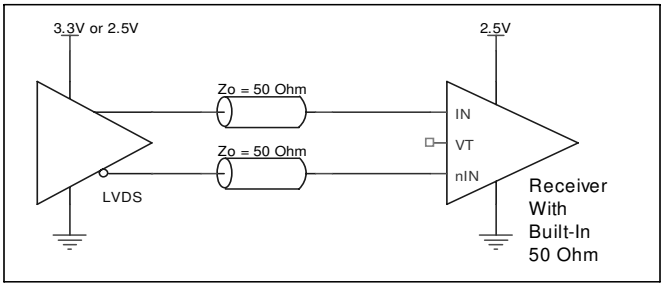


FIGURE 4A. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

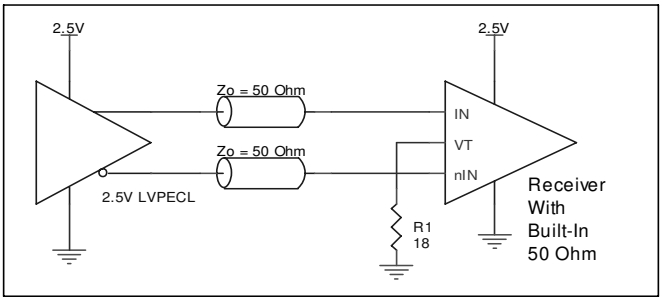


FIGURE 4B. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

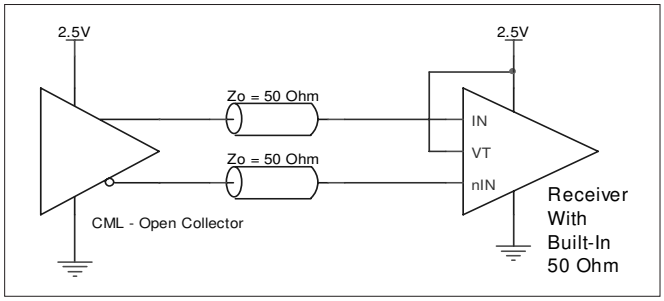


FIGURE 4C. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

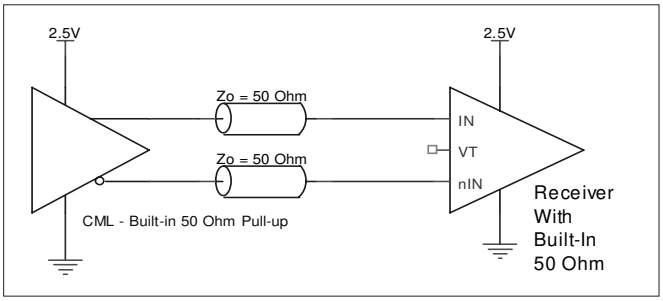


FIGURE 4D. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

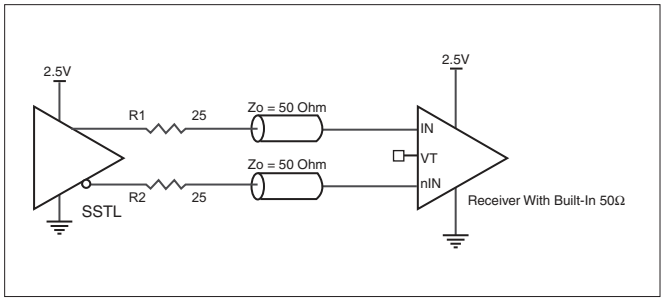


FIGURE 4E. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

3.3V LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACES

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{OUT} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

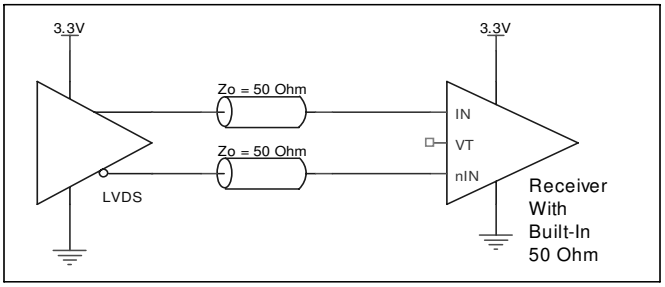


FIGURE 5A. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

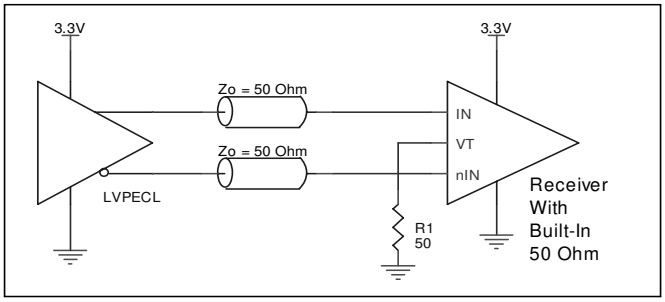


FIGURE 5B. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

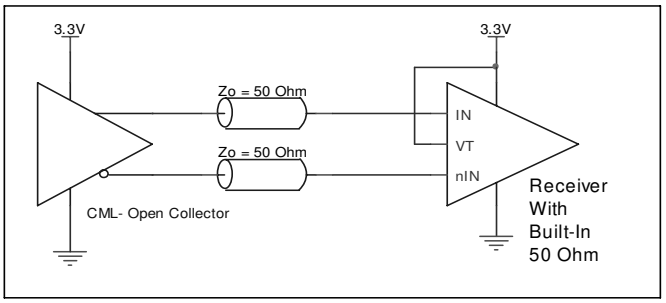


FIGURE 5C. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH OPEN COLLECTOR

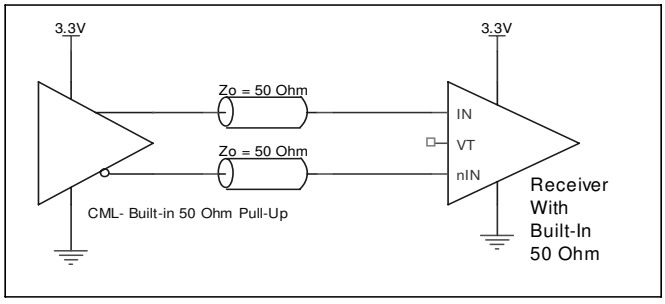


FIGURE 5D. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

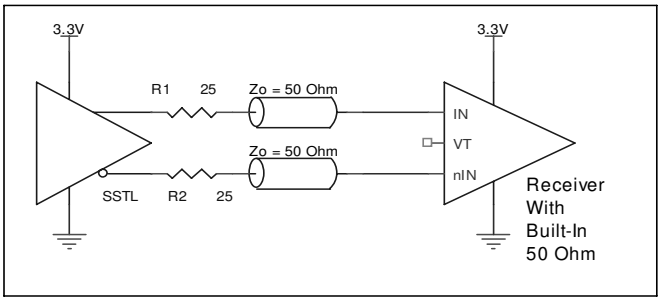


FIGURE 5E. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

3.3V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 6.*

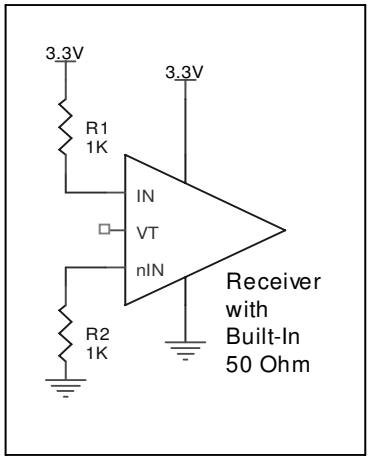


FIGURE 6. UNUSED INPUT HANDLING

2.5V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 7.*

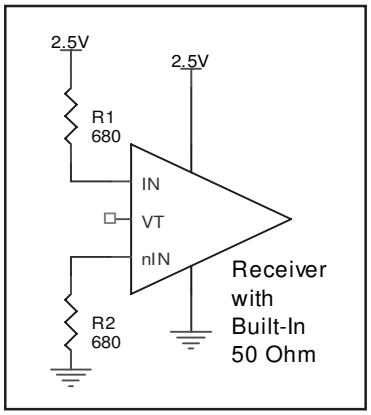


FIGURE 7. UNUSED INPUT HANDLING

SCHEMATIC EXAMPLE

Figure 8 shows a schematic example of the ICS889831. This schematic provides examples of input and output handling. The ICS889831 input has built-in 50Ω termination resistors. The input can directly accept various types of differential signal without AC couple. For AC couple termination, the ICS889831 also provides the VREF_AC pin for proper offset level after the AC couple. This example shows the ICS889831 input driven by a 2.5V LVPECL driver with AC couple. The ICS889831 outputs are LVPECL driver. In this example, we assume the traces are long transmission line and the receiver is high input impedance without built-in matched load. An example of 3.3V LVPECL termination is shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

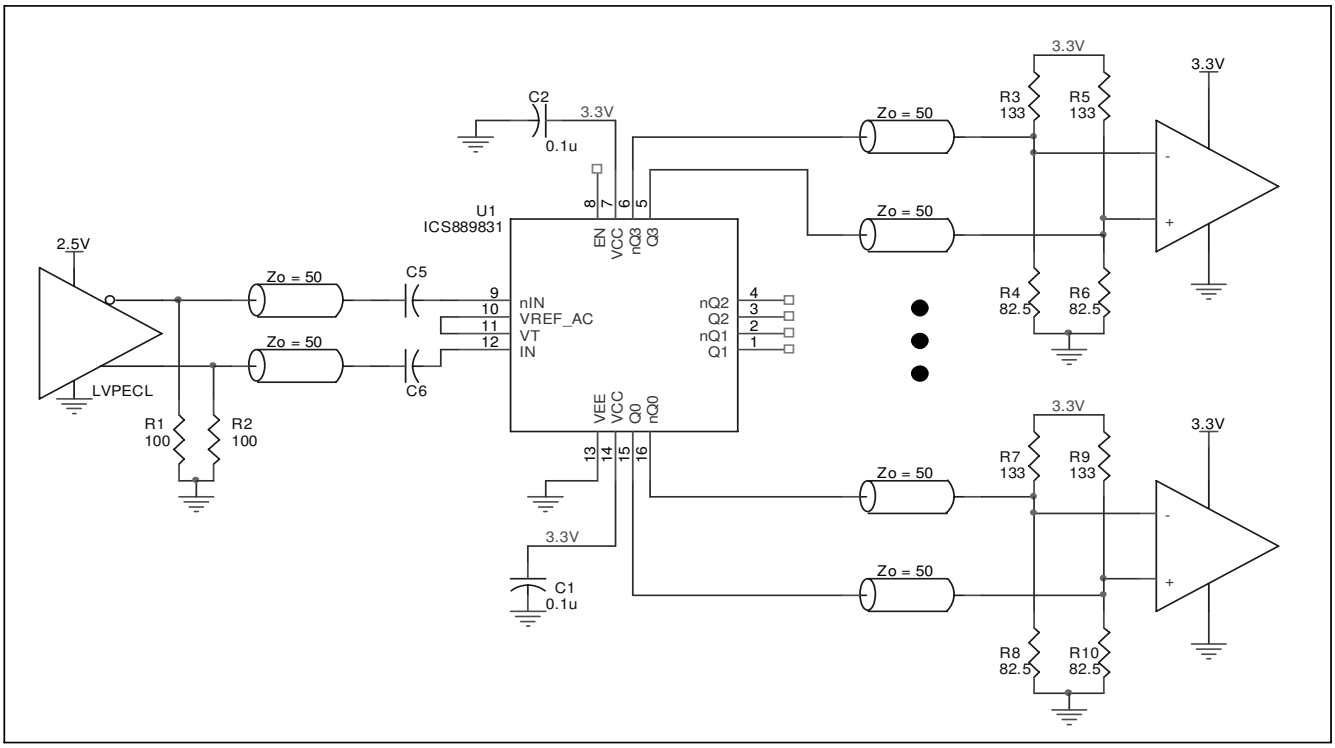


FIGURE 8. ICS889831 APPLICATION SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS839831.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS889831 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.63V * 60mA = **217.8mW**
- Power (outputs)$_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.94mW = **123.8mW**
- Power Dissipation at built-in terminations: Assume the input is driven by a 3.3V SSTL driver as shown in Figure 5E and estimated approximately 1.75V drop across IN and nIN.
  Total Power Dissipation for the two 50Ω built-in terminations is: $(1.75V)^2 / (50\Omega + 50\Omega)$ = **30.6mW**

Total Power$_{_MAX}$ (3.63V, with all outputs switching) = 217.8mW + 123.8mW + 30.6mW = **372.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 0 linear feet per minute and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.372W * 51.5°C/W = 104°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Velocity (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 9.*

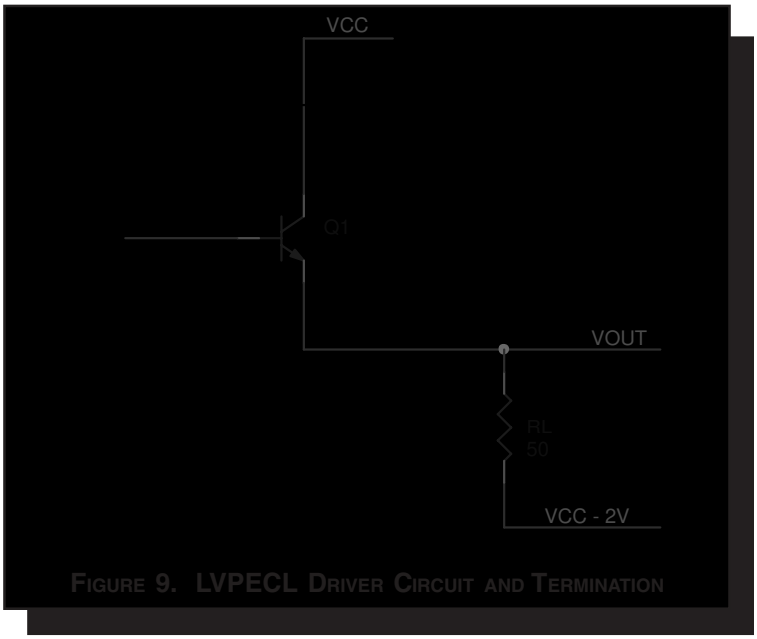


FIGURE 9. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.935V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.935V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.67V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS889831 is: 234

Pin compatible with SY89831U

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

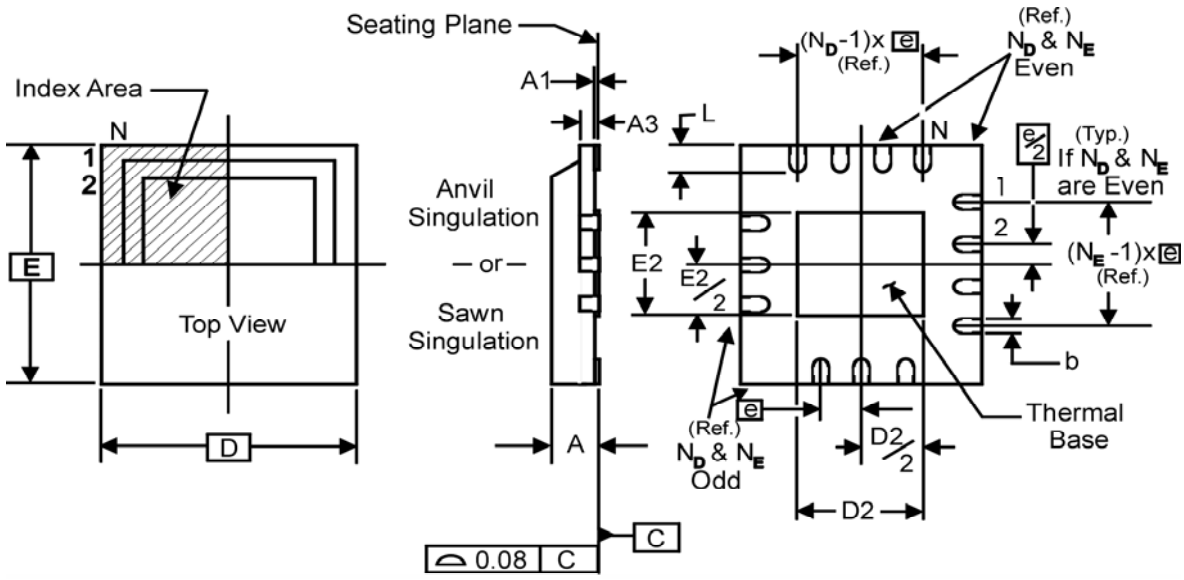


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS889831AK	831A	16 Lead VFQFN	tube	-40°C to 85°C
ICS889831AKT	831A	16 Lead VFQFN	3500 tape & reel	-40°C to 85°C
ICS889831AKLF	TBD	16 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
ICS889831AKLFT	TBD	16 Lead "Lead-Free" VFQFN	3500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.