SN65HVD1050 EMC Optimized CAN Bus Transceiver

1 Features

- Improved Replacement for the TJA1050
- High Electromagnetic Immunity (EMI)
- Very Low Electromagnetic Emissions (EME)
- Meets or Exceeds the Requirements of ISO 11898-2
- CAN Bus-Fault Protection of –27 V to 40 V
- Dominant Time-Out Function
- Power-Up and Power-Down Glitch-Free CAN Bus Inputs and Outputs
  - High Input Impedance With Low V_{CC}
  - Monotonic Outputs During Power Cycling

2 Applications

- Industrial Automation
  - DeviceNet™ Data Buses (Vendor ID #806)
- SAE J2284 High-Speed CAN Bus for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

3 Description

The SN65HVD1050 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN).

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps) (1).

The SN65HVD1050 is designed for operation in especially harsh environments. As a result, the device features cross-wire, overvoltage and loss of ground protection from –27 V to 40 V, overtemperature shutdown, a –12-V to 12-V common-mode range, and will withstand voltage transients from –200 V to 200 V according to ISO 7637.

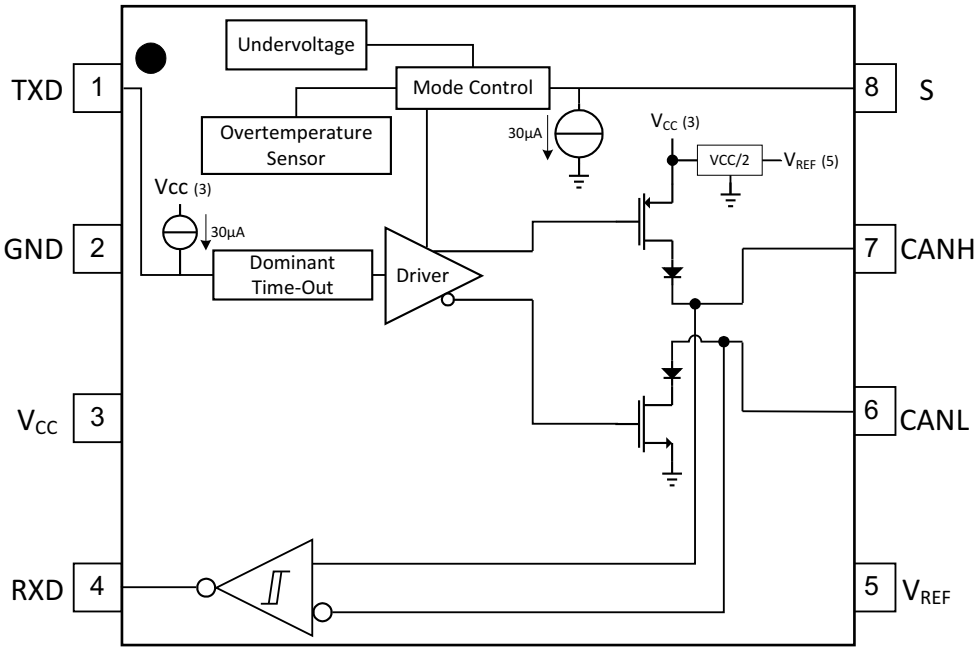
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD1050	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2010) to Revision C **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (May 2007) to Revision B **Page**

- Deleted The device is also qualified for use in ISO 11898-2 automotive applications in accordance with AEC-Q100." and footnote, "The device is available with Q100 qualification as the SN65HVD1050Q." ... 1
- Changed V_{CC} min/max range from 4.75-5.25V to 4.5-5.5V ... 4
- Changed V_{IH} max from 5.25V to 5.5V ... 4
- Added rows for various parameters showing parameters with V_{CC} ±5% and ±10% ... 4
- Added Signaling Rate spec, min 20kbps ... 4
- Changed V_{IH} min from 2 to 2.1V ... 4
- Changed Bus output voltage (Dominant) CANH 4.5V < V_{CC} < 5.5V from 4.75 to 5.2 ... 5

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5 Description (Continued)

Pin 8 provides for two different modes of operation: high-speed or silent mode. The high-speed mode of operation is selected by connecting S (pin 8) to ground.

If a high logic level is applied to the S pin of the SN65HVD1050, the device enters a listen-only silent mode during which the driver is switched off while the receiver remains fully functional.

In silent mode, all bus activity is passed by the receiver output to the local protocol controller. When data transmission is required, the local protocol controller reverses this low-current silent mode by placing a logic-low on the S pin to resume full operation.

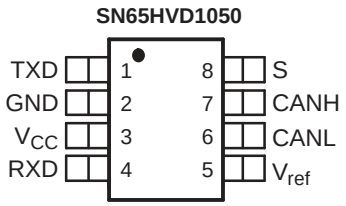
A dominant time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

V_{ref} (pin 5) is available as a $V_{CC}/2$ voltage reference to stabilize the output common mode voltage point.

The SN65HVD1050 is characterized for operation from –40°C to 125°C.

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND	2	GND	Device ground
V_{CC}	3	Supply	Transceiver 5-V supply
RXD	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
V_{REF}	5	O	Reference output voltage
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
S	8	I	Mode select pin (Logic LOW places the device in high-speed mode and logic HIGH places the device in a listen-only silent mode)

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7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.3	7	V
	Voltage range at any bus terminal (CANH, CANL, V_{ref})	–27	40	V
I_O	Receiver output current		20	mA
V_I	Voltage input, transient pulse(3) (CANH, CANL)	–200	200	V
V_I	Voltage input range (TXD, S)	–0.5	6	V
T_J	Junction temperature	–55	170	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±8000	V
			Bus pins vs GND	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
		Machine Model, ANSI/ESDS5.2-1996		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12		12	V
V_{IH}	High-level input voltage	TXD, S	2.1		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			2	
T_J	Junction temperature	See *Absolute Maximum Ratings*(1), 1-Mbps minimum signaling rate with R_L = 54 Ω	–40		150	°C
	Signaling Rate		20			kbps

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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7.4 Thermal Information

THERMAL METRIC[1]		SN65HVD1050 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-air, Low-K thermal resistance[2]	211	°C/W
	Junction-to-air, High-K thermal resistance	131	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79	
$R_{\theta JB}$	Junction-to-board thermal resistance	53	
ψ_{JT}	Junction-to-top characterization parameter	10.3	
ψ_{JB}	Junction-to-board characterization parameter	56.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	112	
P_D	Average power dissipation, V_{CC} = 5.0V, T_j = 27°C, R_L = 60 Ω, S at 0V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF	170	mW
	Average power dissipation, V_{CC} = 5.5V, T_j = 130°C, R_L = 45 Ω, S at 0V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF	170	
$T_{J\_shutdown}$	Junction temperature, thermal shutdown[3]	190	°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.
(3) Extended operation in thermal shutdown may affect device reliability, see APPLICATIONS INFORMATION.

7.5 Driver Electrical Characteristics

over recommended operating conditiions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0V, S at 0V, R_L = 60 Ω, See Figure 11 and Figure 12	4.75V < V_{CC} < 5.25V	2.9	3.4	4.5	V
				4.5V < V_{CC} < 5.5V	2.75		5.2	
		CANL		4.75V < V_{CC} < 5.25V	0.8		1.5	
				4.5V < V_{CC} < 5.5V			1.6	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3V, S at 0V, R_L = 60 Ω, See Figure 11 and Figure 12	4.75V < V_{CC} < 5.25V	2	2.3	3	V
				4.5V < V_{CC} < 5.5V	1.8		3	
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0V, R_L = 60 Ω, S at 0V, See Figure 11, Figure 12, and Figure 13	4.75V < V_{CC} < 5.25V	1.5		3	V
				4.5V < V_{CC} < 5.5V	1.4		3	
			V_I = 0V, R_L = 45 Ω, S at 0V, See Figure 11, Figure 12, and Figure 13	4.75V < V_{CC} < 5.25V	1.4		3	
				4.5V < V_{CC} < 5.5V	1.3		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3V, S at 0V, See Figure 11 and Figure 12		–0.012		0.012	V
			V_I = 3V, S at 0V, No Load		–0.5		0.05	
$V_{OC(ss)}$	Steady state common-mode output voltage		S at 0V, Figure 18	4.75V < V_{CC} < 5.25V	2	2.3	3	V
				4.5V < V_{CC} < 5.5V	1.9		3	
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage					30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}		–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0V		–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0V, TXD at 5V				1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = -12V, CANL Open, See Figure 21		–105	–72		mA
			V_{CANH} = 12V, CANL Open, SeeFigure 21			0.36	1	
			V_{CANL} = -12V, CANH Open, See Figure 21		–1	–0.5		
			V_{CANL} = 12V , CANH Open, See Figure 21			71	105	
C_O	Output capacitance		See receiver input capacitance					

(1) All typical values are at 25°C with a 5-V supply.

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7.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	S at 0V, See Table 1			800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			100	125		
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 16	4.75V < V_{CC} < 5.25V	4	4.6		V
			4.5V < V_{CC} < 5.5V	3.8			
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 16			0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5V, Other pin at 0V, V_{CC} at 0V, TXD at 0V			165	250	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0V, RXD at 5V				20	µA
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3V, V_I = 0.4 sin (4E6πt) + 2.5V			13		pF
C_{ID}	Differential input capacitance	TXD at 3V, V_I = 0.4 sin (4E6πt)			5		
R_{ID}	Differential input resistance	TXD at 3V, S at 0V		30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)			15	30	40	
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] x 100%	$V_{(CANH)}$ = $V_{(CANL)}$		–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

7.7 Device Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	Figure 19, S at 0V	4.75V < V_{CC} < 5.25V	90		190	ns
			4.5V < V_{CC} < 5.5V	85		195	
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		4.75V < V_{CC} < 5.25V	90		190	
			4.5V < V_{CC} < 5.5V	85		195	

7.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0V, See Figure 14		25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	45	90	
t_r	Differential output signal rise time				25		
t_f	Differential output signal fall time				50		
t_{en}	Enable time from silent mode to dominant	See Figure 17				1	µs
$t_{(dom)}$	Dominant time-out	↓V_I, See Figure 20	4.75V < V_{CC} < 5.25V	300	450	700	µs
			4.5V < V_{CC} < 5.5V	280		700	

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7.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0V or V_{CC}, See Figure 16	4.75V < V_{CC} < 5.25V	60	100	130	ns
			4.5V < V_{CC} < 5.5V	60		135	
t_{PHL}	Propagation delay time, high-to-low-level output		4.75V < V_{CC} < 5.25V	45	70	90	
			4.5V < V_{CC} < 5.5V	45		95	
t_r	Output signal rise time				8		
t_f	Output signal fall time				8		

7.10 Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	5-V Supply current	Silent mode	S at V_{CC}, V_I = V_{CC}			6	10	mA
		Dominant	V_I = 0V, 60 Ω Load, S at 0V	4.75V < V_{CC} < 5.25V		50	70	
				4.5V < V_{CC} < 5.5V			75	
		Recessive	V_I = V_{CC}, No Load, S at 0V			6	10	

7.11 S-Pin Characteristics

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	S at 2V	20	40	70	µA
I_{IL}	Low level input current	S at 0.8V	5	20	30	

7.12 VREF-Pin Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference output voltage	–50 µA < I_O < 50 µA	0.4V_{CC}	0.5V_{CC}	0.6V_{CC}	V

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7.13 Typical Characteristics

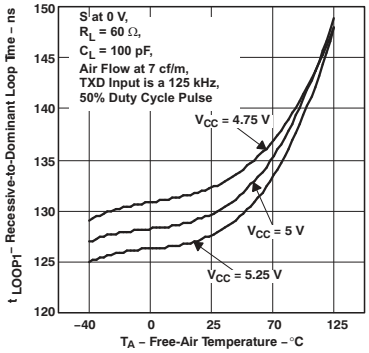

Figure 1. Recessive-to-Dominant Loop Time vs Free-Air Temperature (Across V_{CC})

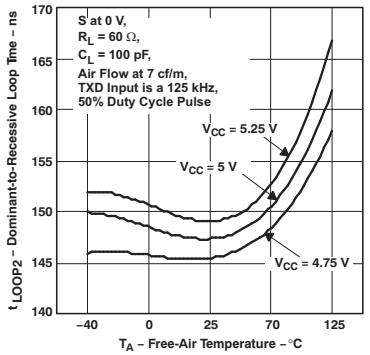

Figure 2. Dominant-to-Recessive Loop Time vs Free-Air Temperature (Across V_{CC})

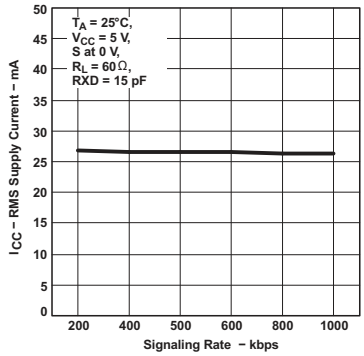

Figure 3. Supply Current (RMS) vs Signaling Rate

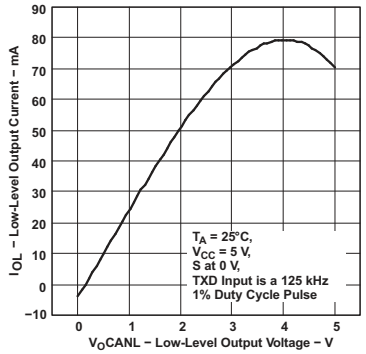

Figure 4. Driver Low-Level Output Voltage vs Low-Level Output Current

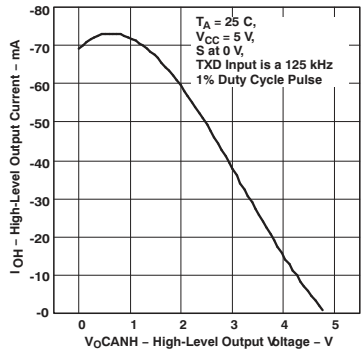

Figure 5. Driver High-Level Output Voltage vs High-Level Output Current

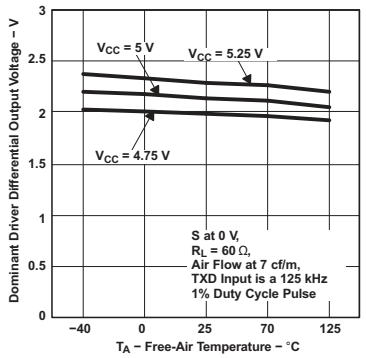

Figure 6. Driver Differential Output Voltage vs Free-Air Temperature (Across V_{CC})

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Typical Characteristics (continued)

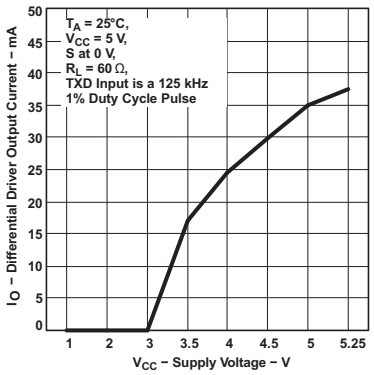

Figure 7. Driver Output Current vs Supply Voltage

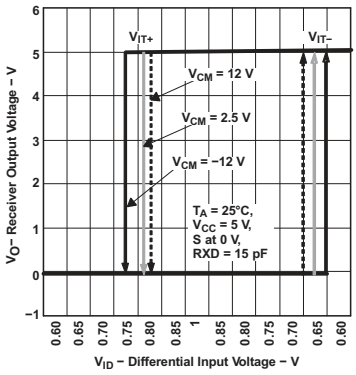

Figure 8. Receiver Output Voltage vs Differential Input Voltage

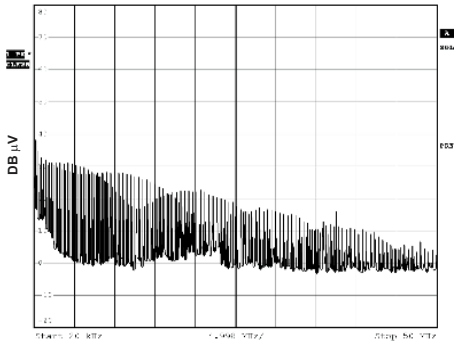

Figure 9. Frequency Spectrum of Common-Mode Emissions

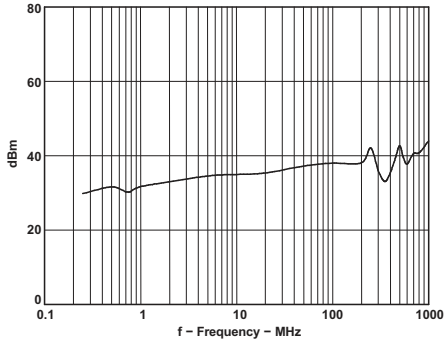

Figure 10. Direct Power Injection (DPI) Response vs Frequency

8 Parameter Measurement Information

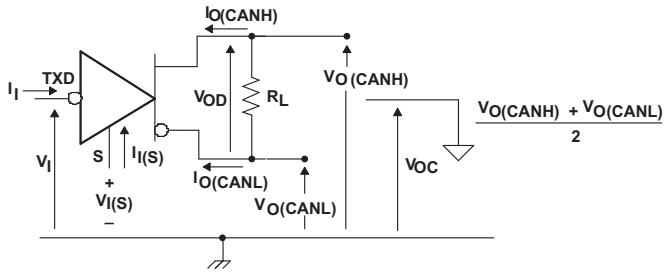

Figure 11. Driver Voltage, Current, and Test Definition

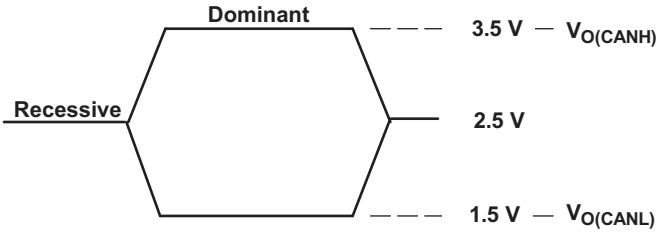

Figure 12. Bus Logic State Voltage Definitions

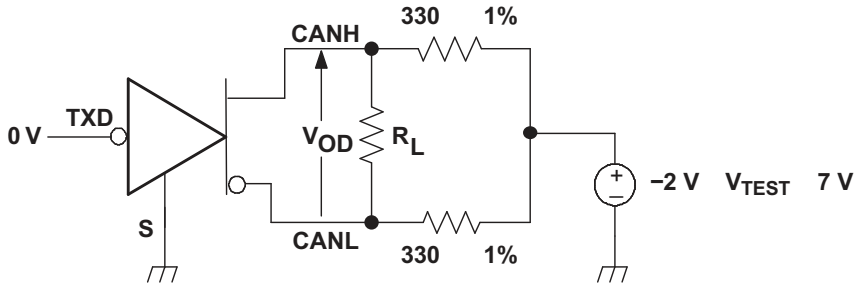

Figure 13. Driver V_{OD} Test Circuit

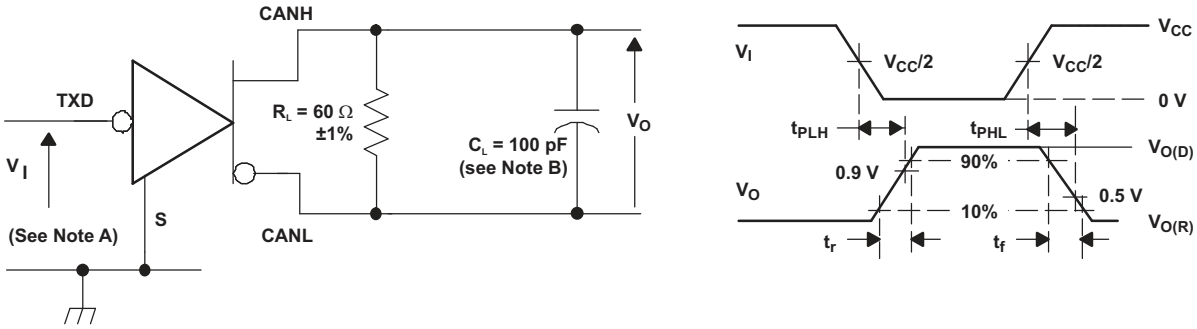

Figure 14. Driver Test Circuit and Voltage Waveforms

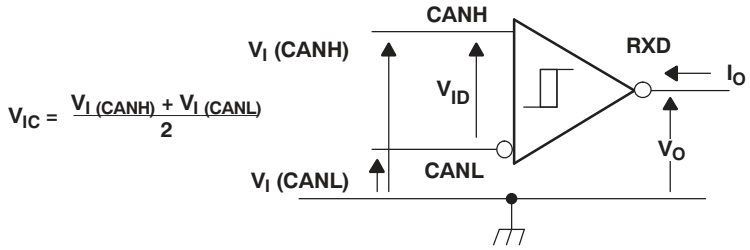

Figure 15. Receiver Voltage and Current Definitions

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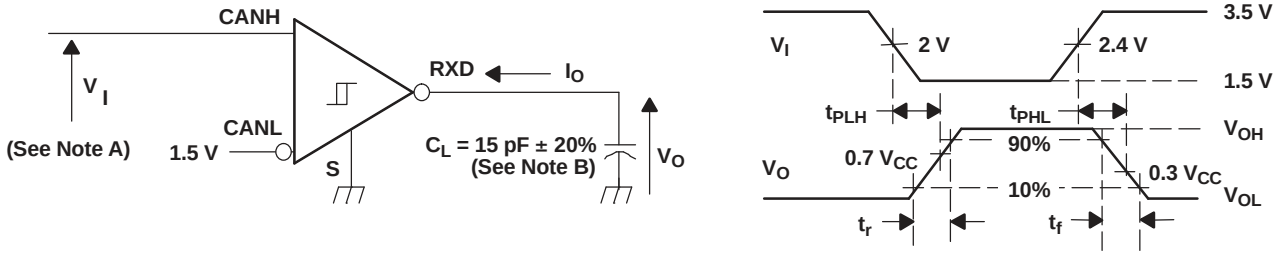
Parameter Measurement Information (continued)



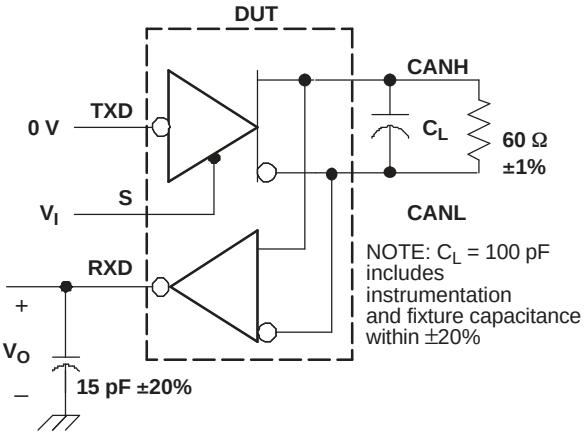
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

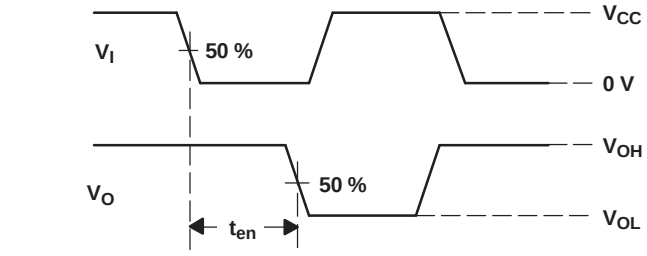
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 16. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1V	–12V	900 mV	L	V_{OL}
12V	11.1V	900 mV	L	
–6V	–12V	6V	L	
12V	6V	6V	L	
–11.5V	–12V	500 mV	H	V_{OH}
12V	11.5V	500 mV	H	
–12V	–6V	6V	H	
6V	12V	6V	H	
Open	Open	X	H	





NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle

Figure 17. T_{EN} Test Circuit and Waveform

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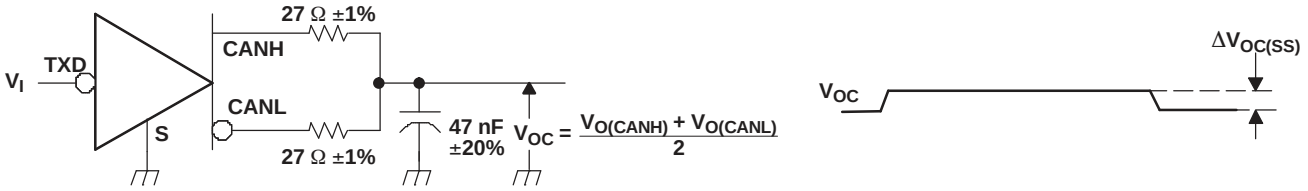
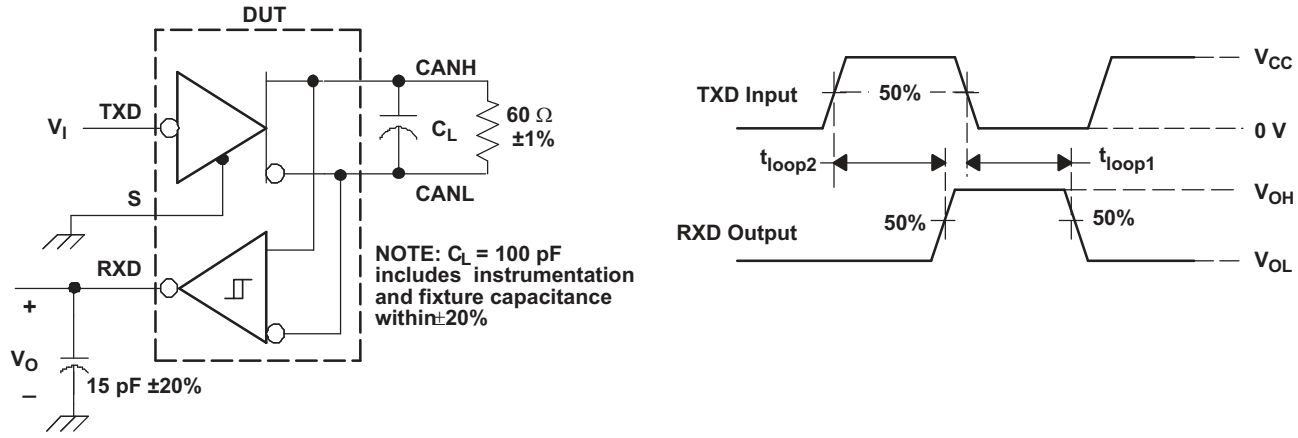


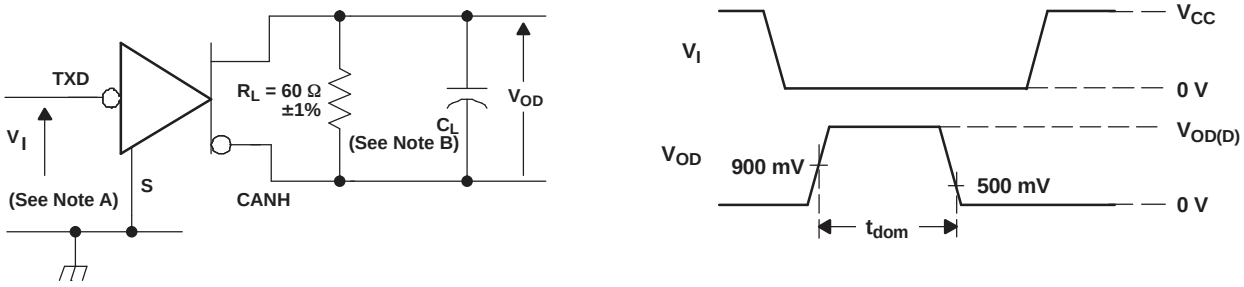
NOTE: All V_I input pulses are from 0V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 18. Common Mode Output Voltage Test and Waveforms



A. All V_I input pulses are from 0V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $T_{(LOOP)}$ Test Circuit and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 20. Dominant Time-Out Test Circuit and Waveforms

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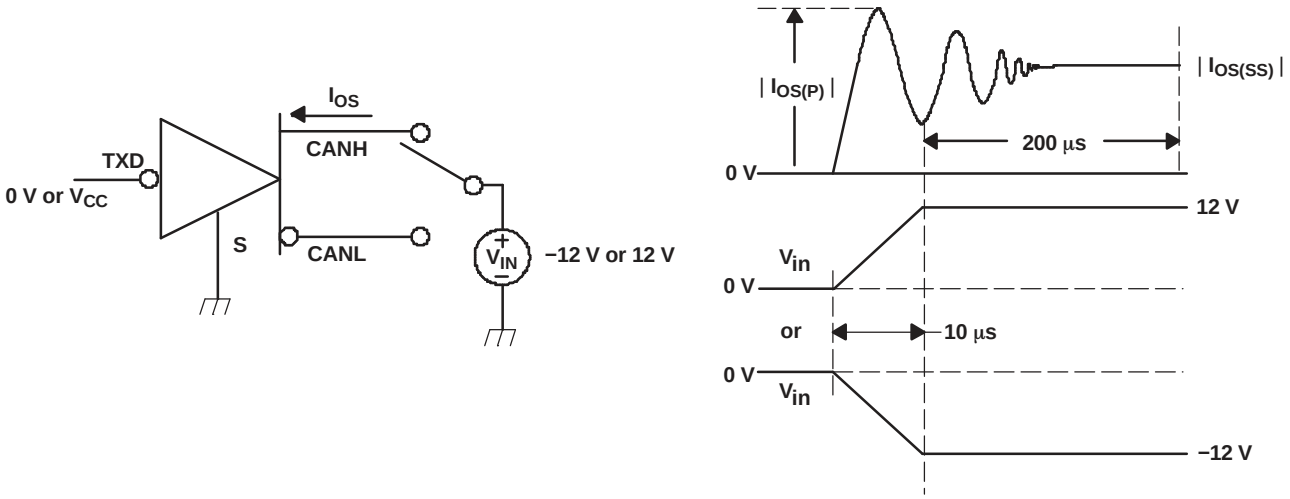


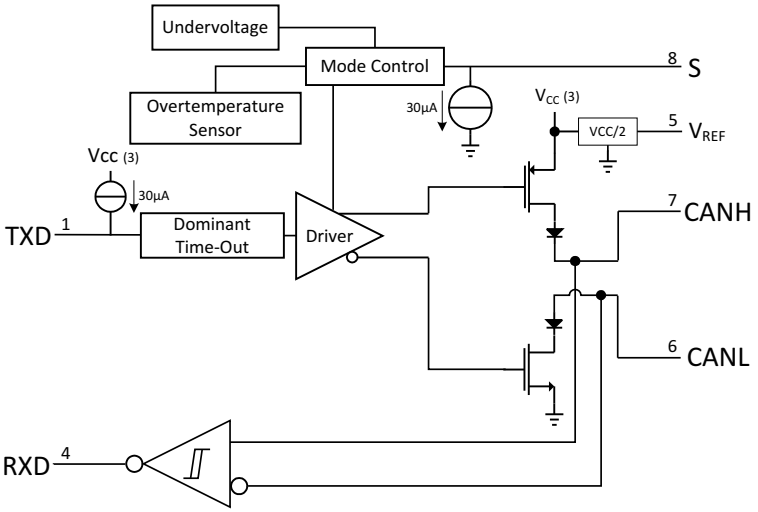
Figure 21. Driver Short-Circuit Current Test and Waveform

9 Detailed Description

9.1 Overview

The SN65HVD1050 CAN tranceivers is compatible with the ISO1189-2 High Speed CAN (Controller Area Network) physical layer standard. It is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Mode Control

9.3.1.1 Normal Mode

Select the normal mode of the device operation by setting the S pin low. The CAN bus driver and receiver are fully operational and the CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

9.3.1.2 Silent Mode

Activate silent mode (receive only) by setting the S pin high. The CAN driver is turned off while the receiver remains active and RXD outputs the received bus data.

NOTE

Silent mode may be used to implement babling idiot protection, to ensure that the driver does not disrupt the network during a local fault. Silent mode may also be used in redundant systems to select or deselect the redundant transceiver (driver) when needed.

9.3.2 TXD Dominant Timeout (DTO)

During normal mode, the mode where the CAN driver is active, the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit is triggered on a falling edge on the driver input, TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen on TXD before the timeout period expires. This frees the CAN bus for communication between other nodes on the network. The CAN driver is re-enabled when a rising edge is seen on the drvier input, TXD, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD DTO.

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Feature Description (continued)

NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate on the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate using: Minimum Data Rate = 11 / t_{TXD_DTO}

9.3.3 Thermal Shutdown

The SN65HVD1050 has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an SN65HVD1050 is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

9.3.4 V_{REF}

A reference voltage of $V_{CC}/2$ is available through the V_{REF} output pin. The V_{REF} voltage should be tied to the common mode point in a split termination network to help stabilize the output common mode voltage. See Figure 27 for more application specific information on properly terminating the CAN bus.

If the V_{REF} output pin is not used it can be left floating.

9.3.5 Operating Temperature Range

The SN65HVD1050 is characterized for operation from –40°C to 125°C.

9.4 Device Functional Modes

Table 2. Driver

INPUTS		OUTPUTS		BUS STATE
TXD(1)	S(1)	CANH(1)	CANL(1)	
L	L or Open	H	L	DOMINANT
H	X	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 3. Receiver

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	OUTPUT RXD(1)	BUS STATE
$V_{ID} \geq 0.9V$	L	DOMINANT
$0.5V < V_{ID} < 0.9V$	?	?
$V_{ID} \leq 0.5V$	H	RECESSIVE
Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

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Table 4. Parametric Cross Reference With the TJA1050

TJA1050 (1)	PARAMETER	HVD1050
TRANSMITTER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
BUS SECTION		
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{i(dif)(hys)}$	Diffrential input hysteresis	Receiver V_{hys}
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{O(dif)(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(dif)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)(m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
C_i	Input capacitance to ground	Receiver C_I
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
Vref PIN SECTION		
V_{ref}	Reference output voltage	V_O
TIMING SECTION		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
	$t_{d(TXD-BUSon)} + t_{d(BUSon-RXD)}$	Device t_{LOOP1}
	$t_{d(TXD-BUSoff)} + t_{d(BUSoff-RXD)}$	Device t_{LOOP2}
$t_{dom(TXD)}$	Dominant time out	Driver $t_{(dom)}$
S PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1050 Product Specification, Philips Semiconductors, 2002 May 16.

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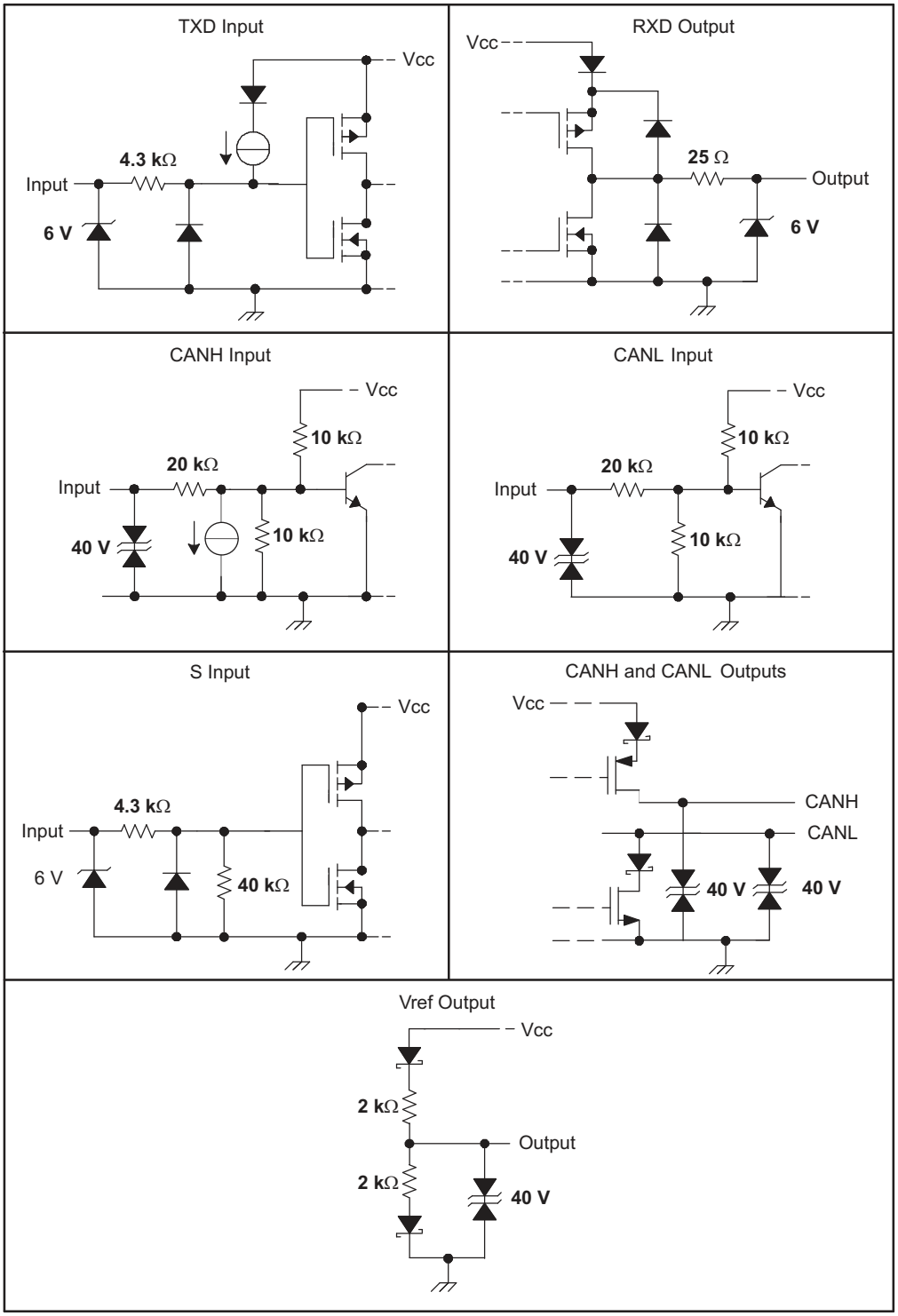

Figure 22. Equivalent Input and Output Schematic Diagrams

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the D and R pins. See Figure 23 and Figure 24.

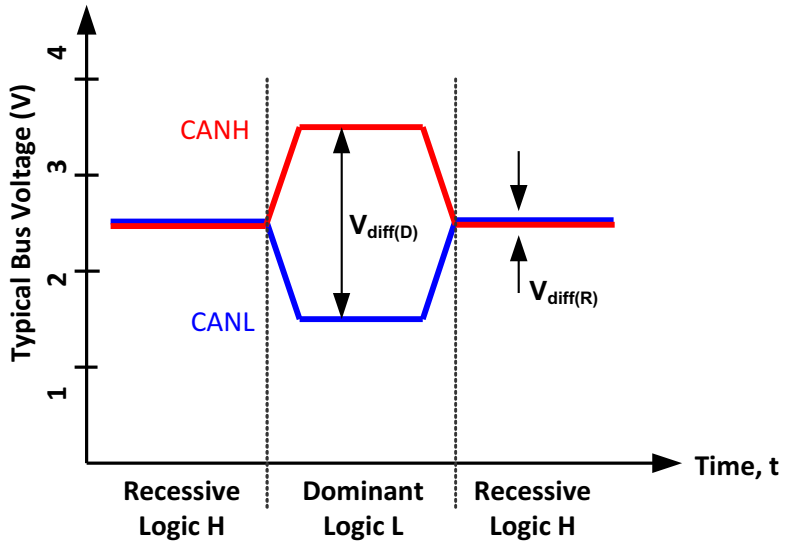

Figure 23. Bus States

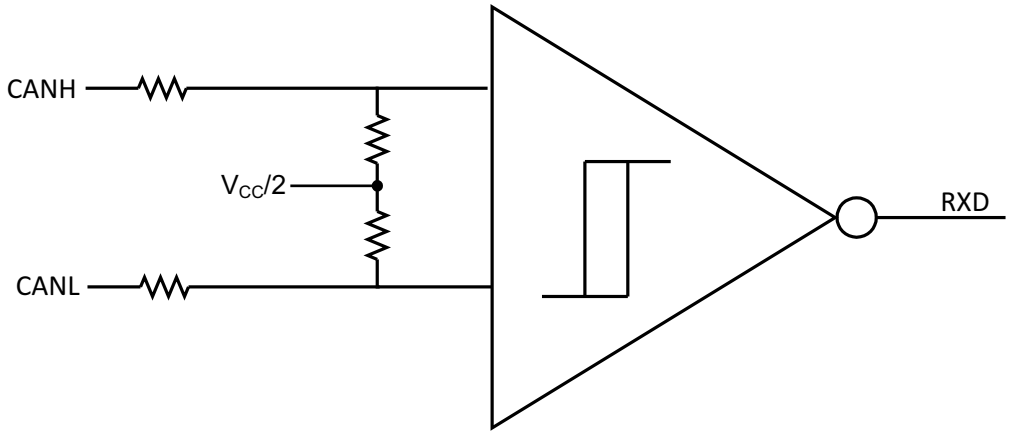

Figure 24. Simplified Recessive Common Mode Bias and Receiver

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120-Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.

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10.2 Typical Application

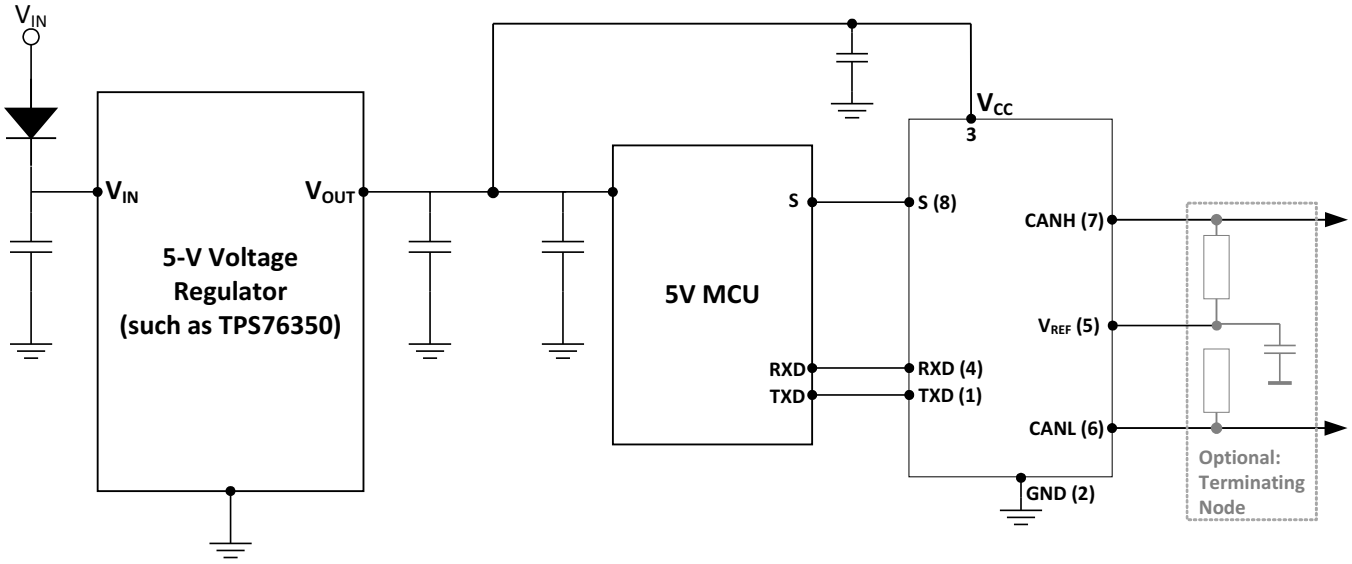

Figure 25. Typical Application Schematic

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO 11898 Standard specifies up to 1 Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

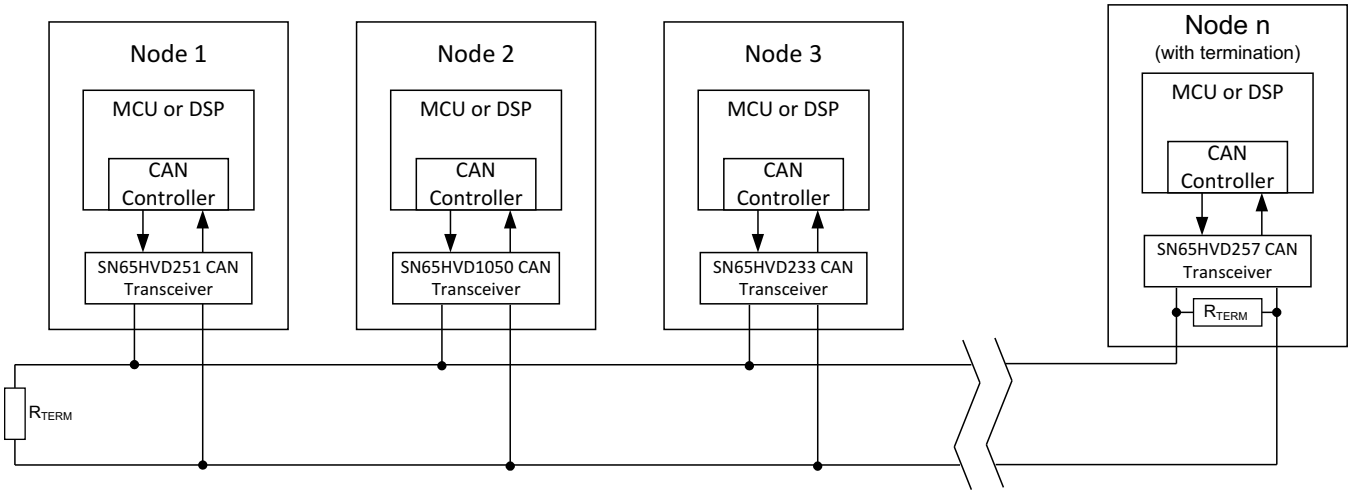

Figure 26. Typical CAN Bus

Typical Application (continued)

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SN65HVD1050 CAN transceiver. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVD1050 device is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 V to 7 V via a 330-Ω coupling network. This network represents the bus loading of 90 SN65HVD1050 transceivers based on their minimum differential input resistance of 30 kΩ. Therefore, the SN65HVD1050 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1-km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

10.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 27). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the CAN transceiver's current limit.

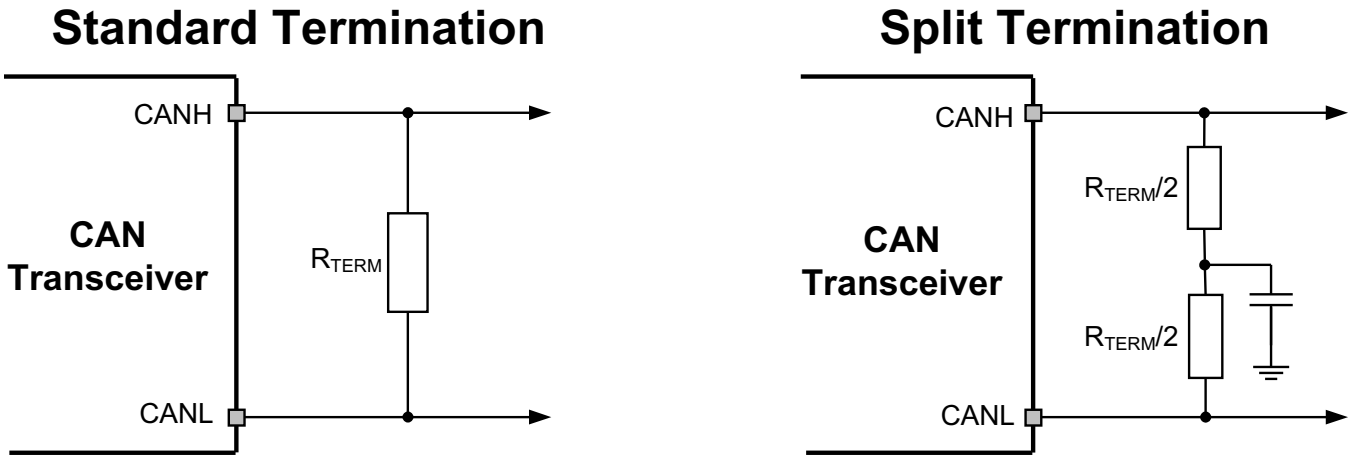

Figure 27. CAN Termination

10.2.1.2.1 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (TXD pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output (RXD pin). A typical loop delay for the SN65HVD1050 transceiver is displayed in Figure 29.

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Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 ESD Protection

A typical application that employees a CAN bus network may require some form of ESD, burst, and surge protection to shield the CAN transceiver against unwanted transients that can potential damage the transceiver. To help shield the SN65HVD1050 transceiver against these high energy transients, transient voltage suppressors can be implemented on the CAN differential bus terminals. These devices will help absorb the impact of a ESD, burst, and/or surge strike.

10.2.2.2 Transient Voltage Suppresser (TVS) Diodes

Transient voltage suppressors are the preferred protection components for a CAN bus due to their low capacitance, which allows them to be designed into every node of a multi-node network without requiring a reduction in data rate. With response times of a few picoseconds and power ratings of up to several kilowatts, TVS diodes present the most effective protection against ESD, burst, and surge transients.

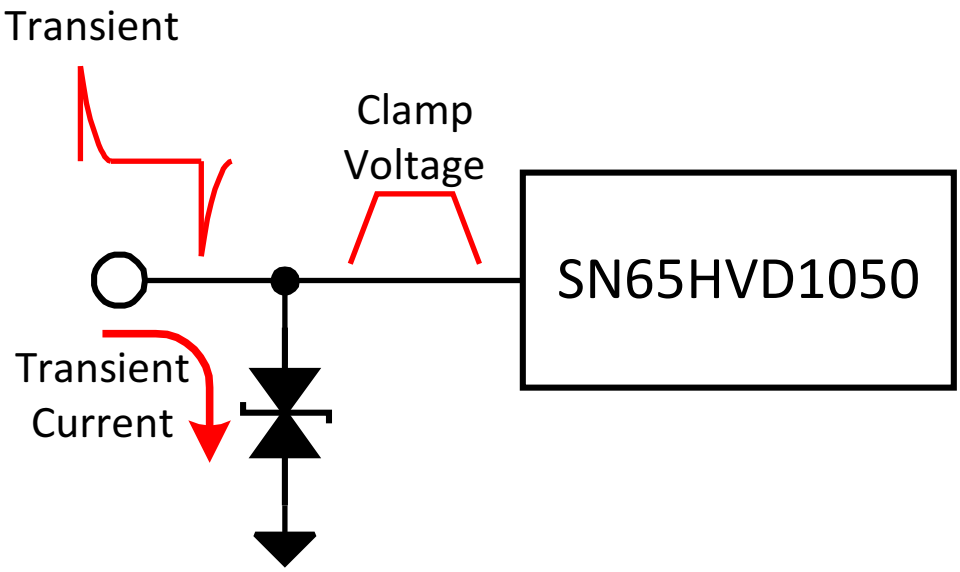

Figure 28. Effect of Transient Voltage Supressor

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Typical Application (continued)

10.2.3 Application Curve

Figure 29 shows the typical loop delay for the SN65HVD1050.

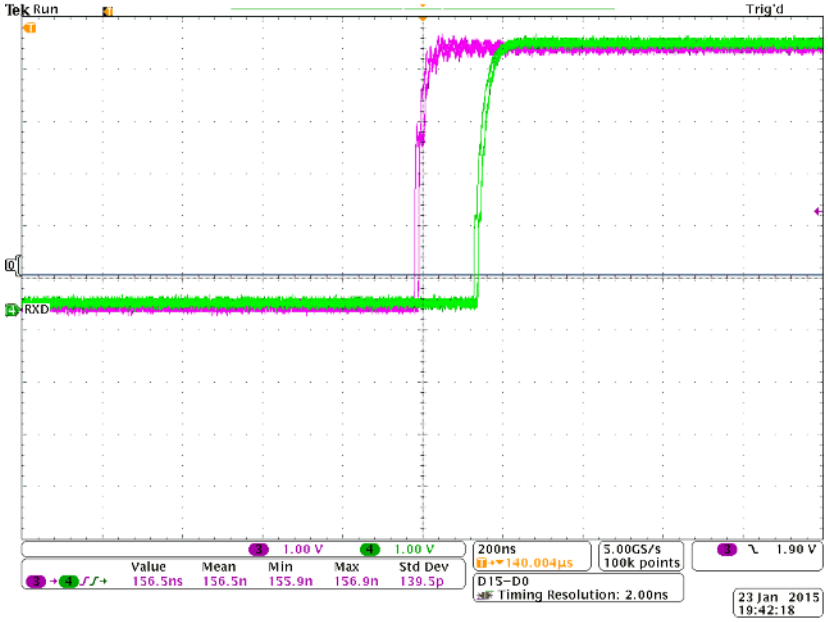

Figure 29. tLOOP Delay Waveform

10.3 System Example

10.3.1 ISO 11898 Compliance of SN65HVD1050 5-V CAN Transceiver

10.3.1.1 Introduction

The SN65HVD1050 CAN transceiver is a 5-V CAN transceiver that meets or exceeds the specification of the ISO 11898 standard for applications employing a controller area network.

10.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

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System Example (continued)

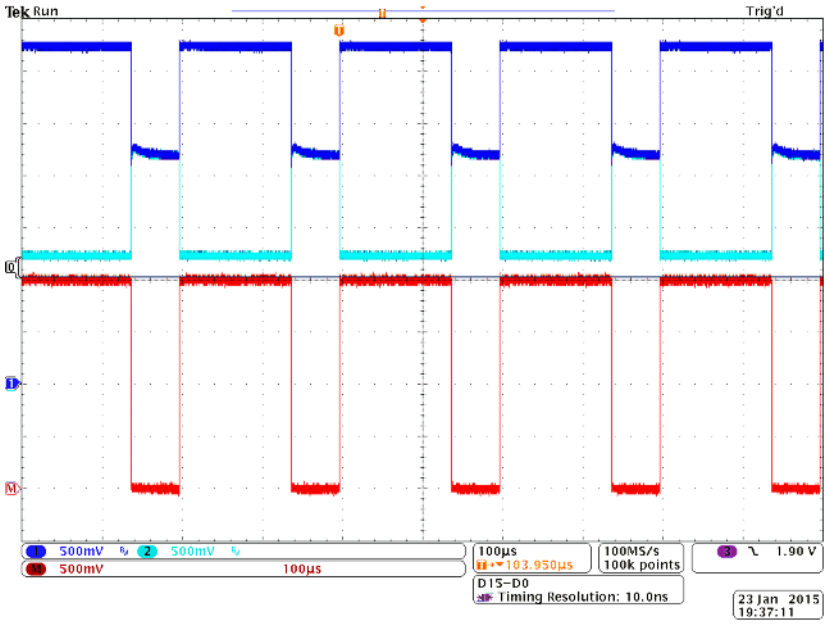

Figure 30. Differential Output Waveform

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD1050 is greater than 1.5 V and less than 3 V across a 60-Ω load as defined by the ISO 11898 standard. Figure 30 shows CANH, CANL, and the diferential dominanat state level for the SN65HVD1050.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V.

10.3.1.3 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Because the bias voltage of the recessive state of the device is dependent on V_{CC}, any noise present or variation of V_{CC} will have an effect on this bias voltage seen by the bus. The SN65HVD1050 CAN transceiver has the recessive bias voltage set to 0.5 × V_{CC} to comply with the ISO 11898-2 CAN standard.

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11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close as possible to the V_{CC} supply pins as possible. The SN65HVD1050 is a linear voltage regulator suitable for the 5-V supply rail.

12 Layout

12.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 25.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 27 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C6. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends.

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device an external pullup resistor between 1 kΩ and 10 kΩ should be used to drive the recessive input state of the device.

Pin 5: V_{REF} should be connected to the center point of a split temrination scheme to help stabalize the common mode volatge to $V_{CC}/2$. If V_{REF} is unused it should be left floating.

Pin 8: Is shown assuming the mode pin, S, will be used. If the device will only be used in normal mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

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12.2 Layout Example

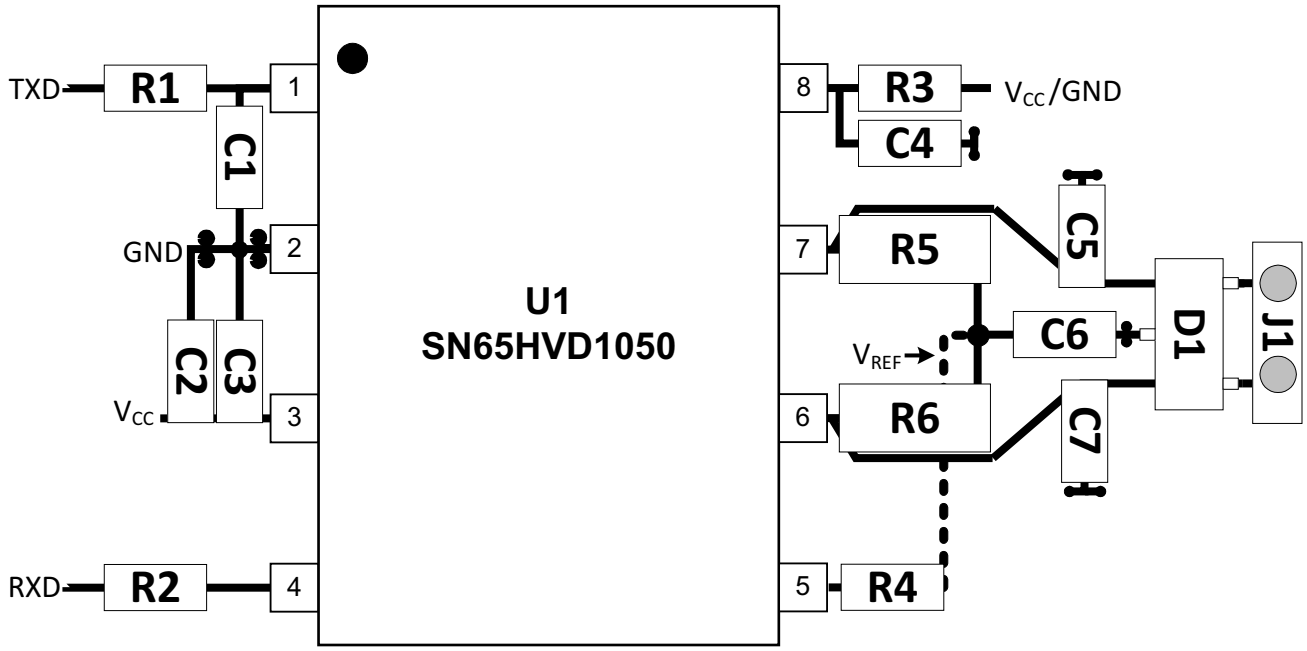

Figure 31. Layout Example

13 Device and Documentation Support

13.1 Trademarks

DeviceNet is a trademark of Open DeviceNet Vendors Association, Inc.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1050D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1050	
SN65HVD1050DG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1050	
SN65HVD1050DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1050	Samples
SN65HVD1050DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65HVD1050 :

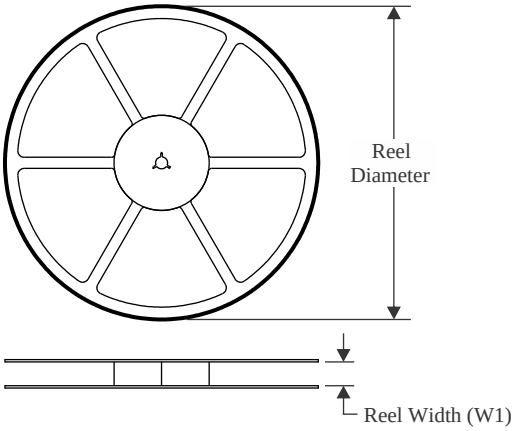
- Automotive : SN65HVD1050-Q1
- Enhanced Product : SN65HVD1050-EP

NOTE: Qualified Version Definitions:

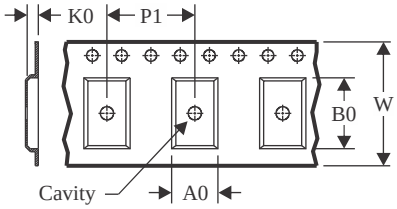
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

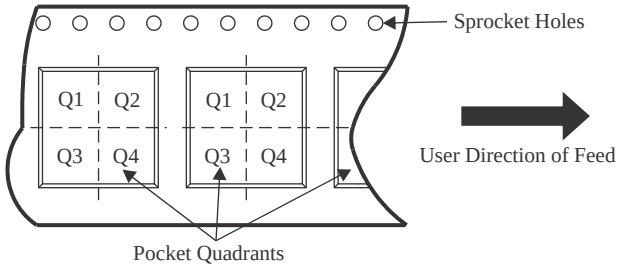


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

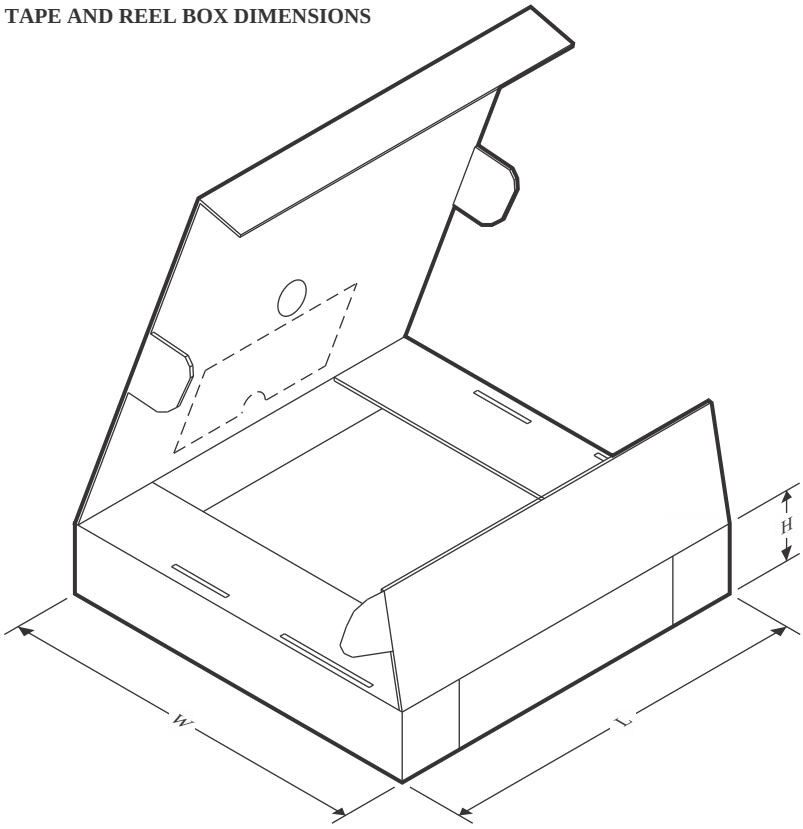
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1050DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

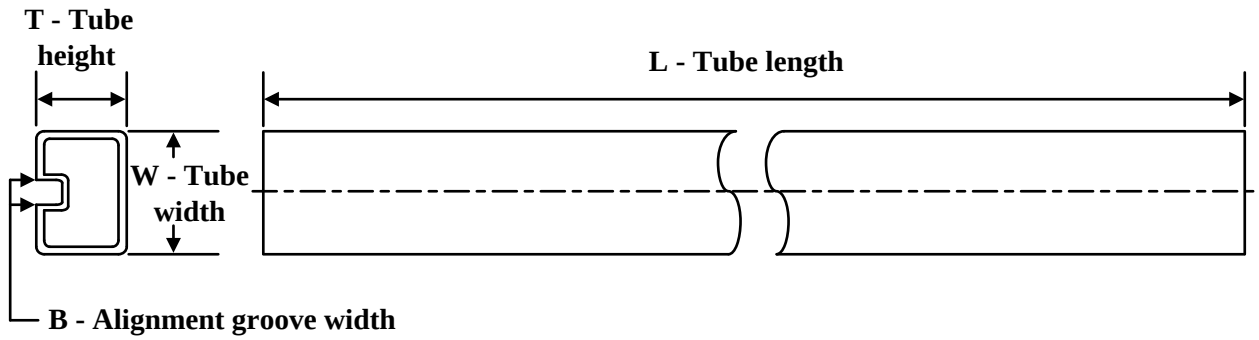
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

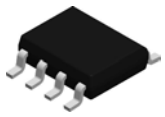
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1050DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD1050D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1050D	D	SOIC	8	75	505.46	6.76	3810	4
SN65HVD1050DG4	D	SOIC	8	75	505.46	6.76	3810	4
SN65HVD1050DG4	D	SOIC	8	75	506.6	8	3940	4.32

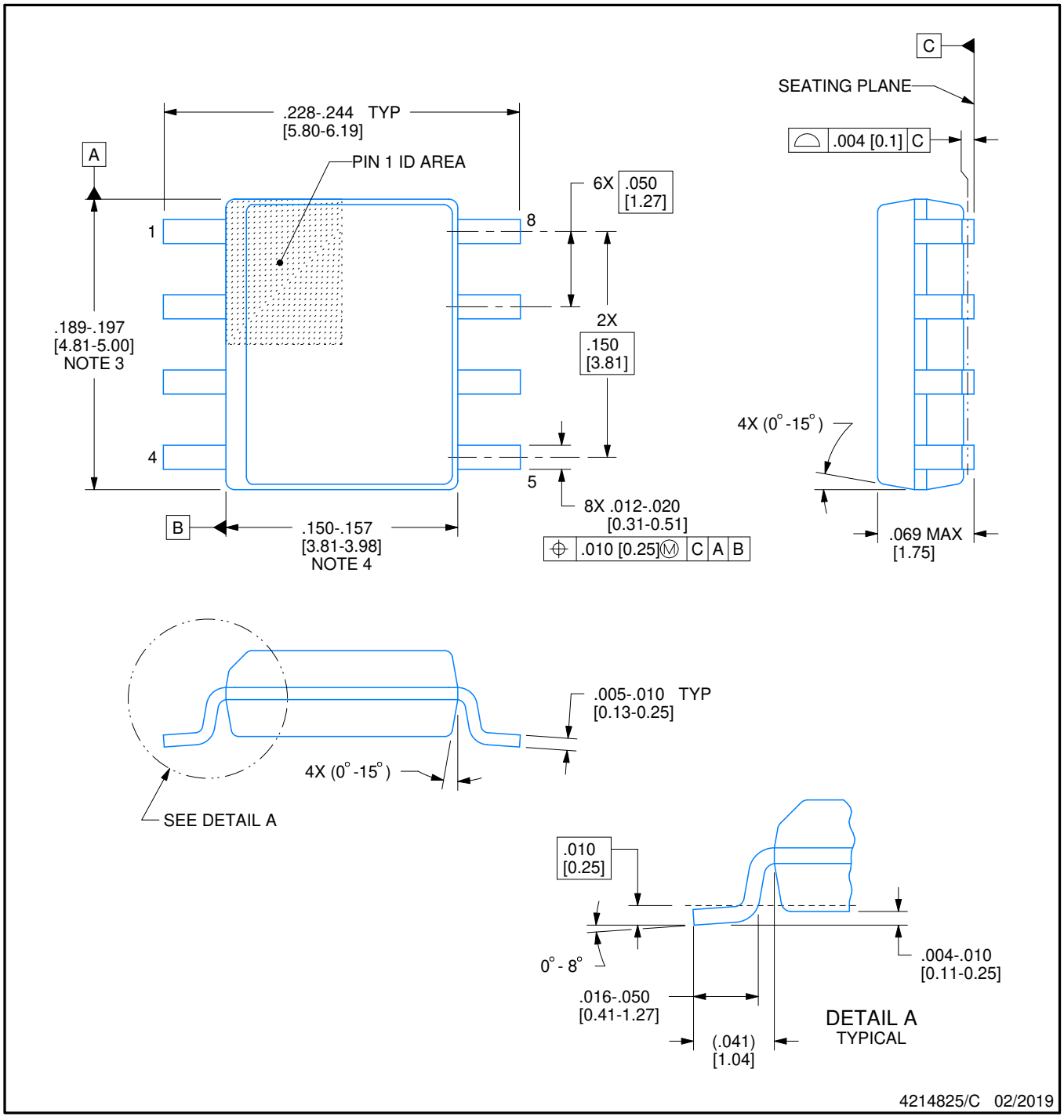


PACKAGE OUTLINE

D0008A

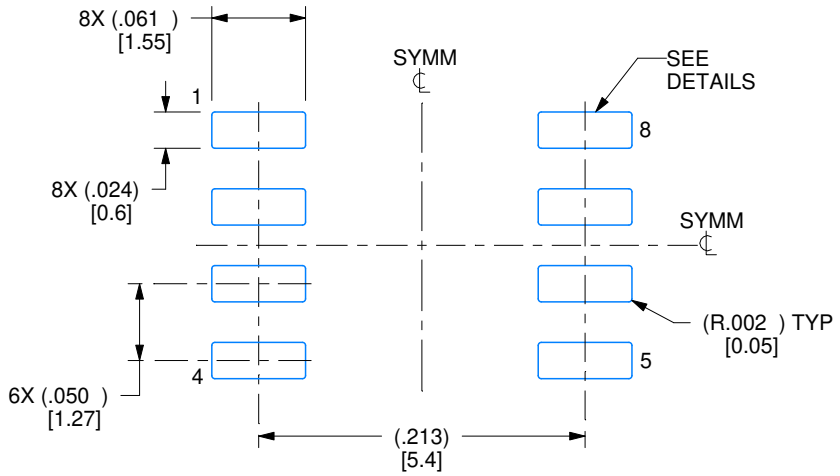
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

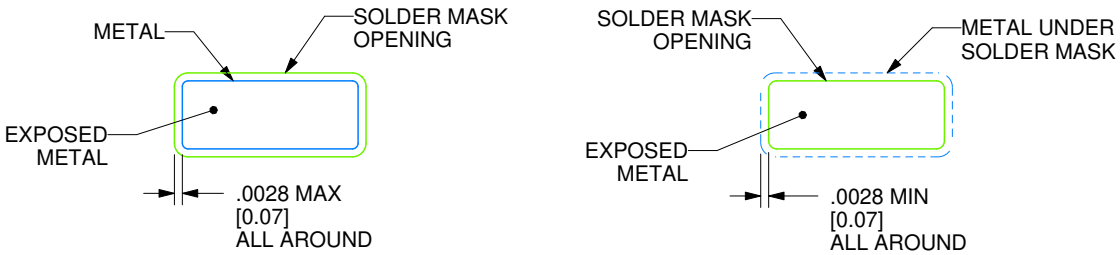


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

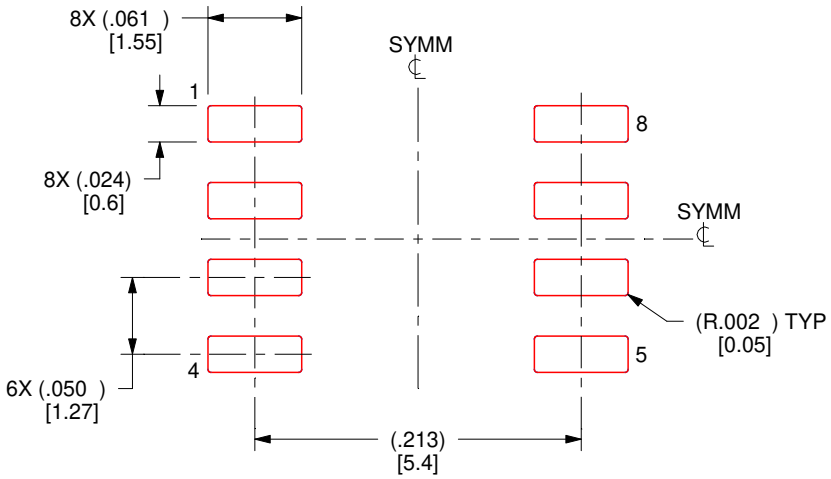
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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