

PGA305 Signal Conditioner and Transmitter for Pressure Sensors

1 Features

- Analog Features
 - Analog Front-End for Resistive Bridge Sensors
 - Accommodates Sensor Sensitivities From 1 mV/V to 135 mV/V
 - On-Chip Temperature Sensor
 - Programmable Gain
 - 24-Bit Sigma-Delta Analog-to-Digital Converter for Signal Channel
 - 24-Bit Sigma-Delta Analog-to-Digital Converter for Temperature Channel
 - 14-Bit Output DAC
- Digital Features
 - < 0.1% FSO Accuracy Across Temperature
 - System Response Time < 220 μ s
 - Third-Order Offset, Gain, and Nonlinearity Temperature Compensation
 - Diagnostic Functions
 - Integrated EEPROM for Device Operation, Calibration Data and User Data
- Peripheral Features
 - I²C interface for Data Reading and Device Configuration
 - One-Wire Interface Enables Communication Through the Power Supply Pin Without Using Additional Lines
 - 4-mA to 20-mA Current Loop Interface
 - Ratiometric and Absolute Voltage Output
 - Power Management Control
 - Analog Low-Voltage Detect
- General Features

- Industrial Temperature Range: -40°C to 150°C
- Power Supply:
 - On-Chip Power Management Accepts Wide Power-Supply Voltage From 3.3 V to 30 V
 - Integrated Reverse-Protection Circuit

2 Applications

- Pressure-Sensor Transmitters and Transducers
- Liquid-Level Meter, Flow Meters
- Resistive Field Transmitters

3 Description

The PGA305 device supplies an interface for piezoresistive and strain-gauge pressure-sense elements. The device is a full system-on-chip (SoC) solution that includes programmable analog front end (AFE), ADC, and digital signal processing that enable direct connection to the sense element. The PGA305 device also includes integrated voltage regulators and an oscillator to minimize the number of external components. The PGA305 device can employ third-order temperature and nonlinearity compensation to achieve high accuracy. The device can also use the integrated I²C interface or the one-wire serial interface (OWI) to achieve external communication and simplify the system calibration process. An Integrated DAC supports absolute-voltage, ratiometric-voltage, and 4-mA to 20-mA current-loop outputs.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| PAG305 | VQFN (36) | 6.00 mm × 6.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PGA305 Simplified Block Diagram

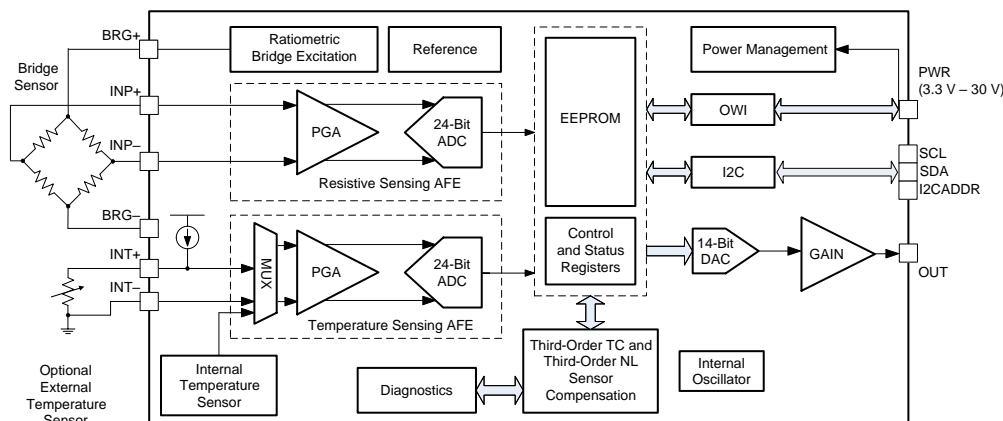


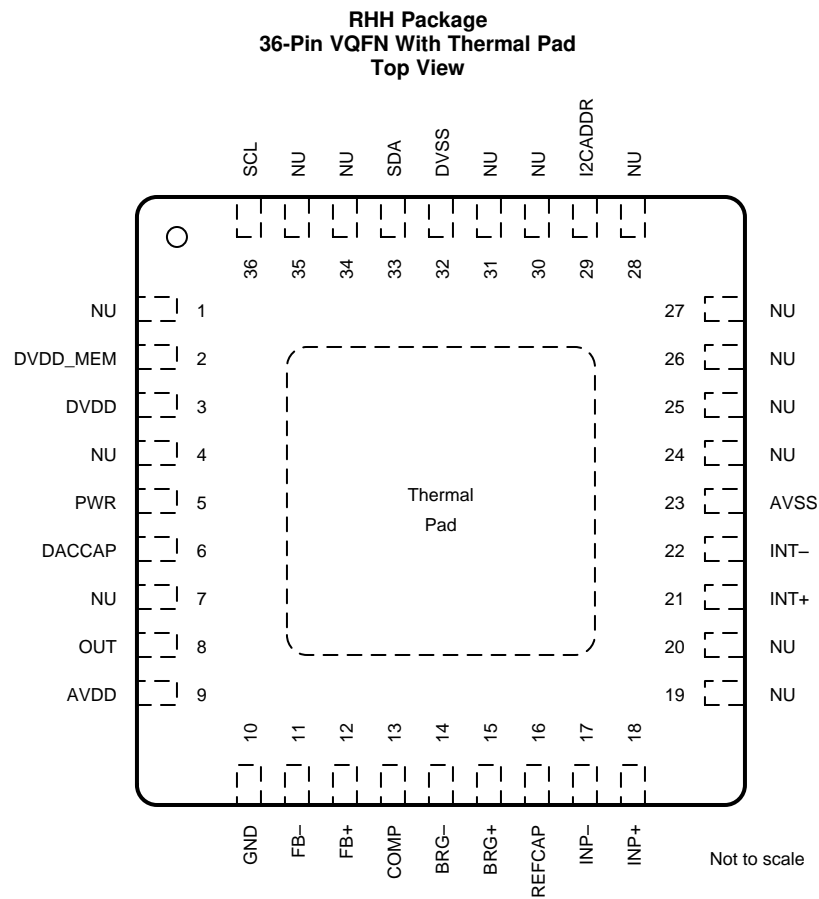
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4 Revision History

| DATE | REVISION | NOTES |
|-------------|----------|------------------|
| August 2018 | * | Initial release. |

5 Pin Configuration and Functions



NU = Make no external connection.

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------------|---|-----|---|
| NAME | NO. | | |
| AVDD | 9 | O | AVDD regulator output. |
| AVSS | 23 | — | Analog ground. |
| BRG+ | 15 | O | Bridge drive, positive. |
| BRG– | 14 | O | Bridge drive, negative. |
| COMP | 13 | I | Output amplifier compensation. |
| DACCAP | 6 | O | DAC capacitor. |
| DVDD | 3 | O | DVDD regulator output. |
| DVDD_MEM | 2 | O | Power supply for EEPROM and OTP. |
| DVSS | 32 | — | Digital ground. |
| FB+ | 12 | I | Feedback, positive. |
| FB– | 11 | I | Feedback, negative. |
| GND | 10 | — | Ground. |
| I2CADDR | 29 | I | I ² C chip address select. |
| INP+ | 18 | I | Resistive sensor positive input. |
| INP– | 17 | I | Resistive sensor negative input. |
| INT+ | 21 | I | External temperature sensor positive input. |
| INT– | 22 | I | External temperature sensor negative input. |
| NU | 1, 4, 7, 19, 20, 24 to 28, 30, 31, 34, 35 | — | Do not connect. |
| OUT | 8 | O | DAC gained output. |
| PWR | 5 | I | Input power supply. |
| REFCAP | 16 | O | ADC reference capacitor. |
| SCL | 36 | I/O | I ² C clock. |
| SDA | 33 | I/O | I ² C data. |
| Thermal pad | — | — | Connect to analog ground. |

6 Specifications

6.1 Absolute Maximum Ratings

see ⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------------------------|---|------|------------------------|------|
| PWR | Supply voltage | -28 | 33 | V |
| | Voltage at sensor input pins: INP+, INP-, INT+, INT- | -0.3 | 2 | V |
| | Voltage at AVDD, AVSS, BRG+, BRG-, COMP, DACCAP, DVDD, DVDD_MEM, DVSS, FB-, GATE, REFCAP, SCL, SDA, I2CADDR | -0.3 | 3.6 | V |
| | Voltage at FB+ pin | -2 | V _{PWR} + 0.3 | V |
| | Voltage at OUT pin | -0.3 | 33 | V |
| I _{PWR, short on OUT pin} | Supply current | | 25 | mA |
| T _{Jmax} | Maximum junction temperature | | 155 | °C |
| T _{stg} | Storage temperature | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|------------------|--|--|-----|-----|------------------|------|
| V _{PWR} | Power supply voltage | | 3.3 | | 30 | V |
| | Slew rate | V _{DD} = 0 to 30 V | | | 0.5 | V/μs |
| I _{PWR} | Power supply current - normal operation | No load on BRG, no load on DAC | | 2.5 | | mA |
| | Power supply current - EEPROM programming | While EEPROM is being programmed, no load on BRG, no load on DAC | | | 9 ⁽¹⁾ | |
| T _A | Operating ambient temperature | | -40 | | 150 | °C |
| | Programming temperature | EEPROM | -40 | | 140 | °C |
| | Start-up time (including analog and digital) | V _{PWR} ramp rate 0.5 V/μs | | | 1 | ms |
| | Capacitor on PWR pin | | 10 | | | nF |

- (1) Programming of the EEPROM results in an additional 6 mA of current on the PWR pin.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | PGA305 | UNIT |
|-------------------------------|--|------------|------|
| | | RHH (VQFN) | |
| | | 36 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 30.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 16.4 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 5.4 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 5.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics – Reverse Voltage Protection

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|-----|-----|------|
| Reverse voltage | | -28 | | | V |
| Voltage drop across reverse voltage protection element | | | 20 | | mV |

6.6 Electrical Characteristics – Regulators

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--------------------------|-----|-----|-----|------|
| V _{AVDD} | AVDD voltage | | 3 | | V |
| V _{DVDD} | DVDD voltage – operating | | 1.8 | | V |

6.7 Electrical Characteristics – Internal Reference

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| High-voltage reference voltage ⁽¹⁾ | | | 1.2 | | V |
| Accurate reference voltage | | | 2.5 | | V |
| Capacitor value on REFCAP pin | | | 100 | | nF |

(1) TEMP_DRIFT = [(Value at TEMP – Value at 25°C) / (Value at 25°C × ΔTEMP)] × 10⁶.

6.8 Electrical Characteristics – Bridge Sensor Supply

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--------------------------|------|-----|------|
| BRG SUPPLY FOR RESISTIVE BRIDGE SENSORS | | | | | |
| V _{BRG+} – V _{BRG-} | Bridge supply control bit = 0b00, no load | | 2.5 | | V |
| | Bridge supply control bit = 0b01, no load | | 2 | | |
| | Bridge supply control bit = 0b10, no load | | 1.25 | | |
| I _{BRG} | Current supply to the bridge | | | 1.5 | mA |
| C _{BRG} | Capacitive load | R _{BRG} = 20 kΩ | | 2 | nF |

6.9 Electrical Characteristics – Temperature Sensor Supply

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------------------|---------------------|-----|-----|------|
| I_{TEMP} SUPPLY FOR TEMPERATURE SENSOR | | | | | |
| I _{TEMP} | Current supply to temperature sensor | Control bit = 0b000 | | 25 | μA |
| | | Control bit = 0b001 | | 50 | μA |
| | | Control bit = 0b010 | | 100 | μA |
| | | Control bit = 0b011 | | 500 | μA |
| | | Control bit = 0b1xx | | OFF | |
| C _{TEMP} | Capacitive load | | | 100 | nF |
| | Output impedance | | 15 | | MΩ |

6.10 Electrical Characteristics – Internal Temperature Sensor

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-----------------|-----|-----|-----|------|
| Temperature range | | -40 | | 150 | °C |

6.11 Electrical Characteristics – P Gain (Chopper Stabilized)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|-----------------|--------|-------|-----|------|
| Gain steps (5 bits) | 00000, at dc | | 5 | | V/V |
| | 00001 | | 5.48 | | |
| | 00010 | | 5.97 | | |
| | 00011 | | 6.56 | | |
| | 00100 | | 7.02 | | |
| | 00101 | | 8 | | |
| | 00110 | | 9.09 | | |
| | 00111 | | 10 | | |
| | 01000 | | 10.53 | | |
| | 01001 | | 11.11 | | |
| | 01010 | | 12.5 | | |
| | 01011 | | 13.33 | | |
| | 01100 | | 14.29 | | |
| | 01101 | | 16 | | |
| | 01110 | | 17.39 | | |
| | 01111 | | 18.18 | | |
| | 10000 | | 19.05 | | |
| | 10001 | | 20 | | |
| | 10010 | | 22.22 | | |
| | 10011 | | 25 | | |
| | 10100 | | 30.77 | | |
| | 10101 | | 36.36 | | |
| | 10110 | | 40 | | |
| | 10111 | | 44.44 | | |
| | 11000 | | 50 | | |
| 11001 | | 57.14 | | | |
| 11010 | | 66.67 | | | |
| 11011 | | 80 | | | |
| 11100 | | 100 | | | |
| 11101 | | 133.33 | | | |
| 11110 | | 200 | | | |
| 11111 | | 400 | | | |

Electrical Characteristics – P Gain (Chopper Stabilized) (continued)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|-----|-----------|------------------------|
| Gain bandwidth product | | | 10 | | MHz |
| Input-referred noise density ⁽¹⁾ | f = 0.1 Hz to 2 kHz, gain = 400 V/V, sampling rate = 128 μ s, across temperature | | 15 | | nV/ $\sqrt{\text{Hz}}$ |
| Input offset voltage | | | 10 | | μ V |
| Input bias current | | | 5 | | nA |
| Frequency response | Gain = 400 V/V, <1 kHz | | | ± 0.1 | %V/V |
| Common-mode voltage range | | Depends on selected gain, bridge supply and sensor span ⁽²⁾ | | | V |
| Common-mode rejection ratio | f _{CM} = 50 Hz at gain = 5 V/V | | 110 | | dB |
| Input impedance | | 10 | | | M Ω |

- (1) Total input-referred noise including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise.
 (2) **Common Mode at P Gain Input and Output:** There are two constraints:
 (a) The single-ended voltage of the positive and negative pins at the P gain input must be between 0.3 V and 1.8 V.
 (b) The single-ended voltage of the positive and negative pins at the P gain output must be between 0.1 V and 2 V.

6.12 Electrical Characteristics – P Analog-to-Digital Converter

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|------|------------------------|-----------|------|
| Sigma-delta modulator frequency | | | 1 | | MHz |
| ADC voltage input range | | -2.5 | | 2.5 | V |
| Number of bits | | | 24 | | bits |
| ADC 2s complement code for -2.5-V differential input | | | 800000 _{hex} | | |
| ADC 2s complement code for 0-V differential input | | | 000000 _{hex} | | |
| ADC 2s complement code for 2.5-V differential input | | | 7FFFFFF _{hex} | | |
| INL Integral nonlinearity | | | | ± 0.5 | LSB |

6.13 Electrical Characteristics – T Gain (Chopper Stabilized)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|--|------|-------|------------------------|
| Gain steps (2 bits) | Gain control bits = 0b00 at dc | | 1.33 | | V/V |
| | Gain control bits = 0b01 | | 2 | | |
| | Gain control bits = 0b10 | | 5 | | |
| | Gain control bits = 0b11 | | 20 | | |
| Gain bandwidth product | | | 350 | | kHz |
| Noise density ⁽¹⁾ | f = 0.1 Hz to 100 Hz at gain = 5 V/V, across temperature | | 110 | | nV/ $\sqrt{\text{Hz}}$ |
| Input offset voltage | | | 95 | | μ V |
| Input bias current | | | 5 | | nA |
| Frequency response | Gain = 20 V/V, <100 Hz | | | 0.335 | %V/V |
| Common mode voltage range | | Depends on selected gain and current supply ⁽²⁾ | | | |
| Common-mode rejection ratio | f _{CM} = 50 Hz | | 110 | | dB |
| Input impedance | | 1 | | | M Ω |

- (1) Total input-referred noise including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise.
 (2) **Common Mode at T Gain Input and Output:** There are two constraints:
 (a) The single-ended voltage of positive/negative pin at the T gain input should be between 5 mV and 1.8 V.
 (b) The single-ended voltage of positive/negative pin at the T gain output should be between 0.1 V and 2 V.

6.14 Electrical Characteristics – T Analog-to-Digital Converter

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------|------|------------------------|------|------|
| Sigma-delta modulator frequency | | | 1 | | MHz |
| ADC voltage input range | | -2.5 | | 2.5 | V |
| Number of bits | | | 24 | | bits |
| ADC 2s complement code for -2.5-V differential input | 2s complement | | 800000 _{hex} | | LSB |
| ADC 2s complement code for 0-V differential input | | | 000000 _{hex} | | LSB |
| ADC 2s complement code for 2.5-V differential input | | | 7FFFFFF _{hex} | | LSB |
| INL | Integral nonlinearity | | | ±0.5 | LSB |

6.15 Electrical Characteristics – One-Wire Interface

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------------------------|------|-----|------|------|
| Communication baud rate ⁽¹⁾ | | 600 | | 9600 | bps |
| OWI_ENH | OWI activation high | 5.95 | | | V |
| OWI_ENL | OWI activation low | | | 5.75 | V |
| OWI_VIH | OWI transceiver Rx threshold for high | 4.8 | | 5.1 | V |
| OWI_VIL | OWI transceiver Rx threshold for low | 3.9 | | 4.2 | V |
| OWI_IOH | OWI transceiver Tx threshold for high | 500 | | 1379 | µA |
| OWI_IOL | OWI transceiver Tx threshold for low | 2 | | 5 | µA |

(1) OWI over power line does not work if there is an LDO between the supply to the sensor and the PWR pin, or if the OWI high and low voltages are greater than the regulated voltage.

6.16 I²C Interface

over operating free-air temperature range at $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------------------|---|-----|----------------------|------|
| V_{IH} | High-level input voltage | $0.7 \times AV_{DD}$ | | | V |
| V_{IL} | Low-level input voltage | | | $0.3 \times AV_{DD}$ | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 3\text{ mA}$, I ² C RATE configuration bit = 0 | | 0.4 | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 20\text{ mA}$, I ² C RATE configuration bit = 1 | | 0.4 | V |
| f_{SCL} | SCL clock frequency | | 400 | 800 | KBPS |

6.17 Electrical Characteristics – DAC Output

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---------------------------------|-----|-----------------------|-----|------|
| DAC reference voltage | Reference bit = 1 | | 1.25 | | V |
| | Reference bit = 0 (ratiometric) | | $0.25 \times V_{PWR}$ | | |
| DAC resolution | | | 14 | | bits |

6.18 Electrical Characteristics – DAC Gain

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|------|-----|-------|
| Buffer gain (see Figure 20) | 2× | | 2 | | V/V |
| | 4× | | 4 | | |
| | 6.67× | | 6.67 | | |
| | 10× | | 10 | | |
| Current loop gain | | | 1001 | | mA/mA |

Electrical Characteristics – DAC Gain (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|-----|-----|------|------|
| Gain-bandwidth product | | | | 1 | | MHz |
| Zero-code voltage (gain = 4×) | | DAC code = 0000h, I _{DAC} = 2.5 mA | | | 20 | mV |
| Full-code voltage (gain = 4×) | | DAC code is 1FFFh, I _{DAC} = –2.5 mA | 4.8 | | | V |
| Output current | | DAC code = 1FFFh, DAC code = 0000h | | | ±2.5 | mA |
| Short-circuit source current | | DAC code = 1FFFh | | 27 | | mA |
| Short-circuit sink current | | DAC code = 0000h | | 27 | | mA |
| Maximum capacitance | | Without compensation | | | 100 | pF |
| | | With compensation | | | 100 | nF |

6.19 Electrical Characteristics – Non-Volatile Memory

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------------|-----------------|-----|-----|------|--------|
| EEPROM | Size | | | 128 | | bytes |
| | Erase-write cycles | | | | 1000 | cycles |
| | Programming time | 1 8-byte page | | | 8 | ms |
| | Data retention | | 10 | | | years |

6.20 Electrical Characteristics – Diagnostics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------|---|-----------------|-----|-----|------|-----|-------------------------|
| OSC_PWR_OV | Oscillator circuit supply overvoltage threshold | | | | 3.3 | | V |
| OSC_PWR_UV | Oscillator circuit supply undervoltage threshold | | | | 2.7 | | V |
| BRG_OV | Resistive bridge sensor supply overvoltage threshold | | | | 10 | | %V _{BRG} |
| BRG_UV | Resistive bridge sensor supply undervoltage threshold | | | | –10 | | %Prog. V _{BRG} |
| AVDD_OV | AVDD overvoltage threshold | | | | 3.3 | | V |
| AVDD_UV | AVDD undervoltage threshold | | | | 2.7 | | V |
| DVDD_OV | DVDD overvoltage threshold | | | | 2 | | V |
| DVDD_UV | DVDD undervoltage threshold | | | | 1.53 | | V |
| REF_OV | Reference overvoltage threshold | | | | 2.75 | | V |
| REF_UV | Reference undervoltage threshold | | | | 2.25 | | V |
| P_DIAG_PU | P gain input diagnostics pulldown resistor value | | PD2 | PD1 | | | MΩ |
| | | | 0 | 0 | 1 | | |
| | | | 0 | 1 | 2 | | |
| | | | 1 | 0 | 3 | | |
| | | | 1 | 1 | 4 | | |

Electrical Characteristics – Diagnostics (continued)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT | | | | | |
|----------------|--|---|---------|---------|---------|-----|-------------------|------|--------------------------|---|---|---|------|
| INP_OV | P gain input overvoltage threshold value | INP+ and INP– each has threshold comparator | THRS[2] | THRS[1] | THRS[0] | | %V _{BRG} | | | | | | |
| | | | | | | | | | V _{BRG} = 2.5 V | 0 | 0 | 0 | 72.5 |
| | | | | | | | | | | 0 | 0 | 1 | 70 |
| | | 0 | 1 | 0 | 65 | | | | | | | | |
| | | V _{BRG} = 2 V | 0 | 1 | 1 | | | | 90 | | | | |
| | | | 1 | 0 | 0 | | | | 87.5 | | | | |
| | | | 1 | 0 | 1 | | | | 82.5 | | | | |
| | | V _{BRG} = 1.25 V | 1 | 1 | 0 | | | | 100 | | | | |
| | | | 1 | 1 | 1 | | | | 95 | | | | |
| | | | | | | | | | | | | | |
| INP_UV | P gain input undervoltage threshold value | INP+ and INP– each has threshold comparator | THRS[2] | THRS[1] | THRS[0] | | %V _{BRG} | | | | | | |
| | | | | | | | | | V _{BRG} = 2.5 V | 0 | 0 | 0 | 7.5 |
| | | | | | | | | | | 0 | 0 | 1 | 10.0 |
| | | 0 | 1 | 0 | 15.0 | | | | | | | | |
| | | V _{BRG} = 2 V | 0 | 1 | 1 | | | | 10.0 | | | | |
| | | | 1 | 0 | 0 | | | | 12.5 | | | | |
| | | | 1 | 0 | 1 | | | | 17.5 | | | | |
| | | V _{BRG} = 1.25 V | 1 | 1 | 0 | | | | 17.5 | | | | |
| | | | 1 | 1 | 1 | | | | 22.5 | | | | |
| | | | | | | | | | | | | | |
| INT_OV | T gain input overvoltage | INT+ and INT– each has threshold comparator | | | 2.1 | | | V | | | | | |
| PGAIN_OV | Output overvoltage (single-ended) threshold for P gain | | | | 2.25 | | | V | | | | | |
| PGAIN_UV | Output undervoltage (single-ended) threshold for P gain | | | | 0.15 | | | V | | | | | |
| TGAIN_OV | Output overvoltage (single-ended) threshold for T gain | | | | 2.25 | | | V | | | | | |
| TGAIN_UV | Output undervoltage (single-ended) threshold for T gain | | | | 0.15 | | | V | | | | | |
| HARNESS_FAULT1 | Open-wire leakage current 1. Open PWR with pullup on OUT | | | | 2 | | | μA | | | | | |
| HARNESS_FAULT2 | Open-wire leakage current 2. Open GND with pulldown on OUT | | | | 20 | | | μA | | | | | |

6.21 Operating Characteristics

over operating ambient temperature range (unless otherwise noted). Start-up time and response time testing performed in 0-5V absolute voltage mode.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|-----|------|-----|------|
| Start-up time ⁽¹⁾ | No IIR filter, Vout step 0 to 2.5 V | | 9.6 | | ms |
| Start-up time ⁽²⁾ | IIR filter = 320Hz, Vout step 0 to 2.5 V | | 10.8 | | ms |
| Output rate | | | 512 | | μs |
| Response time ⁽³⁾ | No IIR filter, Vout step 0 to 2.5 V | | 1700 | | μs |

(1) Time from power up to reach 90% of valid output.

(2) Time from power up to reach valid output, including settling time.

(3) Time to reach 90% of valid output.

Operating Characteristics (continued)

over operating ambient temperature range (unless otherwise noted). Start-up time and response time testing performed in 0-5V absolute voltage mode.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|------|-----|------|
| Response time ⁽⁴⁾ | IIR filter = 320Hz, Vout step 0 to 2.5 V | | 2680 | | μs |
| Absolute-voltage mode, overall accuracy (PGA305 only, no sense element) ⁽⁵⁾ | 3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration | | 0.13 | | %FSO |
| | 3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration | | 0.08 | | |
| | 4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration | | 0.08 | | |
| Ratiometric-voltage mode, overall accuracy (PGA305, no sense element) ⁽⁵⁾ | 3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration | | 0.15 | | %FSO |
| | 3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration | | 0.13 | | |
| | 4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration | | 0.10 | | |
| Current mode, overall accuracy (PGA305, no sense element) ⁽⁵⁾ | 3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration | | 0.18 | | %FSO |
| | 3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration | | 0.08 | | |
| | 4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration | | 0.06 | | |

(4) Time to reach valid output, including settling time.

(5) Sense element held at constant temperature while the PGA305 device was calibrated at –25°C, 25°C, 85°C and 125°C. Accuracy was then measured at –40°C, 50°C and 150 °C.

6.22 I²C Interface Timing Requirements

| | | MIN | TYP | MAX | UNIT |
|-------------|-----------------------------|------|-----|-----|---------|
| t_{STASU} | START condition set-up time | 500 | | | ns |
| t_{STAHD} | START condition hold time | 500 | | | ns |
| t_{LOW} | SCL low time | 1.25 | | | μ s |
| t_{HIGH} | SCL high time | 1.25 | | | μ s |
| t_{RISE} | SCL and SDA rise time | | | 7 | ns |
| t_{FALL} | SCL and SDA fall time | | | 7 | ns |
| t_{DATSU} | Data setup time | 500 | | | ns |
| t_{DATHD} | Data hold time | 500 | | | ns |
| t_{STOSU} | STOP condition set-up time | 500 | | | ns |

6.23 Timing Diagram

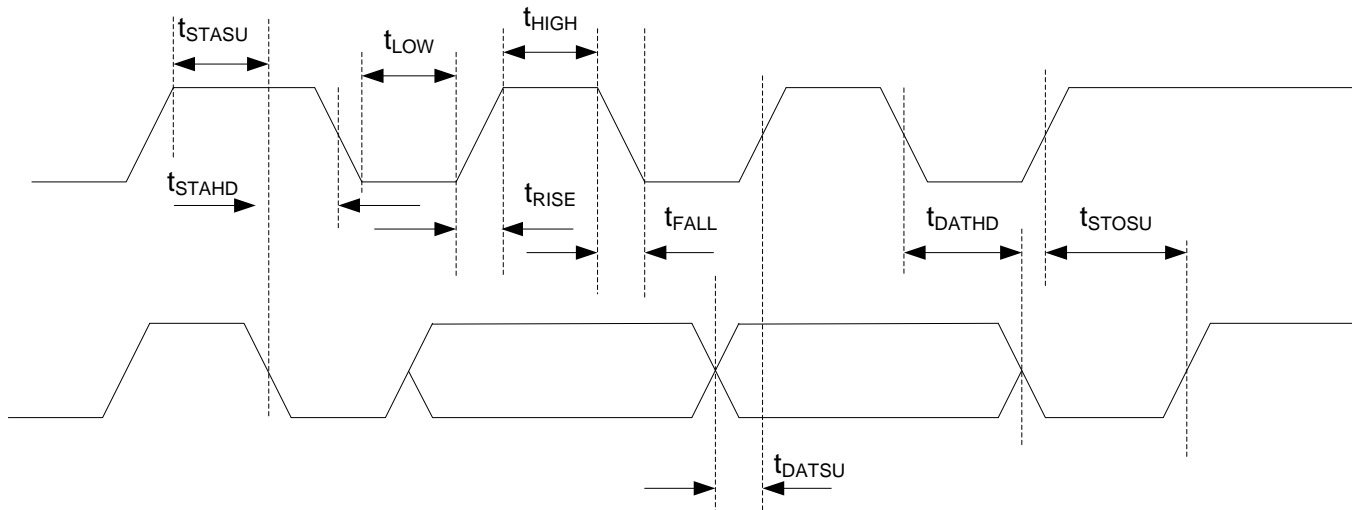
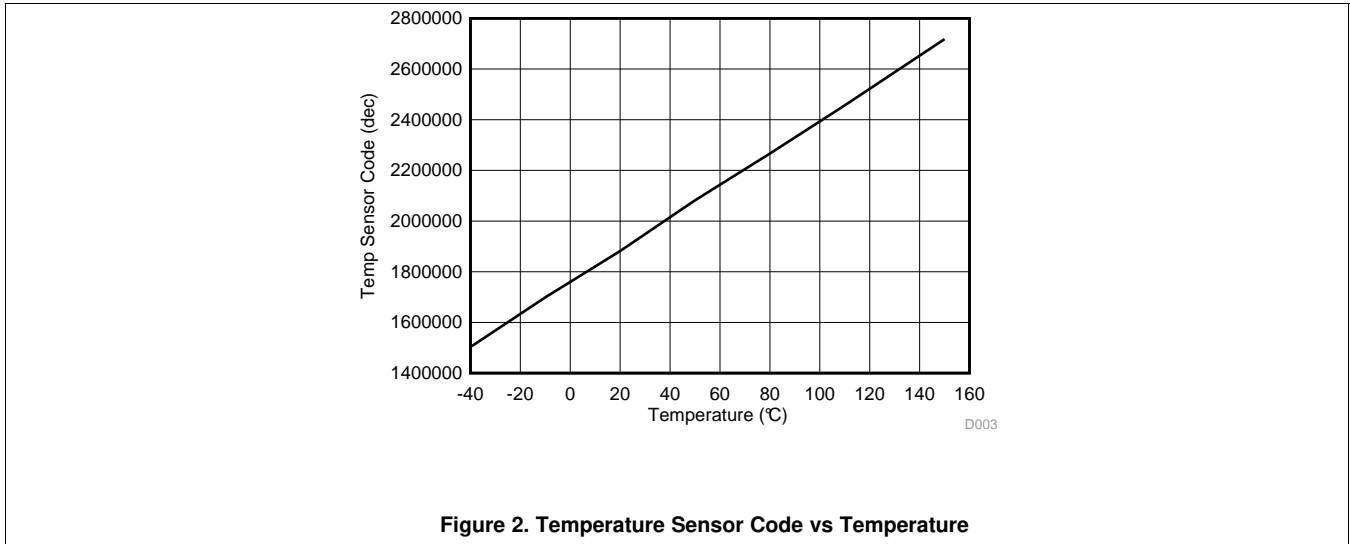


Figure 1. I²C Timing

6.24 Typical Characteristics



7 Detailed Description

7.1 Overview

The PGA305 device can be used in a variety of applications. The most common ones are for pressure and temperature measurement. Depending on the application, the device itself can be configured in different modes. These sections give information regarding these configurations.

The PGA305 device is a high-accuracy, low-drift, low-noise, low-power, and easily programmable signal-conditioner device for resistive-bridge pressure and temperature-sensing applications. The PGA305 device implements a third-order temperature coefficient (TC) and nonlinearity (NL) algorithm to linearize the analog output. The PGA305 device accommodates various sensing element types, such as piezoresistive, ceramic film, and steel membrane. It supports the sensing element spans from 1 mV/V to 135 mV/V. The typical applications supported are pressure sensor transmitters, transducers, liquid-level meters, flow meters, strain gauges, weight scales, thermocouples, thermistors, two-wire resistance thermometers (RTD), and resistive field transmitters. The device can also be used in accelerometer and humidity sensor signal-conditioning applications.

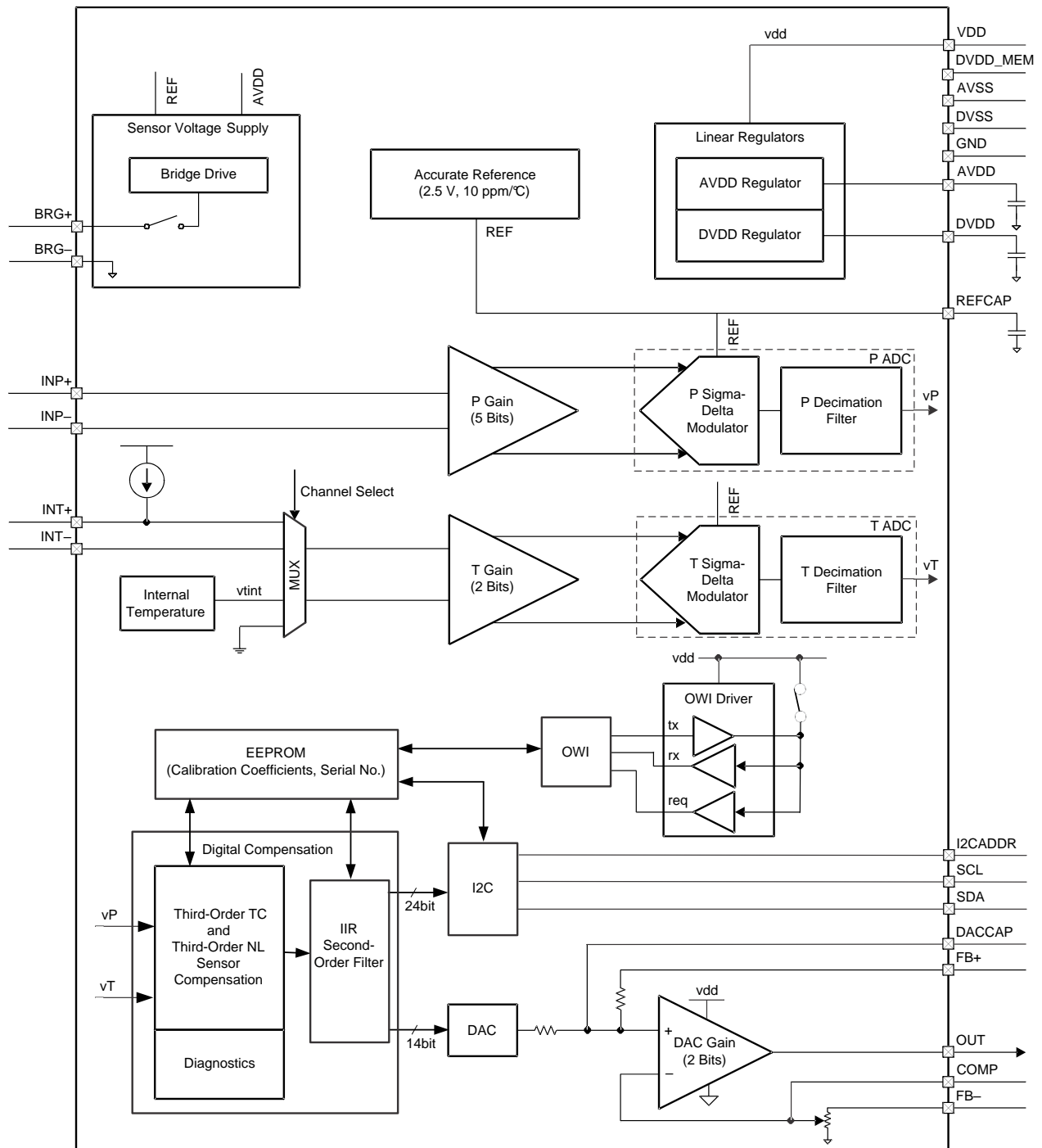
The PGA305 device provides bridge excitation voltages of 2.5 V, 2 V, and 1.25 V, all ratiometric to the ADC reference level. The PGA305 device has the unique one-wire interface (OWI) that supports communication and configuration through the power-supply line during the calibration process. This feature minimizes the number of wires necessary for an application.

The PGA305 device contains two separated analog front-end (AFE) chains for resistive-bridge inputs and temperature-sensing inputs. Each AFE chain has its own gain amplifier and a 16-bit ADC at a 7.8-kHz output rate. The resistive-bridge input AFE chain consists of a programmable gain with 32 steps from 5 V/V to 400 V/V. For the temperature-sensing AFE input chain, the PGA305 device provides a current source that can supply up to 500 μ A for optional external temperature sensing. This current source can also be used as constant-current bridge excitation. The programmable gain in the temperature-sensing chain has four steps from 1.33 V/V to 20 V/V. In addition, the PGA305 device integrates an internal temperature sensor that can be configured as the input of the temperature-sensing AFE chain.

A 128-byte EEPROM is integrated in the PGA305 device to store the calibration coefficients and the PGA305 configuration settings as needed. The PGA305 device has an integrated I²C interface used for data capture and also for device configuration. In addition, 14-bit DAC followed by a buffer gain stage of 2 V/V to 10 V/V. The device supports industrial-standard ratiometric-voltage output, absolute-voltage output, and 4-mA to 20-mA current loop.

The diagnostic function monitors the operating condition of the PGA305 device. The device can operate with a 3.3-V to 30-V power supply directly without using an external LDO. The PGA305 device has a wide ambient-temperature operating range from -40°C to 150°C . The package form is 6-mm \times 6-mm, 36-pin VQFN. In this small package size, the PGA305 device has integrated all the functions necessary for resistive-bridge sensing applications to minimize the PCB area and simplify the overall application design.

7.2 Functional Block Diagram



7.3 Feature Description

This section describes individual functional blocks of the PGA305 device.

7.3.1 Reverse-Voltage Protection Block

The PGA305 device includes a reverse-voltage protection block. This block protects the device from reverse-battery conditions on the external power supply.

7.3.2 Linear Regulators

The PGA305 device has two main linear regulators: an AVDD regulator and a DVDD regulator. The AVDD regulator supplies the 3-V voltage source for internal analog circuitry, while the DVDD regulator supplies the 1.8-V regulated voltage for the digital circuitry. The user must connect bypass capacitors of 100 nF each to the AVDD and DVDD pins of the device.

7.3.3 Internal Reference

The PGA305 device has two internal references. These references are given in these subsections.

7.3.3.1 High-Voltage Reference

The high-voltage reference is an inaccurate reference used in the diagnostic thresholds.

7.3.3.2 Accurate Reference

The accurate reference is used to generate reference voltage for the P ADC, T ADC and DAC. TI recommends to place a 100-nF capacitor on the REFCAP pin to limit the bandwidth of reference noise.

The user can set the ADC_EN_VREF bit in the ALPWR register to 0 to disable the accurate reference buffer. This allows the user to connect an external single-ended reference voltage to the REFCAP pin and then supply the reference voltage to the ADCs and the DAC. Note that the default power-up state of ADC_EN_VREF is such that the reference buffer is disabled.

NOTE

The accurate reference is valid 50 μ s after the digital core starts running at power up.

7.3.4 BRG+ to BRG– Supply for the Resistive Bridge

The sensor voltage-supply block of the PGA305 device supplies power to the resistive-bridge sensor. Use the BRG_CTRL bits in the BRG_CTRL register to configure the sensor supply in the PGA305 device to a 2.5-V, 2-V, or 1.25-V nominal output supply. These three output supply options can accommodate bridge sense elements with different resistor values. This nominal supply is ratiometric to the accurate reference as shown in [Figure 3](#).

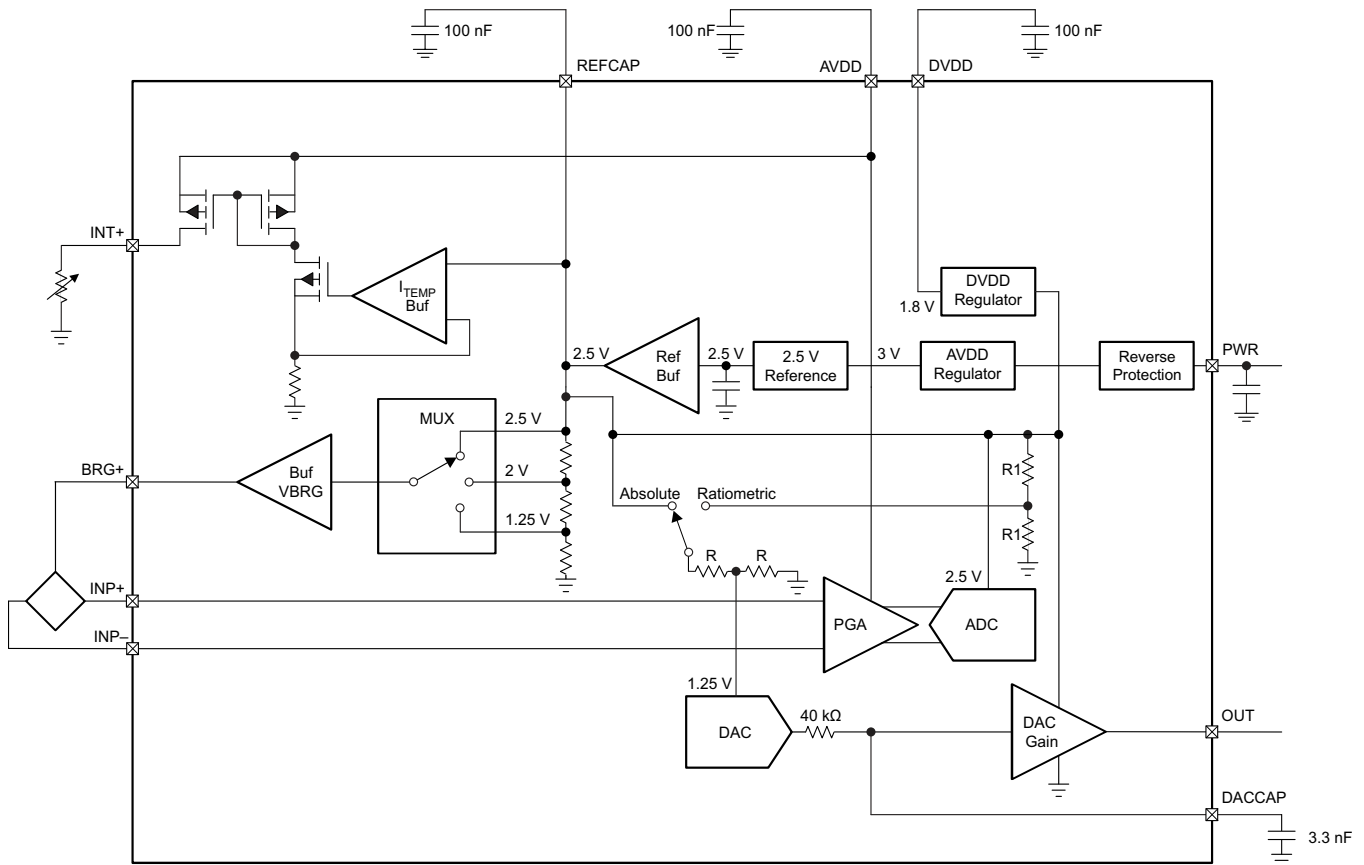
Feature Description (continued)


Figure 3. Bridge Supply and P ADC Reference are Ratiometric

The sensor drive includes a switch. This switch can be used to turn off power to the sense element.

7.3.5 ITEMP Supply for the Temperature Sensor

The ITEMP block in PGA305 device supplies programmable current to an external temperature sensor, such as an RTD temperature probe or NTC or PTC thermistor. The temperature-sensor current source is ratiometric to the accurate reference.

Use the ITEMP_CTRL bits in the TEMP_CTRL register to program the value of the current.

7.3.6 Internal Temperature Sensor

PGA305 device includes an internal temperature sensor whose voltage output is digitized by the T ADC and made available to the microprocessor. This digitized value is used to implement temperature compensation algorithms in software. Note that the voltage generated by the internal temperature sensor is proportional to the junction temperature.

Feature Description (continued)

Figure 4 shows the internal temperature sensor AFE.

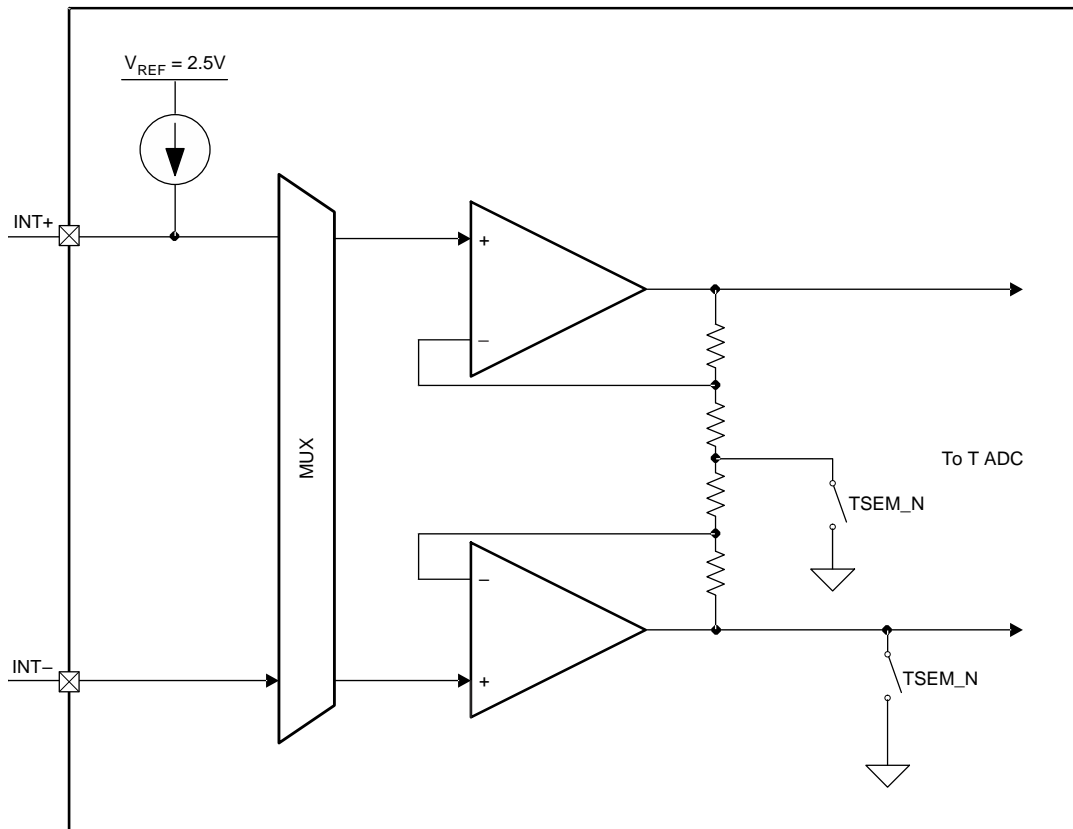


Figure 4. Temperature Sensor AFE

7.3.7 P Gain

P gain is designed with precision, low-drift, low-flicker-noise, chopper-stabilized amplifiers. P gain is implemented as an instrument amplifier as shown in [Figure 5](#).

Feature Description (continued)

The user can use five bits in the P_GAIN_SELECT register to adjust the gain of this stage to accommodate sense elements with a wide range of signal spans.

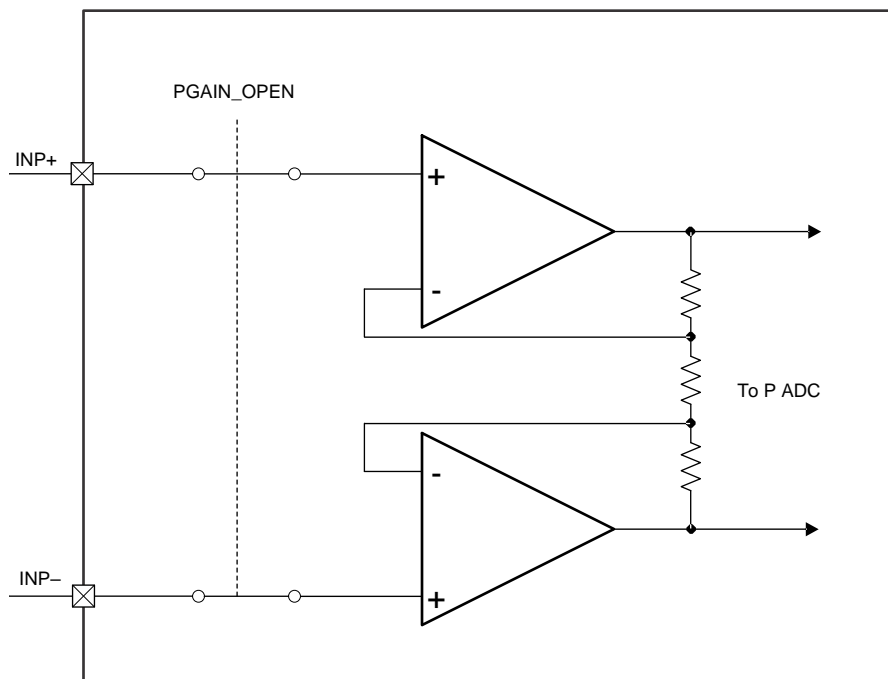


Figure 5. P Gain

7.3.8 P Analog-to-Digital Converter

The P analog-to-digital converter digitizes the voltage output of the P-gain amplifier.

7.3.8.1 P Sigma-Delta Modulator for P ADC

The sigma-delta modulator for P ADC is a 1-MHz, second-order, 3-bit quantizing sigma-delta modulator.

7.3.8.2 P Decimation Filter for P ADC

The pressure signal path internal conversion time is 128 μ s.

The output of the decimation filter in the pressure signal path is a 24-bit *signed* value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in [Table 1](#).

Table 1. Input Voltage to Output Counts for the P ADC

| SIGMA-DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE (V) | 24-BIT NOISE-FREE DECIMATOR OUTPUT |
|--|---------------------------------------|
| -2.5 | -8 388 608 (0x800000) |
| -1.25 | -4 194 304 (0xC00000) |
| 0 | 0 (0x000000) |
| 1.25 | 4 194 303 (0x3FFFFFF) |
| 2.5 | 8 388 607 (0x7FFFFFF) |

7.3.9 T Gain

The device has the ability to perform temperature compensation through an internal or external temperature sensor. The user can select the source of the temperature measurement with the TEMP_MUX_CTRL bits in TEMP_CTRL register. Note that the device connects to an external temperature sensor through the INT+ and INT- pins.

The T gain block is constructed with a low-flicker-noise, low-offset, chopper-stabilized amplifier. The gain is configurable with two bits in the T_GAIN_SELECT register. Figure 6 shows the T-gain amplifier topology.

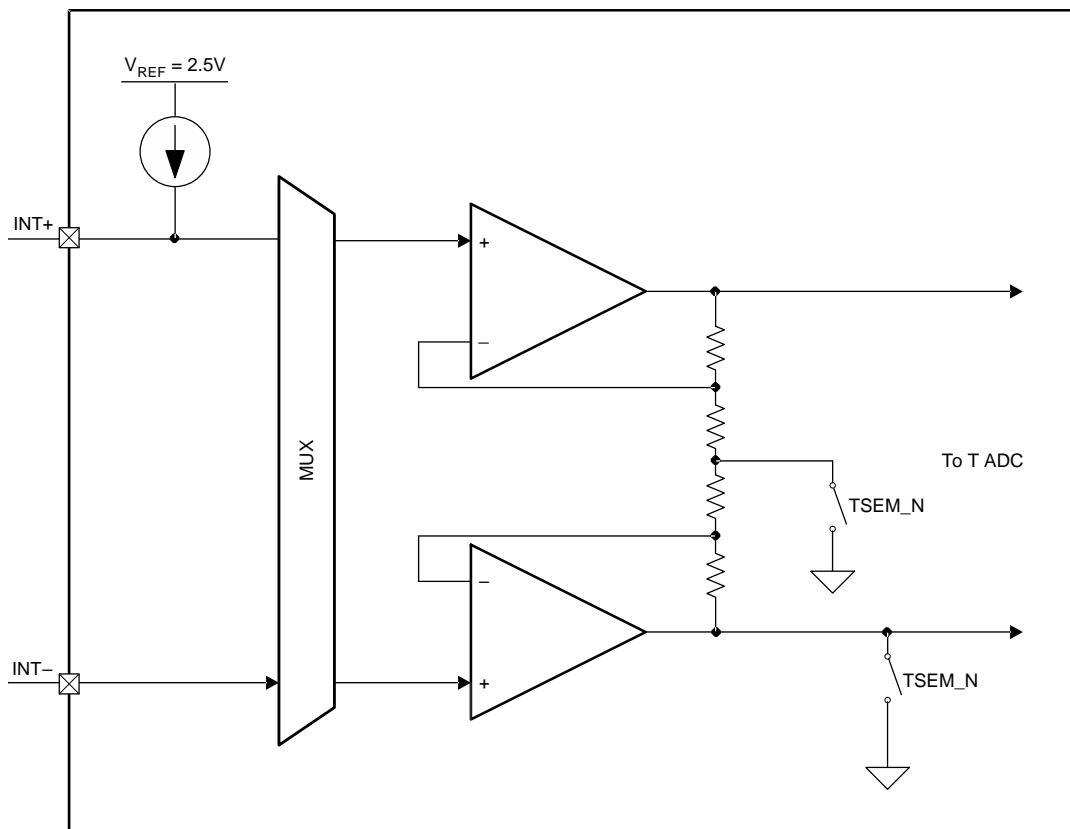


Figure 6. Temperature Sensor AFE

The T-gain amplifier can be configured for single-ended or differential operation using the TSEM_N bit in the AMUX_CTRL register. Note that when the T-gain amplifier is set up for single-ended operation, the differential voltage converted by the T ADC is with respect to ground. Table 2 shows the configuration that the user must select for the different temperature sources.

Table 2. T-Gain Configuration

| TEMPERATURE SOURCE | T GAIN CONFIGURATION |
|---|----------------------|
| Internal temperature sensor | Single-ended |
| External temperature sensor with one terminal of the sensor connected to ground | Single-ended |
| External temperature sensor with neither terminal of the sensor connected to ground | Differential |

The T-gain amplifier must be set up for either the single-ended or differential configuration, depending on the source of signal to the T gain.

NOTE

When T GAIN is configured to measure the internal temperature-sensor output, T GAIN must be configured to operate in single-ended mode and with a gain of 5 V/V.

7.3.10 T Analog-to-Digital Converter

The T analog-to-digital converter is for digitizing the T-gain amplifier output. The digitized value is available in the TADC_DATA2 and TADC_DATA3 registers.

7.3.10.1 T Sigma-Delta Modulator for T ADC

The sigma-delta modulator for T ADC is a 1-MHz, second-order, 3-bit quantizing sigma-delta modulator.

7.3.10.2 T Decimation Filters for T ADC

The temperature signal path contains a decimation filter with an internal output rate of 128 μ s.

The output of the decimation filter in the temperature signal path is 24-bit **signed** value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in [Table 3](#).

Table 3. Input Voltage to Output Counts for T ADC

| SIGMA-DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE | 24-BIT NOISE-FREE DECIMATOR OUTPUT |
|--|------------------------------------|
| -2.5 V | -8 388 608 (0x800000) |
| -1.25 V | -4 194 304 (0xC00000) |
| 0 V | 0 (0x000000) |
| 1.25 V | 4 194 303 (0x3FFFFFF) |
| 2.5 V | 8 388 607 (0x7FFFFFF) |

The nominal relationship between the device junction temperature and 24-bit T ADC Code for T GAIN = 5 V/V is shown in [Equation 1](#).

$$\text{T ADC Code} = 6632.1 \times \text{TEMP} + 1710281.3,$$

where

- TEMP is temperature in $^{\circ}\text{C}$ (1)

7.3.11 P GAIN and T GAIN Calibration

The P_GAIN value should be set based on the maximum bridge output voltage. The maximum bridge voltage is the maximum sum of bridge offset and bridge span across the entire operating temperature range.

The T_GAIN value should be set based on the temperature sense element. The specific values to be used are:

- For the internal temperature sensor, set T_GAIN to 5 V/V gain.
- For an external temperature sensor such as a PTC thermistor, set T_GAIN to 20 V/V gain.

7.3.12 One-Wire Interface (OWI)

The device includes an OWI digital communication interface. The function of OWI is to enable writes to and reads from all memory locations inside the PGA305 device that are available for OWI access.

7.3.12.1 Overview of OWI

The OWI digital communication is a master-slave communication link in which the PGA305 device operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until it is commanded to do so by the master.

The PWR pin of PGA305 device is used as OWI interface, so that when the PGA305 device is embedded inside of a system module, only two pins are needed (PWR and GND) for communication. The OWI master communicates with the PGA305 device by modulating the voltage on the PWR pin, whereas the PGA305 device communicates with the master by modulating the current on the PWR pin. The OWI master activates OWI communication by generating an activation pulse on the PWR pin.

Figure 7 shows a functional equivalent circuit for the structure of the OWI circuitry.

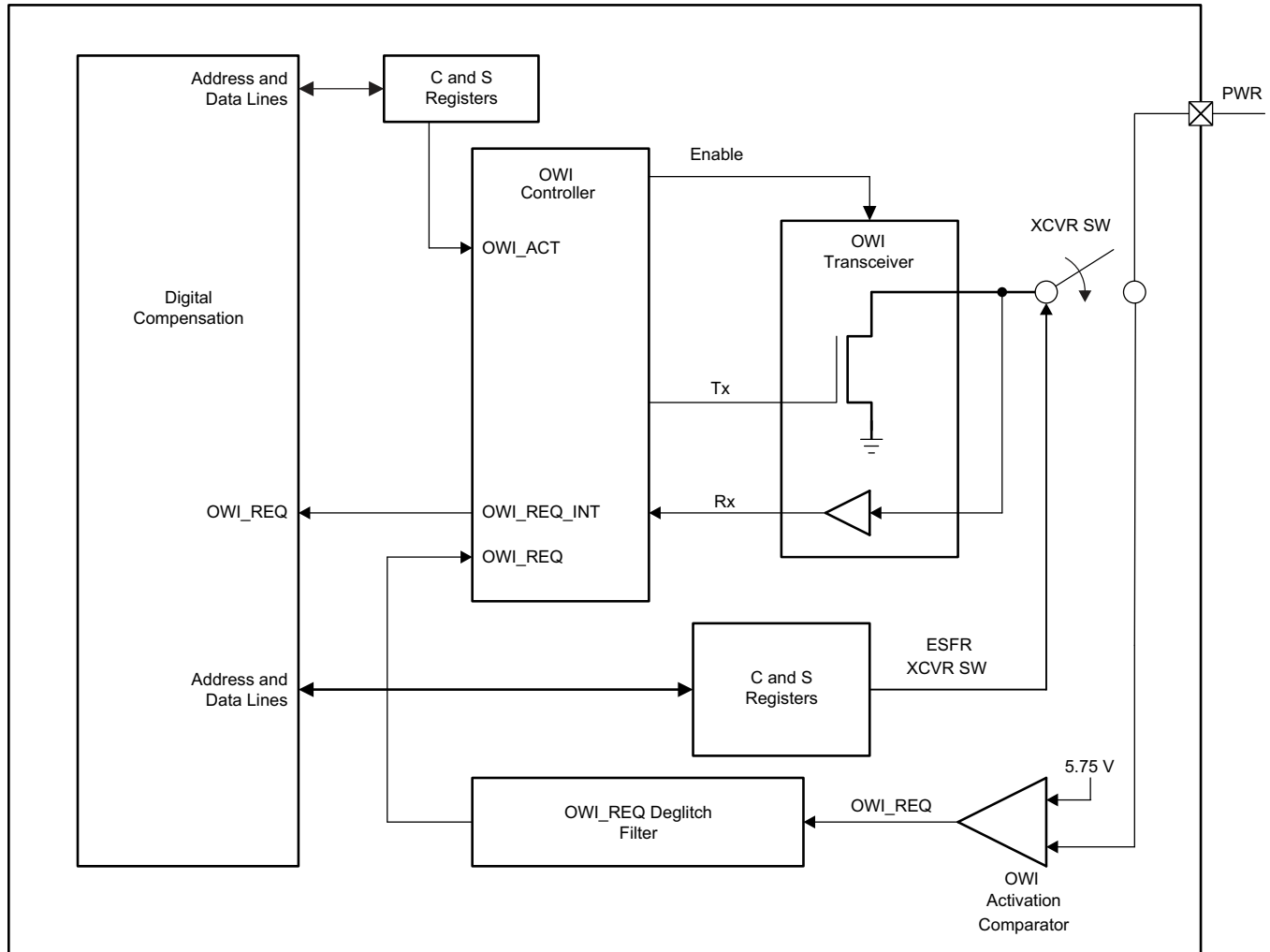


Figure 7. OWI System Components

7.3.12.2 Activating and Deactivating the OWI Interface

7.3.12.2.1 Activating OWI Communication

The OWI master initiates OWI communication when the OWI master generates an **OWI activation-pulse sequence** on the PWR pin. When the PGA305 device receives a valid OWI activation-pulse sequence, it prepares itself for OWI communication. Notice that after the valid OWI activation-pulse sequence is received, the logic checks on the EEPROM lock status. If the EEPROM is locked, the sequence 0x5555 must be sent within 100 ms after the end of the activation-pulse sequence.

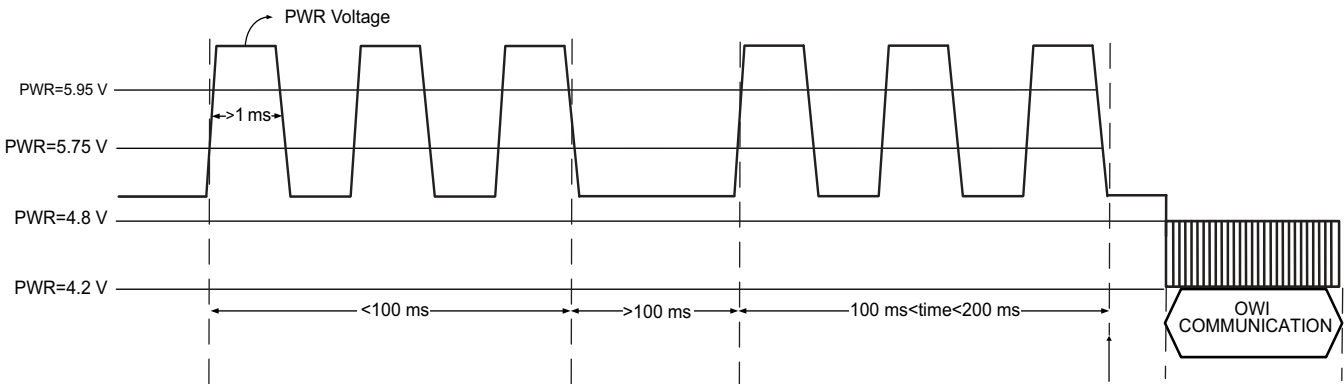


Figure 8. OWI Activation Using Overtvoltage Drive

7.3.12.2.2 Deactivating OWI Communication

To deactivate OWI communication and restart the compensation engine inside the PGA305 device (if it was in reset), these two steps must be performed by the OWI master:

- Set the OWI_XCR_EN bit in the DIG_IF_CTRL register to 0 to turn off the OWI transceiver.
- Set the COMPENSATION_RESET bit in the COMPENSATION_CONTROL register to 0 to de-assert the compensation engine reset.

7.3.12.3 OWI Protocol

7.3.12.3.1 OWI Frame Structure

7.3.12.3.1.1 Standard Field Structure

Data is transmitted on the one-wire interface in byte-sized packets. The first bit of the OWI field is the start bit. The next eight bits of the field are data bits to be processed by the OWI control logic. The final bit in the OWI field is the stop bit. A group of fields make up a transmission frame. A transmission frame is composed of the fields necessary to complete one transmission operation on the one-wire interface. The standard field structure for a one-wire field is shown in [Figure 9](#).

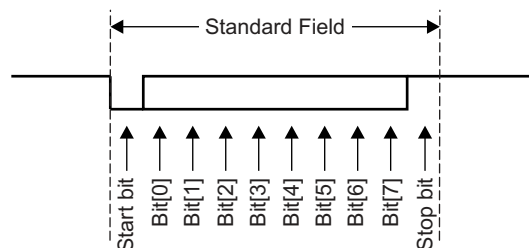


Figure 9. Standard OWI Field

7.3.12.3.1.2 Frame Structure

A complete one-wire data transmission operation is done in a frame with the structure is shown in [Figure 10](#).

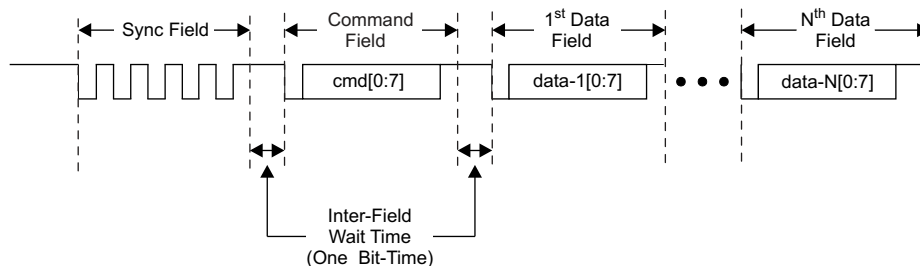


Figure 10. OWI Transmission Frame, N = 1 to 8

Each transmission frame must have a synchronization field and a command field followed by zero to a maximum of eight data fields. The sync field and command fields are always transmitted by the master device. The data fields may be transmitted either by the master or the slave, depending on the command given in the command field. It is the command field which determines direction of travel of the data fields (master-to-slave or slave-to-master). The number of data fields transmitted is also determined by the command in the command field. The inter-field wait time is optional and may be necessary for the slave or the master to process data that has been received.

NOTE

If the OWI remains idle in either the logic-0 or logic-1 state for more than 15 ms, then the PGA305 communication resets and requires a sync field as the next data transmission from the master.

7.3.12.3.1.3 Sync Field

The sync field is the first field in every frame that is transmitted by the master. The sync field is used by the slave device to compute the bit width transmitted by the master. This bit width is used to receive accurately all subsequent fields transmitted by the master. The format of the sync field is shown in [Figure 11](#).

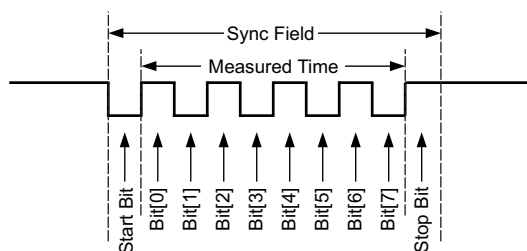


Figure 11. OWI Sync Field

NOTE

Consecutive sync-field bits are measured and compared to determine if a sync field was transmitted to the PGA305 device is valid. If the difference in bit widths of any two consecutive SYNC field bits is greater than $\pm 25\%$, then the PGA305 device ignores the rest of the OWI frame and does not respond to the OWI message.

7.3.12.3.1.4 Command Field

The command field is the second field in every frame sent by the master. The command field contains instructions about what to do with and where to send the data that is transmitted to the slave. The command field can also instruct the slave to send data back to the master during a read operation. The number of data fields to be transmitted is also determined by the command in the command field. The format of the command field is shown in Figure 12.

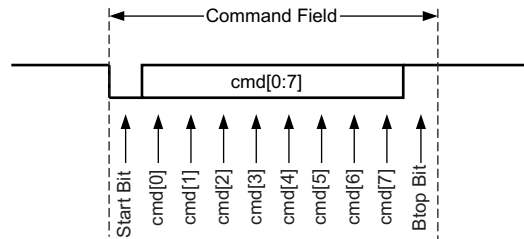


Figure 12. OWI Command Field

7.3.12.3.1.5 Data Fields

After the master has transmitted the command field in the transmission frame, zero or more data fields are transmitted to the slave (write operation) or to the master (read operation). The data fields can be raw EEPROM data or address locations in which to store data. The format of the data is determined by the command in the command field. The typical format of a data field is shown in Figure 13.

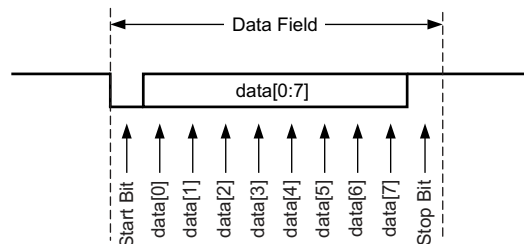


Figure 13. OWI Data Field

7.3.12.3.2 OWI Commands

The following is the list of five OWI commands supported by PGA305:

1. OWI write
2. OWI read initialization
3. OWI read response
4. OWI burst write of EEPROM cache
5. OWI burst read from EEPROM cache

7.3.12.3.2.1 OWI Write Command

| FIELD LOCATION | DESCRIPTION | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|----------------|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Command field | Basic write command | 0 | P2 | P1 | P0 | 0 | 0 | 0 | 1 |
| Data field 1 | Destination address | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Data field 2 | Data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in [Table 4](#).

Table 4. OWI Memory Page Decode

| P2 | P1 | P0 | MEMORY PAGE |
|----|----|----|--|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Control and status registers, DI_PAGE_ADDRESS = 0x02 |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | EEPROM cache |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Control and status registers, DI_PAGE_ADDRESS = 0x07 |

7.3.12.3.2 OWI Read Initialization Command

| FIELD LOCATION | DESCRIPTION | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|----------------|-----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Command field | Read initialization command | 0 | P2 | P1 | P0 | 0 | 0 | 1 | 0 |
| Data field 1 | Fetch address | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in [Table 4](#).

7.3.12.3.3 OWI Read-Response Command

| FIELD LOCATION | DESCRIPTION | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|----------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Command field | Read-response command | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| Data field 1 | Data retrieved (OWI drives data out) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in [Table 4](#).

7.3.12.3.4 OWI Burst-Write Command (EEPROM Cache Access)

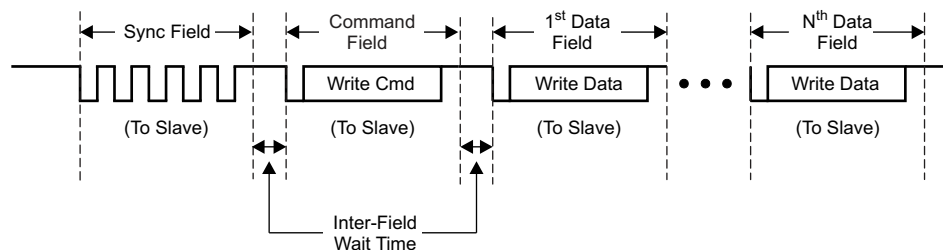
| FIELD LOCATION | DESCRIPTION | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|----------------|--|-------|-------|-------|-------|-------|-------|-------|-------|
| Command field | EE_CACHE write-command cache bytes (0–7) | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Data field 1 | First data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 2 | Second data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 3 | Third data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 4 | Fourth data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 5 | Fifth data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 6 | Sixth data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 7 | Seventh data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 8 | Eighth data byte to be written | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

7.3.12.3.2.5 OWI Burst Read Command (EEPROM Cache Access)

| FIELD LOCATION | DESCRIPTION | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|----------------|---|-------|-------|-------|-------|-------|-------|-------|-------|
| Command field | Burst-read response (8 bytes) | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| Data field 1 | First data byte retrieved EEPROM cache byte 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 2 | Second data byte retrieved EEPROM cache byte 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 3 | Third data byte retrieved EEPROM cache byte 2 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 4 | Fourth data byte retrieved EEPROM cache byte 3 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 5 | Fifth data byte retrieved EEPROM cache byte 4 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 6 | Sixth data byte retrieved EEPROM cache byte 5 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 7 | Seventh data byte retrieved EEPROM cache byte 6 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Data field 8 | Eighth data byte retrieved EEPROM cache byte 7 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

7.3.12.3.3 OWI Operations
7.3.12.3.3.1 Write Operation

The write operation on the one-wire interface is fairly straightforward. The command field specifies the write operation, where the subsequent data bytes are to be stored in the slave, and how many data fields are going to be sent. Additional command instructions can be sent in the first few data fields if necessary. The write operation is shown in [Figure 14](#).


Figure 14. Write Operation, N = 1 to 8
7.3.12.3.3.2 Read Operation

The read operation requires two consecutive transmission frames to move data from the slave to the master. The first frame is the read-initialization frame. It tells the slave to retrieve data from a particular location within the slave device and prepare to send it over the OWI. The data location may be specified in the command field or may require additional data fields for complete data-location specification. The data is not sent until the master commands it to be sent in the subsequent frame called the read-response frame. During the read-response frame, the data direction changes from master → slave to slave → master immediately after the read response command field is sent. Enough time elapses between the command field and data field to allow the signal drivers to change direction. This wait time is 20 μs, and the timer for this wait time is located on the slave device. After this wait time is complete, the slave transmits the requested data. The master device is expected to have switched its signal drivers and is ready to receive data. The read frames are shown in [Figure 15](#).

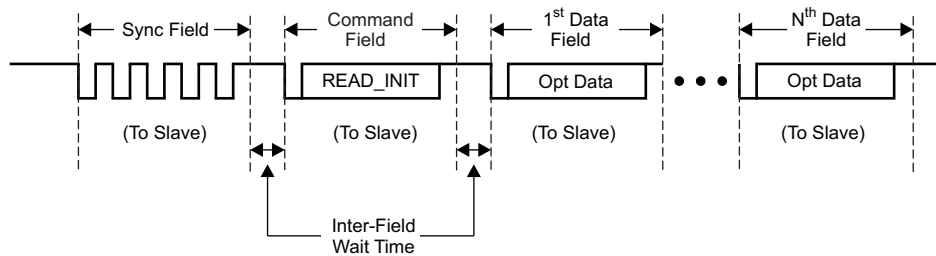


Figure 15. Read-Initialization Frame, N = 1 to 8

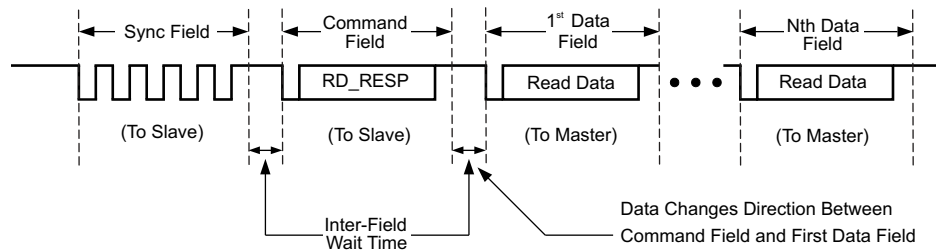


Figure 16. Read-Response Frame, N = 1 to 8

7.3.12.3.3 EEPROM Burst Write

The user can use the EEPROM burst write to write eight bytes of data to the EEPROM cache with one OWI frame to allow fast programming of EEPROM. Note that the EEPROM page must be selected before the EEPROM can transfer the contents of the EEPROM memory cells to the EEPROM cache.

7.3.12.3.4 EEPROM Burst Read

The user can use the EEPROM burst read is used to read eight bytes of data from the EEPROM cache with one OWI frame to allow a fast reading of the EEPROM cache contents. The read process is used to verify the writes to the EEPROM cache.

7.3.12.4 OWI Communication-Error Status

The PGA305 device detects errors in OWI communication. The OWI_ERROR_STATUS_LO and OWI_ERROR_STATUS_HI registers contain OWI communication error bits. The communication errors detected include:

- Out-of-range communication baud rate
- Invalid SYNC field
- Invalid STOP bits in command and data
- Invalid OWI command

7.3.13 I²C Interface

The device includes an I²C digital communication interface capable of running up to 800 kHz. The main function of the I²C is to enable data capture from the PGA305 device as well as writes and reads from all registers available for I²C access.

7.3.13.1 Overview of I²C Interface

I²C is a synchronous serial communication standard that requires the following two pins for communication:

- SDA: I²C serial data line (SDA)
- SCL: I²C serial clock line (SCL)

In addition, the I2CADDR pin is used to select the I²C device address of PGA305. Specifically:

- I2CADDR - Logic 1 - Device address - 0x20, 0x22, 0x25 depending on the Digital Interface Page that is accessed.

- I2CADDR - Logic 0 - Device address - 0x40, 0x42, 0x45 depending on the Digital Interface Page that is accessed.

It is noted that for valid I²C communication to occur I2CADDR should not change value during an I²C transaction.

I²C communicates in a master-and-slave style communication bus where one device, the master, can initiate data transmission. The device always acts as the slave device in I²C communication where the external device that communicates to it acts as the master. The master device is responsible for initiating communication over the SDA line and supplying the clock signal on the SCL line. When the I²C SDA line is pulled low, it is considered a logical zero, and when the I²C SDA line is floating high, it is considered a logical one. For the I²C interface to have access to the configuration registers, the IF_SEL and the COMPENSATION_RESET bits in the COMPENSATION_CONTROL register have to be set to logic one.

7.3.13.2 Clocking Details of I²C Interface

The device samples the data on the SDA line when the rising edge of the SCL line is high, and is changed when the SCL line is low. The only exceptions to this indication are a start, stop, or repeated start condition as shown in Figure 17.

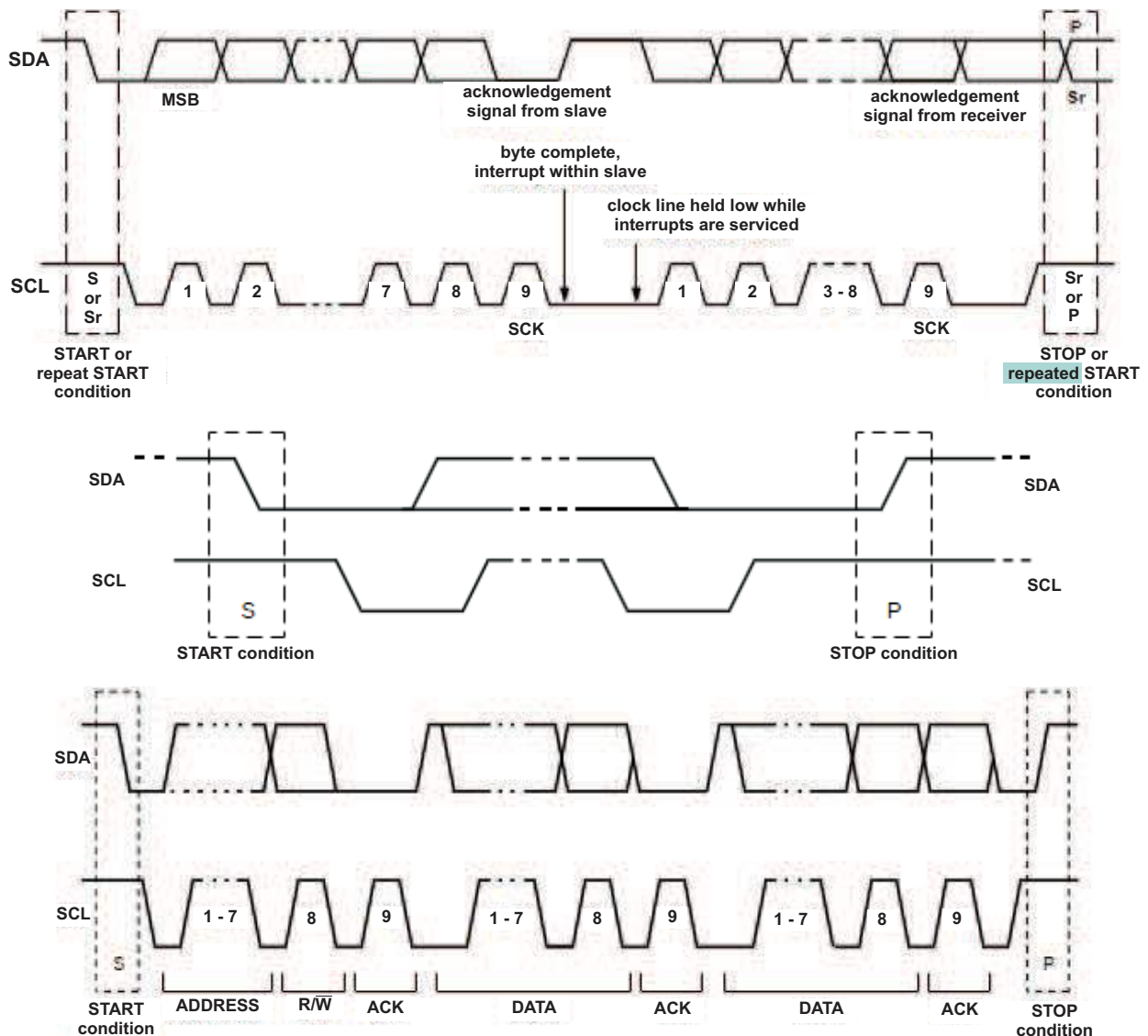


Figure 17. I²C Clocking Details

7.3.13.3 I²C Interface Protocol

Figure 18 shows the basic protocol of the I²C frame for a Write operation.

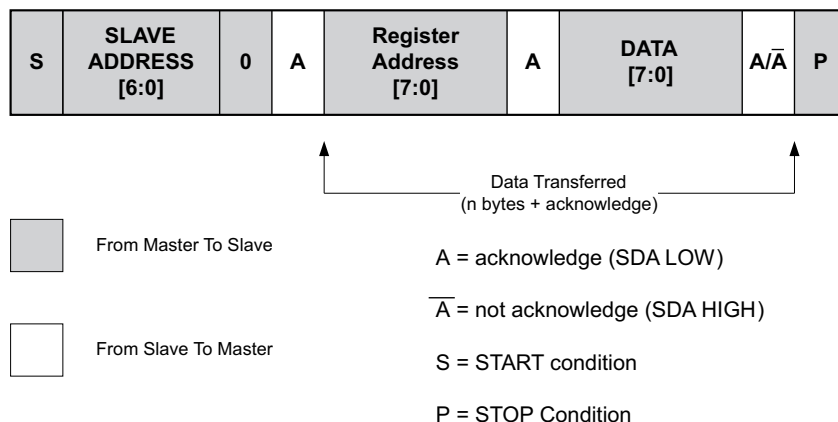


Figure 18. I²C Write Operation: A Master-Transmitter Addressing a PGA305 Slave With a 7-Bit Slave Address

The diagram represents the data fed into or out from the I²C SDA port.

The basic data transfer is to send two bytes of data to the specified slave address. The first data field is the register address and the second data field is the data sent or received.

The I²C slave address is used to determine which memory page is being referenced. Table 5 shows the mapping of the slave address to the memory page.

Table 5. Slave Addresses

| SLAVE ADDRESS WHEN I2CADDR = 1 | SLAVE ADDRESS WHEN I2CADDR = 0 | PGA305 MEMORY PAGE |
|--------------------------------|--------------------------------|---|
| 0x20 | 0x40 | PGA305 Data Read and COMPENSATION_CONTROL register (di_page_address = 0x00) |
| 0x22 | 0x42 | Control and Status Registers (di_page_address = 0x02) |
| 0x25 | 0x45 | EEPROM Registers (di_page_address = 0x05) |

Figure 19 shows the basic PGA305 I²C protocol for a read operation.

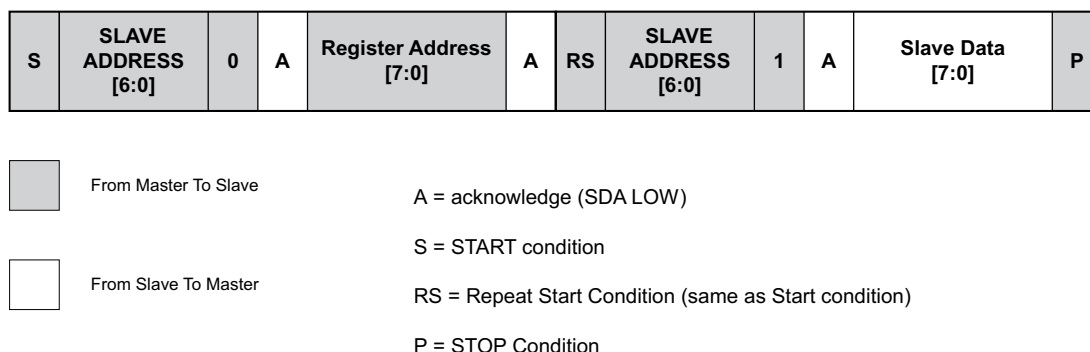


Figure 19. I²C Read Operation: A Master-Transmitter Addressing a PGA305 Slave With a 7-Bit Slave Address

The slave address determines the memory page. The R/W bit is set to 0.

The register address specifies the 8-bit address of the requested data.

The repeat start condition replaces the write data from the above write operation description. This informs the PGA305 devices that Read operation will take place instead of a write operation.

The second slave address contains the memory page from which the data will be retrieved. The R/W bit is set to 1.

Slave data is transmitted after the acknowledge is received by the master.

Table 6 lists a few examples of I²C Transfers.

Table 6. I²C Transfers Examples

| COMMAND | MASTER TO SLAVE DATA ON I2C SDA (I2CADDR = 0) | MASTER TO SLAVE DATA ON I ² C SDA (I2CADDR = 1) |
|--|---|---|
| Write 0x80 to Control and Status Registers 0x30 (DAC_REG0_1) | Slave address: 010 0010 Register address: 0011 0000 Data: 1000 0000 | Slave address: 100 0010 Register address: 0011 0000 Data: 1000 0000 |
| Read from EEPROM Byte 7 | Slave Address: 010 0101 Register Address: 0000 0111 | Slave Address: 100 0101 Register Address: 0000 0111 |
| Write to EEPROM Cache Byte 7 | Slave Address: 010 0101 Register Address: 1000 0111 | Slave Address: 100 0101 Register Address: 1000 0111 |

7.3.13.4 PGA305 I²C Runtime Commands

During the PGA305 Operation while the Compensation Algorithm runs (COMPENSATION_RESET = 0), the I²C interface can collect data from the device when the interface sends I2C commands to the PGA305 device and reads a response from the PGA305 device. The runtime commands used in the PGA305 device are listed in Table 7.

Note that the register address used for I²C Write Command is always 0x09 on DI Page 0x00.

Table 7. I²C Runtime Write Commands

| I ² C WRITE COMMAND | Description | Data Format (I2CADDR = 0) | Data Format (I2CADDR = 1) |
|---|---|---|---|
| 0x00 - Read PADC Source Value | Reads one 24bit sample from the PADC Channel | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0000 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0000 (Data) |
| 0x02 - Read TADC Source Value | Reads one 24-bit sample from the TADC Channel | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0010 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0010 (Data) |
| 0x04 - Read PGA305 Compensated Output Value | Reads One 24-bit or 16-bit sample from the Compensated output of the device. The same value that is read by using this command is fed into the DAC output of the PGA305 device. | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0100 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0100 (Data) |
| 0x06 - Read PGA305 Diagnostics | Reads the PGA305 Diagnostics. For more Information see "Reading Diagnostics Information through I2C" Chapter. | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0110 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0000 0110 (Data) |

Table 7. I²C Runtime Write Commands (continued)

| I ² C WRITE COMMAND | Description | Data Format (I2CADDR = 0) | Data Format (I2CADDR = 1) |
|--------------------------------|---|---|---|
| 0x70 - Read Trail Word | Loads the lower 16bits of any previously executed command | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0111 0000 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 1001 (Register Address) Data: 0111 0000 (Data) |

After the I²C interface sends a Write Command to the PGA305 device, the I²C interface reads the response is read through a read response command presented in the following table.

Note that there are two 8-bit I²C registers that are used to read 16 bits of PGA305 response. The register addresses used for I²C Read Response are 0x05 on DI Page 0x00 for the Most Significant Byte and 0x04 on DI Page 0x00 for the Least Significant Byte.

Table 8. I²C Runtime Read Response Command

| I ² C Read Response | Data Format (I2CADDR = 0) | Data Format (I2CADDR = 1) |
|--------------------------------|---|---|
| Read Most Significant Byte | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 0101 (Register Address) Data: 0000 0000 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 0101 (Register Address) Data: 0000 0000 (Data) |
| Read Least Significant Byte | Slave address: 100 0000 (Slave Address + DI Page) Register address: 0000 0100 (Register Address) Data: 0000 0000 (Data) | Slave address: 010 0000 (Slave Address + DI Page) Register address: 0000 0100 (Register Address) Data: 0000 0000 (Data) |

7.3.13.5 PGA305 I²C Transfer Example

This I²C example presents the read of a single 24-bit sample from the PGA device. In this example, Command 0x04 *Read PGA305 Compensated Output Value* is used while the PGA305 slave address is 0x20 (I2CADDR = 1).

Table 9. I²C Transfer Example

| I ² C Data Flow Description | I2C Master | PGA305 |
|---|--|---|
| 1. Master Sends Command 0x04 (Read PGA305 Compensated Output Value) | 0x40 (Slave Address + DI Page + R/W bit) 0x09(Register Address) 0x04 (Data) | Acknowledge Acknowledge Acknowledge |
| 2. Master Reads Byte2 (MS Byte) | 0x40 (Slave Address + DI Page + R/W bit) 0x04(Register Address) 0x41 (Slave Address + DI Page + R/W bit) | Acknowledge Acknowledge 0xbb (Where 'bb' is the data Value) |
| 3. Master sends Commands 0x70 (Read Trail Word) | 0x40 (Slave Address + DI Page + R/W bit) 0x09(Register Address) 0x70 (Data) | Acknowledge Acknowledge Acknowledge |
| 4. Master Reads Byte1 (Mid Significant Byte) | 0x40 (Slave Address + DI Page + R/W bit) 0x05(Register Address) 0x41 (Slave Address + DI Page + R/W bit) | Acknowledge Acknowledge 0xbb (Where 'bb' is the data Value) |
| 5. Master Reads Byte0 (Least Significant Byte) | 0x40 (Slave Address + DI Page + R/W bit) 0x04(Register Address) 0x41 (Slave Address + DI Page + R/W bit) | Acknowledge Acknowledge 0xbb (Where 'bb' is the data Value) |

If the PGA305 device operates in 16-bit mode ($\text{ADC_24BIT_EN} = 0$), step 2 can be skipped.

7.3.14 DAC Output

The device includes a 14-bit digital-to-analog converter that produces an absolute output voltage with respect to the accurate reference voltage or a ratiometric output voltage with respect to the PWR supply.

When the microprocessor undergoes a reset, the DAC registers are driven to the 0x000 code.

7.3.14.1 Ratiometric vs Absolute

Use the DAC_RATIOMETRIC bit in DAC_CONFIG to configure the DAC output in either ratiometric-to-PWR mode or independent-of-PWR (or absolute) mode.

NOTE

In ratiometric mode, changes in the V_{PWR} voltage result in a proportional change in the output voltage because the current reference for the DAC is derived from V_{PWR} .

7.3.15 DAC Gain

The DAC gain buffer is a configurable buffer stage for the DAC output. The DAC gain amplifier can be configured to operate in voltage amplification mode for voltage output or current amplification mode for 4-mA to 20-mA applications. In voltage output mode, set the DAC_GAIN bits in the DAC_CONFIG register to a specific value to configure the DAC gain as shown in [Figure 20](#). Use the 2-bit DAC_GAIN field to configure the DAC gain to one of four possible gain configurations.

The final step of DAC gain is connected to PWR and ground, which gives the user the ability to drive the V_{OUT} voltage close to the V_{PWR} voltage.

The DAC gain buffer also implements a COMP pin to allow the user to implement compensation when driving large capacitive loads.

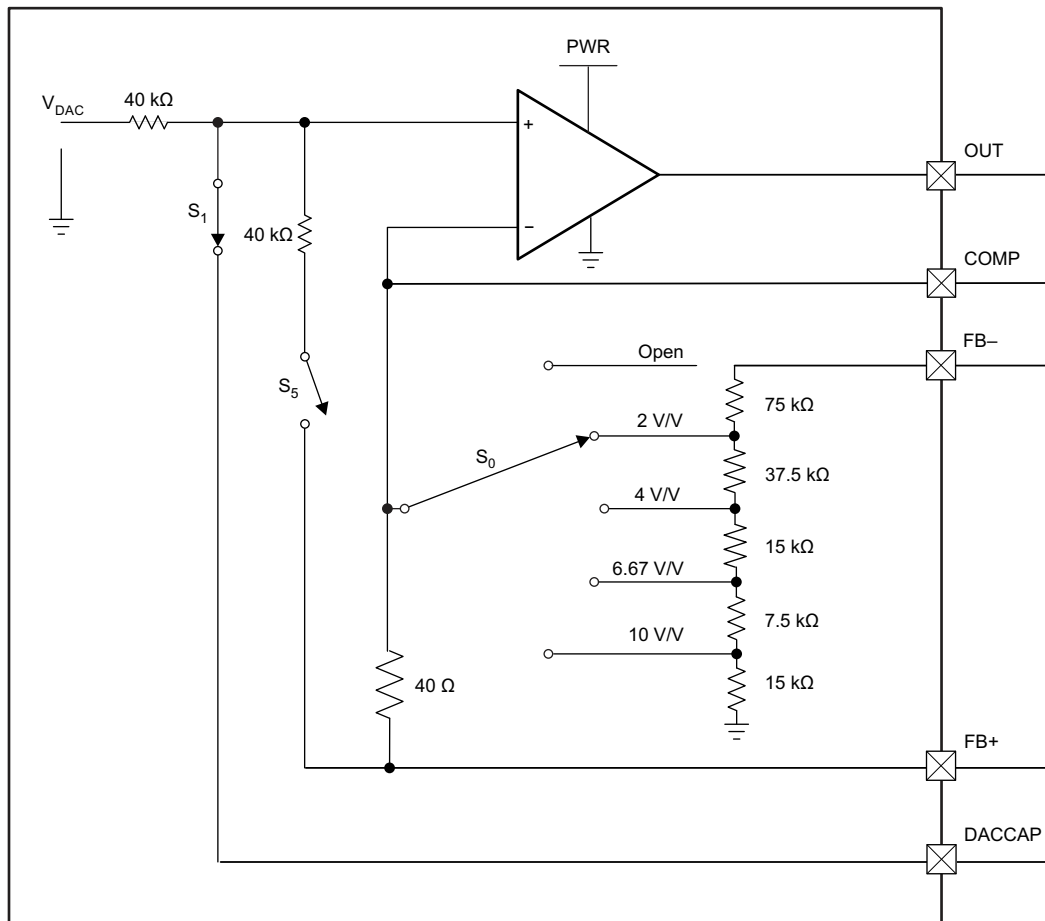


Figure 20. PGA305 Output Buffer

7.3.16 Memory

7.3.16.1 EEPROM Memory

Figure 21 shows the EEPROM structure. The contents of the EEPROM must be transferred to the EEPROM cache before writes. This means that the EEPROM can be programmed eight bytes at a time. EEPROM reads occur without the EEPROM cache.

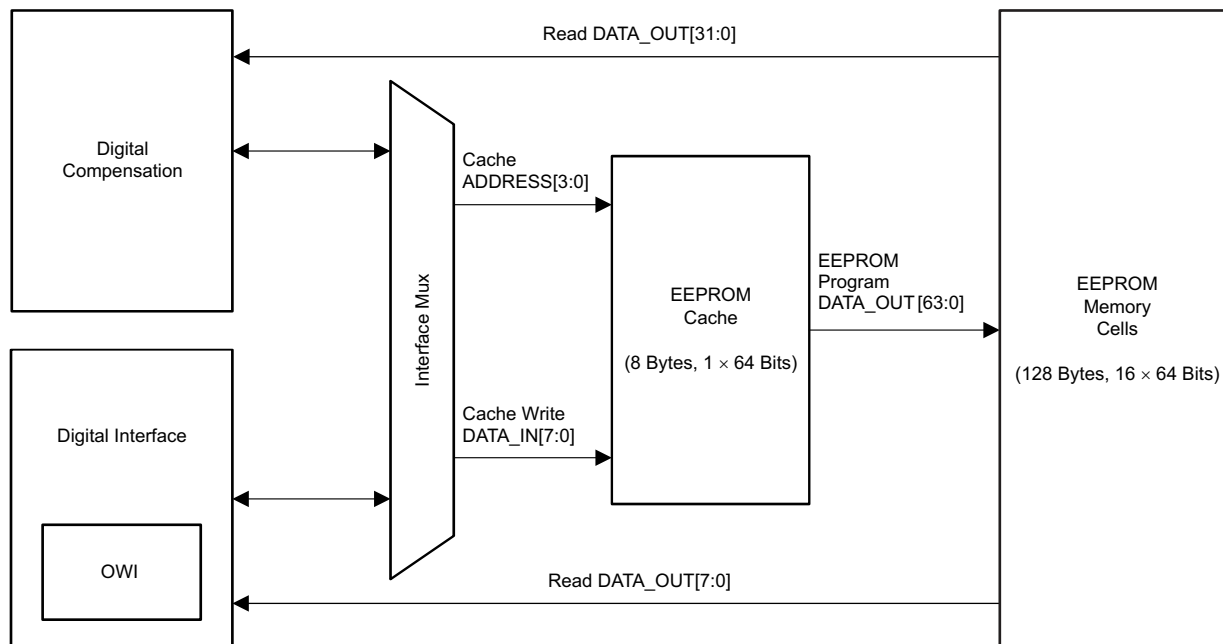


Figure 21. Structure of the EEPROM Interface

7.3.16.1.1 EEPROM Cache

The EEPROM cache serves as temporary storage of data being transferred to selected EEPROM locations during the programming process.

7.3.16.1.2 EEPROM Programming Procedure

For programming the EEPROM, the EEPROM is organized in 16 pages of eight bytes each. Write to the 8-byte EEPROM cache to program the EEPROM memory cells. Select the EEPROM memory page to transfer the contents of the EEPROM cache.

1. Write the upper four bits of the 7-bit EEPROM address to the EEPROM_PAGE_ADDRESS register to select the EEPROM page.
2. Write to the EEPROM_CACHE register to load the 8-byte EEPROM cache. Note that all eight bytes must be loaded into the EEPROM_CACHE register.
3. Set the ERASE_AND_PROGRAM bit in the EEPROM_CTRL register. Setting this bit automatically erases the selected EEPROM memory page and programs it with the contents of the EEPROM_CACHE register. Alternatively, the user can write 1 to the ERASE bit in the EEPROM_CTRL register to erase the selected EEPROM memory page, and then write 1 to the PROGRAM bit in the EEPROM_CTRL register once the erase is complete. The status of the erase and program operations can be monitored through the EEPROM_STATUS register.

7.3.16.1.3 EEPROM Programming Current

The EEPROM programming process results in an additional 6-mA current on the PWR pin for the duration of programming.

7.3.16.1.4 CRC

The last byte of the EEPROM memory is reserved for the CRC. This CRC value covers all data in the EEPROM memory. Every time the last byte is programmed, the CRC value is automatically calculated and validated. The validation process checks the calculated CRC value with the last byte programmed in the EEPROM memory cell. If the calculated CRC matches the value programmed in the last byte, the CRC_GOOD bit is set in the EEPROM_CRC_STATUS register.

The user can set the `CALCULATE_CRC` bit in the `EEPROM_CRC` register to initiate the CRC check. The status of the CRC calculation is available in the `CRC_CHECK_IN_PROG` bit in the `EEPROM_CRC_STATUS` register, while the result of the CRC validation is available in the `CRC_GOOD` bit in the `EEPROM_CRC_STATUS` register.

The CRC calculation pseudo code is as follows:

```

currentCRC8 = 0xFF; // Current value of CRC8

for NextData
  D = NextData;
  C = currentCRC8;

  begin
    nextCRC8_BIT0 = D_BIT7 ^ D_BIT6 ^ D_BIT0 ^ C_BIT0 ^ C_BIT6 ^ C_BIT7;
    nextCRC8_BIT1 = D_BIT6 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT6;
    nextCRC8_BIT2 = D_BIT6 ^ D_BIT2 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT2 ^ C_BIT6;
    nextCRC8_BIT3 = D_BIT7 ^ D_BIT3 ^ D_BIT2 ^ D_BIT1 ^ C_BIT1 ^ C_BIT2 ^ C_BIT3 ^ C_BIT7;
    nextCRC8_BIT4 = D_BIT4 ^ D_BIT3 ^ D_BIT2 ^ C_BIT2 ^ C_BIT3 ^ C_BIT4;
    nextCRC8_BIT5 = D_BIT5 ^ D_BIT4 ^ D_BIT3 ^ C_BIT3 ^ C_BIT4 ^ C_BIT5;
    nextCRC8_BIT6 = D_BIT6 ^ D_BIT5 ^ D_BIT4 ^ C_BIT4 ^ C_BIT5 ^ C_BIT6;
    nextCRC8_BIT7 = D_BIT7 ^ D_BIT6 ^ D_BIT5 ^ C_BIT5 ^ C_BIT6 ^ C_BIT7;
  end

  currentCRC8 = nextCRC8_D8;
endfor

```

NOTE

The EEPROM CRC calculation is complete 340 μ s after the digital core starts running at power up.

7.3.16.2 Control and Status Registers Memory

The digital compensator uses the Control and Status registers to interact with the analog blocks of the device.

7.3.17 Diagnostics

The PGA305 device implements the diagnostics listed in [Table 10](#).

Table 10. Programming Diagnostics

| DIAGNOSTICS DESCRIPTION | ACTION |
|---|--|
| Digital-compensation-logic execution-timing error | DAC is disabled and compensation logic is set to reset |
| Digital-compensation-logic checksum error | DAC is disabled and compensation logic is set to reset |
| EEPROM is corrupted or EEPROM CRC = 0 | DAC code is driven to 0 code |
| Power-supply and signal-chain errors | DAC output is driven to the value determined by the FAULT register in EEPROM |

The user can set the `DIAG_ENABLE` register in EEPROM to a non-zero value to enable the diagnostics listed in [Table 10](#). To disable diagnostics, set the `DIAG_ENABLE` register in EEPROM to 0.

7.3.17.1 Power Supply Diagnostics

The PGA305 device includes circuits to monitor the reference and power supply for faults. Specifically, the signals that are monitored are:

- AVDD voltage
- DVDD voltage
- Bridge supply voltage
- Internal oscillator supply voltage
- Reference output voltage

The [Electrical Characteristics – Diagnostics](#) table lists the voltage thresholds for each of the power rails.

7.3.17.2 Signal Chain Faults

The PGA305 device includes circuits to monitor the P and T signal chains for faults. This section describes the faults monitored by the PGA305 device.

7.3.17.2.1 P Gain and T Gain Input Faults

The PGA305 device includes circuits to monitor for sensor connectivity faults. Specifically, the device monitors the bridge sensor pins for opens (including loss of connection from the sensor), short to ground, and short-to-sensor supply. The device can compare the voltage at INP+ and INP– pins with the overvoltage and undervoltage thresholds listed in the [Electrical Characteristics – Diagnostics](#) table as a way to monitor for sensor connectivity faults.

The device also includes an overvoltage monitor at the INT+ and INT– pins through the use of 1-M Ω pullup resistors.

[Figure 22](#) shows the block diagram of the P gain and T gain input faults.

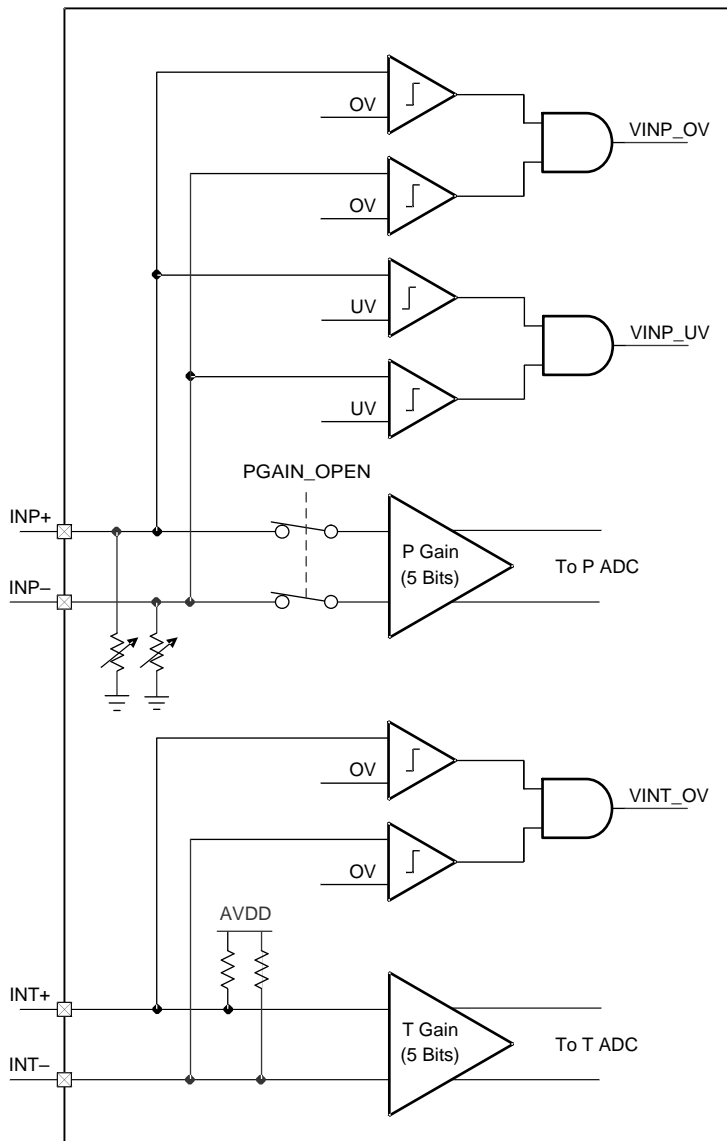


Figure 22. Block Diagram of P Gain and T Gain Diagnostics

The bridge-sensor connectivity faults are detected through the use of an internal pulldown resistor. The value of the pulldown resistor and the threshold can be configured using the AFEDIAG_CFG EEPROM register. Table 11 describes the possible configurations.

Table 11. Definition of AFEDIAG_CFG EEPROM Register

| BITS | DESCRIPTION |
|--|---|
| 0: PD1 1: PD2 | See Electrical Characteristics – Diagnostics . |
| 2: THRS[0] 3: THRS[1] 4: THRS[2] | See Electrical Characteristics – Diagnostics . |
| 5: DIS_R_P | 1: Disables pulldown resistors used for open and short diagnostics on the INP+ and INP– pins 0: Enables pulldown resistors used for open and short diagnostics on the INP+ and INP– pins |
| 6: DIS_R_T | 1: Disables pullup resistors used for open and short diagnostics on the INT+ and INT– pins 0: Enables pullup resistors used for open and short diagnostics on the INT+ and INT– pins |
| 7: | — |

7.3.17.2.2 P Gain and T Gain Output Diagnostics

The PGA305 device includes modules that verify that the output signal of each gain is within a certain range. This ensures that gain stages in the signal chain are working correctly.

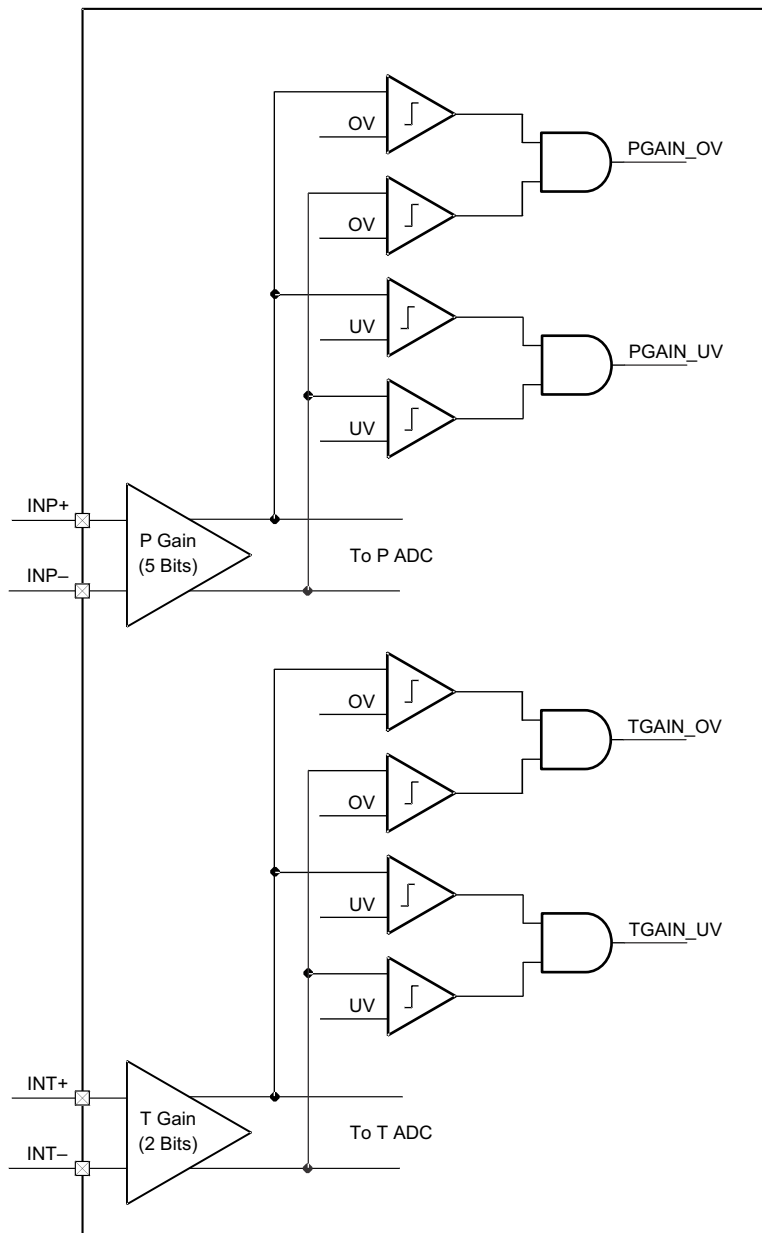


Figure 23. Block Diagram of P Gain and T Gain Output Diagnostics

7.3.17.2.3 Masking Signal Chain Faults

Use the bits in the AFEDIAG_MASK register in EEPROM to selectively enable and disable the signal chain diagnostics. Table 12 lists the mask bits. The user can set a bit to 1 enables detection of the corresponding fault and set the bit to 0 to disable the detection of corresponding fault.

Table 12. Signal Chain Fault Masking Bits

| BIT | DESCRIPTION |
|-----|---------------------------|
| 0 | INP+ or INP– overvoltage |
| 1 | INP+ or INP– undervoltage |

Table 12. Signal Chain Fault Masking Bits (continued)

| BIT | DESCRIPTION |
|-----|----------------------------|
| 2 | INT+ or INT– overvoltage |
| 3 | N/A |
| 4 | P GAIN output overvoltage |
| 5 | P GAIN output undervoltage |
| 6 | T GAIN output overvoltage |
| 7 | T GAIN output undervoltage |

7.3.17.2.4 Fault Detection Timing

The PGA305 fault-monitoring circuits monitor faults either at power up or periodically. [Table 13](#) shows the fault-detection timing.

Table 13. Fault Detection Timing

| FAULT | POWER UP OR RUN TIME | MINIMUM TIME AFTER FAULT OCCURS | MAXIMUM TIME AFTER FAULT OCCURS |
|---|---|---------------------------------|---------------------------------|
| Digital-compensation execution-timing error | Run time | 500 ms | — |
| Digital-compensation checksum error | Run time | 500 ms | — |
| EEPROM is corrupted or EEPROM CRC = 0 | Power up only (EEPROM is accessed only at power up) | N/A | N/A |
| Power supply and signal chain errors | Run time | 8 ms | 16 ms |

7.3.18 Reading Diagnostics Information Through I²C

To receive Diagnostics Information through the I²C Interface while the PGA305 compensation algorithm runs, the I²C command 0x06 is used. The Implemented Diagnostics in PGA305 are stuck fault, which means that if a diagnostic fault occurred in the past, this will be reported when the next diagnostics read occurs even in the case where the fault is not present in the system any longer. When the I²C command has been received, the I²C will report the Power Supply diagnostics and the Analog Front End Diagnostics and will clear the stuck diagnostic flags.

The I²C example in [Table 14](#) shows the diagnostics read process from the PGA device. In this example the PGA305 slave address is assumed to be 0x20 (I2CADDR = 1).

Table 14. Diagnostics Information

| I ² C Data Flow Description | I ² C Master | PGA305 |
|--|--|---|
| 1. Master Sends Command 0x06 (Read PGA305 Diagnostics) | 0x40 (Slave Address + DI Page + R/W bit) 0x09(Register Address) 0x06 (Data) | Acknowledge Acknowledge Acknowledge |
| 2. Master Reads Byte1 (Power Supply Diagnostics) | 0x40 (Slave Address + DI Page + R/W bit) 0x05(Register Address) 0x41 (Slave Address + DI Page + R/W bit) | Acknowledge Acknowledge 0xbb (Where 'bb' is the data Value) |
| 2. Master Reads Byte0 (Analog Front-End Diagnostics) | 0x40 (Slave Address + DI Page + R/W bit) 0x04(Register Address) 0x41 (Slave Address + DI Page + R/W bit) | Acknowledge Acknowledge 0xbb (Where 'bb' is the data Value) |

Further, [Table 15](#) lists the bits that order for the Power Supply Diagnostics (Byte1) and the Analog Front End Diagnostics (Byte2).

Table 15. Diagnostics Information

| Power Supply (Byte 1) | Analog Front End (Byte 0) |
|---|--|
| Bit 7: Digital Regulator DVDD Under Voltage (DVDD_UV) | Bit 7: Temperature Channel AFE Output Under Voltage (TGAIN_UV) |
| Bit 6: Digital Regulator DVDD Over Voltage (DVDD_OV) | Bit 6: Temperature Channel AFE Output Over Voltage (TGAIN_OV) |
| Bit 5: Analog Regulator AVDD Under Voltage (AVDD_UV) | Bit 5: Pressure Channel AFE Output Under Voltage (PGAIN_UV) |
| Bit 4: Analog Regulator AVDD Over Voltage (AVDD_OV) | Bit 4: Pressure Channel AFE Output Over Voltage (PGAIN_OV) |
| Bit 3: Reference Under Voltage (REF_UV) | Bit 3: Unused (N/A) |
| Bit 2: Reference Over Voltage (REF_OV) | Bit 2: INT+ and INT- pins Over Voltage (INT_OV) |
| Bit 1: Bridge Supply Over Voltage (VBRG_OV) | Bit 1: INP+ and INP- pins Under Voltage (INP_UV) |
| Bit 0: Bridge Supply Under Voltage (VBRG_UV) | Bit 0: INP+ and INP- pins Over Voltage (INP_OV) |

7.3.19 Digital Compensation and Filter

The PGA305 device implements a third-order TC and NL correction of the pressure and temperature inputs. The user can use a second-order IIR filter to filter and write the corrected output to the DAC as shown in [Figure 24](#).

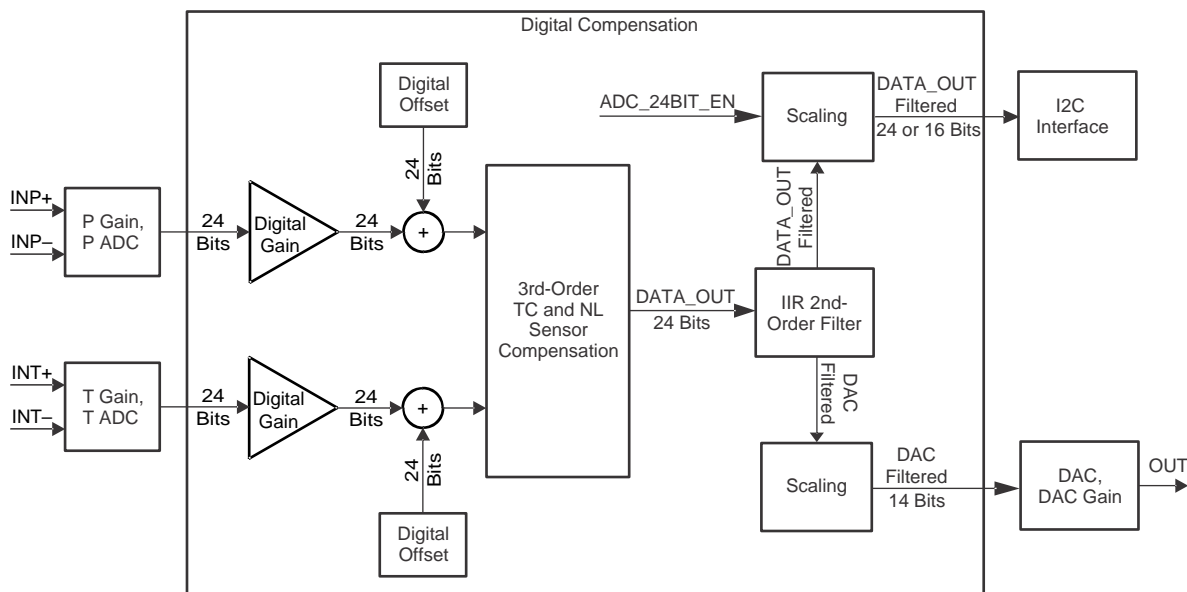


Figure 24. Digital Transfer Block Diagram

7.3.19.1 Digital Gain and Offset

The digital compensation implements digital gain and offset for both pressure and temperature. These are calculated based on the OFF_EN bit in the OFFSET_ENABLE register. Use [Equation 2](#) and [Equation 3](#) when the OFF_EN bit is 0.

$$P = P_{GAIN} \times P_{ADC} + P_{OFFSET}$$

where

- P_{GAIN} is the Pressure digital gain defined by the PADC_GAIN_MSB, PADC_GAIN_LSB registers
- P_{OFFSET} is the Pressure digital offset defined by the PADC_OFFSET_BYTE1, PADC_OFFSET_BYTE0 (MSB, LSB) registers
- P is the pressure

- P ADC is the pressure digital output (2)

$$T = T_{\text{GAIN}} \times T_{\text{ADC}} + T_{\text{OFFSET}}$$

where

- T_{GAIN} is the Temperature digital gain defined by the TADC_GAIN_MSB, TADC_GAIN_LSB registers
- T_{OFFSET} is the Temperature digital offset defined by the TADC_OFFSET_BYTE1, TADC_OFFSET_BYTE0 (MSB, LSB) registers
- T is the temperature
- T ADC is the temperature digital output (3)

Use Equation 4 and Equation 5 if the OFF_EN bit is set to 1:

$$P = P_{\text{GAIN}} \times (P_{\text{ADC}} + P_{\text{OFFSET}})$$

where

- P_{GAIN} is the Pressure digital gain defined by the PADC_GAIN_MSB, PADC_GAIN_LSB registers
- P_{OFFSET} is the Pressure digital offset defined by the PADC_OFFSET_BYTE1, PADC_OFFSET_BYTE0 (MSB, LSB) registers
- P is the pressure
- P ADC is the pressure digital output (4)

$$T = T_{\text{GAIN}} \times (T_{\text{ADC}} + T_{\text{OFFSET}})$$

where

- T_{GAIN} is the Temperature digital gain defined by the TADC_GAIN_MSB, TADC_GAIN_LSB registers
- T_{OFFSET} is the Temperature digital offset defined by the TADC_OFFSET_BYTE1, TADC_OFFSET_BYTE0 (MSB, LSB) registers
- T is the temperature
- T ADC is the temperature digital output (5)

NOTE

For high-offset sensors or sensor bridges with a low or high common mode, it may be useful to use the Offset Enabled (OFF_EN = 1) option which will cancel the offset and the amplify the values in the digital domain. The PGA305 device allows the ability to cancel the offset and amplify the signal further before being used in the compensation equation. The determination of the digital gain and offset values is implemented automatically by the PGA305 GUI.

7.3.19.2 TC and NL Correction

Use Equation 6 to calculate the digital compensation.

$$\text{DATA_OUT} = (h_0 + h_1 \times T + h_2 \times T^2 + h_3 \times T^3) + (g_0 + g_1 \times T + g_2 \times T^2 + g_3 \times T^3) \times P + (n_0 + n_1 \times T + n_2 \times T^2 + n_3 \times T^3) \times P^2 + (m_0 + m_1 \times T + m_2 \times T^2 + m_3 \times T^3) \times P^3$$

where

- DATA_OUT = Data that is available to read using the I²C Interface
- DAC = Digitally compensated value at the input of the DAC
- h_x , g_x , n_x and m_x are TC and NL compensation coefficients programmed in EEPROM
- P is pressure
- T is temperature (6)

DAC = DATA_OUT / 1024 in 24-bit mode, or

DAC = DATA_OUT / 4 in 16-bit mode

7.3.19.2.1 TC and NL Coefficients

The PGA305 device implements third-order TC and NL compensation of the bridge offset, bridge span, and bridge nonlinearity. The equation has 16 coefficients, and hence requires at least 16 different measurement points to compute a unique set of 16 coefficients. Use Equation 7 to calculate the TC-compensated DAC output.

$$\text{DATA_OUT} = (h_0 + h_1 T + h_2 T^2 + h_3 T^3) + (g_0 + g_1 T + g_2 T^2 + g_3 T^3) \times P + (n_0 + n_1 T + n_2 T^2 + n_3 T^3) \times P^2 + (m_0 + m_1 T +$$

$$m_2T^2 + m_3T^3) \times P^3 \quad (7)$$

The 16 different P ADC and T ADC measurements can be made, for example, at four temperatures and at four different pressures. Note that:

- P GAIN and T GAIN values must be set to a fixed value for all measurements.
- At each measurement point, the P ADC value and the T ADC value must be recorded in order to compute the 16 coefficients.
- Sometimes, it may be expensive to measure P ADC and T ADC at different temperatures and pressures. In this case, there are three approaches:
 - Use a model of the bridge to estimate P ADC and T ADC measurements instead of actually measuring.
 - Use *batch modeling*, in which a family of sense elements is characterized across temperature, and the TC coefficients of the compensation equation are determined prior to calibration. On a production line, measurements are made at a limited number of temperature and pressure set points, and coefficients are adjusted accordingly. Discuss with TI application engineers for details.
 - Reduce the number of coefficients by reducing the order of TC compensation. Discuss the procedure to use fewer coefficients with TI application engineers.

7.3.19.2.1.1 No TC and NL Coefficients

Use [Equation 8](#) for the P ADC-to-DAC conversion.

$$\text{DATA_OUT} = H_{0EE} + G_{0EE} \times \text{P ADC} \quad (8)$$

Table 16. Coefficient Values for No TC and NL Compensation

| COEFFICIENT | VALUE (HEX) |
|-------------|-----------------|
| h_0 | $H_{0EE}^{(1)}$ |
| h_1 | 0x000000 |
| h_2 | 0x000000 |
| h_3 | 0x000000 |
| g_0 | $G_{0EE}^{(1)}$ |
| g_1 | 0x000000 |
| g_2 | 0x000000 |
| g_3 | 0x000000 |
| n_0 | 0x000000 |
| n_1 | 0x000000 |
| n_2 | 0x000000 |
| n_3 | 0x000000 |
| m_0 | 0x000000 |
| m_1 | 0x000000 |
| m_2 | 0x000000 |
| m_3 | 0x000000 |

(1) H_{0EE} and G_{0EE} are the values stored in EEPROM, which are 2^{22} times the actual H_0 and G_0 coefficients.

Consider an example of scaling the positive half of the 16-bit P ADC to a 14-bit DAC value. In this case, $H_0 = 0$ and $G_0 = 0.5$. Therefore, $H_{0EE} = 0$, and $G_{0EE} = 2^{21}$.

7.3.19.2.2 TC Compensation Using the Internal Temperature Sensor

Temperature compensation can be performed using the internal temperature sensor with T GAIN = 5 V/V gain. The internal temperature ADC values at the different temperatures listed in [Table 17](#).

Table 17. T ADC Value for the Internal Temperature Sensor

| TEMPERATURE | T ADC VALUE (HEX VALUE) |
|-------------|-------------------------|
| –40°C | 0x16C900 (TBD) |
| 0°C | 0x1ACF00 (TBD) |
| 150°C | 0x29E500 (TBD) |

For T ADC at intermediate temperatures, use linear interpolation.

7.3.19.3 Clamping

The output of the digital compensation is clamped. The low and high clamp values are programmable using the LOW_CLAMP and HIGH_CLAMP registers in the EEPROM. In addition, the user can use the NORMAL_LOW and NORMAL_HIGH registers in the EEPROM to configure the normal operating output. Figure 25 shows an example of the clamping feature for a 0-V to 5-V output operational mode. In a similar way, the output of the compensation can be configured when the 4-mA to 20-mA operational mode is used. In such case, however, the LOW_CLAMP value must be larger than the maximum current necessary for normal operation of the device.

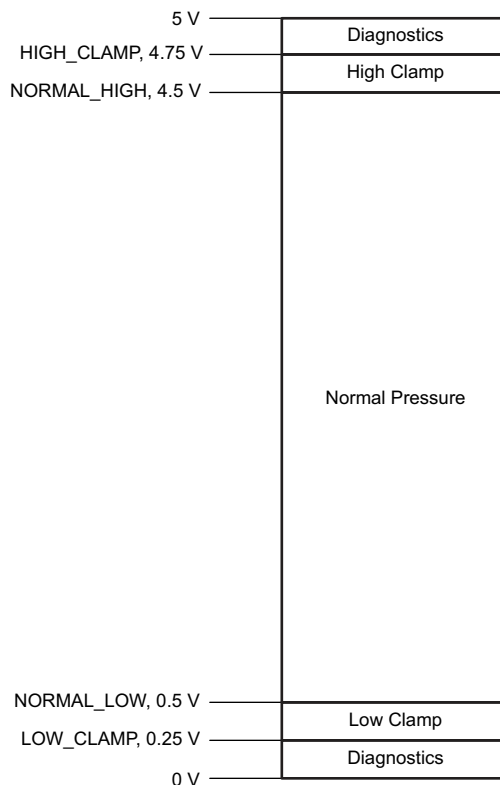


Figure 25. Example of Clamping the Digital Compensation Output

7.3.19.4 Filter

The IIR filter is as follows:

$$w(n) = (a_0 \times \text{DATA_OUT}(n) + a_1 \times w(n - 1) + a_2 w(n - 2))$$

where

- a_0 , a_1 , and a_2 are the IIR filter coefficients,
- $\text{DATA_OUT}(n)$ is the DATA_OUT output prior to the IIR filter, (9)

$$\text{DATA_OUTF}(n) = (b_0 \times w(n) + b_1 \times w(n - 1) + b_2 w(n - 2))$$

where

- b_0 , b_1 , and b_2 are the IIR filter coefficients,
- and $\text{DATA_OUTF}(n)$ is the output of the PGA305 device after the second-order IIR filter. (10)

7.3.20 Filter Coefficients

7.3.20.1 No Filtering

If filtering must be disabled, set $a_0 = 0x0000$.

7.3.20.2 Filter Coefficients for P ADC Sampling Rate = 1024 μ s
Table 18. Filter Cutoff Frequency and Filter Coefficients

| CUTOFF FREQUENCY (Hz) | a ₀ (Hex) | a ₁ (Hex) | a ₂ (Hex) | b ₀ (Hex) | b ₁ (Hex) | b ₂ (Hex) |
|-----------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| 76.8 | 4000 | AAA1 | 2060 | 0B01 | 1602 | 0B01 |
| 89.6 | 4000 | B169 | 1CEE | 0E57 | 1CAF | 0E57 |
| 102.4 | 4000 | B818 | 19E0 | 11F8 | 23F0 | 11F8 |
| 115.2 | 4000 | BEAE | 172D | 15DB | 2BB7 | 15DB |
| 128 | 4000 | C52D | 14CE | 19FB | 33F6 | 19FB |
| 140.8 | 4000 | CB95 | 12BC | 1E52 | 3CA3 | 1E52 |
| 153.6 | 4000 | D1EA | 10F2 | 22DC | 45B8 | 22DC |
| 166.4 | 4000 | D82D | 0F6A | 2798 | 4F2F | 2798 |
| 179.2 | 4000 | DE61 | 0E21 | 2C82 | 5905 | 2C82 |
| 192 | 4000 | E487 | 0D14 | 319B | 6336 | 319B |
| 204.8 | 4000 | EAA3 | 0C3F | 36E2 | 6DC4 | 36E2 |
| 217.6 | 4000 | F0B6 | 0BA1 | 3C56 | 78AD | 3C56 |
| 230.4 | 4000 | F6C3 | 0B37 | 41FA | 83F4 | 41FA |
| 243.2 | 4000 | FCCC | 0B02 | 47CE | 8F9C | 47CE |
| 256 | 4000 | 02D4 | 0B01 | 4DD4 | 9BA9 | 4DD4 |
| 268.8 | 4000 | 08DD | 0B33 | 540F | A81F | 540F |
| 281.6 | 4000 | 0EE9 | 0B99 | 5A82 | B504 | 5A82 |
| 294.4 | 4000 | 14FC | 0C33 | 612F | C25E | 612F |
| 307.2 | 4000 | 1B17 | 0D05 | 681B | D037 | 681B |
| 320 | 4000 | 213C | 0E0F | 6F4B | DE96 | 6F4B |

For Other Filter Cutoff frequencies please contact Texas Instruments support.

7.4 Device Functional Modes

There are two main functional modes for the PGA305 device: current (4-mA to 20-mA loop) and voltage modes. Depending on which mode is in use, the external components and connections are slightly different.

7.4.1 Voltage Mode

When configured in this mode, the FB⁻ pin must be connected to the OUT pin. If the OUT pin is driving a large capacitive load, a compensation capacitor can be connected to the COMP pin and an isolation resistor can be placed between the OUT and FB⁻ pins. The FB⁺ pin is not used in voltage mode.

7.4.2 Current Mode

When configured in this mode, the OUT pin is driving the base of a bipolar junction transistor (BJT) as shown in [Figure 47](#). The COMP pin is connected to the emitter of the BJT and the FB⁺ pin is connected to the return terminal of the supply. The FB⁻ pin is not used in current mode.

7.5 Register Maps

7.5.1 Register Settings

Before the PAG305 device can be used in any application, the device must be configured by setting various control registers to the desired values. [Table 19](#) lists all the registers that must be configured and their respective default configurations. Note that the registers are configured by writing to the appropriate EEPROM addresses listed in the [Control and Status Registers](#) section.

Register Maps (continued)
Table 19. Default Register Settings

| REGISTER | VALUE (HEX) | DESCRIPTION |
|---------------------------|-------------|--|
| DIG_IF_CTRL | 0x62 | I2C Interface Enabled in Fast Mode (400kHz - 800kHz) |
| DAC_CONFIG | 0x00 | DAC is set for absolute voltage output. |
| OP_STAGE_CTRL | 0x02 | Output is configured for 0V - 5V absolute Voltage Output (DAC Gain 4V/V). |
| BRG_CTRL | 0x01 | Bridge excitation is set to 2.5 V. |
| P_GAIN_SELECT | 0x80 | P_GAIN is set to 5 V/V gain with Signal Inversion. |
| T_GAIN_SELECT | 0x00 | T_GAIN is set for 1.33 V/V gain without Signal Inversion. |
| TEMP_CTRL | 0x40 | I _{TEMP} drive is disabled and T signal chain is set for V _{INT+} - V _{INT-} . |
| TEMP_SE | 0x00 | T GAIN is in single-ended configuration. |
| NORMAL_LOW_LSB | 0x67 | DAC normal low output set to 0x0667. Must be updated during calibration |
| NORMAL_LOW_MSB | 0x06 | DAC normal low output set to 0x0667. Must be updated during calibration |
| NORMAL_HIGH_LSB | 0x9A | DAC normal high output set to 0x399A. Must be updated during calibration |
| NORMAL_HIGH_MSB | 0x39 | DAC normal high output set to 0x399A. Must be updated during calibration |
| LOW_CLAMP_LSB | 0x34 | DAC clamp low output set to 0x0334. Must be updated during calibration |
| LOW_CLAMP_MSB | 0x03 | DAC clamp low output set to 0x0334. Must be updated during calibration |
| HIGH_CLAMP_LSB | 0xCF | DAC clamp high output set to 0x3CCF. Must be updated during calibration |
| HIGH_CLAMP_MSB | 0x3C | DAC clamp high output set to 0x3CCF. Must be updated during calibration |
| DIAG_ENABLE | 0x00 | Application Diagnostics are Disabled (The device will not Reset on WatchDog Error or EEPROM CRC Error) |
| EEPROM_LOCK | 0x00 | EEPROM is unlocked. |
| AFEDIAG_CFG | 0x07 | Diagnostics pulldown (1 MΩ) and pullup (1 MΩ) resistors enabled, VINP_UV threshold = 10% and VINP_OV threshold = 70% |
| DIAG_ENABLE | 0x00 | Diagnostics are disabled. |
| AFEDIAG_MASK | 0x21 | VINP_OV and PGAIN_UV detection enabled |
| SERIAL_NUMBER_BYTE0-1-2-3 | 0x00000000 | Serial number specified by customer |

7.5.2 Control and Status Registers
Table 20. Control and Status Registers

| Register Name | DI Page Address | DI Offset Address | EEPROM Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|-----------------|-------------------|----------------|-----|-------------------|---------|---------|---------|---------|---------|---------|---------|
| H0_LSB | N/A | N/A | 0x40000000 | RW | H0 [7] | H0 [6] | H0 [5] | H0 [4] | H0 [3] | H0 [2] | H0 [1] | H0 [0] |
| H0_MID | N/A | N/A | 0x40000001 | RW | H0 [15] | H0 [14] | H0 [13] | H0 [12] | H0 [11] | H0 [10] | H0 [9] | H0 [8] |
| H0_MSB | N/A | N/A | 0x40000002 | RW | H0 [23] - SIGN | H0 [22] | H0 [21] | H0 [20] | H0 [19] | H0 [18] | H0 [17] | H0 [16] |
| H1_LSB | N/A | N/A | 0x40000003 | RW | H1 [7] | H1 [6] | H1 [5] | H1 [4] | H1 [3] | H1 [2] | H1 [1] | H1 [0] |
| H1_MID | N/A | N/A | 0x40000004 | RW | H1 [15] | H1 [14] | H1 [13] | H1 [12] | H1 [11] | H1 [10] | H1 [9] | H1 [8] |
| H1_MSB | N/A | N/A | 0x40000005 | RW | H1 [23] - SIGN | H1 [22] | H1 [21] | H1 [20] | H1 [19] | H1 [18] | H1 [17] | H1 [16] |
| H2_LSB | N/A | N/A | 0x40000006 | RW | H2 [7] | H2 [6] | H2 [5] | H2 [4] | H2 [3] | H2 [2] | H2 [1] | H2 [0] |
| H2_MID | N/A | N/A | 0x40000007 | RW | H2 [15] | H2 [14] | H2 [13] | H2 [12] | H2 [11] | H2 [10] | H2 [9] | H2 [8] |
| H2_MSB | N/A | N/A | 0x40000008 | RW | H2 [23] - SIGN | H2 [22] | H2 [21] | H2 [20] | H2 [19] | H2 [18] | H2 [17] | H2 [16] |
| H3_LSB | N/A | N/A | 0x40000009 | RW | H3 [7] | H3 [6] | H3 [5] | H3 [4] | H3 [3] | H3 [2] | H3 [1] | H3 [0] |
| H3_MID | N/A | N/A | 0x4000000A | RW | H3 [15] | H3 [14] | H3 [13] | H3 [12] | H3 [11] | H3 [10] | H3 [9] | H3 [8] |
| H3_MSB | N/A | N/A | 0x4000000B | RW | H3 [23] - SIGN | H3 [22] | H3 [21] | H3 [20] | H3 [19] | H3 [18] | H3 [17] | H3 [16] |
| G0_LSB | N/A | N/A | 0x4000000C | RW | G0 [7] | G0 [6] | G0 [5] | G0 [4] | G0 [3] | G0 [2] | G0 [1] | G0 [0] |
| G0_MID | N/A | N/A | 0x4000000D | RW | G0 [15] | G0 [14] | G0 [13] | G0 [12] | G0 [11] | G0 [10] | G0 [9] | G0 [8] |
| G0_MSB | N/A | N/A | 0x4000000E | RW | G0 [23] - SIGN | G0 [22] | G0 [21] | G0 [20] | G0 [19] | G0 [18] | G0 [17] | G0 [16] |
| G1_LSB | N/A | N/A | 0x4000000F | RW | G1 [7] | G1 [6] | G1 [5] | G1 [4] | G1 [3] | G1 [2] | G1 [1] | G1 [0] |
| G1_MID | N/A | N/A | 0x40000010 | RW | G1 [15] | G1 [14] | G1 [13] | G1 [12] | G1 [11] | G1 [10] | G1 [9] | G1 [8] |
| G1_MSB | N/A | N/A | 0x40000011 | RW | G1 [23] - SIGN | G1 [22] | G1 [21] | G1 [20] | G1 [19] | G1 [18] | G1 [17] | G1 [16] |
| G2_LSB | N/A | N/A | 0x40000012 | RW | G2 [7] | G2 [6] | G2 [5] | G2 [4] | G2 [3] | G2 [2] | G2 [1] | G2 [0] |
| G2_MID | N/A | N/A | 0x40000013 | RW | G2 [15] | G2 [14] | G2 [13] | G2 [12] | G2 [11] | G2 [10] | G2 [9] | G2 [8] |
| G2_MSB | N/A | N/A | 0x40000014 | RW | G2 [23] - SIGN | G2 [22] | G2 [21] | G2 [20] | G2 [19] | G2 [18] | G2 [17] | G2 [16] |
| G3_LSB | N/A | N/A | 0x40000015 | RW | G3 [7] | G3 [6] | G3 [5] | G3 [4] | G3 [3] | G3 [2] | G3 [1] | G3 [0] |
| G3_MID | N/A | N/A | 0x40000016 | RW | G3 [15] | G3 [14] | G3 [13] | G3 [12] | G3 [11] | G3 [10] | G3 [9] | G3 [8] |
| G3_MSB | N/A | N/A | 0x40000017 | RW | G3 [23] - SIGN | G3 [22] | G3 [21] | G3 [20] | G3 [19] | G3 [18] | G3 [17] | G3 [16] |
| N0_LSB | N/A | N/A | 0x40000018 | RW | N0 [7] | N0 [6] | N0 [5] | N0 [4] | N0 [3] | N0 [2] | N0 [1] | N0 [0] |
| N0_MID | N/A | N/A | 0x40000019 | RW | N0 [15] | N0 [14] | N0 [13] | N0 [12] | N0 [11] | N0 [10] | N0 [9] | N0 [8] |

Table 20. Control and Status Registers (continued)

| Register Name | DI Page Address | DI Offset Address | EEPROM Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|-----------------|-------------------|----------------|-----|----------------|-----------------|---------------|---------------|---------------|---------------|--------------|--------------|
| N0_MSB | N/A | N/A | 0x4000001A | RW | N0 [23] - SIGN | N0 [22] | N0 [21] | N0 [20] | N0 [19] | N0 [18] | N0 [17] | N0 [16] |
| N1_LSB | N/A | N/A | 0x4000001B | RW | N1 [7] | N1 [6] | N1 [5] | N1 [4] | N1 [3] | N1 [2] | N1 [1] | N1 [0] |
| N1_MID | N/A | N/A | 0x4000001C | RW | N1 [15] | N1 [14] | N1 [13] | N1 [12] | N1 [11] | N1 [10] | N1 [9] | N1 [8] |
| N1_MSB | N/A | N/A | 0x4000001D | RW | N1 [23] - SIGN | N1 [22] | N1 [21] | N1 [20] | N1 [19] | N1 [18] | N1 [17] | N1 [16] |
| N2_LSB | N/A | N/A | 0x4000001E | RW | N2 [7] | N2 [6] | N2 [5] | N2 [4] | N2 [3] | N2 [2] | N2 [1] | N2 [0] |
| N2_MID | N/A | N/A | 0x4000001F | RW | N2 [15] | N2 [14] | N2 [13] | N2 [12] | N2 [11] | N2 [10] | N2 [9] | N2 [8] |
| N2_MSB | N/A | N/A | 0x40000020 | RW | N2 [23] - SIGN | N2 [22] | N2 [21] | N2 [20] | N2 [19] | N2 [18] | N2 [17] | N2 [16] |
| N3_LSB | N/A | N/A | 0x40000021 | RW | N3 [7] | N3 [6] | N3 [5] | N3 [4] | N3 [3] | N3 [2] | N3 [1] | N3 [0] |
| N3_MID | N/A | N/A | 0x40000022 | RW | N3 [15] | N3 [14] | N3 [13] | N3 [12] | N3 [11] | N3 [10] | N3 [9] | N3 [8] |
| N3_MSB | N/A | N/A | 0x40000023 | RW | N3 [23] - SIGN | N3 [22] | N3 [21] | N3 [20] | N3 [19] | N3 [18] | N3 [17] | N3 [16] |
| M0_LSB | N/A | N/A | 0x40000024 | RW | M0 [7] | M0 [6] | M0 [5] | M0 [4] | M0 [3] | M0 [2] | M0 [1] | M0 [0] |
| M0_MID | N/A | N/A | 0x40000025 | RW | M0 [15] | M0 [14] | M0 [13] | M0 [12] | M0 [11] | M0 [10] | M0 [9] | M0 [8] |
| M0_MSB | N/A | N/A | 0x40000026 | RW | M0 [23] - SIGN | M0 [22] | M0 [21] | M0 [20] | M0 [19] | M0 [18] | M0 [17] | M0 [16] |
| M1_LSB | N/A | N/A | 0x40000027 | RW | M1 [7] | M1 [6] | M1 [5] | M1 [4] | M1 [3] | M1 [2] | M1 [1] | M1 [0] |
| M1_MID | N/A | N/A | 0x40000028 | RW | M1 [15] | M1 [14] | M1 [13] | M1 [12] | M1 [11] | M1 [10] | M1 [9] | M1 [8] |
| M1_MSB | N/A | N/A | 0x40000029 | RW | M1 [23] - SIGN | M1 [22] | M1 [21] | M1 [20] | M1 [19] | M1 [18] | M1 [17] | M1 [16] |
| M2_LSB | N/A | N/A | 0x4000002A | RW | M2 [7] | M2 [6] | M2 [5] | M2 [4] | M2 [3] | M2 [2] | M2 [1] | M2 [0] |
| M2_MID | N/A | N/A | 0x4000002B | RW | M2 [15] | M2 [14] | M2 [13] | M2 [12] | M2 [11] | M2 [10] | M2 [9] | M2 [8] |
| M2_MSB | N/A | N/A | 0x4000002C | RW | M2 [23] - SIGN | M2 [22] | M2 [21] | M2 [20] | M2 [19] | M2 [18] | M2 [17] | M2 [16] |
| M3_LSB | N/A | N/A | 0x4000002D | RW | M3 [7] | M3 [6] | M3 [5] | M3 [4] | M3 [3] | M3 [2] | M3 [1] | M3 [0] |
| M3_MID | N/A | N/A | 0x4000002E | RW | M3 [15] | M3 [14] | M3 [13] | M3 [12] | M3 [11] | M3 [10] | M3 [9] | M3 [8] |
| M3_MSB | N/A | N/A | 0x4000002F | RW | M3 [23] - SIGN | M3 [22] | M3 [21] | M3 [20] | M3 [19] | M3 [18] | M3 [17] | M3 [16] |
| DIG_IF_CTRL | N/A | N/A | 0x40000030 | RW | | I2C_DEGLITCH_EN | I2C_RATE | Reserved | Reserved | Reserved | I2C_EN | Reserved |
| PADC_DATA1 | 0x2 | 0x20 | N/A | R | PADC_DATA[7] | PADC_DATA[6] | PADC_DATA[5] | PADC_DATA[4] | PADC_DATA[3] | PADC_DATA[2] | PADC_DATA[1] | PADC_DATA[0] |
| PADC_DATA2 | 0x2 | 0x21 | N/A | R | PADC_DATA[15] | PADC_DATA[14] | PADC_DATA[13] | PADC_DATA[12] | PADC_DATA[11] | PADC_DATA[10] | PADC_DATA[9] | PADC_DATA[8] |

Table 20. Control and Status Registers (continued)

| Register Name | DI Page Address | DI Offset Address | EEPROM Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----------------|-------------------|----------------|-----|-----------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|--------------------|
| PADC_DATA3 | 0x2 | 0x22 | N/A | R | PADC_DATA_SIGN | PADC_DATA[22] | PADC_DATA[21] | PADC_DATA[20] | PADC_DATA[19] | PADC_DATA[18] | PADC_DATA[17] | PADC_DATA[16] |
| TADC_DATA1 | 0x2 | 0x24 | N/A | R | TADC_DATA[7] | TADC_DATA[6] | TADC_DATA[5] | TADC_DATA[4] | TADC_DATA[3] | TADC_DATA[2] | TADC_DATA[1] | TADC_DATA[0] |
| TADC_DATA2 | 0x2 | 0x25 | N/A | R | TADC_DATA[15] | TADC_DATA[14] | TADC_DATA[13] | TADC_DATA[12] | TADC_DATA[11] | TADC_DATA[10] | TADC_DATA[9] | TADC_DATA[8] |
| TADC_DATA3 | 0x2 | 0x26 | N/A | R | TADC_DATA_SIGN | TADC_DATA[22] | TADC_DATA[21] | TADC_DATA[20] | TADC_DATA[19] | TADC_DATA[18] | TADC_DATA[17] | TADC_DATA[16] |
| DAC_REG0_1 | 0x2 | 0x30 | N/A | RW | DAC_REG0[7] | DAC_REG0[6] | DAC_REG0[5] | DAC_REG0[4] | DAC_REG0[3] | DAC_REG0[2] | DAC_REG0[1] | DAC_REG0[0] |
| DAC_REG0_2 | 0x2 | 0x31 | N/A | RW | | | DAC_REG0[13] | DAC_REG0[12] | DAC_REG0[11] | DAC_REG0[10] | DAC_REG0[9] | DAC_REG0[8] |
| DAC_CTRL_STATUS | 0x2 | 0x38 | 0x40000031 | RW | | | | | | | | DAC_ENABLE |
| DAC_CONFIG | 0x2 | 0x39 | 0x40000032 | RW | | | | | | | | DAC_RATIO_METER_IC |
| OP_STAGE_CTRL | 0x2 | 0x3B | 0x40000033 | RW | | | | DACCAP_EN | 4_20MA_EN | DAC_GAIN[2] | DAC_GAIN[1] | DAC_GAIN[0] |
| BRDG_CTRL | 0x2 | 0x46 | 0x40000034 | RW | | | | | | VBRDG_CTRL[1] | VBRDG_CTRL[0] | BRDG_EN |
| P_GAIN_SELECT | 0x2 | 0x47 | 0x40000035 | RW | P_INV | | | P_GAIN[4] | P_GAIN[3] | P_GAIN[2] | P_GAIN[1] | P_GAIN[0] |
| T_GAIN_SELECT | 0x2 | 0x48 | 0x40000036 | RW | T_INV | | | | | | T_GAIN[1] | T_GAIN[0] |
| TEMP_CTRL | 0x2 | 0x4C | 0x40000037 | RW | | ITEMP_CTRL[2] | ITEMP_CTRL[1] | ITEMP_CTRL[0] | TEMP_MUX_CTRL[3] | TEMP_MUX_CTRL[2] | TEMP_MUX_CTRL[1] | TEMP_MUX_CTRL[0] |
| TEMP_SE | N/A | N/A | 0x4000003A | RW | | | | | | | | TEMP_SE |
| NORMAL_LOW_LSB | N/A | N/A | 0x4000003C | RW | NORMAL_LOW[7] | NORMAL_LOW[6] | NORMAL_LOW[5] | NORMAL_LOW[4] | NORMAL_LOW[3] | NORMAL_LOW[2] | NORMAL_LOW[1] | NORMAL_LOW[0] |
| NORMAL_LOW_MSB | N/A | N/A | 0x4000003D | RW | NORMAL_LOW[15] | NORMAL_LOW[14] | NORMAL_LOW[13] | NORMAL_LOW[12] | NORMAL_LOW[11] | NORMAL_LOW[10] | NORMAL_LOW[9] | NORMAL_LOW[8] |
| NORMAL_HIGH_LSB | N/A | N/A | 0x4000003E | RW | NORMAL_HIGH[7] | NORMAL_HIGH[6] | NORMAL_HIGH[5] | NORMAL_HIGH[4] | NORMAL_HIGH[3] | NORMAL_HIGH[2] | NORMAL_HIGH[1] | NORMAL_HIGH[0] |
| NORMAL_HIGH_MSB | N/A | N/A | 0x4000003F | RW | NORMAL_HIGH[15] | NORMAL_HIGH[14] | NORMAL_HIGH[13] | NORMAL_HIGH[12] | NORMAL_HIGH[11] | NORMAL_HIGH[10] | NORMAL_HIGH[9] | NORMAL_HIGH[8] |
| LOW_CLAMP_LSB | N/A | N/A | 0x40000040 | RW | LOW_CLAMP[7] | LOW_CLAMP[6] | LOW_CLAMP[5] | LOW_CLAMP[4] | LOW_CLAMP[3] | LOW_CLAMP[2] | LOW_CLAMP[1] | LOW_CLAMP[0] |

Table 20. Control and Status Registers (continued)

| Register Name | DI Page Address | DI Offset Address | EEPROM Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----------------|-------------------|----------------|-----|------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|
| LOW_CLAMP_MSB | N/A | N/A | 0x40000041 | RW | LOW_CLAMP[15] | LOW_CLAMP[14] | LOW_CLAMP[13] | LOW_CLAMP[12] | LOW_CLAMP[11] | LOW_CLAMP[10] | LOW_CLAMP[9] | LOW_CLAMP[8] |
| HIGH_CLAMP_LSB | N/A | N/A | 0x40000042 | RW | HIGH_CLAMP[7] | HIGH_CLAMP[6] | HIGH_CLAMP[5] | HIGH_CLAMP[4] | HIGH_CLAMP[3] | HIGH_CLAMP[2] | HIGH_CLAMP[1] | HIGH_CLAMP[0] |
| HIGH_CLAMP_MSB | N/A | N/A | 0x40000043 | RW | HIGH_CLAMP[15] | HIGH_CLAMP[14] | HIGH_CLAMP[13] | HIGH_CLAMP[12] | HIGH_CLAMP[11] | HIGH_CLAMP[10] | HIGH_CLAMP[9] | HIGH_CLAMP[8] |
| PADC_GAIN_LSB | N/A | N/A | 0x40000044 | RW | PADC_GAIN[7] | PADC_GAIN[6] | PADC_GAIN[5] | PADC_GAIN[4] | PADC_GAIN[3] | PADC_GAIN[2] | PADC_GAIN[1] | PADC_GAIN[0] |
| PADC_GAIN_MID | N/A | N/A | 0x40000045 | RW | PADC_GAIN[15] | PADC_GAIN[14] | PADC_GAIN[13] | PADC_GAIN[12] | PADC_GAIN[11] | PADC_GAIN[10] | PADC_GAIN[9] | PADC_GAIN[8] |
| PADC_GAIN_MSB | N/A | N/A | 0x40000046 | RW | PADC_GAIN_SIGN[22] | PADC_GAIN[21] | PADC_GAIN[20] | PADC_GAIN[19] | PADC_GAIN[18] | PADC_GAIN[17] | PADC_GAIN[16] | PADC_GAIN[15] |
| PADC_OFFSET_LSB | N/A | N/A | 0x40000047 | RW | PADC_OFFSET[7] | PADC_OFFSET[6] | PADC_OFFSET[5] | PADC_OFFSET[4] | PADC_OFFSET[3] | PADC_OFFSET[2] | PADC_OFFSET[1] | PADC_OFFSET[0] |
| PADC_GAIN_MID | N/A | N/A | 0x40000048 | RW | PADC_OFFSET[15] | PADC_OFFSET[14] | PADC_OFFSET[13] | PADC_OFFSET[12] | PADC_OFFSET[11] | PADC_OFFSET[10] | PADC_OFFSET[9] | PADC_OFFSET[8] |
| PADC_OFFSET_MSB | N/A | N/A | 0x40000049 | RW | PADC_OFFSET_SIGN[22] | PADC_OFFSET[21] | PADC_OFFSET[20] | PADC_OFFSET[19] | PADC_OFFSET[18] | PADC_OFFSET[17] | PADC_OFFSET[16] | PADC_OFFSET[15] |
| A0_LSB | N/A | N/A | 0x4000004A | RW | IIR_FILTER_A0[7] | IIR_FILTER_A0[6] | IIR_FILTER_A0[5] | IIR_FILTER_A0[4] | IIR_FILTER_A0[3] | IIR_FILTER_A0[2] | IIR_FILTER_A0[1] | IIR_FILTER_A0[0] |
| A0_MSB | N/A | N/A | 0x4000004B | RW | IIR_FILTER_A0[15] | IIR_FILTER_A0[14] | IIR_FILTER_A0[13] | IIR_FILTER_A0[12] | IIR_FILTER_A0[11] | IIR_FILTER_A0[10] | IIR_FILTER_A0[9] | IIR_FILTER_A0[8] |
| A1_LSB | N/A | N/A | 0x4000004C | RW | IIR_FILTER_A1[7] | IIR_FILTER_A1[6] | IIR_FILTER_A1[5] | IIR_FILTER_A1[4] | IIR_FILTER_A1[3] | IIR_FILTER_A1[2] | IIR_FILTER_A1[1] | IIR_FILTER_A1[0] |
| A1_MSB | N/A | N/A | 0x4000004D | RW | IIR_FILTER_A1_SIGN[14] | IIR_FILTER_A1[13] | IIR_FILTER_A1[12] | IIR_FILTER_A1[11] | IIR_FILTER_A1[10] | IIR_FILTER_A1[9] | IIR_FILTER_A1[8] | IIR_FILTER_A1[7] |
| A2_LSB | N/A | N/A | 0x4000004E | RW | IIR_FILTER_A2[7] | IIR_FILTER_A2[6] | IIR_FILTER_A2[5] | IIR_FILTER_A2[4] | IIR_FILTER_A2[3] | IIR_FILTER_A2[2] | IIR_FILTER_A2[1] | IIR_FILTER_A2[0] |
| A2_MSB | N/A | N/A | 0x4000004F | RW | IIR_FILTER_A2[15] | IIR_FILTER_A2[14] | IIR_FILTER_A2[13] | IIR_FILTER_A2[12] | IIR_FILTER_A2[11] | IIR_FILTER_A2[10] | IIR_FILTER_A2[9] | IIR_FILTER_A2[8] |
| B0_LSB | N/A | N/A | 0x40000050 | RW | IIR_FILTER_B0[7] | IIR_FILTER_B0[6] | IIR_FILTER_B0[5] | IIR_FILTER_B0[4] | IIR_FILTER_B0[3] | IIR_FILTER_B0[2] | IIR_FILTER_B0[1] | IIR_FILTER_B0[0] |
| B0_MSB | N/A | N/A | 0x40000051 | RW | IIR_FILTER_B0[15] | IIR_FILTER_B0[14] | IIR_FILTER_B0[13] | IIR_FILTER_B0[12] | IIR_FILTER_B0[11] | IIR_FILTER_B0[10] | IIR_FILTER_B0[9] | IIR_FILTER_B0[8] |
| B1_LSB | N/A | N/A | 0x40000052 | RW | IIR_FILTER_B1[7] | IIR_FILTER_B1[6] | IIR_FILTER_B1[5] | IIR_FILTER_B1[4] | IIR_FILTER_B1[3] | IIR_FILTER_B1[2] | IIR_FILTER_B1[1] | IIR_FILTER_B1[0] |
| B1_MSB | N/A | N/A | 0x40000053 | RW | IIR_FILTER_B1_SIGN[15] | IIR_FILTER_B1[14] | IIR_FILTER_B1[13] | IIR_FILTER_B1[12] | IIR_FILTER_B1[11] | IIR_FILTER_B1[10] | IIR_FILTER_B1[9] | IIR_FILTER_B1[8] |

Table 20. Control and Status Registers (continued)

| Register Name | DI Page Address | DI Offset Address | EEPROM Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------|-----------------|-------------------|----------------|-----|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| B2_LSB | N/A | N/A | 0x40000054 | RW | IIR_FILT_B2[7] | IIR_FILT_B2[6] | IIR_FILT_B2[5] | IIR_FILT_B2[4] | IIR_FILT_B2[3] | IIR_FILT_B2[2] | IIR_FILT_B2[1] | IIR_FILT_B2[0] |
| B2_MSB | N/A | N/A | 0x40000055 | RW | IIR_FILT_B2[15] | IIR_FILT_B2[14] | IIR_FILT_B2[13] | IIR_FILT_B2[12] | IIR_FILT_B2[11] | IIR_FILT_B2[10] | IIR_FILT_B2[9] | IIR_FILT_B2[8] |
| DIAG_ENABLE | N/A | N/A | 0x40000056 | RW | | | | | | | | DIAG_ENABLE |
| EEPROM_LOCK | N/A | N/A | 0x40000057 | RW | | | | | | | | EEPROM_LOCK |
| AFEDIAG_CFG | N/A | N/A | 0x40000058 | RW | - | DIS_R_T | DIS_R_P | THRS[2] | THRS[1] | THRS[0] | PD2 | PD1 |
| AFEDIAG_MASK | N/A | N/A | 0x40000059 | RW | TGAIN_UV | TGAIN_OV | PGAIN_UV | PGAIN_OV | - | INT_OV | INP_UV | INP_OV |
| FAULT_LSB | N/A | N/A | 0x4000005C | RW | | | | | | | | |
| FAULT_MSB | N/A | N/A | 0x4000005D | RW | | | | | | | | |
| TADC_GAIN_LSB | N/A | N/A | 0x4000005E | RW | TADC_GAIN[7] | TADC_GAIN[6] | TADC_GAIN[5] | TADC_GAIN[4] | TADC_GAIN[3] | TADC_GAIN[2] | TADC_GAIN[1] | TADC_GAIN[0] |
| TADC_GAIN_MID | N/A | N/A | 0x4000005F | RW | TADC_GAIN[15] | TADC_GAIN[14] | TADC_GAIN[13] | TADC_GAIN[12] | TADC_GAIN[11] | TADC_GAIN[10] | TADC_GAIN[9] | TADC_GAIN[8] |
| TADC_GAIN_MSB | N/A | N/A | 0x40000060 | RW | TADC_GAIN_SIGN | TADC_GAIN[22] | TADC_GAIN[21] | TADC_GAIN[20] | TADC_GAIN[19] | TADC_GAIN[18] | TADC_GAIN[17] | TADC_GAIN[16] |
| TADC_OFFSET_LSB | N/A | N/A | 0x40000061 | RW | TADC_OFFSET[7] | TADC_OFFSET[6] | TADC_OFFSET[5] | TADC_OFFSET[4] | TADC_OFFSET[3] | TADC_OFFSET[2] | TADC_OFFSET[1] | TADC_OFFSET[0] |
| TADC_OFFSET_MID | N/A | N/A | 0x40000062 | RW | TADC_OFFSET[15] | TADC_OFFSET[14] | TADC_OFFSET[13] | TADC_OFFSET[12] | TADC_OFFSET[11] | TADC_OFFSET[10] | TADC_OFFSET[9] | TADC_OFFSET[8] |
| TADC_OFFSET_MSB | N/A | N/A | 0x40000063 | RW | TADC_OFFSET_SIGN | TADC_OFFSET[22] | TADC_OFFSET[21] | TADC_OFFSET[20] | TADC_OFFSET[19] | TADC_OFFSET[18] | TADC_OFFSET[17] | TADC_OFFSET[16] |
| SERIAL_NUMBER_BYTE0 | N/A | N/A | 0x40000064 | RW | | | | | | | | |
| SERIAL_NUMBER_BYTE1 | N/A | N/A | 0x40000065 | RW | | | | | | | | |
| SERIAL_NUMBER_BYTE2 | N/A | N/A | 0x40000066 | RW | | | | | | | | |
| SERIAL_NUMBER_BYTE3 | N/A | N/A | 0x40000067 | RW | | | | | | | | |
| ADC_24BIT_ENABLE | N/A | N/A | 0x40000068 | RW | | | | | | | | ADC_24BIT_EN |
| OFFSET_ENABLE | N/A | N/A | 0x40000069 | RW | | | | | | | | OFF_EN |
| EEPROM_CRC_VALUE | 0x5 | 0x8D | 0x4000007F | R | EEPROM_CRC[7] | EEPROM_CRC[6] | EEPROM_CRC[5] | EEPROM_CRC[4] | EEPROM_CRC[3] | EEPROM_CRC[2] | EEPROM_CRC[1] | EEPROM_CRC[0] |

Table 20. Control and Status Registers (continued)

| Register Name | DI Page Address | DI Offset Address | EEPROM Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------|-----------------|-------------------|----------------|-----|----|----|----|----|-----------------------|---------------------|--------------------|-------------------|
| COMPENSATION_CONTROL | 0x0 | 0x0C | N/A | RW | | | | | | | COMPENSATION_RESET | IF_SEL |
| EEPROM_ARRAY | 0x5 | 0x00-0x7F | N/A | RW | | | | | | | | |
| EEPROM_CACHE | 0x5 | 0x80-0x87 | N/A | RW | | | | | | | | |
| EEPROM_PAGE_ADDRESS | 0x5 | 0x88 | N/A | RW | | | | | | ADDR[2] | ADDR[1] | ADDR[0] |
| EEPROM_CTRL | 0x5 | 0x89 | N/A | RW | | | | | FIXED_ERASE_PROG_TIME | ERASE_AND_PROGRAM | ERASE | PROGRAM |
| EEPROM_CRC | 0x5 | 0x8A | N/A | RW | | | | | | | | CALCULATE_CRC |
| EEPROM_STATUSES | 0x5 | 0x8B | N/A | R | | | | | | PROGRAM_IN_PROGRESS | ERASE_IN_PROGRESS | READ_IN_PROGRESS |
| EEPROM_CRC_STATUS | 0x5 | 0x8C | N/A | R | | | | | | | CRC_GOOD | CRC_CHECK_IN_PROG |

7.5.2.1 Digital Interface Control (M0 Address = 0x40000506) (DI Page Address = 0x2) (DI Page Offset = 0x06)
Table 21. DIG_IF_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|-----------------|----------|---|---|---|--------|---|
| | I2C_DEGLITCH_EN | I2C_RATE | - | - | - | I2C_EN | - |
| | RW | RW | R | R | R | RW | R |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

Table 22. DIG_IF_CTRL Field Descriptions

| Register | Bit | Description |
|-------------|--------------------|---|
| DIG_IF_CTRL | 0: | |
| | 1: I2C_EN | 1: I2C is Enabled 0: I2C is Disabled |
| | 2: | |
| | 3: | |
| | 4: | |
| | 5: I2C_RATE | 1: I2C transfer rate is >400KPBPS, ≤800 KBPS 0: I2C transfer rate is ≤400 KBPS |
| | 6: I2C_DEGLITCH_EN | 1: Enables deglitch filters on I2C interface 0: Disables deglitch filters on I2C interface |
| | 7: | |

7.5.2.2 DAC_CTRL_STATUS (M0 Address: 0x40000538) (DI Page Address: 0x2) (DI Page Offset: 0x38)
Table 23. DAC_CTRL_STATUS Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|----|------------|
| | | | | | | | DAC_ENABLE |
| | | R | R | | | RW | RW |
| | | 0 | 0 | | | 0 | 0 |

Table 24. DAC_CTRL_STATUS Field Descriptions

| Register | Bit | Description |
|-----------------|---------------|--|
| DAC_CTRL_STATUS | 0: DAC_ENABLE | 1: DAC is enabled to drive DAC GAIN; i.e., DAC GAIN output is based on DAC_REG0 value 0: DAC GAIN output is based on the setting of PWM_EN bit in PWM_EN register |
| | 1: | |
| | 3: | |
| | 4: | |
| | 4: | |
| | 5: | |
| | 6: | |
| | 7: | |

7.5.2.3 DAC_CONFIG (EEPROM Address = 0x40000032) (DI Page Address: 0x2) (DI Page Offset: 0x39)
Figure 26. DAC_CONFIG Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|-----------------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | DAC_RATIOMETRIC |
| | | | | | | | RW |
| | | | | | | | 0 |

Table 25. DAC_CONFIG Field Descriptions

| Register | Bit | Description |
|------------|--------------------|---|
| DAC_CONFIG | 0: DAC_RATIOMETRIC | 1: DAC is in ratiometric mode 0: DAC is in absolute mode |
| | 1–7: UNUSED | |

7.5.2.4 OP_STAGE_CTRL (EEPROM Address = 0x40000033) (DI Page Address: 0x2) (DI Page Offset: 0x3B)
Figure 27. OP_STAGE_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|-----------|-----------|-----------|-------------|-------------|-------------|
| UNUSED | UNUSED | PULLUP_EN | DACCAP_EN | 4_20MA_EN | DAC_GAIN[2] | DAC_GAIN[1] | DAC_GAIN[0] |
| | | RW | RW | RW | RW | RW | RW |
| | | 0 | 0 | 0 | 1 | 0 | 1 |

Table 26. OP_STAGE_CTRL Field Descriptions

| Register | Bit | Description |
|---------------|--|--|
| OP_STAGE_CTRL | 0: DAC_GAIN[0] | DAC_GAIN[2] DAC_GAIN[1] DAC_GAIN[0] Description |
| | 1: DAC_GAIN[1] | 0 0 0 Voltage mode disabled |
| | 2: DAC_GAIN[2] | 0 0 1 Gain = 10V/V |
| | | 0 1 0 Gain = 4V/V |
| | | 0 1 1 Reserved |
| | | 1 0 0 Gain = 2V/V |
| | | 1 0 1 Reserved |
| | | 1 1 0 Gain = 6.67V/V |
| | | 1 1 1 Reserved |
| | 3: 4_20MA_EN | 1: Enable 4 to 20mA Current Loop (Close switch S5 in DAC Gain) 0: Disable 4 to 20mA Current Loop (Open switch S5 in DAC Gain) |
| | 4: DACCAP_EN | 1: Enable DACCAP capacitor (Close switch S4 in DAC Gain) 0: Disable DACCAP capacitor (Open switch S4 in DAC Gain) |
| 5: PULLUP_EN | 1: Enable Pull up at the input of DAC Gain (Close switch S8 in DAC Gain) 0: Disable Pull up at the input of DAC Gain (Open switch S8 in DAC Gain) | |
| 6–7: UNUSED | | |

7.5.2.5 BRDG_CTRL (EEPROM Address = 0x40000034) (DI Page Address: 0x2) (DI Page Offset: 0x46)
Figure 28. BRDG_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|---------------|---------------|---------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | VBRDG_CTRL[1] | VBRDG_CTRL[0] | BRDG_EN |
| | | | | | RW | RW | |
| | | | | | 0 | 0 | |

Table 27. BRDG_CTRL Field Descriptions

| Register | Bit | Description |
|---|--------------------------------------|--|
| BRDG_CTRL | 0: BRDG_EN | 0: Bridge Voltage Disabled 1: Bridge Voltage Enabled |
| | 1: VBRDG_CTRL[0] 2: VBRDG_CTRL[1] | VBRDG_CTRL[1] VBRDG_CTRL[0] Bridge Supply Voltage |
| | | 0 0 2.5V |
| | | 0 1 2.0V |
| | | 1 0 1.25V |
| 1 1 1.25V | | |
| 3–7: UNUSED | | |

7.5.2.6 P_GAIN_SELECT (EEPROM Address = 0x40000035) (DI Page Address: 0x2) (DI Page Offset: 0x47)
Figure 29. P_GAIN_SELECT Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|--------|-----------|-----------|-----------|-----------|-----------|
| P_INV | UNUSED | UNUSED | P_GAIN[4] | P_GAIN[3] | P_GAIN[2] | P_GAIN[1] | P_GAIN[0] |
| RW | | | RW | RW | RW | RW | RW |
| 0 | | | 0 | 0 | 0 | 0 | 0 |

Table 28. P_GAIN_SELECT Field Descriptions

| Register | Bit | Description |
|---------------|--|--|
| P_GAIN_SELECT | 0: P_GAIN[0] 1: P_GAIN[1] 2: P_GAIN[2] 3: P_GAIN[3] 4: P_GAIN[4] | See Electrical Parameters for Gain Selections |
| | 5–6: UNUSED | |
| | 7: P_INV | 1: Inverts the output of the PGAIN Output 0: No Inversion |

7.5.2.7 T_GAIN_SELECT (EEPROM Address = 0x40000036) (DI Page Address: 0x2) (DI Page Offset: 0x48)
Figure 30. T_GAIN_SELECT Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|--------|--------|--------|--------|-----------|-----------|
| T_INV | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | T_GAIN[1] | T_GAIN[0] |
| RW | | | | | | RW | RW |
| 0 | | | | | | 0 | 0 |

Table 29. T_GAIN_SELECT Field Descriptions

| Register | Bit | Description |
|---------------|------------------------------|---|
| T_GAIN_SELECT | 0: T_GAIN[0] 1: T_GAIN[1] | See Electrical Parameters for Gain Selections |
| | 2–6: UNUSED | |
| | 7: T_INV | 1: Inverts the output of the T GAIN Output 0: No Inversion |

7.5.2.8 TEMP_CTRL (EEPROM Address = 0x40000037) (DI Page Address: 0x2) (DI Page Offset: 0x4C)
Figure 31. TEMP_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|---------------|---------------|------------------|------------------|------------------|------------------|
| UNUSED | ITEMP_CTRL[2] | ITEMP_CTRL[1] | ITEMP_CTRL[0] | TEMP_MUX_CTRL[3] | TEMP_MUX_CTRL[2] | TEMP_MUX_CTRL[1] | TEMP_MUX_CTRL[0] |
| | RW | RW | RW | RW | RW | RW | RW |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 30. TEMP_CTRL Field Descriptions

| Register | Bit | Description | | | | Description | |
|-----------|---------------------|--------------------|------------------|--------------------|------------------|---|-------------|
| | | TEMP_MUX_CTRL[3] | TEMP_MUX_CTRL[2] | TEMP_MUX_CTRL[1] | TEMP_MUX_CTRL[0] | | |
| TEMP_CTRL | 0: TEMP_MUX_CTRL[0] | 0 | 0 | 0 | 0 | INT+ and INT– | |
| | 1: TEMP_MUX_CTRL[1] | 0 | 0 | 1 | 1 | VTEMP_INT-GND (Internal Temperature Sensor) | |
| | 2: TEMP_MUX_CTRL[2] | Other Combinations | | Other Combinations | | Reserved | |
| | 3: TEMP_MUX_CTRL[3] | | | | | | |
| | | ITEMP_CTRL[2] | | ITEMP_CTRL[1] | ITEMP_CTRL[0] | | Description |
| | | 4: ITEMP_CTRL[0] | 0 | | 0 | 0 | 25µA |
| | | 5: ITEMP_CTRL[1] | 0 | | 0 | 1 | 50µA |
| | | 6: ITEMP_CTRL[2] | 0 | | 1 | 0 | 100µA |
| | | | 0 | | 1 | 1 | 500µA |
| | | | 1 | | X | X | OFF |
| | | 7: UNUSED | | | | | |

7.5.2.9 TEMP_SE (EEPROM Address = 0x4000003A)
Figure 32. TEMP_SE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|---------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | TEMP_SE |
| | | | | | | | RW |
| | | | | | | | 0 |

Table 31. TEMP_SE Field Descriptions

| Register | Bit | Description |
|----------|-------------|--|
| TEMP_SE | 0: TEMP_SE | 1: Output of Temperature Mux is differential 0: Output of Temperature Mux is single-ended |
| | 1–7: UNUSED | |

7.5.2.10 DIAG_ENABLE (EEPROM Address = 0x40000056)
Figure 33. DIAG_ENABLE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|-------------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | DIAG_ENABLE |
| | | | | | | | RW |
| | | | | | | | 0 |

Table 32. DIAG_ENABLE Field Descriptions

| Register | Bit | Description |
|-------------|----------------|---|
| DIAG_ENABLE | 0: DIAG_ENABLE | Read: 1: Enables Diagnostics 0: Disables Diagnostics |
| | 1–7: UNUSED | |

7.5.2.11 EEPROM_LOCK (EEPROM Address = 0x40000057)
Figure 34. EEPROM_LOCK Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|-------------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | EEPROM_LOCK |
| | | | | | | | RW |
| | | | | | | | 0 |

Table 33. EEPROM_LOCK Field Descriptions

| Register | Bit | Description |
|-------------|----------------|--|
| EEPROM_LOCK | 0: EEPROM_LOCK | 1: EEPROM is locked - EEPROM is not accessible 0: EEPROM is unlocked - EEPROM is accessible |
| | 1–7: UNUSED | |

7.5.2.12 AFEDIAG_CFG (EEPROM Address = 0x40000058)
Figure 35. AFEDIAG_CFG Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|---------|---------|---------|---------|-----|-----|
| UNUSED | DIS_R_T | DIS_R_P | THRS[2] | THRS[1] | THRS[0] | PD2 | PD1 |
| | RW | RW | RW | RW | RW | RW | RW |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 34. AFEDIAG_CFG Field Descriptions

| Register | Bit | Description | | | | | |
|-------------|------------|---|----------------|----------------|----------------|---------------------------------|---------------------------|
| AFEDIAG_CFG | | PD2 | | | PD1 | Pull Down Resistor Value | |
| | 0: PD1 | 0 | | | 0 | 4MΩ | |
| | 1: PD2 | 1 | | | 0 | 3MΩ | |
| | | 0 | | | 1 | 2MΩ | |
| | | 1 | | | 1 | 1MΩ | |
| | | | THRS[2] | THRS[1] | THRS[0] | VINP_UV Threshold | VINP_OV Threshold |
| | 2: THRS[0] | 0 | 0 | 0 | | 5% of Programmed VBRDG | 95% of Programmed VBRDG |
| | 3: THRS[1] | 0 | 0 | 1 | | 7.5% of Programmed VBRDG | 92.5% if Programmed VBRDG |
| | 4: THRS[2] | 0 | 1 | 0 | | 10% of Programmed VBRDG | 90% of Programmed VBRDG |
| | | 0 | 1 | 1 | | 12.5% of Programmed VBRDG | 87.5% of Programmed VBRDG |
| | | 1 | 0 | 0 | | 15% of Programmed VBRDG | 85% of Programmed VBRDG |
| | | 1 | 0 | 1 | | 20% of Programmed VBRDG | 80% of Programmed VBRDG |
| | | 1 | 1 | 0 | | 25% of Programmed VBRDG | 75% of Programmed VBRDG |
| | | 1 | 1 | 1 | | 30% of Programmed VBRDG | 70% of Programmed VBRDG |
| | 5: DIS_R_P | 1: Disables pulldown resistors used for open/short diagnostics on the INP+ and INP– pins 0: Enables pulldown resistors used for open/short diagnostics on the INP+ and INP– pins | | | | | |
| | 6: DIS_R_T | 1: Disables pullup resistors used for open/short diagnostics on the INT+ and INT– pins 0: Enables pullup resistors used for open/short diagnostics on the INT+ and INT– pins | | | | | |
| 7: UNUSED | | | | | | | |

7.5.2.13 AFEDIAG_MASK (EEPROM Address = 0x40000059)
Figure 36. AFEDIAG_MASK Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|--------|--------|--------|--------|
| TGAIN_UV | TGAIN_OV | PGAIN_UV | PGAIN_OV | UNUSED | INT_OV | INP_UV | INP_OV |
| RW | RW | RW | RW | | RW | RW | RW |
| 0 | 0 | 0 | 0 | | 0 | 0 | 0 |

Table 35. AFEDIAG_MASK Field Descriptions

| Register | Bit | Description |
|----------|-------------|---|
| AFEDIAG | 0: INP_OV | 1: Enable overvoltage detection at input pins of P Gain 0: Disable overvoltage detection at input pins of P Gain |
| | 1: INP_UV | 1: Enable undervoltage detection at input pins of P Gain 0: Disable undervoltage detection at input pins of P Gain |
| | 2: INT_OV | 1: Enable overvoltage detection at input pins of T Gain 0: Disable overvoltage detection at input pins of T Gain |
| | 3: UNUSED | |
| | 4: PGAIN_OV | 1: Enable overvoltage detection at output pins of P Gain 0: Disable overvoltage detection at output pins of P Gain |
| | 5: PGAIN_UV | 1: Enable undervoltage detection at output pins of P Gain 0: Disable undervoltage detection at output pins of P Gain |
| | 6: TGAIN_OV | 1: Enable overvoltage detection at output pins of T Gain 0: Disable overvoltage detection at output pins of T Gain |
| | 7: TGAIN_UV | 1: Enable undervoltage detection at output pins of T Gain 0: Disable undervoltage detection at output pins of T Gain |

7.5.2.14 ADC_24BIT_ENABLE (EEPROM Address = 0x40000068)
Figure 37. ADC_24BIT_ENABLE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|------------------|
| | | | | | | | ADC_24BIT_E N |
| | | | | | | | RW |
| | | | | | | | 1 |

Table 36. ADC_24BIT_ENABLE Field Descriptions

| Register | Bit | Description |
|----------------------|-----------------|--|
| ADC_24BIT_EN ABLE | 0: ADC_24BIT_EN | 1: 24 bit Data Compensation and Output 0: 16 bit Data Compensation and Output |
| | 1: | |
| | 2: | |
| | 3: | |
| | 4: | |
| | 5: | |
| | 6: | |
| | 7: | |

7.5.2.15 OFFSET_ENABLE (EEPROM Address = 0x40000069)
Figure 38. OFFSET_ENABLE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|--------|
| | | | | | | | OFF_EN |
| | | | | | | | RW |
| | | | | | | | 0 |

Table 37. OFFSET_ENABLE Field Descriptions

| Register | Bit | Description |
|---------------|-----------|--|
| OFFSET_ENABLE | 0: OFF_EN | 1: Offset Sensor Digital Gain and Offset Compensation Used 0: Normal Sensor Digital Gain and Offset Compensation Used |
| | 1: | |
| | 2: | |
| | 3: | |
| | 4: | |
| | 5: | |
| | 6: | |
| | 7: | |

7.5.2.16 COMPENSATION_CONTROL (EEPROM Address = N/A) (DI Page Address: 0x0) (DI Page Offset: 0x0C)
Figure 39. COMPENSATION_CONTROL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------------------|--------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | COMPENSATION_RESET | IF_SEL |
| | | | | | | RW | RW |
| | | | | | | 0 | 0 |

Table 38. COMPENSATION_CONTROL Field Descriptions

| Register | Bit | Description |
|----------------------|-----------------------|---|
| COMPENSATION_CONTROL | 0: IF_SEL | 1: Digital Interface accesses the PAG305 resources 0: Calculation Engine accesses the PAG305 resources |
| | 1: COMPENSATION_RESET | 1: Compensation Engine is in Reset 0: Compensation Engine is Running |
| | 2–7: UNUSED | |

7.5.2.17 EEPROM_PAGE_ADDRESS (EEPROM Address = N/A) (DI Page Address: 0x5) (DI Page Offset: 0x88)
Figure 40. EEPROM_PAGE_ADDRESS Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|---------|---------|---------|---------|
| UNUSED | UNUSED | UNUSED | UNUSED | ADDR[3] | ADDR[2] | ADDR[1] | ADDR[0] |
| | | | | RW | RW | RW | RW |
| | | | | 0 | 0 | 0 | 0 |

Table 39. EEPROM_PAGE_ADDRESS Field Descriptions

| Register | Bit | Description |
|---------------------|----------------|--|
| EEPROM_PAGE_ADDRESS | 0–3: ADDR[0-3] | EEPROM page address used in the EEPROM Programming Procedure |
| | 4–7: UNUSED | |

7.5.2.18 EEPROM_CTRL (EEPROM Address = N/A) (DI Page Address: 0x5) (DI Page Offset: 0x89)
Figure 41. EEPROM_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|-----------------------|-------------------|-------|---------|
| UNUSED | UNUSED | UNUSED | UNUSED | FIXED_ERASE_PROG_TIME | ERASE_AND_PROGRAM | ERASE | PROGRAM |

| | | | | | | | |
|---|---|---|---|----|----|----|----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | RW | RW | RW | RW |
| | | | | 0 | 0 | 0 | 0 |

Table 40. EEPROM_CTRL Field Descriptions

| Register | Bit | Description |
|-------------|--------------------------|---|
| EEPROM_CTRL | 0: PROGRAM | 1: Program contents of EEPROM cache into EEPROM memory pointed to by EEPROM_PAGE_ADDRESS 0: No action |
| | 1: ERASE | 1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS 0: No action |
| | 2: ERASE_AND_PROGRAM | 1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS and program of contents of EEPROM cache 0: No action |
| | 3: FIXED_ERASE_PROG_TIME | 1: Use Fixed 8ms as the Erase/Program time 0: Use Variable time <8ms as the Erase/Program time. The EEPROM programming logic will determine the duration to program the EEPROM memory. |
| | 4–7: UNUSED | |

7.5.2.19 EEPROM_CRC (EEPROM Address = N/A) (DI Page Address: 0x5) (DI Page Offset: 0x8A)

Figure 42. EEPROM_CRC Register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | CALCULATE_CRC |
| | | | | | | | RW |
| | | | | | | | 0 |

Table 41. EEPROM_CRC Field Descriptions

| Register | Bit | Description |
|------------|------------------|---|
| EEPROM_CRC | 0: CALCULATE_CRC | 1: Calculate EEPROM CRC 0: No action |
| | 1–7: UNUSED | |

7.5.2.20 EEPROM_STATUS (EEPROM Address = N/A) (DI Page Address: 0x5) (DI Page Offset: 0x8B)

Figure 43. EEPROM_STATUS Register

| | | | | | | | |
|--------|--------|--------|--------|--------|---------------------|-------------------|------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | PROGRAM_IN_PROGRESS | ERASE_IN_PROGRESS | READ_IN_PROGRESS |
| | | | | | R | R | R |
| | | | | | 0 | 0 | 0 |

Table 42. EEPROM_STATUS Field Descriptions

| Register | Bit | Description |
|---------------|------------------------|--|
| EEPROM_STATUS | 0: READ_IN_PROGRESS | 1: EEPROM Read in progress 0: EEPROM Read not in progress |
| | 1: ERASE_IN_PROGRESS | 1: EEPROM Erase in progress 0: EEPROM Erase not in progress |
| | 2: PROGRAM_IN_PROGRESS | 1: EEPROM Program in progress 0: EEPROM Program not in progress |
| | 3–7: UNUSED | |

7.5.2.21 EEPROM_CRC_STATUS (EEPROM Address = N/A) (DI Page Address: 0x5) (DI Page Offset: 0x8C)
Figure 44. EEPROM_CRC_STATUS Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|----------|-------------------|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | CRC_GOOD | CRC_CHECK_IN_PROG |
| | | | | | | R | R |
| | | | | | | 0 | 0 |

Table 43. EEPROM_CRC_STATUS Field Descriptions

| Register | Bit | Description |
|-------------------|--------------------------|---|
| EEPROM_CRC_STATUS | 0: CRC_CHECK_IN_PROGRESS | 1: EEPROM CRC check in progress 0: EEPROM CRC check not in progress |
| | 1: CRC_GOOD | 1: EEPROM Programmed CRC matches calculated CRC 0: EEPROM Programmed CRC does not match calculated CRC |
| | 2–7: UNUSED | |

7.5.2.22 EEPROM_CRC_VALUE (EEPROM Address = 0x4000007F) (DI Page Address: 0x5) (DI Page Offset: 0x8D)
Figure 45. EEPROM_CRC_VALUE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| R | R | R | R | R | R | R | R |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 44. EEPROM_CRC_VALUE Field Descriptions

| Register | Bit | Description |
|------------------|-----|--|
| EEPROM_CRC_VALUE | 0–7 | CRC value as calculated by the digital logic |

EEPROM CRC value should be located in the last byte of the EEPROM

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA305 can be used in a variety of applications to measure pressure and temperature. Depending on the application, the device can be configured in different modes.

8.2 Typical Applications

Figure 46 depicts the PGA305 in a typical application, including device power, connections for the analog inputs from a resistive bridge sensor and temperature sensor, as well as I2C communication lines, and finally the output stage in a voltage output configuration.

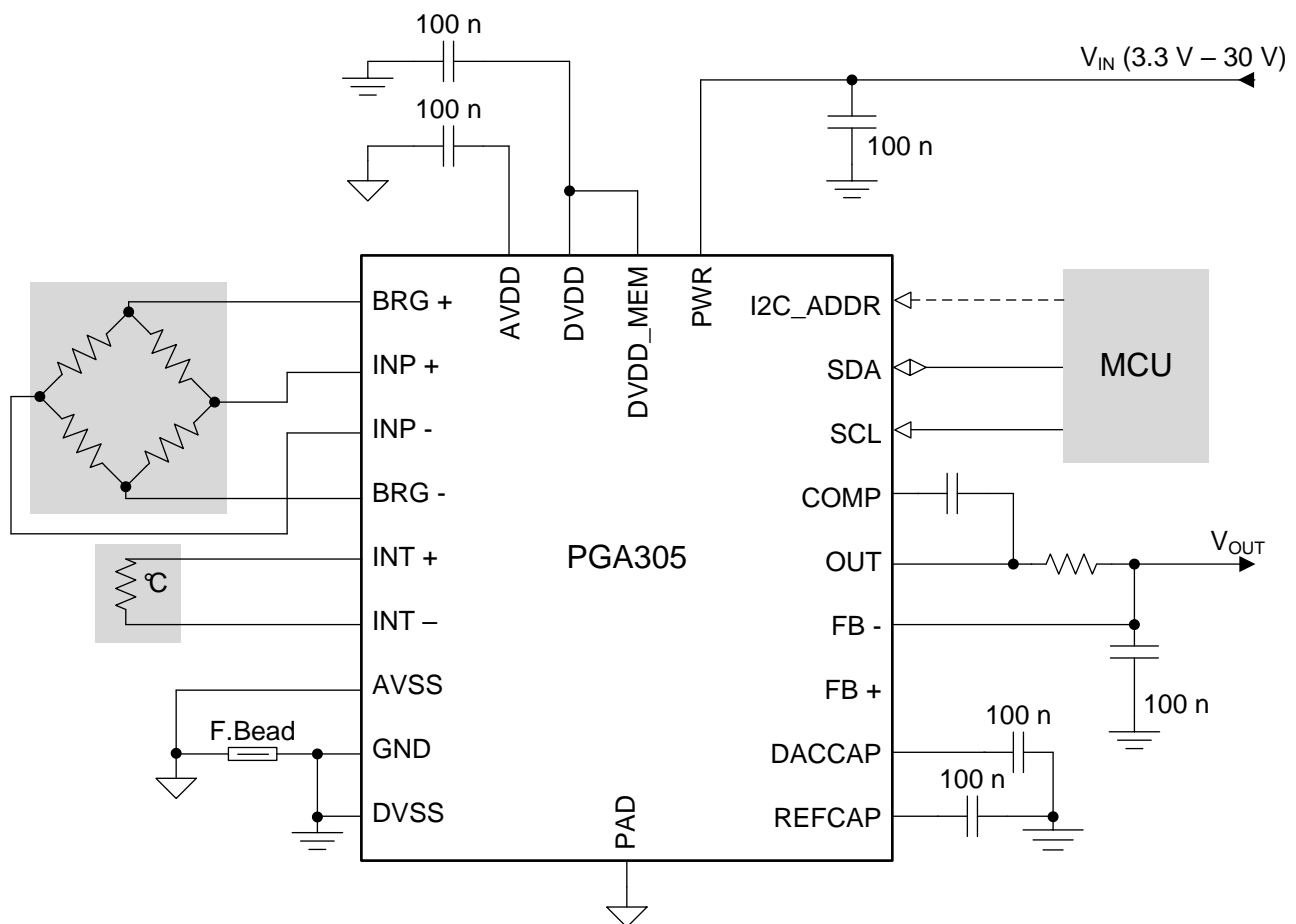


Figure 46. Typical Application Diagram

Typical Applications (continued)

8.2.1 4-mA to 20-mA Output With Internal Sense Resistor

Figure 47 provides an example of how to wire a PGA305 device for 4 to 20mA current output mode. The internal structure of the output stage is shown, including the states of the internal switches when the device is configured for 4 to 20mA current output mode.

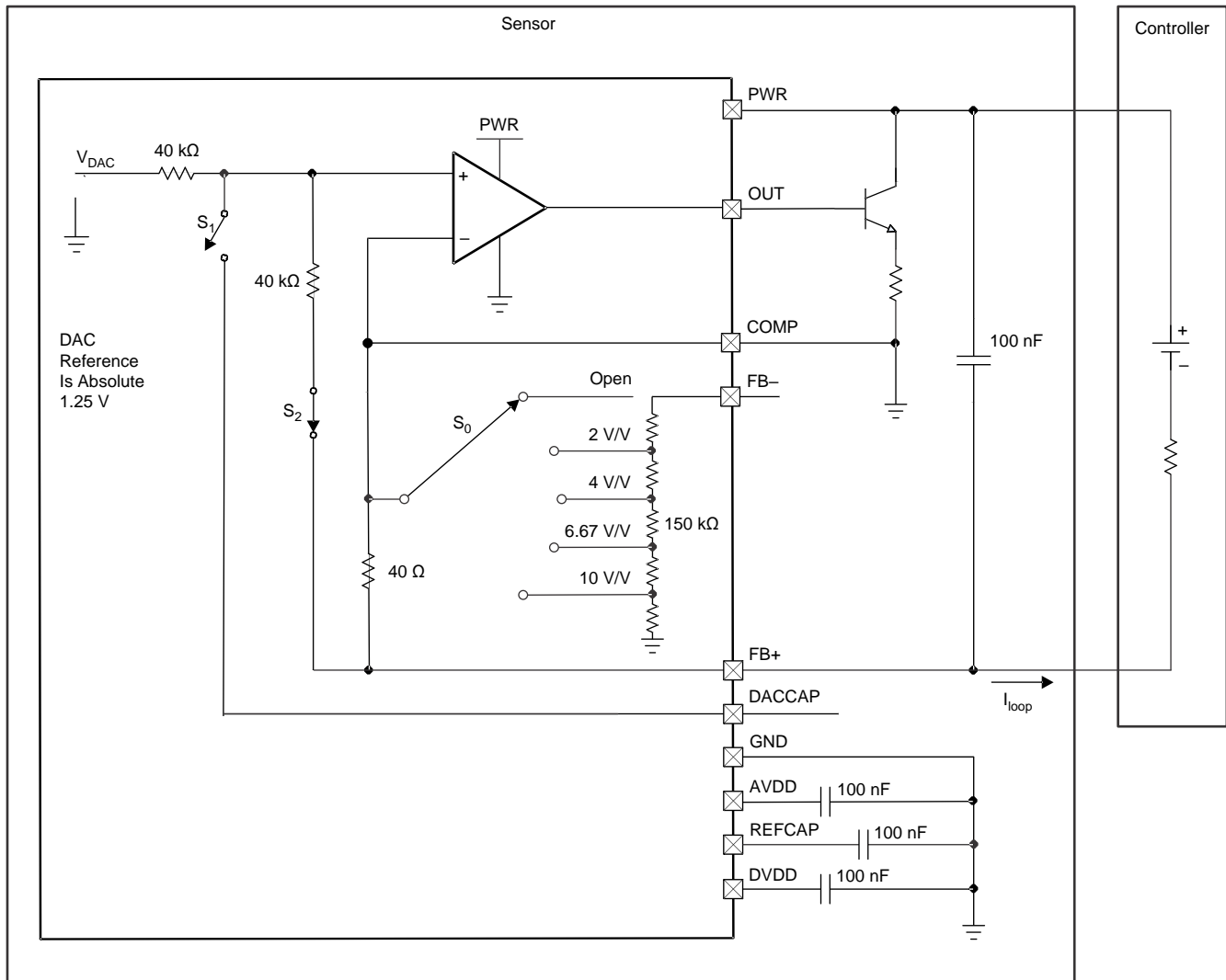


Figure 47. 4-mA to 20-mA Output With Internal Sense Resistor Diagram

8.2.1.1 Design Requirements

There are only a few requirements to take into account when using the PGA305 device in a design:

- Do not exceed the maximum slew rate of 0.5 V/ μ s at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close to the AVDD pin as possible.
- Place a 100-nF capacitor from the DVDD pin to ground, as close to the DVDD pin as possible.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground as close to the REFCAP pin as possible.
- Place a 150- Ω resistor between the COMP pin and the emitter of the BJT for current-loop stability purposes.
- Place a 10- Ω resistor between the FB+ pin and the negative terminal of the controller for current measurement.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Calibration Tips

8.2.1.2.1.1 Programming the EEPROM for 4-mA to 20-mA Output

The EEPROM in the PGA305 is configured by default to operate in current mode using the OP_STG_CTRL register. If not, the user must follow this sequence to change it to current mode:

1. Send an OWI activation pulse to stop the digital compensation from running.
2. Set OP_STAGE_CTRL to 0x80 for current mode and DAC_CONFIG EEPROM to 0x00 or 0x01 for No_Gain.
3. Let the digital compensation run again to read the new EEPROM values.

8.2.1.3 Application Curve



Voltage measured between the GND pin in the PGA305 device and the negative terminal of the controller. This includes the internal 40- Ω resistor and an external 10- Ω resistor, $V_{PWR} = 15$ V. The DAC codes used were 0x880 and 0x2760 for 4 mA and 20 mA, respectively.

Figure 48. Loop Current Step From 4 mA to 20 mA

Typical Applications (continued)

8.2.2 0- to 10-V Absolute Output With Internal Drive

Figure 49 provides an example of how to wire a PGA305 device for 0 to 10V absolute output voltage mode. The internal structure of the output stage is shown, including the states of the internal switches when the device is configured for absolute voltage output. Note that the position of S0 is dependent on the configuration of the voltage output gain selected in the OP_STAGE_CTRL register.

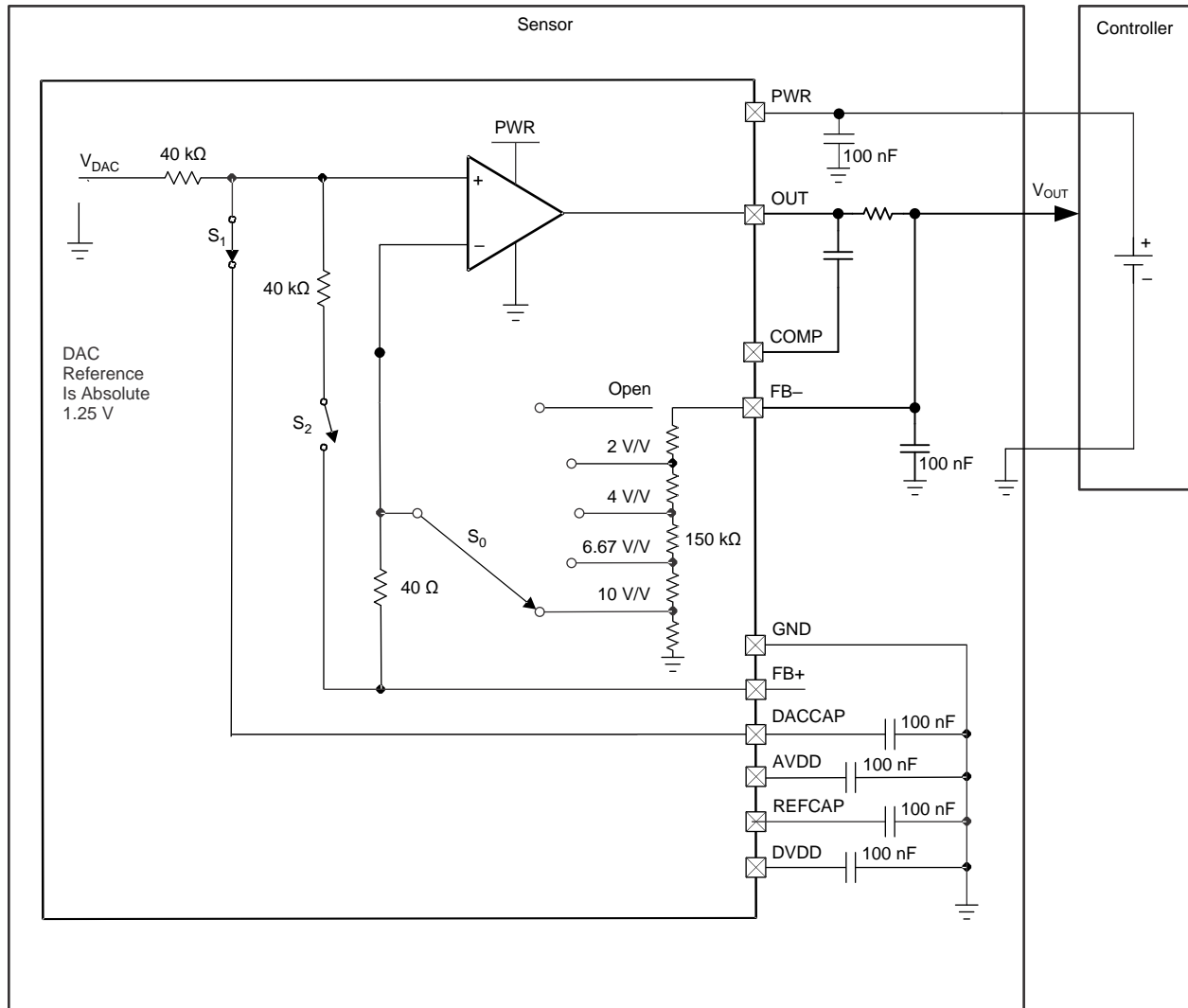


Figure 49. 0- to 10-V Absolute Output With Internal Drive Diagram

8.2.2.1 Design Requirements

There are only a few requirements to take into account when using the PGA305 in a design:

- Do not exceed the maximum slew rate of 0.5 V/ μ s at the VDD pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close to the AVDD pin as possible.
- Place a 100-nF capacitor from the DVDD pin to ground, as close to the DVDD pin as possible.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close to the REFCAP pin as possible.
- Use the COMP pin and an isolation resistor to implement compensation when driving large capacitive loads with the OUT pin.

Typical Applications (continued)

8.2.3 0- to 5-V Ratiometric Output With Internal Drive

Figure 50 provides an example of how to wire a PGA305 device for 0 to 5V ratiometric output voltage mode. The internal structure of the output stage is shown, including the states of the internal switches when the device is configured for ratiometric voltage output. Note that the position of S₀ is dependent on the configuration of the voltage output gain selected in the OP_STAGE_CTRL register.

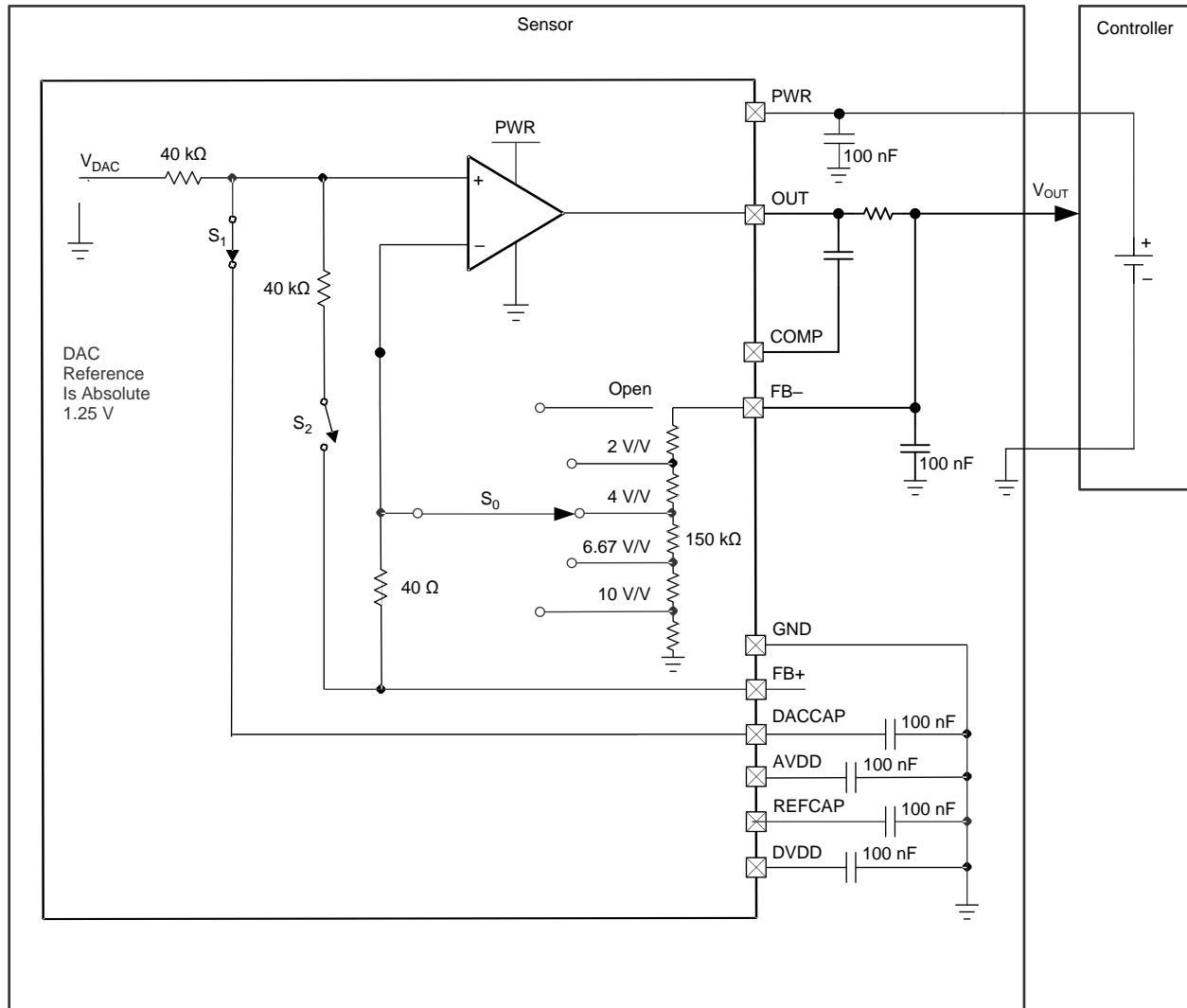


Figure 50. 0- to 5-V Ratiometric Output With Internal Drive Diagram

8.2.3.1 Design Requirements

There are only a few requirements to take into account when using the PGA305 in a design:

- Do not exceed the maximum slew rate of 0.5 V/μs at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close to the AVDD pin as possible.
- Place a 100-nF capacitor from the DVDD pin to ground, as close to the DVDD pin as possible.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close to the REFCAP pin as possible.
- Use the COMP pin and an isolation resistor to implement compensation when driving large capacitive loads with the OUT pin.

Typical Applications (continued)

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Programmer Tips

8.2.3.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The user must configure these bits to reset the M0 microprocessor and enable digital interface:

1. Set the IF_SEL bit in the MICRO_INTERFACE_CONTROL register to 1.
2. Set the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register to 1.

8.2.3.2.1.2 Turning On the Accurate Reference Buffer (REFCAP Voltage)

The following bits must be configured to turn ON the accurate reference buffer:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on the REFCAP pin is connected to the reference buffer.

8.2.3.2.1.3 Turning On DAC and DAC GAIN

The user must configure these bits to turn on DAC and DAC GAIN:

- Set the SD bit in ALPWR register to 0.
- Set the ADC_EN_VREF bit in the ALPWR register to 1.
- Set the DAC_ENABLE bit in the DAC_CTRL_STATUS register to 1.
- Set the 4_20_MA_EN bit in the OP_STAGE_CTRL register for the voltage-output or current-output mode.
- Set the DACCAP_EN bit in the OP_STAGE_CTRL register to connect or disconnect the external capacitor at the DAC output.
- Set the DAC_RATIOMETRIC bit in the DAC_CONFIG register for ratiometric or absolute-voltage output mode.
- Set the TEST_MUX_DAC_EN bit in the AMUX_CTRL register to 1.

9 Power Supply Recommendations

The PGA305 device has a single pin, PWR, for the input power supply. The maximum slew rate for the PWR pin is 0.5 V/ μ s as specified in the [Recommended Operating Conditions](#). Faster slew rates might generate a POR. A decoupling capacitor for PWR should be placed as close to the pin as possible.

10 Layout

10.1 Layout Guidelines

Standard good layout practices must be used when designing a board to test the PGA305 device. Depending on the number of layers in the board, one or more GND planes should be inserted as internal layers. However, given the limited number of external components required for an application using the PGA305 device and the number of NC pins in the device, so it is possible to design a simple two-layer board. In addition, the PWR decoupling capacitor must be placed as close to the pin as possible. In a similar way, the 100-nF recommended capacitors for the AVDD and DVDD regulators as well as the 10-nF to 1000-nF recommended capacitor for REFCAP must be placed as close to their respective pins as possible.

Depending on the application, the signal traces for FB–, FB+, COMP, and OUT must be routed so that they do not cross one another to minimize coupling.

10.2 Layout Example

[Figure 51](#) shows how the main guidelines listed in these layout guidelines can be implemented in a six-layer, socketed EVM of the PGA305 device. Two main GND planes (layer 2 and 5) were used to provide a nearby GND plane to each of the signal layers and the power plane (layer 3) in the EVM. This EVM supports voltage and current modes for the device, so depending on the application, GND separation may be necessary as a result. For this example, layer 2 is a solid GND plane for the majority of the circuitry in the EVM (IRETURN). Most of the circuitry is referred to this GND plane, so layers 3 and 4 also contain copper pours connected to IRETURN. This GND plane is the return path for the supply used in the 4-mA to 20-mA loop. Layer 5 is a split plane for the ground references for the digital communication signals used for this EVM (USBGND) and the ground pins in the device (GND, AVSS and DVSS), referred to as ASICGND. The EVM provides jumpers to connect, or disconnect, these three planes one from another, depending on the desired configuration.

[Figure 51](#) shows the recommended capacitors for the proper operation of the PGA305 device. These capacitors are placed as close to their respective pins of the socket used for this particular EVM as possible. The signal traces for FB–, FB+, COMP, and OUT are also routed in the same layer to avoid crossing each other and to minimize coupling.

Layout Example (continued)

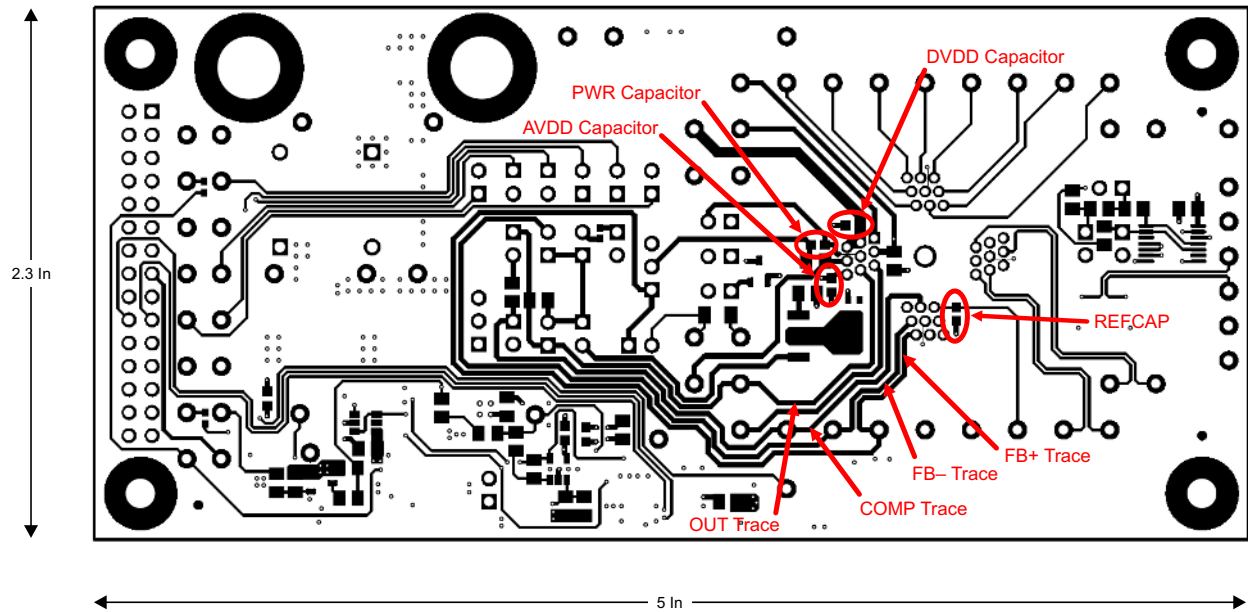


Figure 51. Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary



[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| PGA305ARHHR | ACTIVE | VQFN | RHH | 36 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | PGA305A RHH |  |
| PGA305ARHHT | ACTIVE | VQFN | RHH | 36 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | PGA305A RHH |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

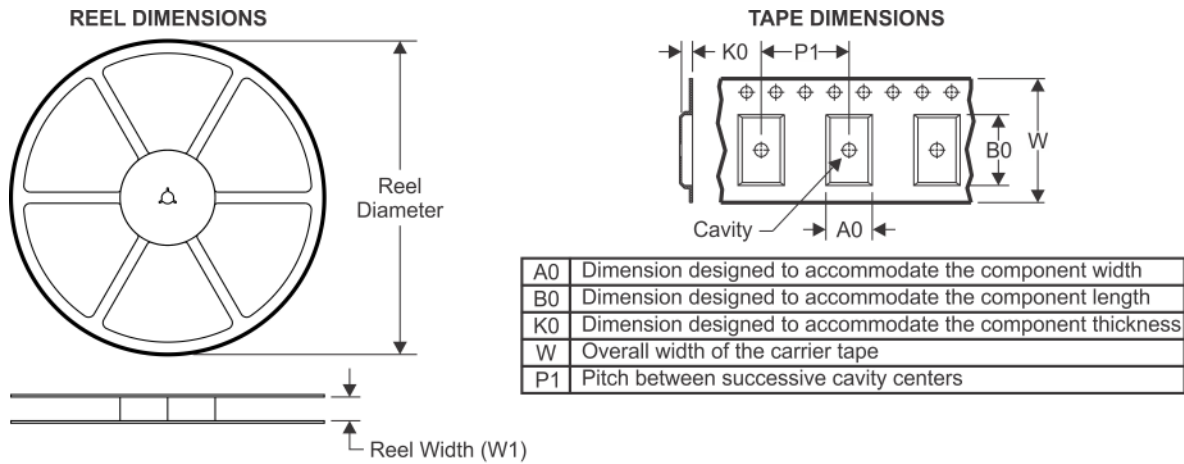
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

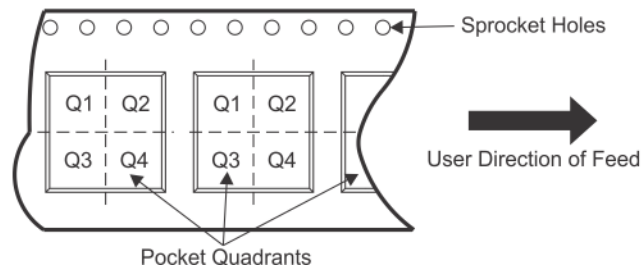
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PGA305ARHHR | VQFN | RHH | 36 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| PGA305ARHHT | VQFN | RHH | 36 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PGA305ARHHR | VQFN | RHH | 36 | 2500 | 367.0 | 367.0 | 38.0 |
| PGA305ARHHT | VQFN | RHH | 36 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

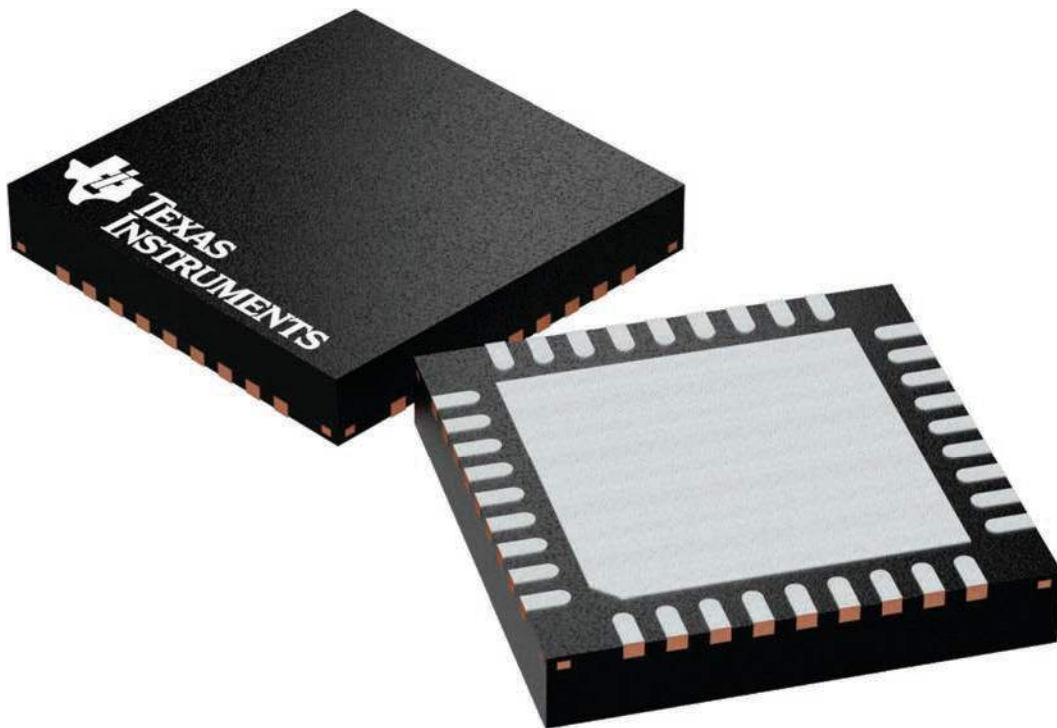
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

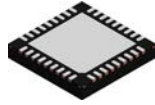
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225440/A

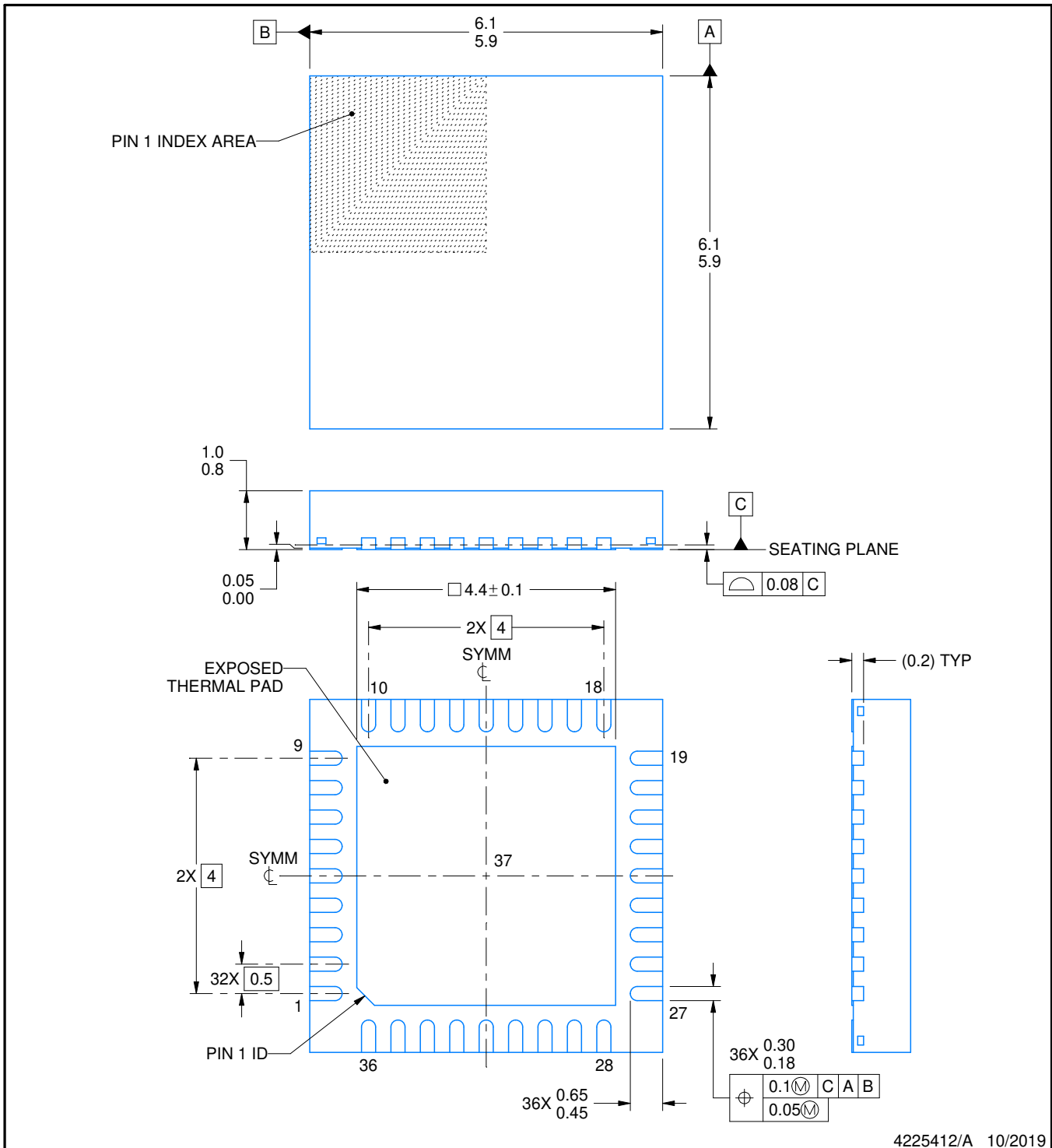
RHH0036C



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

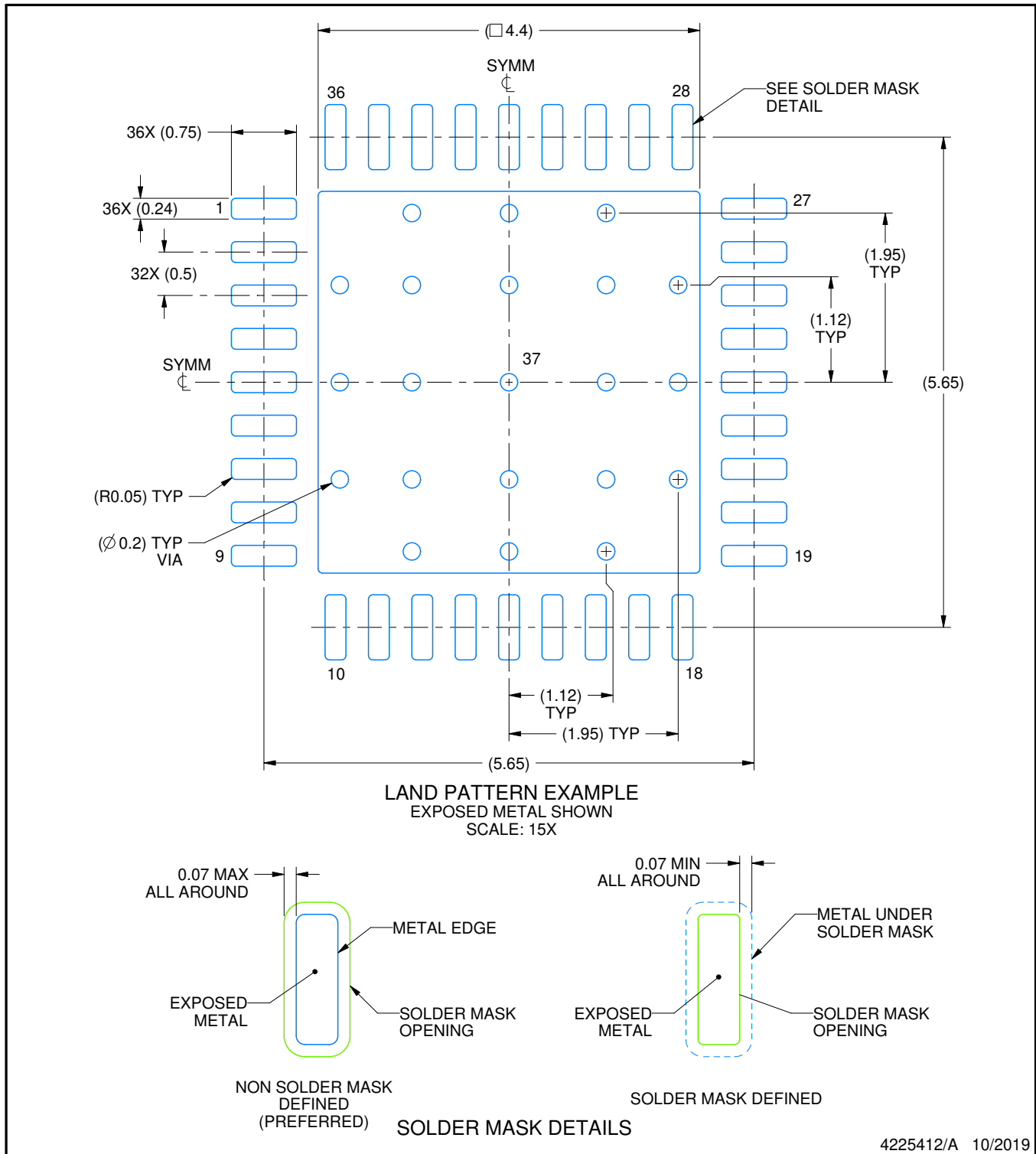
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHH0036C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

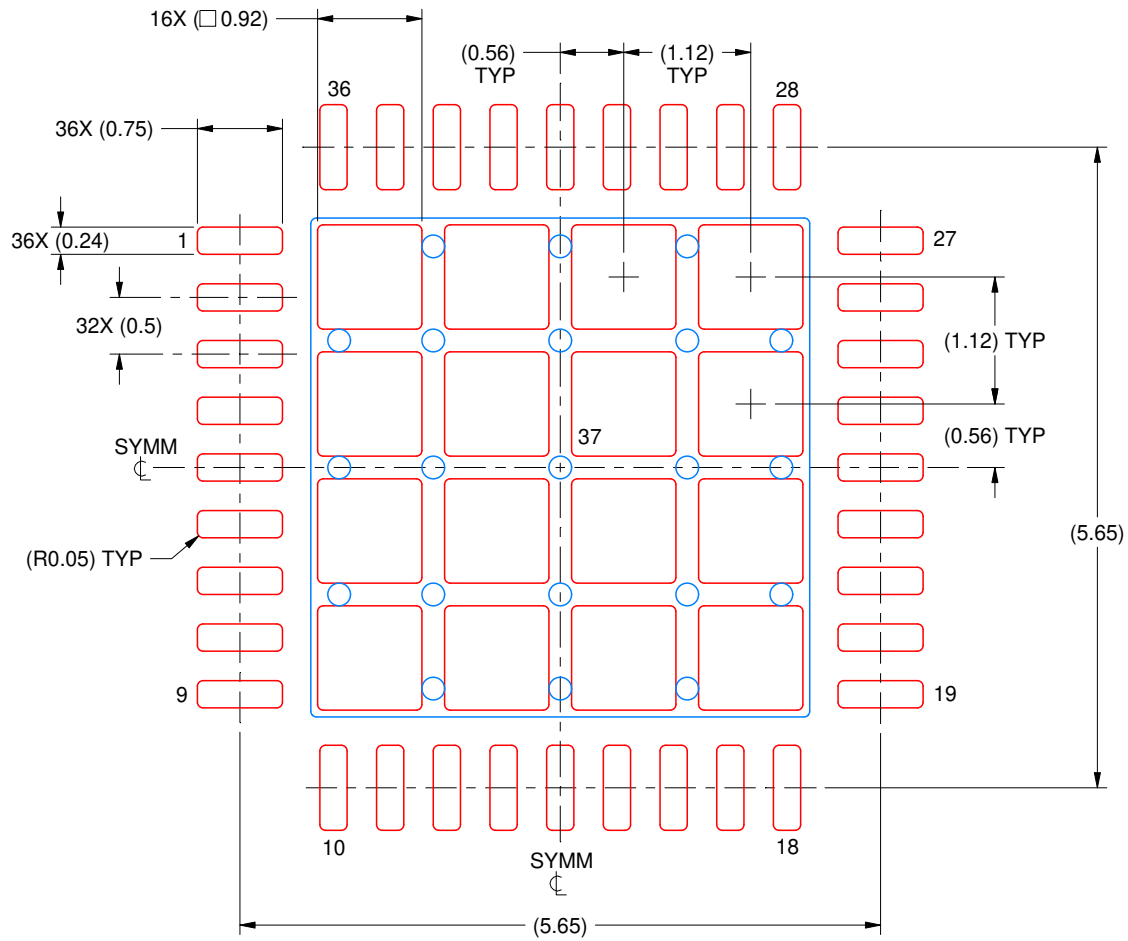
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHH0036C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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