MIC2790/1/3

Supervisor with High-Accuracy, Ultra-Fast Propagation Delay, and Capacitor-Programmable Reset Delay

General Description

The MIC2790/1/3 is ideal for monitoring highly-accurate core voltages that require rapid response in the event of a fault condition. The voltage supervisor IC features a manual reset input, enable input (MIC2793 only), a capacitor-programmable reset timeout delay and both an active-low and active-high reset output.

The MIC2790/1/3 monitors system voltages that are in the range of 0.4V to 5.5V, with a typical sense accuracy of 0.5% at +25°C and ±1.0% across –40°C to +125°C. The IC asserts a reset output when the sense voltage drops below the threshold or when the manual reset is pulled to a logic low. The active-low reset stays low for the duration of the reset timeout delay once the sense voltage returns to normal and the manual reset transitions to a logic high state. The reset timeout delay period is programmable from 1ms to 10s with an external capacitor.

The MIC2790/1/3 operates from a low supply voltage of 1.5V to 5.5V, and is rated to operate over the temperature range of –40˚C to +125˚C. The MIC2790 is available in a 6-pin TSOT-23 package or a 6-pin 2mm × 2mm × 0.55mm DFN package. The MIC2791 is available in a tiny 6-pin 1.6mm × 1.6mm × 0.55mm DFN package. The MIC2793 is available in a 8-pin 2mm × 2mm × 0.55mm DFN package.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

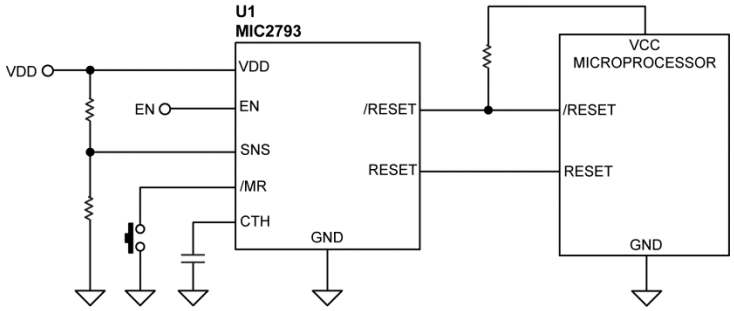
Features

- 1.5V to 5.5V operating supply voltage range
- Ultra-fast propagation delay (1µs typically)
- 0.4V reference voltage (SNS pin)
  - ±1.0% threshold accuracy from –40°C to +125°C
  - Monitored voltage range from 0.4V to 5.5V
- Programmable reset timeout delay (from 1ms to 10s)
- Manual reset input with an internal pull-up resistor
- Active-high enable input pin (MIC2793 only)
- The MIC2790/1/3 features multiple output options:
  - Open-drain active-low (/RESET)
  - Push-pull active-low (/RESET)
  - Push-pull active-high (RESET)
- –40°C to 125°C junction temperature range
- 6-pin TSOT-23 (MIC2790)
- 6-pin 2mm × 2mm Thin DFN (MIC2790)
- 6-pin 1.6mm × 1.6mm Thin DFN (MIC2791)
- 8-pin 2mm × 2mm Thin DFN (MIC2793)

Applications

- Telecom
- Computer/servers
- Medical equipment
- Portable
- Set-top boxes
- Critical microprocessor monitoring

Typical Application



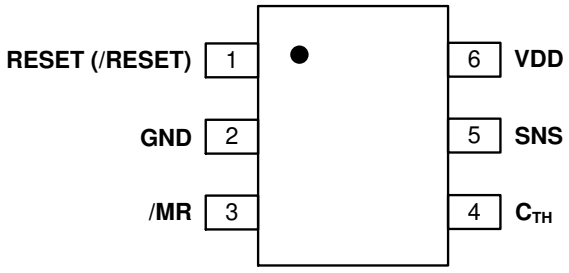
Ordering Information

Part Number	Marking Code	Threshold Voltage (SNS)[1]	/RESET Output (Active-Low)	RESET Output (Active-High)	Enable Pin Feature	Junction Temperature Range	Package[2, 3]
MIC2790N-04VD6	9NB	0.4V	Open-Drain	–	–	–40°C to +125°C	6-pin TSOT-23
MIC2790L-04VD6	9LB	0.4V	Push-Pull	–	–	–40°C to +125°C	6-pin TSOT-23
MIC2790H-04VD6	9LC	0.4V	–	Push-Pull	–	–40°C to +125°C	6-pin TSOT-23
MIC2790N-04VMT	9NA	0.4V	Open-Drain	–	–	–40°C to +125°C	6-pin 2mm × 2mm TDFN
MIC2791N-04VMT	1N	0.4V	Open-Drain	–	–	–40°C to +125°C	6-pin 1.6mm ×1.6mm TDFN
MIC2791L-04VMT	1L	0.4V	Push-Pull	–	–	–40°C to +125°C	6-pin 1.6mm × 1.6mm TDFN
MIC2791H-04VMT	XH	0.4V	–	Push-Pull	–	–40°C to +125°C	6-pin 1.6mm ×1.6mm TDFN
MIC2793LH-04VMT	3LH	0.4V	Push-Pull	Push-Pull	Yes	–40°C to +125°C	8-pin 2mm × 2mm TDFN
MIC2793NH-04VMT	3NH	0.4V	Open-Drain	Push-Pull	Yes	–40°C to +125°C	8-pin 2mm × 2mm TDFN

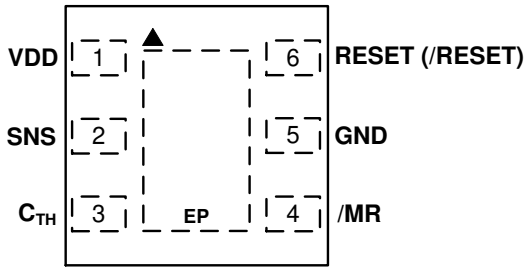
Notes:

1. Other voltage options are available. Contact Micrel for details.
2. Thin DFN pin 1 identifier = "▲".
3. Thin DFN is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen free.

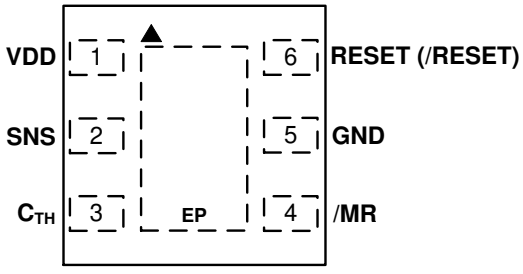
Pin Configuration



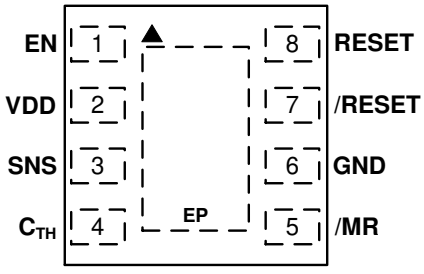
6-Pin TSOT (D6)
(Top View)



6-Pin 1.6mm x 1.6mm TDFN (MT)
(Top View)



6-Pin 2mm x 2mm TDFN (MT)
(Top View)



8-Pin 2mm x 2mm TDFN (MT)
(Top View)

Pin Description

Pin Number TSOT-23 (6L)	Pin Number 1.6 × 1.6 (6L)	Pin Number 2 × 2 (6L)	Pin Number 2 × 2 (8L)	Pin Name	Pin Function
1	6	6	7	/RESET	/RESET is an active-low output pin and is available in an open-drain or push-pull configuration. In the open-drain configuration, a pull-up resistor to VDD is required and /RESET pin is asserted low when /MR is set to a logic low or the SNS voltage decreases below the threshold voltage. /RESET will remain low for the reset timeout delay after SNS > (V_{TH} + V_{HYST}) and /MR is set to a logic high. The push-pull configuration does not require a pull-up resistor and behaves exactly the same as the open-drain configuration.
1	6	6	8	RESET	Reset is an active-high push-pull output and is asserted high when /MR is set to a logic low or the SNS voltage decreases below the threshold voltage. RESET will remain high for the reset timeout delay after SNS > (V_{TH} + V_{HYST}) and /MR is set to a logic high.
2	5	5	6	GND	Supply Ground.
3	4	4	5	/MR	Manual reset is an active-low input logic level pin and is internally pulled to VDD through a 90kΩ pull-up resistor. Pulling the /MR input to a logic low asserts RESET and /RESET pins. /RESET will remain low and RESET will remain high for the reset timeout delay after /MR is pulled to logic high.
4	3	3	4	CTH	Programmable timeout delay. Connect a capacitor to ground to set a user defined reset delay time.
5	2	2	3	SNS	Voltage monitor input. Connect sense pin to the voltage to be monitored through a resistor divider. When this voltage decreases below the threshold voltage, VTH, /RESET is asserted low and RESET is asserted high.
6	1	1	2	VDD	Supply voltage pin. Bypass with a 1µF capacitor from this pin to GND.
–	–	–	1	EN	Enable input function is only available in the MIC2793 version. This pin enables the /MR input function and RESET and /RESET outputs. When EN is in a logic low state, the reset outputs are de-asserted. The EN pin has an internal 90kΩ pull-up resistor to VDD.
–	EP	EP	EP	ePad	Exposed Pad. Connect to ground plane.

Absolute Maximum Ratings[4]

Supply Voltage (V_{DD}) ..... –0.3V to +6.0V
SNS ..... –0.3V to 4.5V
/MR, EN, C_{TH} ..... –0.3V to V_{DD}
RESET, /RESET ..... –0.3V to V_{DD}
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature (T_S) ..... –55°C to +150°C
ESD Ratings[6] ..... ESD Sensitive

Operating Ratings[5]

Supply Voltage (V_{DD}) ..... +1.5V to +5.5V
SNS ..... 0V to 4.0V
/MR, EN, C_{TH} ..... 0V to V_{DD}
RESET, /RESET ..... 0V to V_{DD}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
6-pin, TSOT-23 (θ_{JA}) ..... 177.2°C/W
6-pin, 1.6mm × 1.6mm TDFN (θ_{JA}) ..... 92.4°C/W
6-pin, 2mm × 2mm TDFN (θ_{JA}) ..... 90°C/W
8-pin, 2mm × 2mm TDFN (θ_{JA}) ..... 90°C/W

Electrical Characteristics[7]

V_{DD} = 3.3V; $R_{/RESET}$ = 100kΩ; C_{TH} = 1nF; T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +125°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Specifications						
V_{DD}	Supply Voltage	/RESET Output Valid	**1.5**		**5.5**	V
I_{DD}	Supply Current	V_{DD} = EN = /MR = 3.3V RESET and /RESET not asserted		40	**70**	µA
		V_{DD} = EN = /MR = 5V RESET and /RESET not asserted		50	**80**	
Sense Specifications						
V_{TH}	Sense Threshold Voltage			0.4		V
	Sense Threshold Accuracy		**–1.0**		**+1.0**	%
V_{HYST}	Hysteresis	Sense rising	**–2.5**	± 1.5	**+2.5**	%
I_{SNS}	Sense Input Bias Current		**–15**		**+15**	nA
RESET & /RESET Output Specifications						
$t_{p,SNS}$	SNS to RESET and /RESET Propagation Delay[8]	SNS = V_{TH} × 1.05 to V_{TH} × 0.95		1	**2.2**	µs
V_{OL}	/RESET Logic Low Output Voltage	I_{OL} = 1mA (open-drain only)			**0.3**	V
V_{OH}	RESET Logic High Output Voltage	I_{OH} ≤ 1mA (push-pull only)	**>0.9 × V_{DD}**			V
I_{OH}	/RESET Leakage Current	/RESET not asserted (open-drain only)			1	µA
t_d	RESET and /RESET Timeout Delay	C_{TH} = 100pF	**0.45**	1.05	**1.8**	ms
		C_{TH} = 180nF	**0.5**	1.2	**1.9**	s

Notes:

4. Exceeding the absolute maximum ratings may damage the device.
5. The device is not guaranteed to function outside its operating ratings.
6. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
7. Specification for packaged product only.
8. SNS to RESET and or /RESET propagation delay is the delay time for SNS voltage to transition from V_{TH} × 1.05 to V_{TH} × 0.95 to RESET and or /RESET.

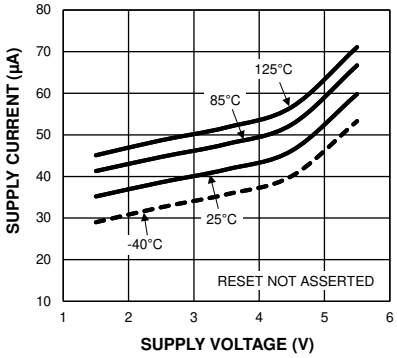
Electrical Characteristics[7] (Continued)

V_{DD} = 3.3V; $R_{/RESET}$ = 100kΩ; C_{TH} = 1nF; T_A = 25°C, **bold** values indicate −40°C ≤ T_A ≤ +125°C, unless noted.

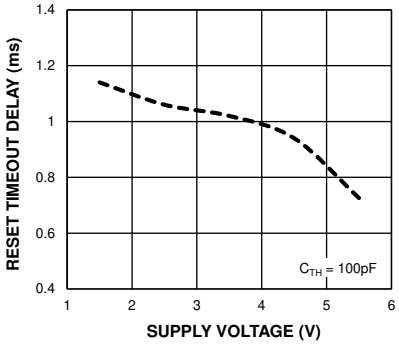
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
/MR Input Specifications						
$R_{/MR}$	/MR Internal Pull-Up Resistance			90		kΩ
$t_{p,/MR}$	/MR to RESET and /RESET Propagation Delay			100		ns
V_{IL}	/MR Logic Low Input Voltage				**0.5**	V
V_{IH}	/MR Logic High Input Voltage		**1.2**			V
EN Input Specifications (MIC2793 only)						
R_{EN}	EN Internal Pull-Up Resistance			90		kΩ
$t_{p,EN}$	EN to RESET and /RESET Propagation Delay	/MR = logic low		100		ns
V_{ENL}	EN Logic Low Input Voltage				**0.5**	V
V_{ENH}	EN Logic High Input Voltage		**1.2**			V

Typical Characteristics

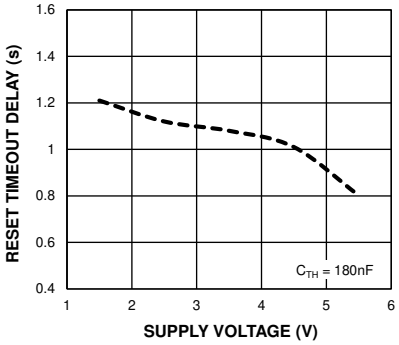
Supply Current vs. Supply Voltage



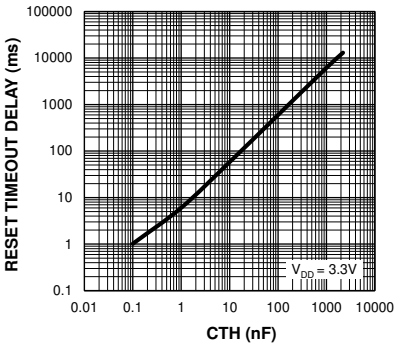
Reset Timeout Delay vs. Supply Voltage



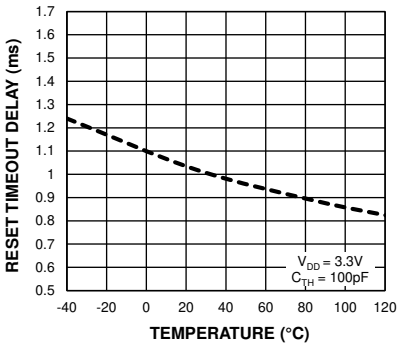
Reset Timeout Delay vs. Supply Voltage



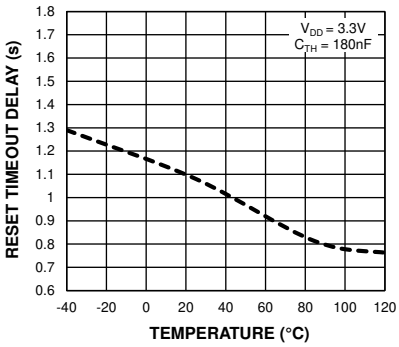
Reset Timeout Delay vs. C_{TH}



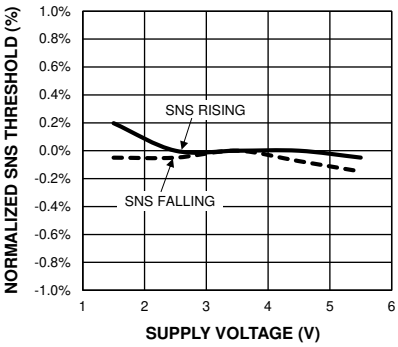
Reset Timeout Delay vs. Temperature



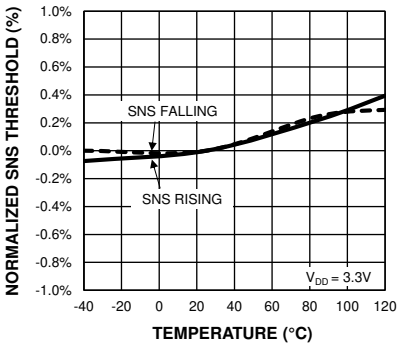
Reset Timeout Delay vs. Temperature



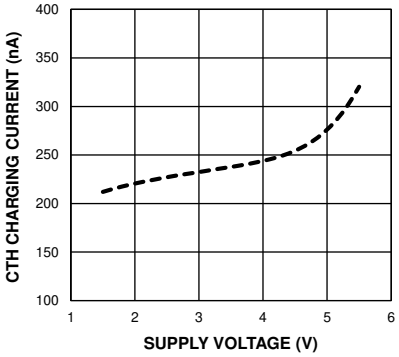
Normalized SNS Threshold vs. Supply Voltage



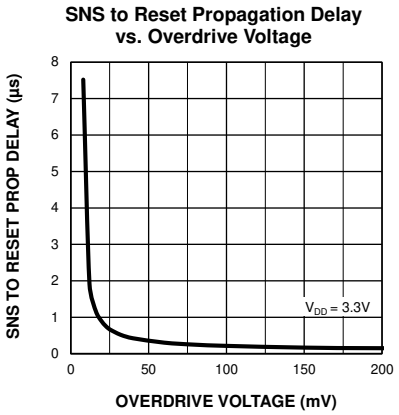
Normalized SNS Threshold vs. Temperature



C_{TH} Charging Current vs. Supply Voltage



Typical Characteristics (Continued)



Timing Diagrams

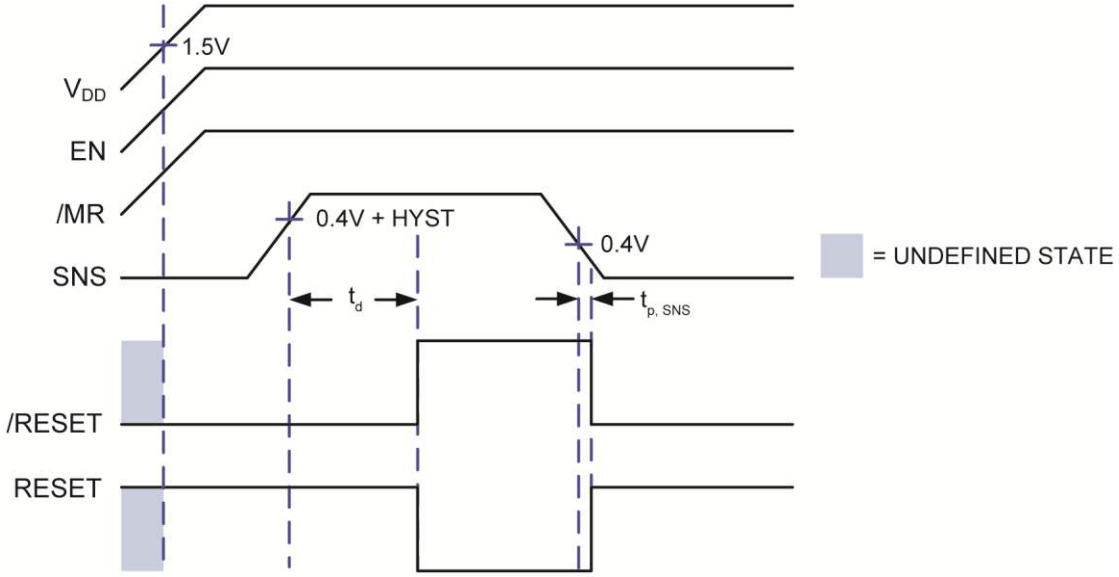


Figure 1. Timeout and Propagation Delay from Sense to RESET and /RESET

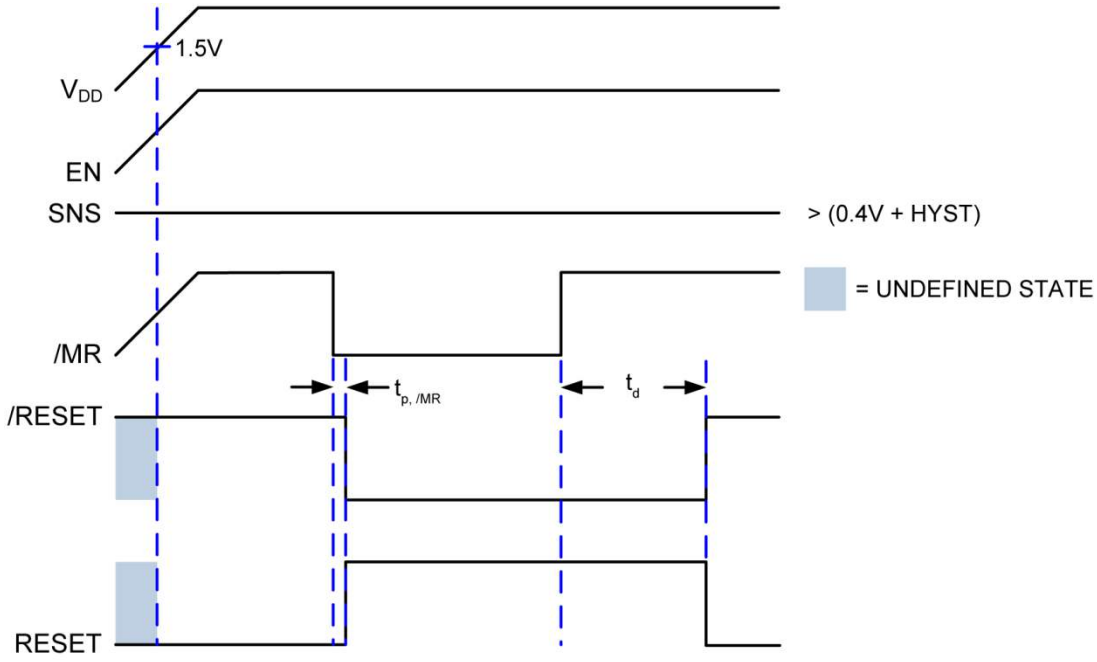


Figure 2. Timeout and Propagation Delay from /MR to RESET and /RESET

Timing Diagrams (Continued)

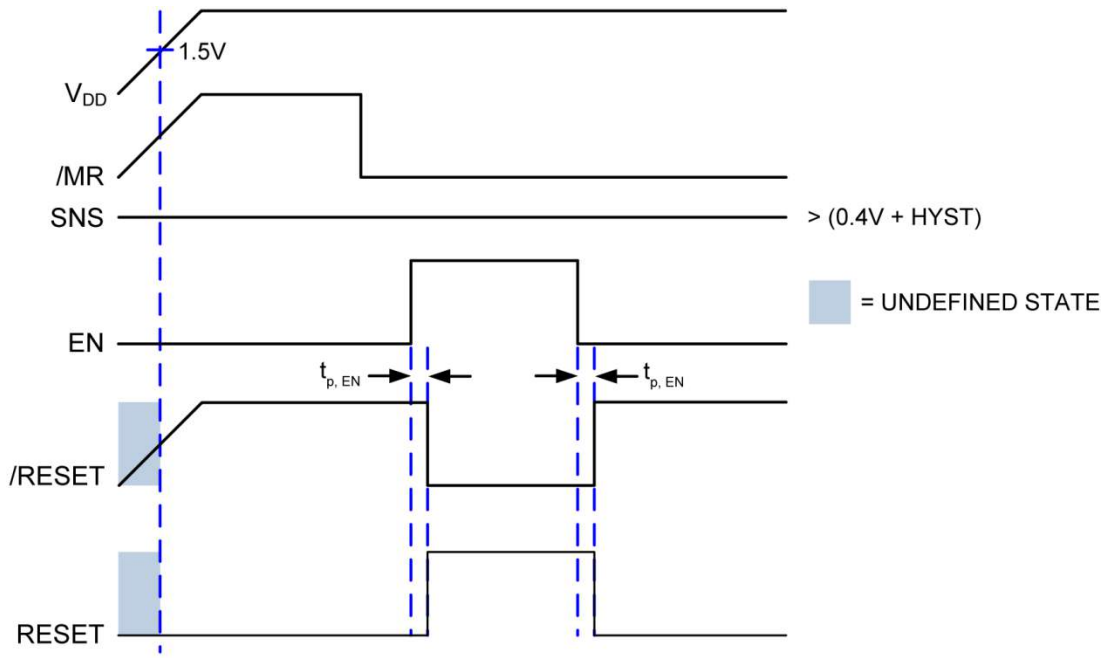


Figure 3. Hold and Propagation Delay from EN to RESET and /RESET

Functional Diagram

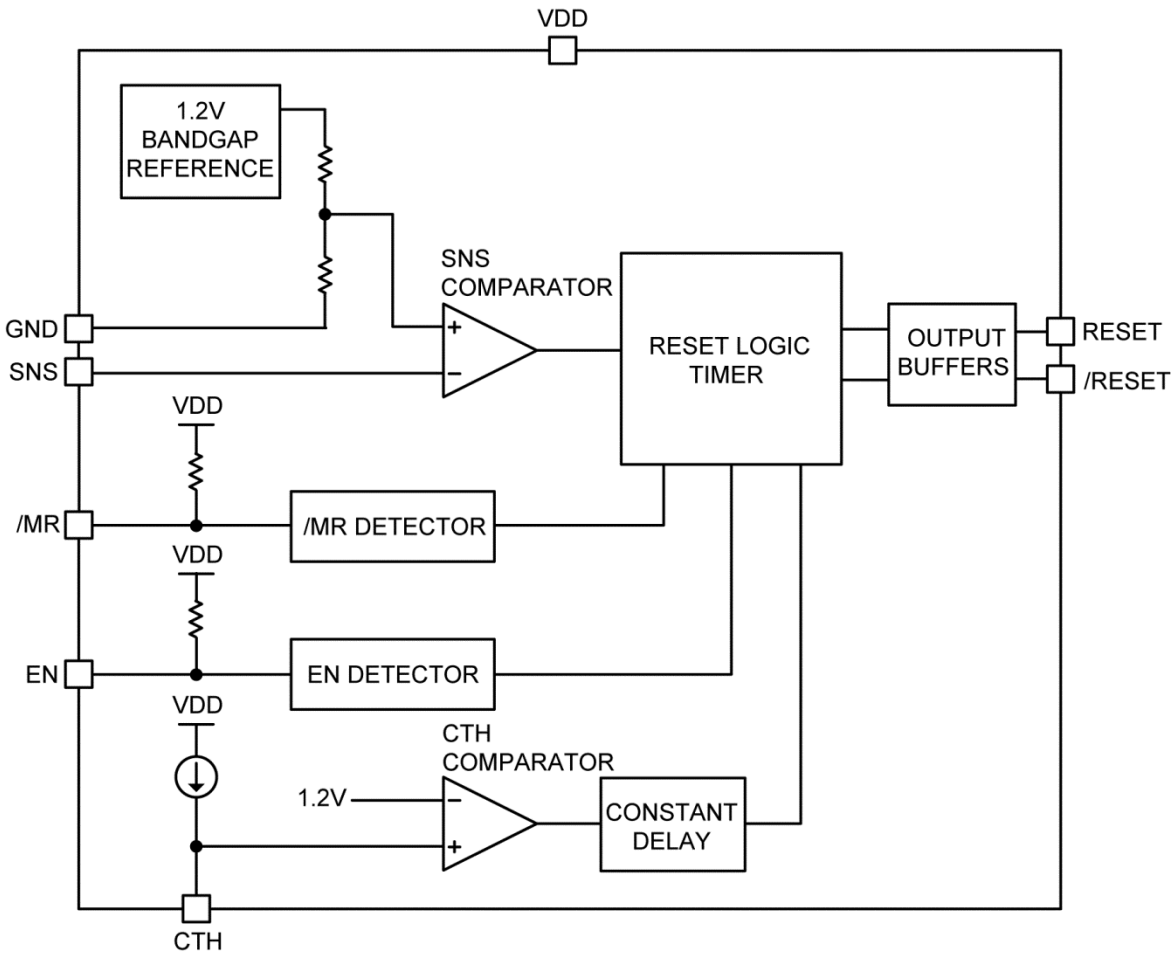


Figure 4. Simplified MIC2793 Functional Block Diagram

Functional Description

Design and Product Advantages

The MIC2790/1/3 is a highly-accurate supervisor circuit with an ultra-fast propagation delay of 2.2µs (maximum) over the temperature range of –40°C to +125°C. Additional features in the MIC2790/1/3 include a manual reset input pin, a capacitor-programmable reset timeout delay and both an active-low and active-high reset output. The capacitor-programmable reset delay help protect against accidental system glitch during a reset timeout.

VDD

The input supply (V_{DD}) provides power to the comparators and logic timers. V_{DD} operating range is 1.5V to 5.5V. A ceramic input capacitor of 1µF with a minimum voltage rating of 6.3V is recommended between VDD and GND. Refer to *PCB Layout Recommendations* for details.

EN

The enable (EN) pin feature is only available in the MIC2793 option and has an internal pull-up of 90kΩ resistor to VDD. A logic high signal on EN pin enables the reset logic outputs, while a logic low signal disables the reset outputs. See Figure 3 in the *Timing Diagrams* section for more information.

CTH

C_{TH} is a programmable timeout delay pin. Connect a capacitor to ground to set a reset timeout delay ranging from 1ms to 10s. Refer to the Reset Timeout Delay vs. C_{TH} plot in the *Typical Characteristics* section for examples.

SNS

The sense (SNS) input pin monitors the user's voltage through a resistor divider network as shown in Figure 5.

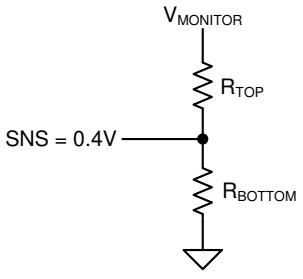


Figure 5. Resistor Divider on SNS pin

To set R_{TOP} and R_{BOTTOM}, use Equation 1 and set an arbitrary R_{TOP} value greater than 100kΩ and solve for R_{BOTTOM} or vice versa.

$$V_{MONITOR} = 0.4V \times \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right) \quad \text{Eq. 1}$$

GND

The ground (GND) pin is the return path for VDD, logic gates, and output pins. Refer to *PCB Layout Recommendations* for details.

/MR

Manual reset (/MR) is an active-low input pin that is internally pulled to VDD with a 90kΩ resistor. When /MR is asserted to a logic-low level, /RESET will transition to a logic low state while RESET will transition to a logic high state. See the *Timing Diagrams* section for more information.

/RESET

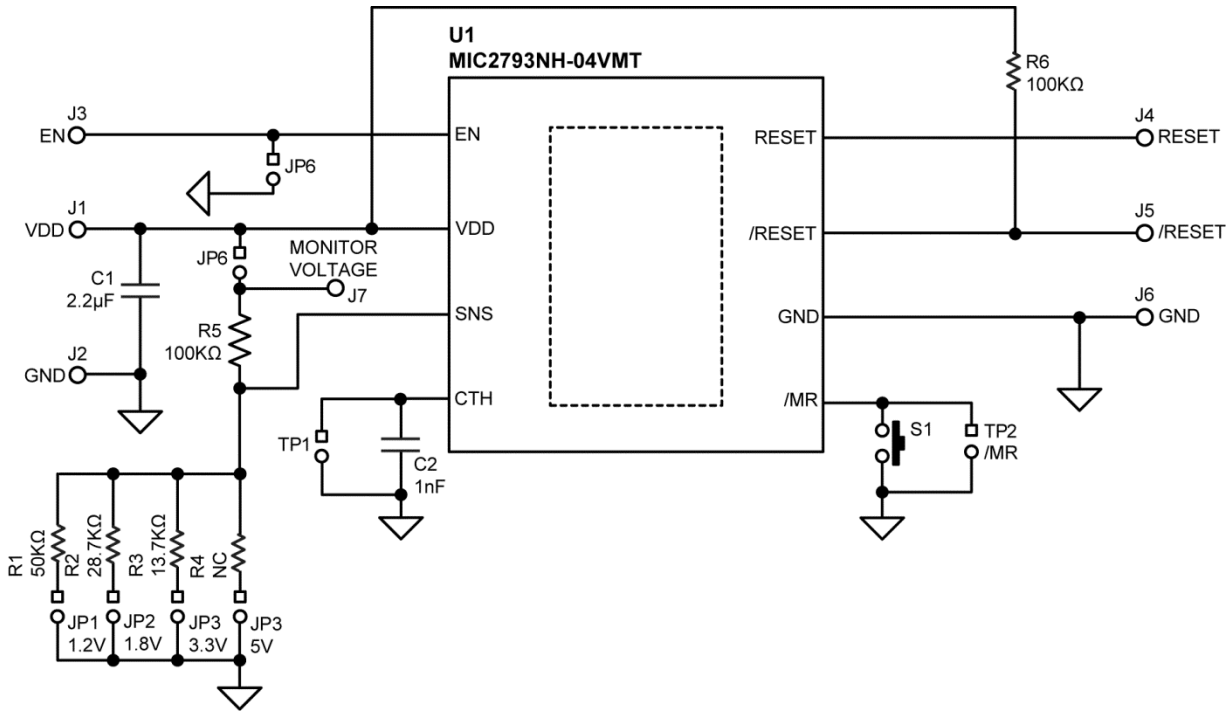
/RESET is an active-low output and is available in two output configurations: open-drain or push-pull. The open-drain configuration requires an external pull-up resistor, while the push-pull does not.

/RESET is asserted low when /MR is set to a logic-low or the SNS voltage decreases below the threshold voltage. /RESET will remain low for the programmed reset timeout delay after SNS > (V_{TH} + V_{HYST}) and /MR is set to a logic-high, and then /RESET will transition high to indicate normal regulation. See the *Timing Diagrams* section for more information.

RESET

RESET is an active-high push-pull output and is asserted high when /MR is set to a logic low or the SNS voltage decreases below the threshold voltage. RESET will remain high for the programmed reset timeout delay after SNS > (V_{TH} + V_{HYST}) and /MR is set to a logic high, and then RESET will transition low to indicate normal regulation. See the *Timing Diagrams* section for more information.

Typical Application Schematic



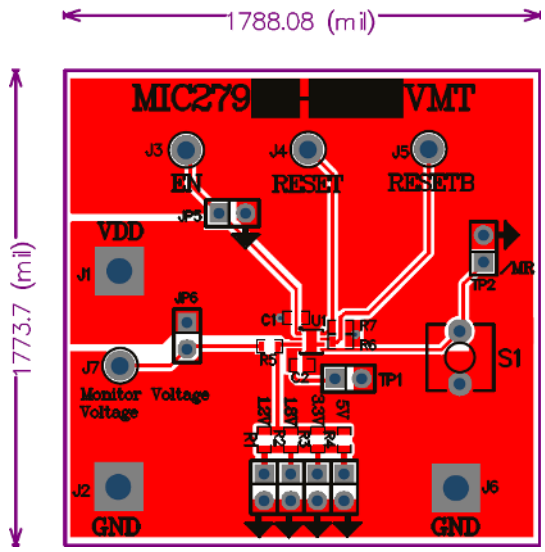
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	06036D225KAT2A	AVX[9]	2.2µF, 6.3V, X5R, 0603	1
	GRM188R60J225KE19D	Murata[10]		
	C1608X5R0J225KT	TDK[11]		
C2	01016D102KAT2A	AVX	1nF, 6.3V, X5R, 0603	1
	GRM155R60J102KA01D	Murata		
	C0402X5R0J102K020BC	TDK		
R1	CRCW060350K0FKEA	Vishay/Dale[12]	50kΩ, 1%, 1/10W, 0603	1
R2	CRCW060328K7FKEA	Vishay/Dale	28.7kΩ, 1%, 1/10W, 0603	1
R3	CRCW060313K7FKEA	Vishay/Dale	13.7kΩ, 1%, 1/10W, 0603	1
R5, R6	CRCW06031003FKEA	Vishay/Dale	100kΩ, 1%, 1/10W, 0603	2
U1	**MIC2793NH-04VMT**	**Micrel, Inc.[13]**	**Supervisor with High-Accuracy, Ultra-Fast Propagation Delay, and Capacitor-Programmable Reset Delay**	**1**

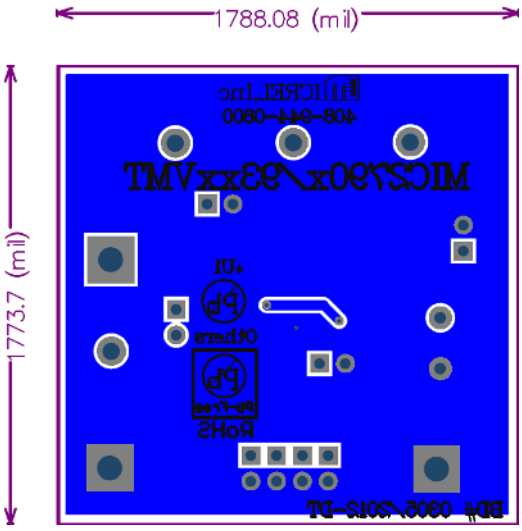
Notes:

9. AVX: www.avx.com.
10. Murata: www.murata.com.
11. TDK: www.tdk.com.
12. Vishay: www.vishay.com.
13. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

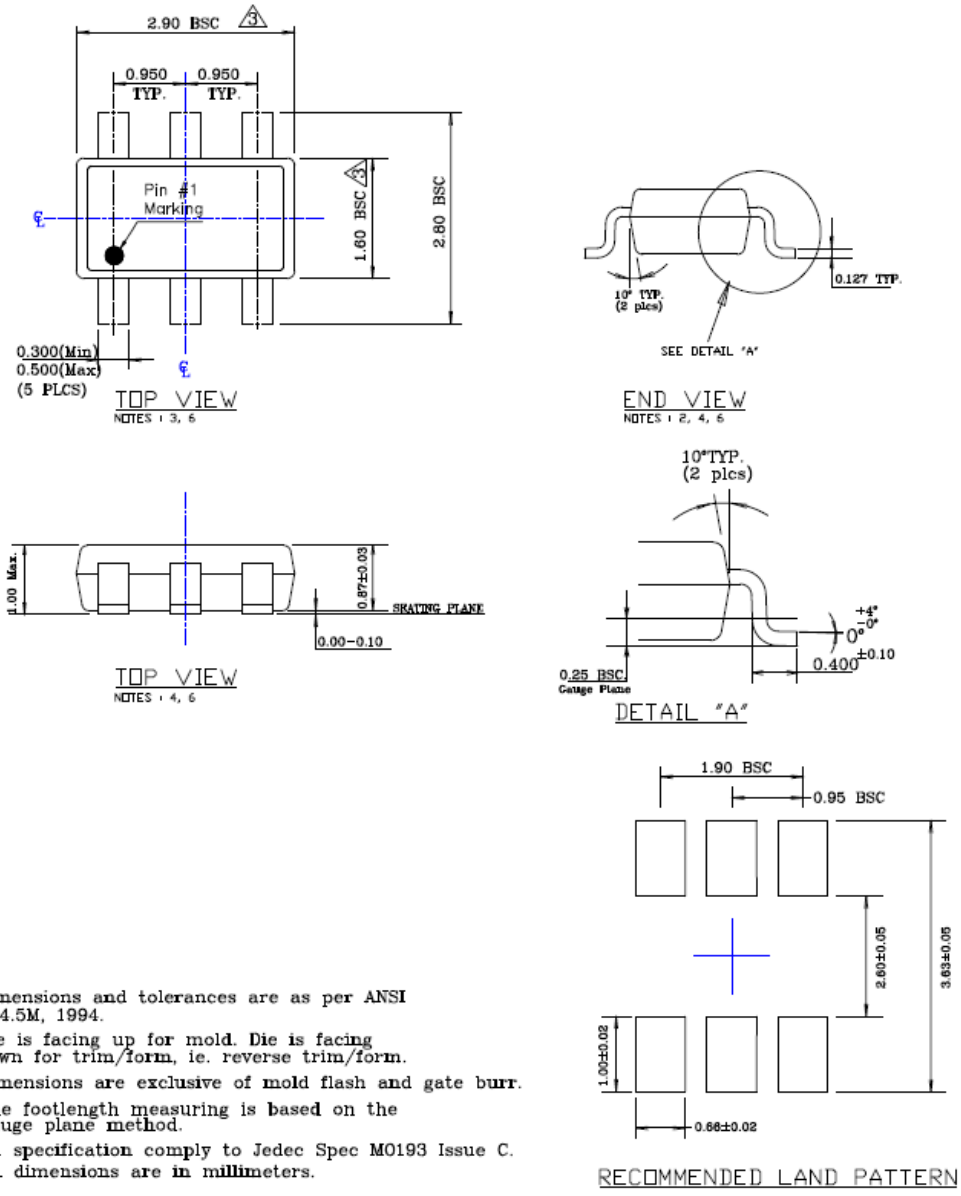


Top Layer



Bottom Layer

Package Information[14] and Recommended Land Pattern (TSOT-23-6L)



NOTE:

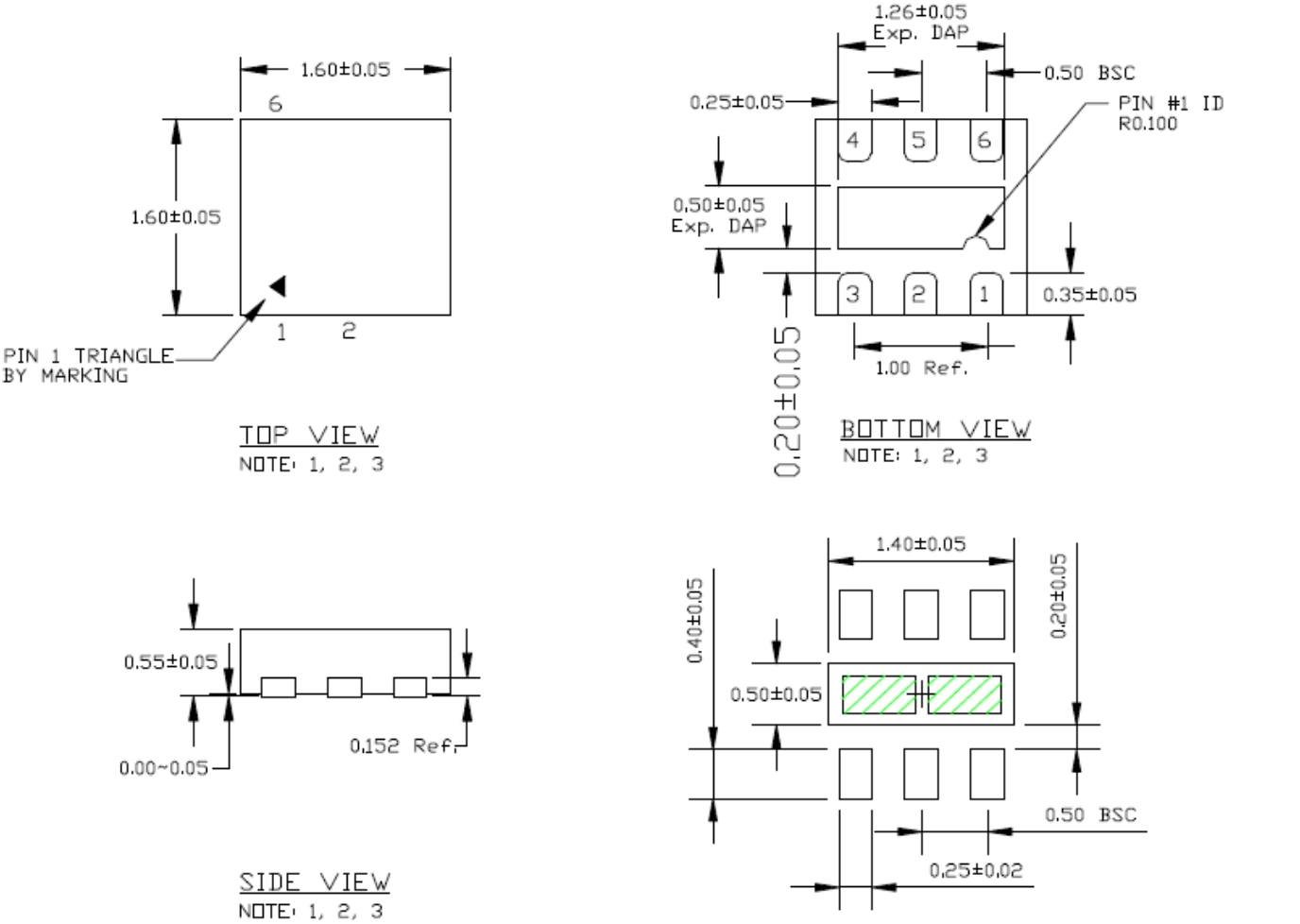
1. Dimensions and tolerances are as per ANSI Y14.5M, 1994.
2. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specification comply to Jedec Spec M0193 Issue C.
6. All dimensions are in millimeters.

6-pin TSOT-23 (D6)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

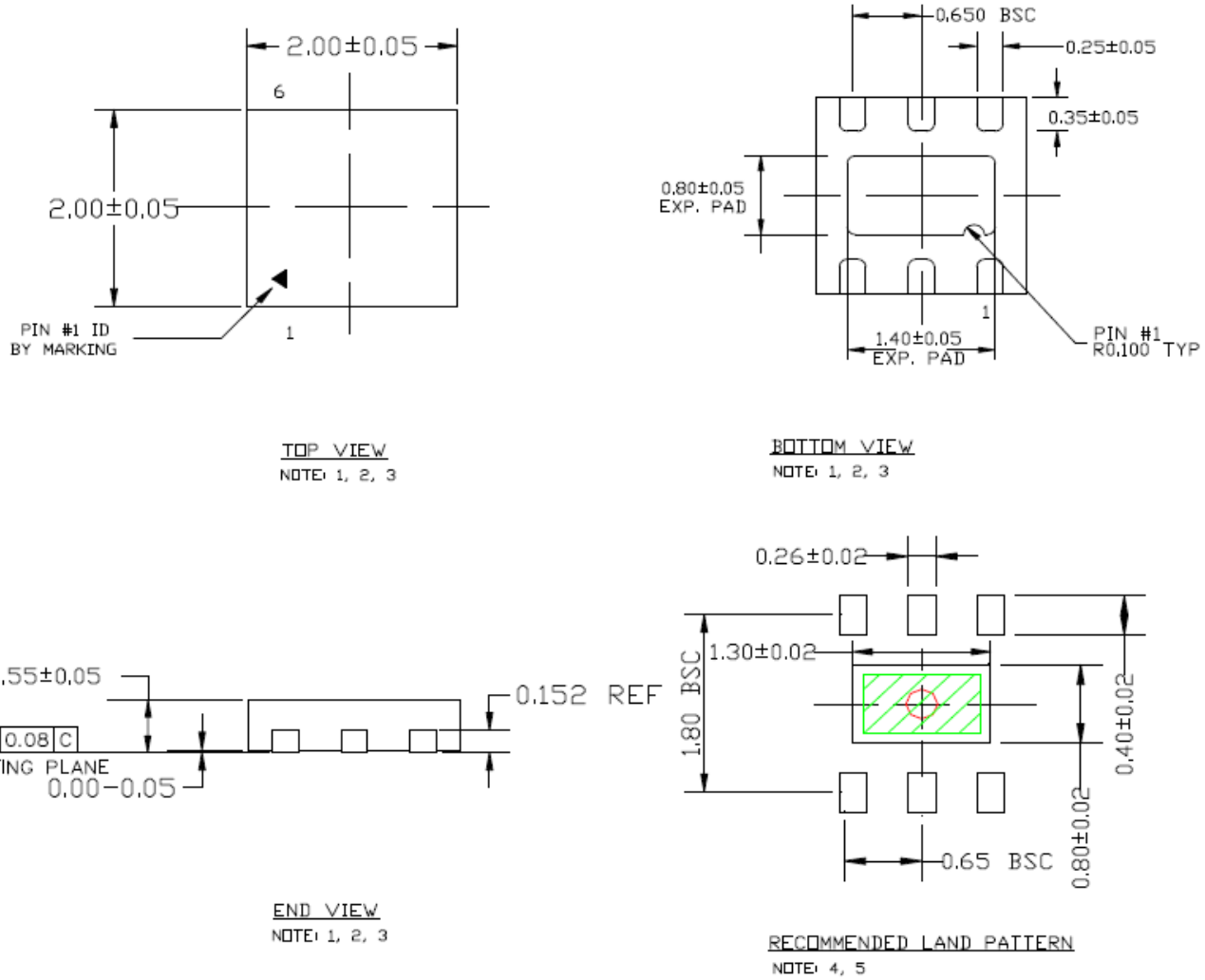
Package Information[14] and Recommended Land Pattern (1.6mm × 1.6mm TDFN-6L)



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN SHADED AREA REPRESENT SOLDER STENCIL OPENING (OPTIONAL) FOR IMPROVED THERMAL PERFORMANCE. SIZE: 0.55x0.30MM

6-pin 1.6mm × 1.6mm TDFN (MT)

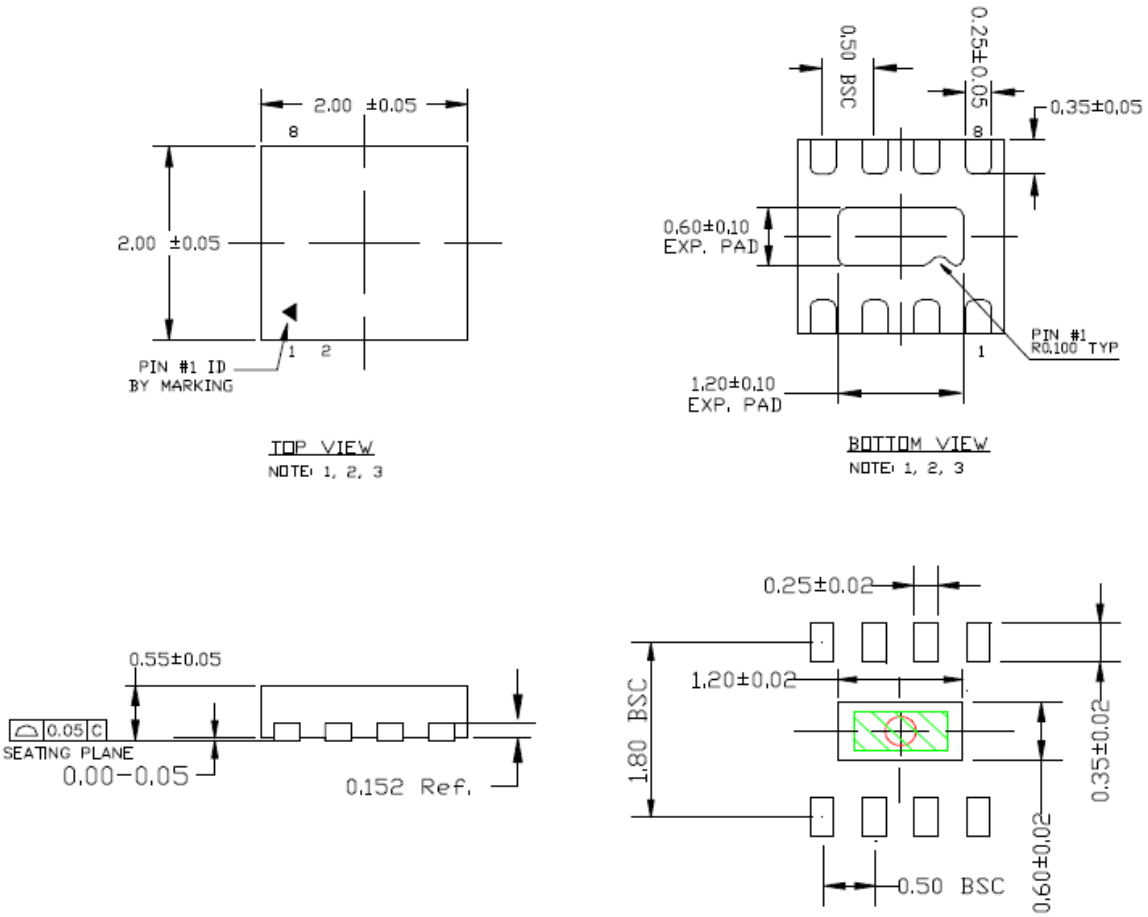
Package Information[14] and Recommended Land Pattern (2mm × 2mm TDFN-6L)



NOTE:
1. MAX PACKAGE WARPAGE IS 0.08 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENTS THERMAL VIA. SIZE SHOULD BE 0.30-0.3 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENTS SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.10x0.60 MM.

6-pin 2mm × 2mm TDFN (MT)

Package Information[14] and Recommended Land Pattern (2mm × 2mm TDFN-8L)



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENTS THERMAL VIA. SIZE SHOULD BE 0.30-0.3 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENTS SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.40x0.90 MM.

8-pin 2mm × 2mm TDFN (MT)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com