

N-channel 80 V, 3.3 mΩ typ., 90 A STripFET™ F7 Power MOSFET in a H2PAK-2 package

Datasheet - production data

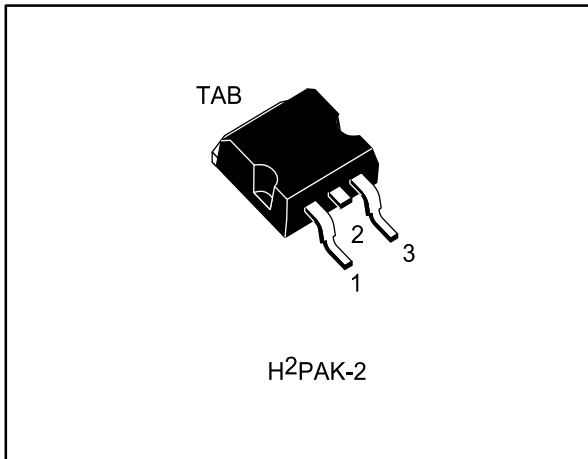
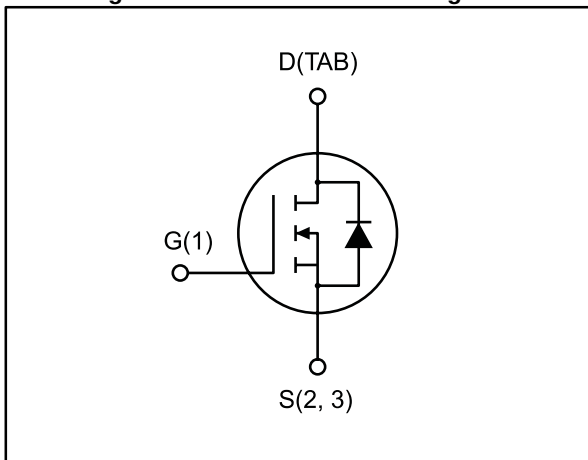


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STH140N8F7-2	80 V	4 mΩ	90 A	200 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STH140N8F7-2	140N8F7	H ² PAK-2	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	90 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	90	A
I_{DM} ⁽²⁾	Drain current (pulsed)	360	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	200	W
E_{AS} ⁽³⁾	Single pulse avalanche energy	515	mJ
T_j	Operating junction temperature	- 55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

Notes:

⁽¹⁾Limited by package

⁽²⁾Pulse width is limited by safe operating area

⁽³⁾Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 18.5\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	0.75	$^\circ\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

(T_{CASE} = 25 ° C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	80			V
I _{DSS}	Zero gate voltage Drain current	V _{GS} = 0, V _{DS} = 80 V			1	μA
		V _{GS} = 0, V _{DS} = 80 V, T _J = 125 ° C			10	μA
I _{GSS}	Gate-source leakage current	V _{DS} = 0, V _{GS} = ± 20 V			± 100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 45 A		3.3	4	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 40 V, f = 1 MHz	-	6340	-	pF
C _{OSS}	Output capacitance		-	1195	-	pF
C _{rSS}	Reverse transfer capacitance		-	105	-	pF
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 64 A, V _{GS} = 10 V	-	96	-	nC
Q _{gs}	Gate-source charge		-	30	-	nC
Q _{gd}	Gate-drain charge		-	26	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 40 V, I _D = 45 A R _G = 4.7 Ω, V _{GS} = 10 V	-	26	-	ns
t _r	Rise time		-	51	-	ns
t _{d(off)}	Turn-off-delay time		-	82	-	ns
t _f	Fall time		-	44	-	ns

Table 7: Source drain diode

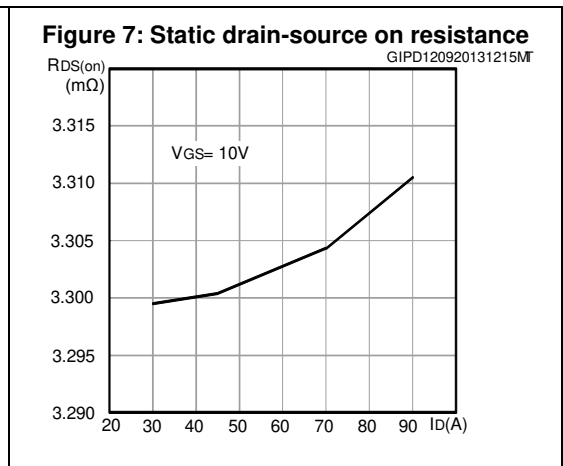
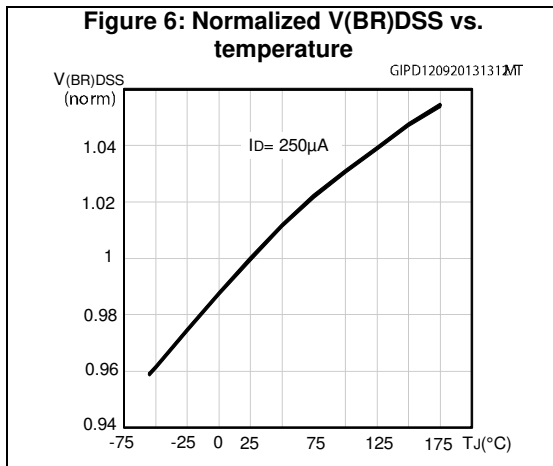
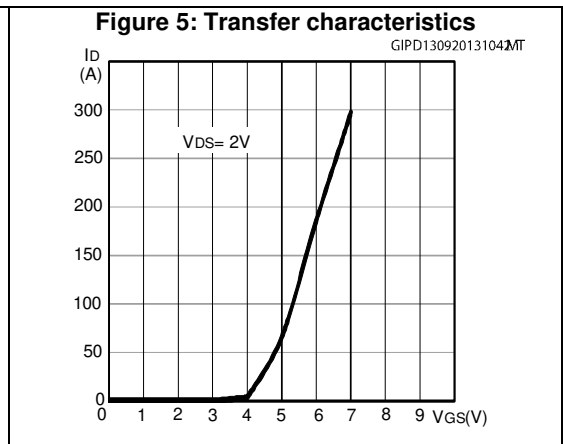
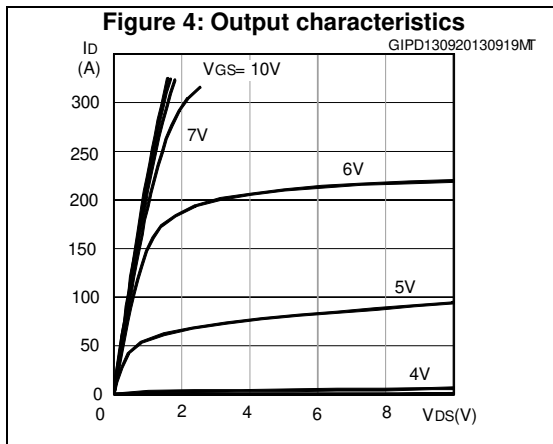
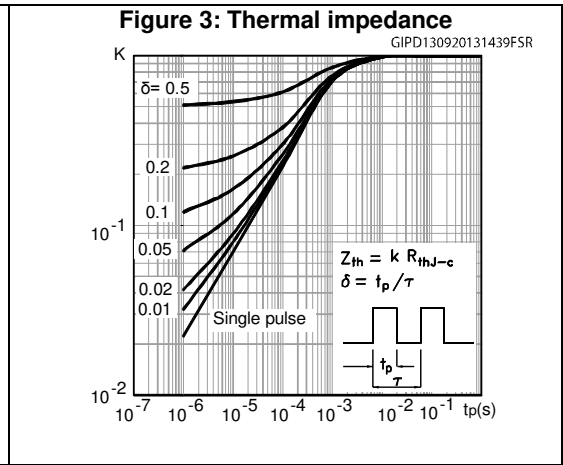
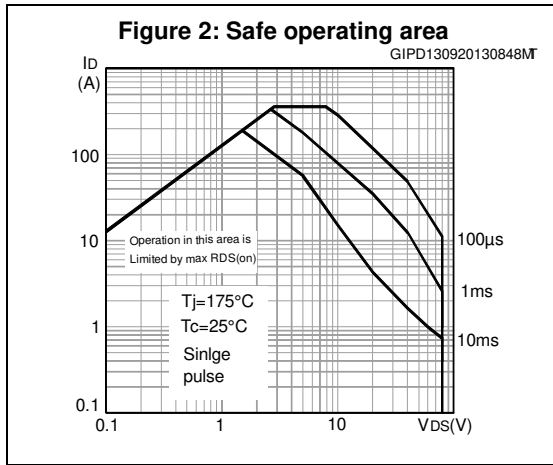
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		90	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		360	A
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0, I _{SD} = 90 A	-		1.2	V
t _{rr}	Reverse recovery time	I _{SD} = 64 A, di/dt = 100 A/μs, V _{DD} = 60 V, T _J = 150 ° C	-	58		ns
Q _{rr}	Reverse recovery charge		-	92		nC
I _{RRM}	Reverse recovery current		-	3.2		A

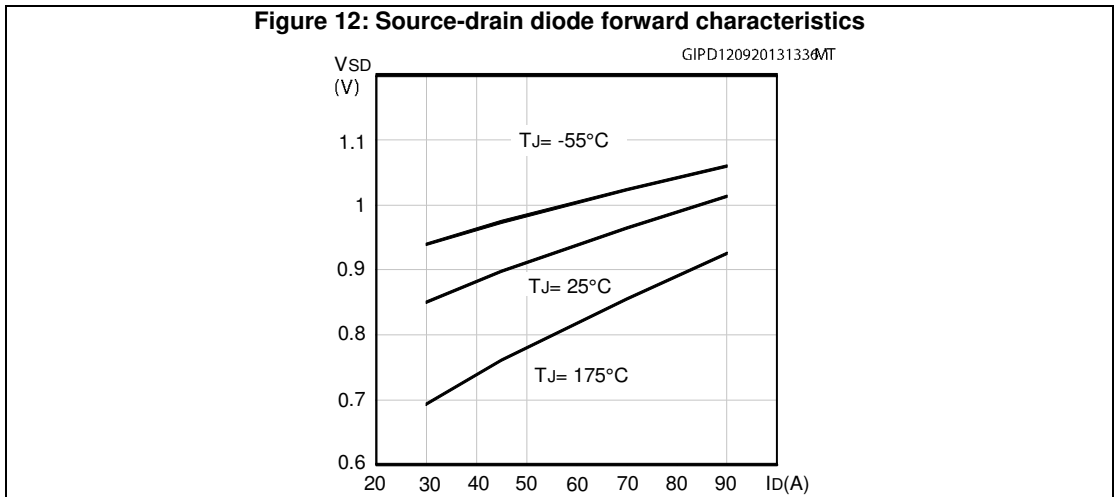
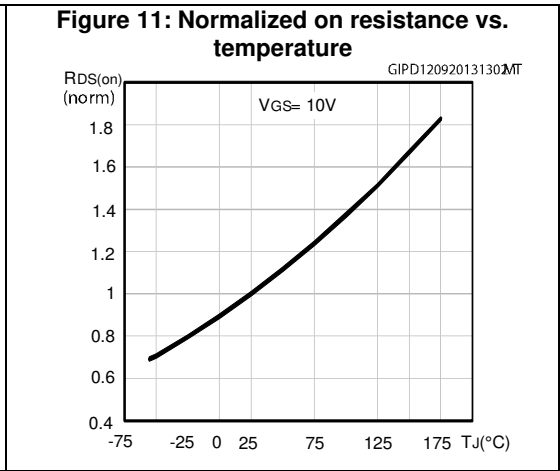
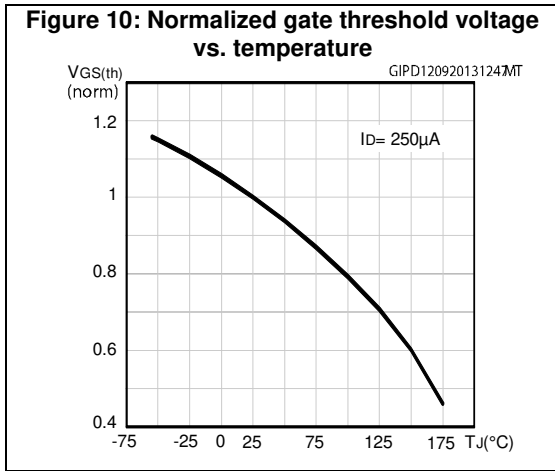
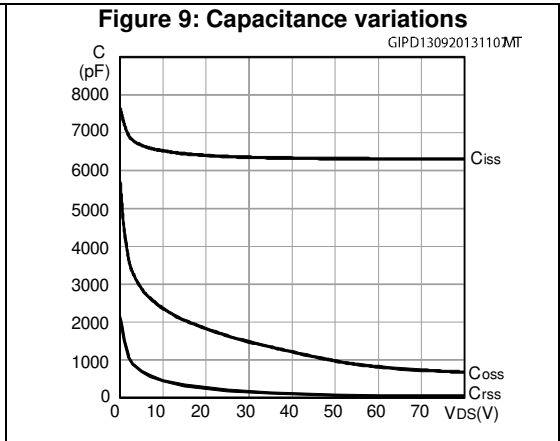
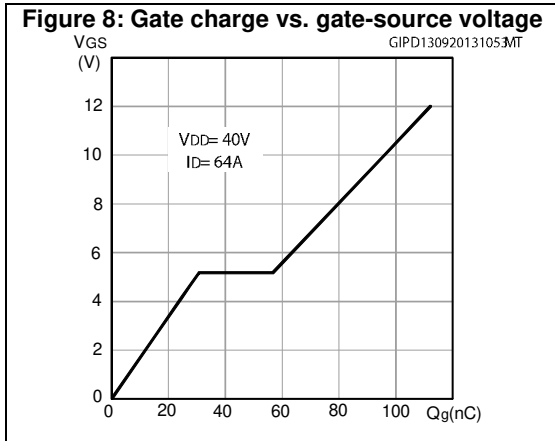
Notes:

⁽¹⁾Pulse width is limited by safe operating area

⁽²⁾Pulse test: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuit

Figure 13: Switching times test circuit for resistive load

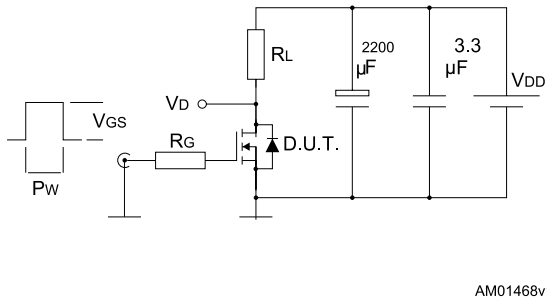


Figure 14: Gate charge test circuit

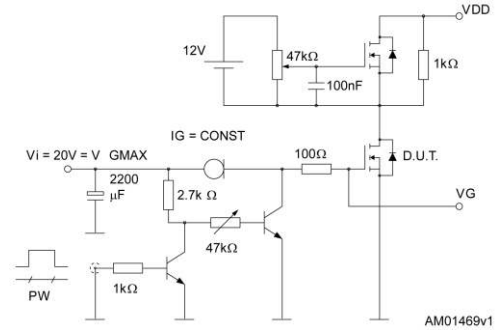


Figure 15: Test circuit for inductive load switching and diode recovery times

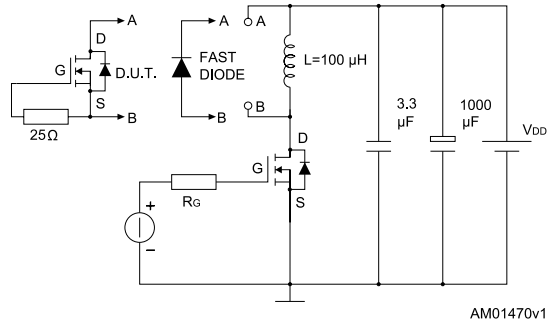


Figure 16: Unclamped inductive load test circuit

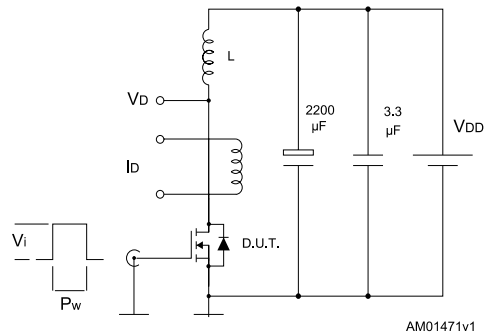


Figure 17: Unclamped inductive waveform

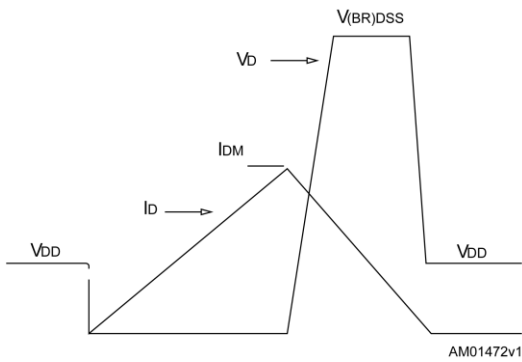
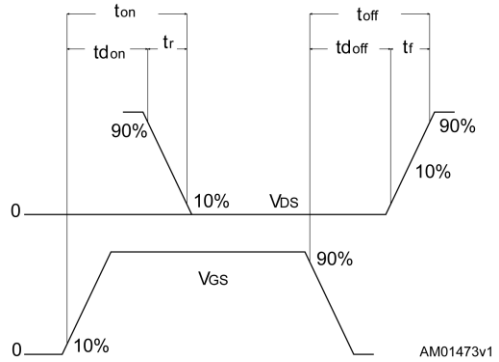


Figure 18: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 H2PAK-2 mechanical data

Figure 19: H²PAK-2 leads drawing

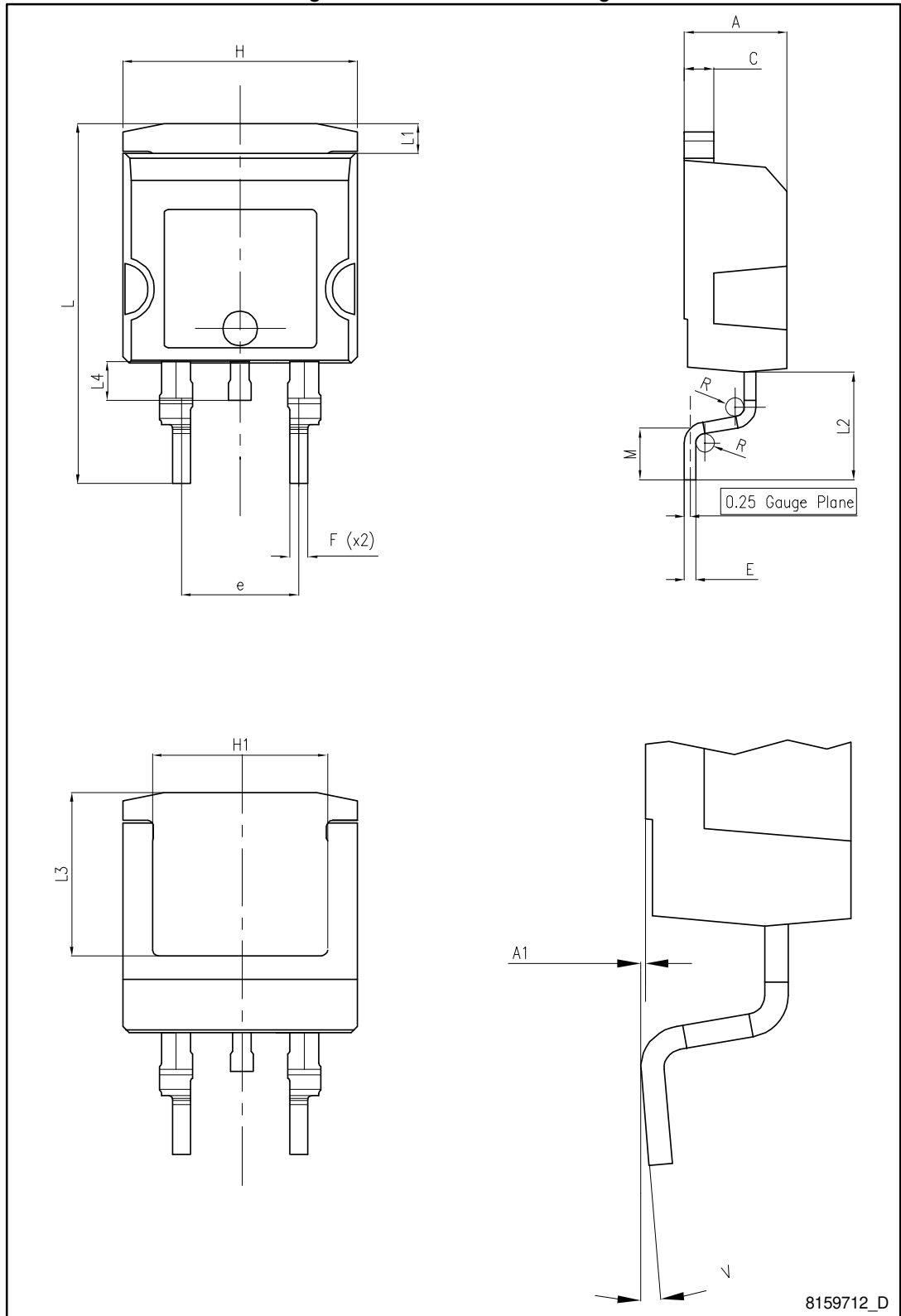
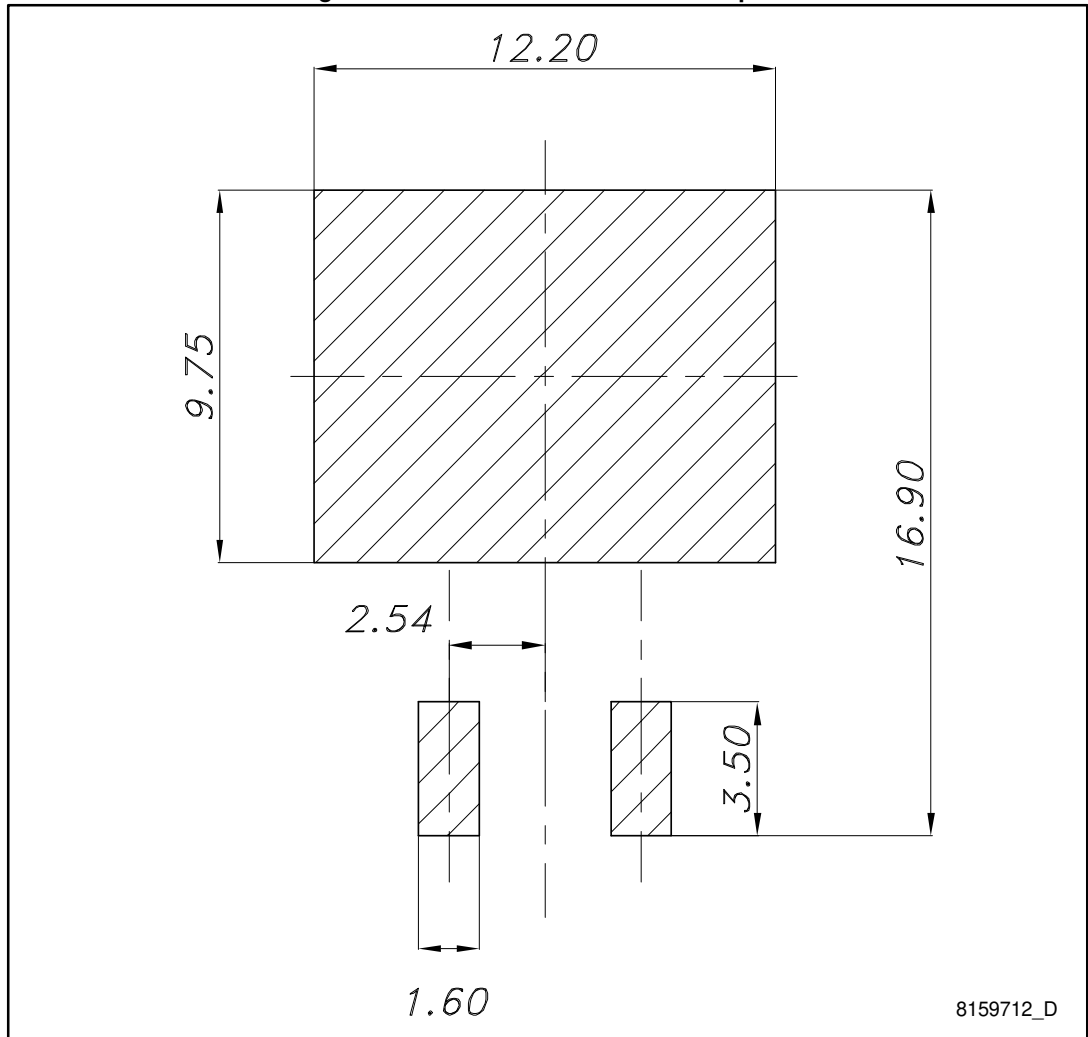


Table 8: H²PAK-2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

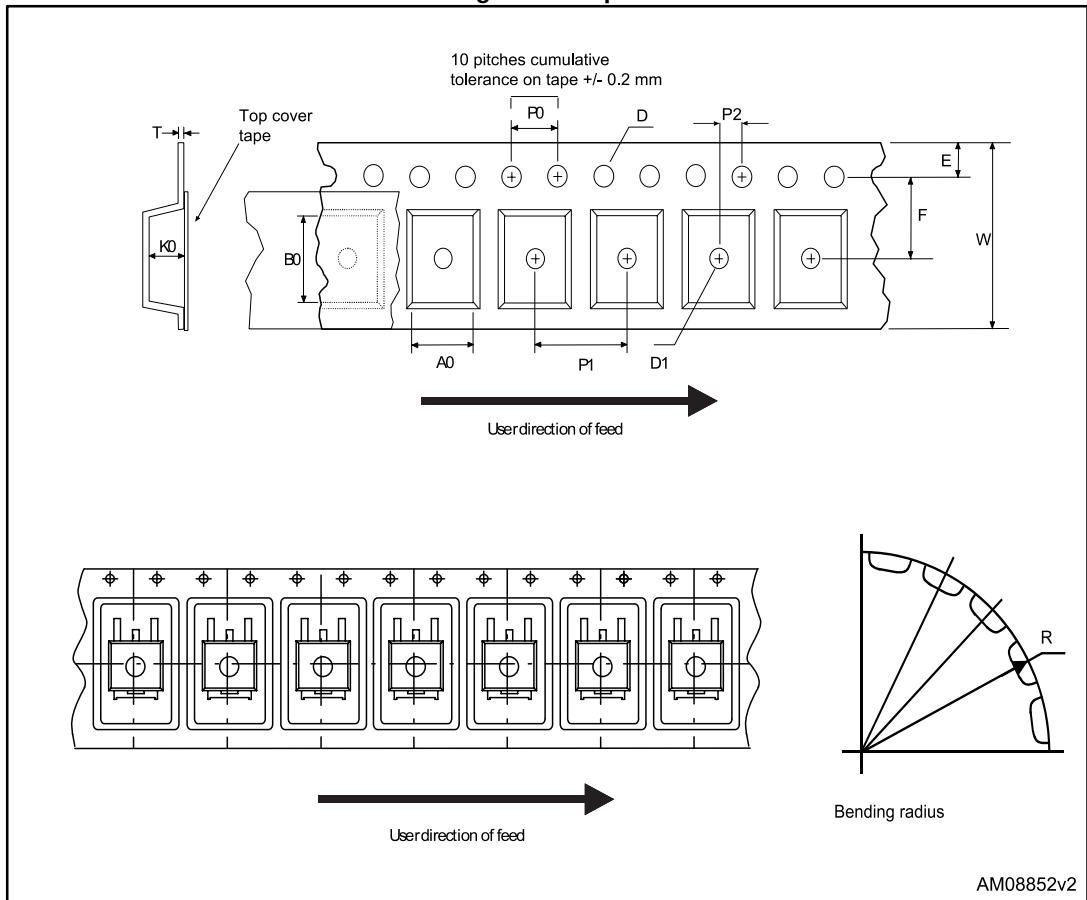
Figure 20: H²PAK-2 recommended footprint



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5 Packaging mechanical data

Figure 21: Tape



AM08852v2

Figure 22: Reel

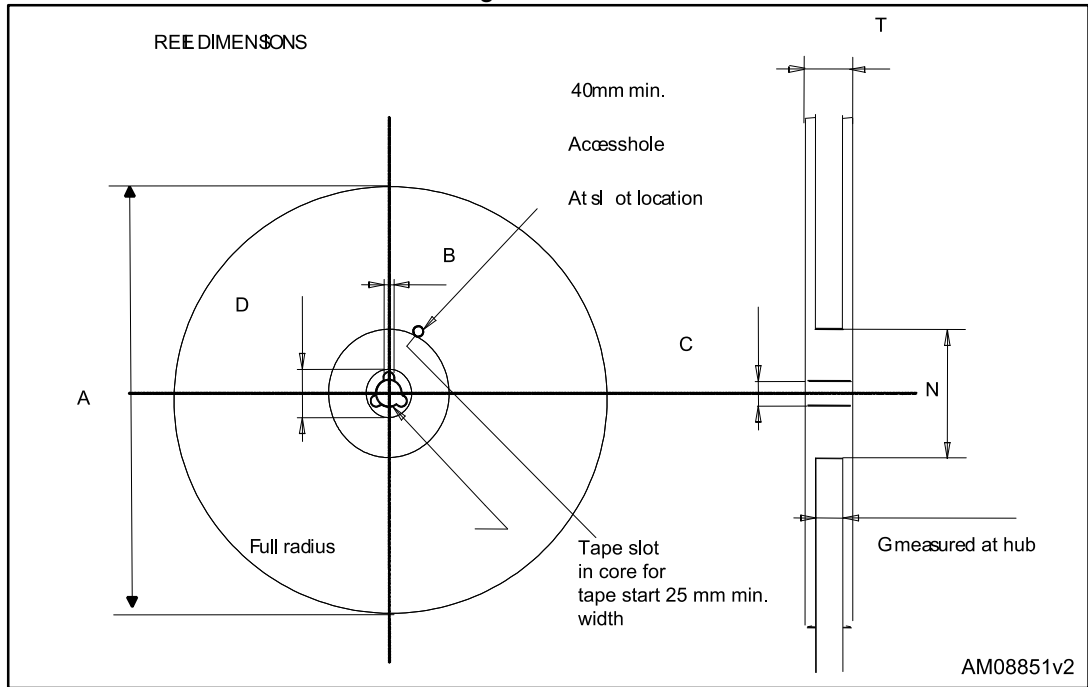


Table 9: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 10: Document revision history

Date	Revision	Changes
25-Aug-2014	1	First release. Part numbers STF140N8F7 and STP140N8F7 previously included in the datasheet DocID023888.
10-Oct-2014	2	Updated Figure 3: "Thermal impedance"

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