# PCIe-6351 and USB-6351

# Contents

# PCIe-6351 and USB-6351 Specifications

The following specifications are typical at 25 °C, unless otherwise noted. For more information about the PCIe-6351 and USB-6351, refer to the **X Series User Manual** available from ni.com/manuals.

## Analog Input

| | |
|---|---|
| Number of channels | 8 differential or 16 single ended |
| ADC resolution | 16 bits |
| DNL | No missing codes guaranteed |
| INL | Refer to the **AI Absolute Accuracy** section. |
| **Sample rate** | |
| Single channel maximum | 1.25 MS/s |
| Multichannel maximum (aggregate) | 1.00 MS/s |
| Minimum | No minimum |
| Timing resolution | 10 ns |
| Timing accuracy | 50 ppm of sample rate |
| Input coupling | DC |

| Input range | ±0.1 V, ±0.2 V, ±0.5 V, ±1 V, ±2 V, ±5 V, ±10 V |
|---|---|
| Maximum working voltage for analog inputs (signal + common mode) | ±11 V of AI GND |
| CMRR (DC to 60 Hz) | 100 dB |

**Input impedance**

**Device on**

| AI+ to AI GND | >10 GΩ in parallel with 100 pF |
|---|---|
| AI- to AI GND | >10 GΩ in parallel with 100 pF |

**Device off**

| AI+ to AI GND | 820 Ω |
|---|---|
| AI- to AI GND | 820 Ω |

| Input bias current | ±100 pA |
|---|---|

**Crosstalk (at 100 kHz)**

| Adjacent channels | -75 dB |
|---|---|
| Non-adjacent channels | -95 dB |

| Small signal bandwidth (-3 dB) | 1.7 MHz |
|---|---|
| Input FIFO size | 2,047 samples |

| Scan list memory | 4,095 entries |
|---|---|

**Data transfers**

PCIe        DMA (scatter-gather), programmed I/O

USB         USB Signal Stream, programmed I/O

**Overvoltage protection for all analog input and sense channels**

Device on                              ±25 V for up to two AI pins

Device off                             ±15 V for up to two AI pins

| Input current during overvoltage condition | ±20 mA max/AI pin |
|---|---|

## Settling Time for Multichannel Measurements

| Range | ±60 ppm of Step (±4 LSB for Full-Scale Step) | ±15 ppm of Step (±1 LSB for Full-Scale Step) |
|---|---|---|
| ±10 V, ±5 V, ±2 V, ±1 V | 1 µs | 1.5 µs |
| ±0.5 V | 1.5 µs | 2 µs |
| ±0.2 V, ±0.1 V | 2 µs | 8 µs |

# Typical Performance Graphs

Figure 1. Settling Error versus Time for Different Source Impedances
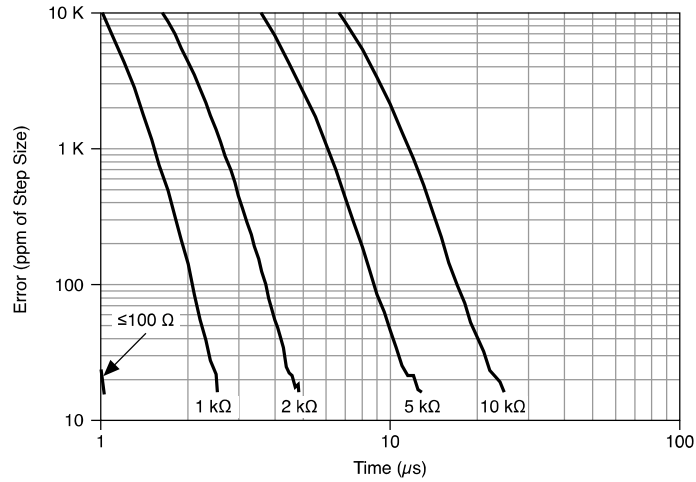


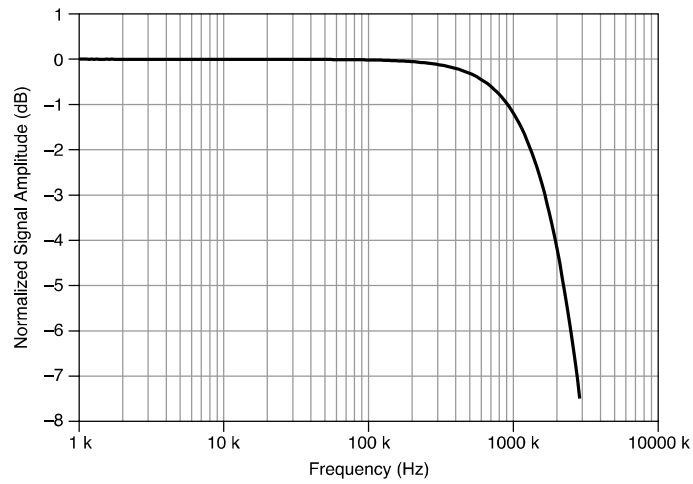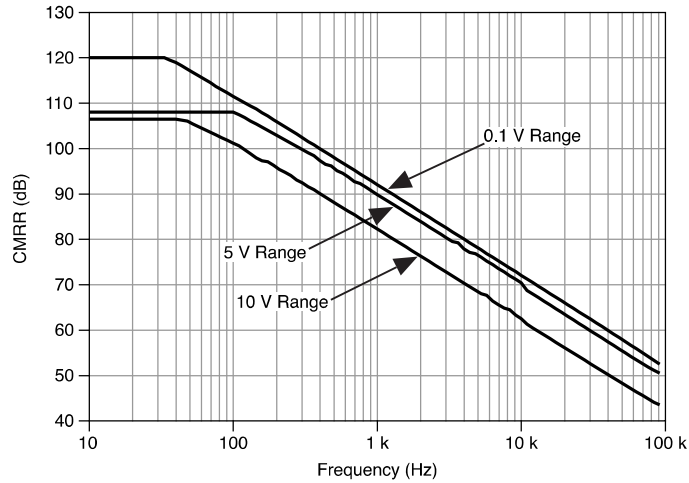Figure 2. AI <0..15> Small Signal Bandwidth

Figure 3. AI <0..15> CMRR



## AI Absolute Accuracy

| Nominal Range Positive Full Scale | Nominal Range Negative Full Scale | Residual Gain Error (ppm of Reading) | Residual Offset Error (ppm of Range) | Offset Tempco (ppm of Range/°C) | Random Noise, σ (µVrms) | Absolute Accuracy at Full Scale (µV) |
|---|---|---|---|---|---|---|
| 10 | -10 | 48 | 13 | 21 | 281 | 1,520 |
| 5 | -5 | 55 | 13 | 21 | 137 | 800 |
| 2 | -2 | 55 | 13 | 24 | 56 | 320 |
| 1 | -1 | 65 | 17 | 27 | 35 | 180 |
| 0.5 | -0.5 | 68 | 17 | 34 | 26 | 95 |
| 0.2 | -0.2 | 95 | 27 | 55 | 21 | 50 |
| 0.1 | -0.1 | 108 | 45 | 90 | 16 | 32 |

Table 1. AI Absolute Accuracy

For more information about absolute accuracy at full scale, refer to the AI Absolute Accuracy Example section.

| Gain tempco | 13 ppm/°C |
|---|---|
| Reference tempco | 1 ppm/°C |

| INL error | 46 ppm of range |
|---|---|

> **Note** Accuracies listed are valid for up to two years from the device external calibration.

## AI Absolute Accuracy Equation

**AbsoluteAccuracy** = **Reading** · **(GainError)** + **Range** · **(OffsetError)** + **NoiseUncertainity**

- **GainError** = **ResidualGainError** + **GainTempco** · **(TempChangeFromLastInternalCal)** + **ReferenceTempco** · **(TempChangeFromLastExternalCal)**

- **OffsetError** = **ResidualOffsetError** + **OffsetTempco** · **(TempChangeFromLastInternalCal)** + **INLError**

- **NoiseUncertainty** =

$$\frac{Random\ Noise \cdot 3}{\sqrt{10,000}}$$

for a coverage factor of 3 σ and averaging 10,000 points.

## AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- TempChangeFromLastExternalCal = 10 °C
- TempChangeFromLastInternalCal = 1 °C
- number_of_readings = 10,000
- CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- GainError = 48 ppm + 13 ppm · 1 + 1 ppm · 10 = 71 ppm
- OffsetError = 13 ppm + 21 ppm · 1 + 46 ppm = 80 ppm

- NoiseUncertainty =

$$\frac{281 \ \mu V \quad 3}{\sqrt{10,000}}$$

= 8.4 µV

- AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty = 1,520 µV

# Analog Triggers

| Number of triggers | 1 |
|---|---|
| Source | AI <0..15>, APFI 0 |
| Functions | Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase |

| **Source level** | | |
|---|---|---|
| AI <0..15> | | ±Full scale |
| APFI 0 | | ±10 V |

| Resolution | 16 bits |
|---|---|
| Modes | Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering |

| **Bandwidth (-3 db)** | | |
|---|---|---|
| AI <0..15> | | 3.4 MHz |
| APFI 0 | | 3.9 MHz |

| Accuracy | ±1% of range |
|---|---|

**APFI 0 characteristics**

| | |
|---|---|
| Input impedance | 10 kΩ |
| Coupling | DC |
| Protection, power on | ±30 V |
| Protection, power off | ±15 V |

# Analog Output

| | |
|---|---|
| Number of channels | 2 |
| DAC resolution | 16 bits |
| DNL | ±1 LSB |
| Monotonicity | 16 bit guaranteed |
| Accuracy | Refer to the AO Absolute Accuracy table. |
| **Maximum update rate** | |
| 1 channel | 2.86 MS/s |
| 2 channels | 2.00 MS/s |
| Timing accuracy | 50 ppm of sample rate |
| Timing resolution | 10 ns |

| | |
|---|---|
| Output range | ±10 V, ±5 V, ±external reference on APFI 0 |
| Output coupling | DC |
| Output impedance | 0.2 Ω |
| Output current drive | ±5 mA |
| Overdrive protection | ±25 V |
| Overrdrive current | 26 mA |
| Power-on state | ±5 mV |

**Power on/off glitch**

| | |
|---|---|
| PCIe | 1.5 V peak for 200 ms |
| USB | 1.5 V for 1.2 s[1] |

| | |
|---|---|
| Output FIFO size | 8,191 samples shared among channels used |

**Data transfers**

| | |
|---|---|
| PCIe | DMA (scatter-gather), programmed I/O |
| USB | USB Signal Stream, programmed I/O |

| | |
|---|---|
| AO waveform modes | Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update |
| Settling time, full-scale step, 15 ppm (1 LSB) | 2 µs |

| Slew rate | 20 V/µs |
|---|---|
| Glitch energy at midscale transition, ±10 V range | 10 nV · s |

## External Reference

**APFI 0 characteristics**

| | |
|---|---|
| Input impedance | 10 kΩ |
| Coupling | DC |
| Protection, device on | ±30 V |
| Protection, device off | ±15 V |
| Range | ±11 V |
| Slew rate | 20 V/µs |

Figure 4. AO External Reference Bandwidth
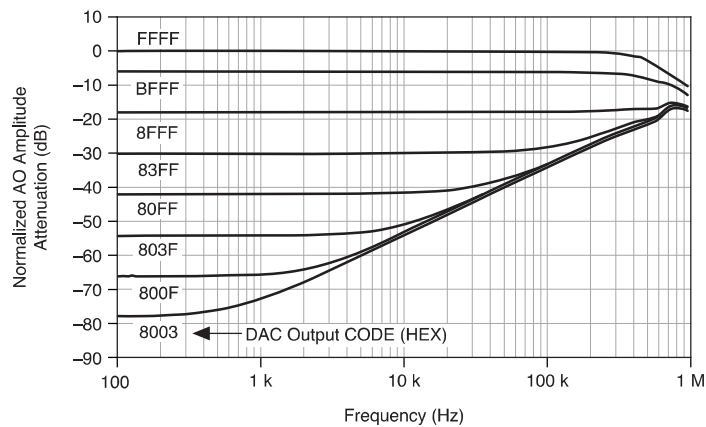
## AO Absolute Accuracy

Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.

| Nominal Range Positive Full Scale | Nominal Range Negative Full Scale | Residual Gain Error (ppm of Reading) | Gain Tempco (ppm/°C) | Reference Tempco (ppm/°C) | Residual Offset Error (ppm of Range) | Offset Tempco (ppm of Range/°C) | INL Error (ppm of Range) | Absolute Accuracy at Full Scale (μV) |
|---|---|---|---|---|---|---|---|---|
| 10 | -10 | 63 | 17 | 1 | 33 | 2 | 64 | 1,890 |
| 5 | -5 | 70 | 8 | 1 | 33 | 2 | 64 | 935 |

Table 2. AO Absolute Accuracy

> **Note** Accuracies listed are valid for up to two years from the device external calibration.

### AO Absolute Accuracy Equation

**AbsoluteAccuracy** = **OutputValue** · (**GainError**) + **Range** · (**OffsetError**)

- **GainError** = **ResidualGainError** + **GainTempco** · (**TempChangeFromLastInternalCal**) + **ReferenceTempco** · (**TempChangeFromLastExternalCal**)
- **OffsetError** = **ResidualOffsetError** + **OffsetTempco** · (**TempChangeFromLastInternalCal**) + **INLError**

# Digital I/O/PFI

## Static Characteristics

| Number of channels | 24 total, 8 (P0.<0..7>), 16 (PFI <0..7>/P1, PFI <8..15>/P2) |
|---|---|

| Ground reference | D GND |
|---|---|
| Direction control | Each terminal individually programmable as input or output |
| Pull-down resistor | 50 kΩ typical, 20 kΩ minimum |
| Input voltage protection | ±20 V on up to two pins |

**Caution** Stresses beyond those listed under the **Input voltage protection** specification may cause permanent damage to the device.

## Waveform Characteristics (Port 0 Only)

| Terminals used | Port 0 (P0.<0..7>) |
|---|---|
| Port/sample size | Up to 8 bits |
| Waveform generation (DO) FIFO | 2,047 samples |
| Waveform acquisition (DI) FIFO | 255 samples |

**DI Sample Clock frequency**

PCIe     0 to 10 MHz, system and bus activity dependent

USB     0 to 1 MHz, system and bus activity dependent

**DO Sample Clock frequency**

**PCIe**

Regenerate from FIFO        0 to 10 MHz

| Streaming from memory | 0 to 10 MHz, system and bus activity dependent |
|---|---|
| **USB** | |
| Regenerate from FIFO | 0 to 10 MHz |
| Streaming from memory | 0 to 1 MHz, system and bus activity dependent |

| **Data transfers** | |
|---|---|
| PCIe | DMA (scatter-gather), programmed I/O |
| USB | USB Signal Stream, programmed I/O |

| Digital line filter settings | 160 ns, 10.24 µs, 5.12 ms, disable |
|---|---|

## PFI/Port 1/Port 2 Functionality

| Functionality | Static digital input, static digital output, timing input, timing output |
|---|---|
| Timing output sources | Many AI, AO, counter, DI, DO timing signals |
| Debounce filter settings | 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input |

## Recommended Operating Conditions

| **Input high voltage ($V_{IH}$)** | |
|---|---|
| Minimum | 2.2 V |
| Maximum | 5.25 V |

| Input low voltage ($V_{IL}$) | |
|---|---|
| Minimum | 0 V |
| Maximum | 0.8 V |

| Output high current ($I_{OH}$) | |
|---|---|
| P0.<0..7> | -24 mA maximum |
| PFI <0..15>/P1/P2 | -16 mA maximum |

| Output low current ($I_{OL}$) | |
|---|---|
| P0.<0..7> | 24 mA maximum |
| PFI <0..15>/P1/P2 | 16 mA maximum |

# Digital I/O Characteristics

| | |
|---|---|
| Positive-going threshold (VT+) | 2.2 V maximum |
| Negative-going threshold (VT-) | 0.8 V minimum |
| Delta VT hysteresis (VT+ - VT-) | 0.2 V minimum |
| $I_{IL}$ input low current ($V_{IN}$ = 0 V) | -10 µA maximum |
| $I_{IH}$ input high current ($V_{IN}$ = 5 V) | 250 µA maximum |

Figure 5. P0.<0..7>: $I_{OH}$ versus $V_{OH}$
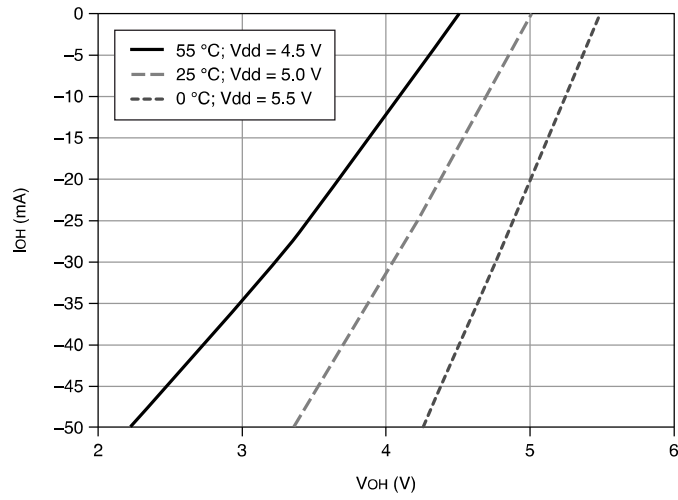


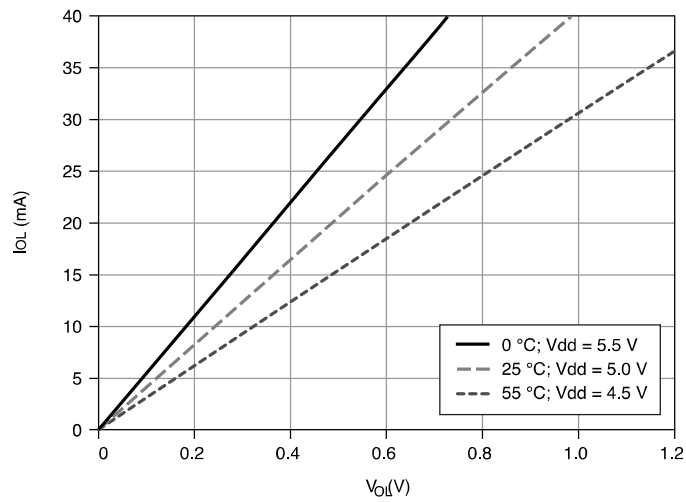Figure 6. P0.<0..7>: $I_{OL}$ versus $V_{OL}$

Figure 7. PFI <0..15>/P1/P2: $I_{OH}$ versus $V_{OH}$



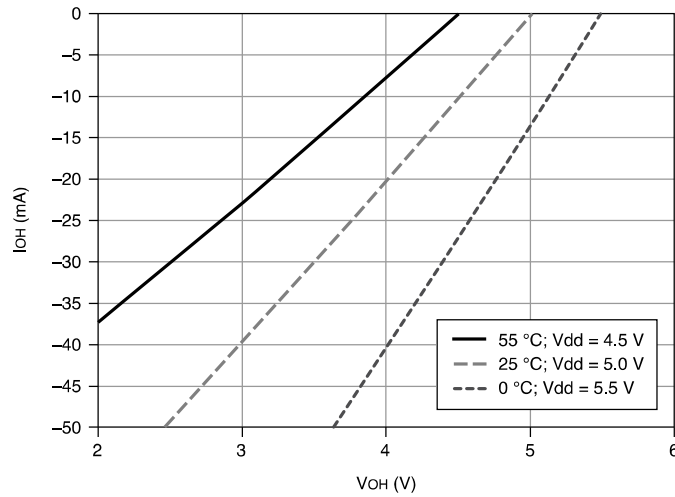Figure 8. PFI <0..15>/P1/P2: $I_{OL}$ versus $V_{OL}$
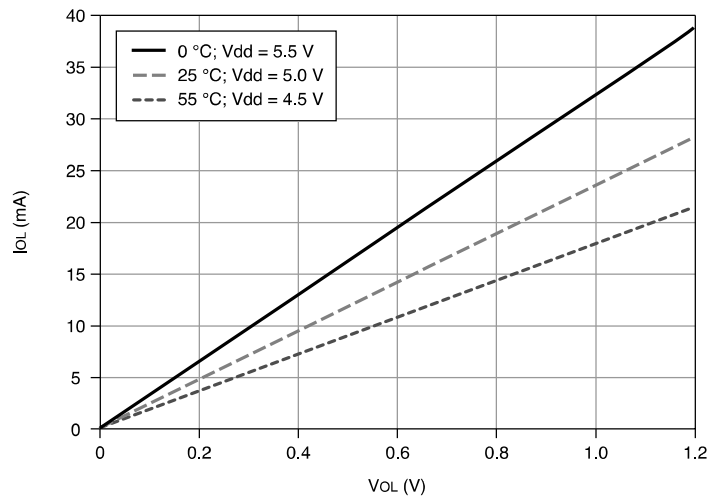


# General-Purpose Counters

| Number of counter/timers | 4 |
|---|---|
| Resolution | 32 bits |
| Counter measurements | Edge counting, pulse, pulse width, semi-period, period, two-edge separation |

| Position measurements | X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding |
|---|---|
| Output applications | Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling |
| Internal base clocks | 100 MHz, 20 MHz, 100 kHz |
| External base clock frequency | 0 MHz to 25 MHz |
| Base clock accuracy | 50 ppm |
| Inputs | Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock |

**Routing options for inputs**

PCIe     Any PFI, RTSI, analog trigger, many internal signals

USB      Any PFI, analog trigger, many internal signals

| FIFO | 127 samples per counter |
|---|---|

**Data transfers**

PCIe   Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O

USB   USB Signal Stream, programmed I/O

# Frequency Generator

| Number of channels | 1 |
|---|---|
| Base clocks | 20 MHz, 10 MHz, 100 kHz |

| Divisors | 1 to 16 |
|---|---|
| Base clock accuracy | 50 ppm |

Output can be available on any PFI or RTSI terminal.

## Phase-Locked Loop

| Number of PLLs | | | 1 |
|---|---|---|---|

| Reference Signal | PCIe Locking Input Frequency (MHz) | USB Locking Input Frequency (MHz) |
|---|---|---|
| RTSI <0..7> | 10, 20 | — |
| PFI <0..15> | 10, 20 | 10 |

Table 3. Reference Clock Locking Frequencies

| Output of PLL | 100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases |
|---|---|

## External Digital Triggers

| Source | |
|---|---|
| PCIe | Any PFI, RTSI |
| USB | Any PFI |
| Polarity | Software-selectable for most signals |
| Analog input function | Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase |

| | |
|---|---|
| Analog output function | Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase |
| Counter/timer functions | Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock |
| Digital waveform generation (DO) function | Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase |
| Digital waveform acquisition (DI) function | Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase |

## Device-to-Device Trigger Bus

| **Input Source** | |
|---|---|
| PCIe | RTSI <0..7> |
| USB | None |

| **Output destination** | |
|---|---|
| PCIe | RTSI <0..7> |
| USB | None |

| | |
|---|---|
| Output selections | 10 MHz Clock, frequency generator output, many internal signals |
| Debounce filter settings | 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input |

## Bus Interface

| **PCIe** |
|---|

| | |
|---|---|
| Form factor | x1 PCI Express, specification v1.1 compliant |
| Slot compatibility | x1, x4, x8, and x16 PCI Express slots [2] |
| DMA channels | 8, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3 |

**USB**

| | |
|---|---|
| USB compatibility | USB 2.0 Hi-Speed or full-speed[3] |
| USB Signal Stream | 8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3 |

# Power Requirements

**PCIe**

**Without disk drive power connector installed**

| | |
|---|---|
| +3.3 V | 4.6 W |
| +12 V | 5.4 W |

**With disk drive power connector installed**

| | |
|---|---|
| +3.3 V | 1.6 W |
| +12 V | 5.4 W |
| +5.0 V | 15 W |

**USB**

| Power supply requirements | 11 to 30 VDC, 30 W, 2 positions 3.5 mm pitch pluggable screw terminal with screw locks similar to Phoenix Contact MC 1,5/2-STF-3,5 BK |
|---|---|
| Power input mating connector | Phoenix Contact MC 1,5/2-GF-3,5 BK or equivalent |

> **Caution** NI USB-6351 devices must be powered with an NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

## Current Limits

> **Caution** Exceeding the current limits may cause unpredictable behavior by the device and/or PC.

**PCIe**

**Without disk drive power connector installed**

| | |
|---|---|
| P0/PFI/P1/P2 and +5 V terminals combined | 0.59 A max |

**With disk drive power connector installed**

| | |
|---|---|
| +5 V terminal (connector 0) | 1 A max[4] |
| +5 V terminal (connector 1) | 1 A max[4] |
| P0/PFI/P1/P2 combined | 1 A max |

**USB**

| | |
|---|---|
| +5 V terminal | 1 A max[4] |
| P0/PFI/P1/P2 and +5 V terminals combined | 2 A max |

## Physical Characteristics

**Printed circuit board dimensions**

| | |
|---|---|
| PCIe | 9.9 × 16.8 cm (3.9 × 6.6 in.) (half-length) |

**Enclosure dimensions (includes connectors)**

| | |
|---|---|
| USB | 26.4 × 17.3 × 3.6 cm (10.4 × 6.8 × 1.4 in.) |

**Weight**

| | |
|---|---|
| PCIe | 161 g (5.6 oz) |
| USB | 1.42 kg (3 lb 2 oz) |

**I/O connector**

| | |
|---|---|
| PCIe | 1 68-pin VHDCI |
| USB | 64 screw terminals |

| Manufacturer, Part Number | Description |
|---|---|
| MOLEX 71430-0011 | 68-Pos Right Angle Single Stack PCB-Mount VHDCI (Receptacle) |
| MOLEX 74337-0016 | 68-Pos Right Angle Dual Stack PCB-Mount VHDCI (Receptacle) |
| MOLEX 71425-3001 | 68-Pos Offset IDC Cable Connector (Plug) (SHC68-*) |

Table 4. PCIe Mating Connectors

| PCIe disk drive power connector | Standard ATX peripheral connector (not serial ATA) |
| --- | --- |
| USB screw terminal wiring | 16-24 AWG |

# Calibration

| Recommended warm-up time | 15 minutes |
| --- | --- |
| Calibration interval | 2 years |

# Maximum Working Voltage

**Maximum working voltage** refers to the signal voltage plus the common-mode voltage.

| Channel to earth | 11 V, Measurement Category I |
| --- | --- |

**Caution** Do not use for measurements within Categories II, III, or IV.

# Environmental

| **Operating temperature** | |
| --- | --- |
| PCIe | 0 to 50 °C |
| USB | 0 to 45 °C |
| Storage temperature | -40 to 70 ºC |
| Operating humidity | 10 to 90% RH, noncondensing |

| Storage humidity | 5 to 95% RH, noncondensing |
|---|---|
| Pollution Degree | 2 |
| Maximum altitude | 2,000 m |

Indoor use only.

## Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

> **Note** For safety certifications, refer to the product label or the Product Certifications and Declarations section.

## Electromagnetic Compatibility

## CE Compliance $C\,E$

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)
- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

# Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

# Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

## EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

## 电子信息产品污染控制管理办法（中国 RoHS）

- 中国 RoHS— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

# Device Pinouts

Figure 9. NI PCIe-6351 Pinout

| | | | |
|---|---|---|---|
| AI 0 (AI 0+) | 68 | 34 | AI 8 (AI 0–) |
| AI GND | 67 | 33 | AI 1 (AI 1+) |
| AI 9 (AI 1–) | 66 | 32 | AI GND |
| AI 2 (AI 2+) | 65 | 31 | AI 10 (AI 2–) |
| AI GND | 64 | 30 | AI 3 (AI 3+) |
| AI 11 (AI 3–) | 63 | 29 | AI GND |
| AI SENSE | 62 | 28 | AI 4 (AI 4+) |
| AI 12 (AI 4–) | 61 | 27 | AI GND |
| AI 5 (AI 5+) | 60 | 26 | AI 13 (AI 5–) |
| AI GND | 59 | 25 | AI 6 (AI 6+) |
| AI 14 (AI 6–) | 58 | 24 | AI GND |
| AI 7 (AI 7+) | 57 | 23 | AI 15 (AI 7–) |
| AI GND | 56 | 22 | AO 0 |
| AO GND | 55 | 21 | AO 1 |
| AO GND | 54 | 20 | APFI 0 |
| D GND | 53 | 19 | P0.4 |
| P0.0 | 52 | 18 | D GND |
| P0.5 | 51 | 17 | P0.1 |
| D GND | 50 | 16 | P0.6 |
| P0.2 | 49 | 15 | D GND |
| P0.7 | 48 | 14 | +5 V |
| P0.3 | 47 | 13 | D GND |
| PFI 11/P2.3 | 46 | 12 | D GND |
| PFI 10/P2.2 | 45 | 11 | PFI 0/P1.0 |
| D GND | 44 | 10 | PFI 1/P1.1 |
| PFI 2/P1.2 | 43 | 9 | D GND |
| PFI 3/P1.3 | 42 | 8 | +5 V |
| PFI 4/P1.4 | 41 | 7 | D GND |
| PFI 13/P2.5 | 40 | 6 | PFI 5/P1.5 |
| PFI 15/P2.7 | 39 | 5 | PFI 6/P1.6 |
| PFI 7/P1.7 | 38 | 4 | D GND |
| PFI 8/P2.0 | 37 | 3 | PFI 9/P2.1 |
| D GND | 36 | 2 | PFI 12/P2.4 |
| D GND | 35 | 1 | PFI 14/P2.6 |

CONNECTOR 0 (AI 0–15)

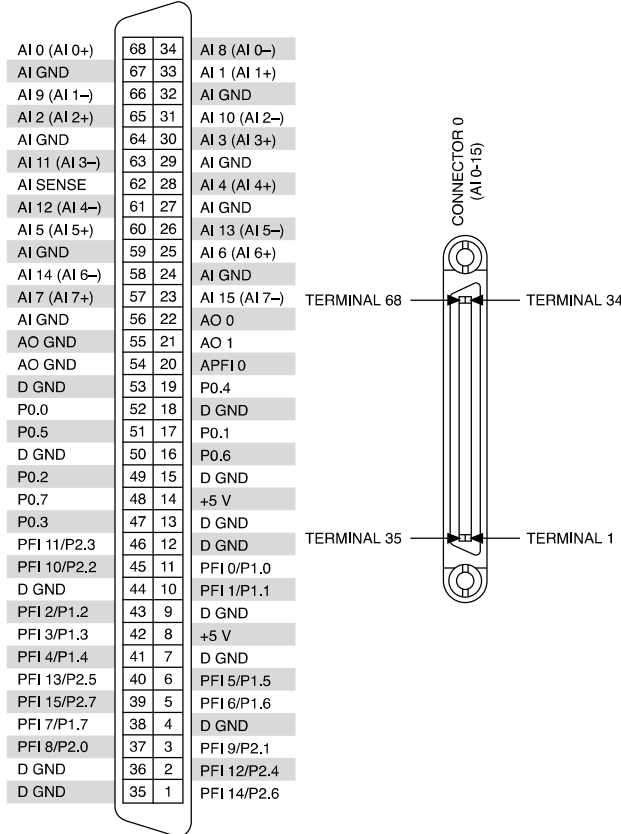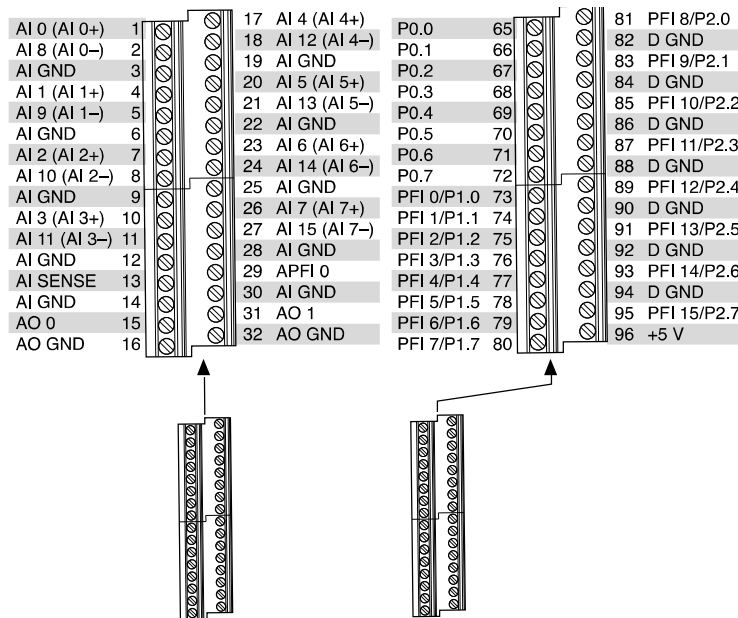TERMINAL 68 — TERMINAL 34

TERMINAL 35 — TERMINAL 1

Figure 10. NI USB-6351 Pinout



[1] Typical behavior. Time period may be longer due to host system USB performance. Time period will be longer during firmware updates.

[2] Some motherboards reserve the x16 slot for graphics use. For PCI Express guidelines, refer to ni.com/pciexpress.

[3] Operating on a full-speed bus results in lower performance, and you might not be able to achieve maximum sampling/update rates.

[4] Has a self-resetting fuse that opens when current exceeds this specification.