Atmel

ATA6629/ATA6631

LIN Bus Transceiver with Integrated Voltage Regulator

DATASHEET

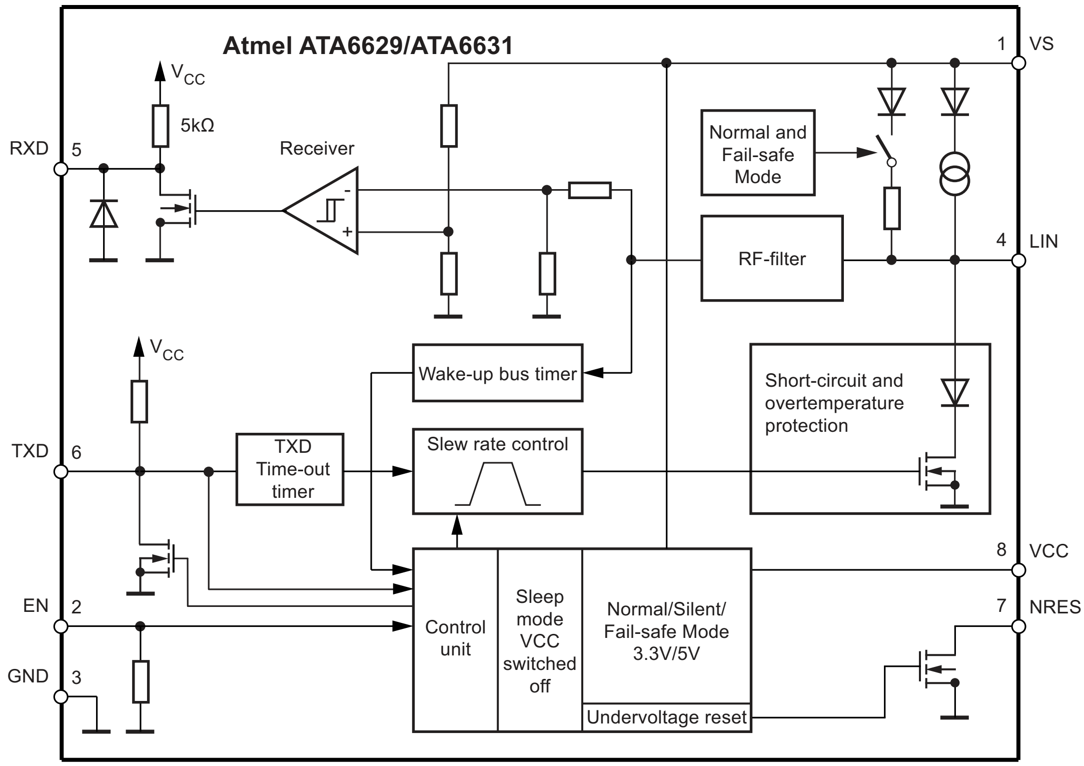
Features

- Supply voltage up to 40V
- Operating voltage V_S = 5V to 27V
- Typically 10µA supply current during sleep mode
- Typically 35µA supply current in silent mode
- Linear low-drop voltage regulator, 85mA current capability:
  - Normal, fail-safe, and silent mode
  - Atmel ATA6629: V_{CC} = 3.3V ±2%
  - Atmel ATA6631: V_{CC} = 5.0V ±2%
  - Sleep mode: V_{CC} is switched off
- V_{CC} undervoltage detection with reset open drain output NRES (4ms reset time)
- Voltage regulator is short-circuit and over-temperature protected
- LIN physical layer according to LIN 2.0, 2.1 and SAEJ2602-2
- Wake-up capability via LIN bus (90µs dominant)
- TXD time-out timer
- Bus pin is overtemperature and short-circuit protected versus GND and battery
- Advanced EMC and ESD performance
- Fulfills the OEM “hardware requirements for LIN in automotive applications rev.1.1”
- Interference and damage protection according to ISO7637
- Package: SO8

1. Description

Atmel® ATA6629/ATA6631 is a fully integrated LIN transceiver, designed according to the LIN specification 2.0, 2.1 and SAEJ2602-2, with a low-drop voltage regulator (3.3V/5V/85mA). The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful, slave nodes in LIN bus systems. ATA6629/ATA6631 is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20kBaud. The bus output is designed to withstand high voltage. Sleep mode and silent mode guarantee minimized current consumption even in the case of a floating or a short circuited LIN-bus.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO8

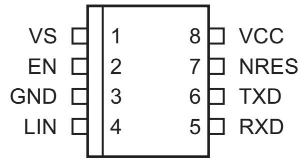


Table 2-1. Pin Description

Pin	Symbol	Function
1	VS	Battery supply
2	EN	Enables normal mode if the input is high
3	GND	Ground, heat sink
4	LIN	LIN bus line input/output
5	RXD	Receive data output
6	TXD	Transmit data input
7	NRES	Output undervoltage reset, low at reset
8	VCC	Output voltage regulator 3.3V/5V/50mA

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which are according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

3.2 Supply Pin (VS)

LIN operating voltage is V_S = 5V to 27V. An undervoltage detection is implemented to disable transmission if V_S falls below 5V, in order to avoid false bus messages. After switching on V_S, the IC starts with the fail-safe mode and the voltage regulator is switched on.

The supply current in sleep mode is typically 10µA and 35µA in silent mode.

3.3 Ground Pin (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It is able to handle a ground shift up to 11.5% of V_S.

3.4 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85mA, supplying the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun}.

3.5 Undervoltage Reset Output (NRES)

If the V_{CC} voltage falls below the undervoltage detection threshold V_{thun}, NRES switches to low after tres_f (Figure 6-1 on page 15). Even if V_{CC} = 0V the NRES stays low, because it is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays low until V_S < 1.5V and then becomes highly resistant.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 4ms after V_{CC} reaches its nominal value.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the event of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled.

3.7 Input/Output (TXD)

In normal mode the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state. During fail-safe mode, this pin is used as output and is signalling the fail-safe source.

3.8 Dominant Time-out Function (TXD)

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 27ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10µs).

3.9 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up resistor with typically 5kΩ to V_{CC}. The AC characteristics are measured with an external load capacitor of 20pF.

The output is short-circuit protected. In unpowered mode (that is, V_S = 0V), RXD is switched off.

3.10 Enable Input Pin (EN)

The enable input pin controls the operation mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced to silent mode. No data transmission is then possible, and the current consumption is reduced to I_{VS} typ. 35µA. The VCC regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced to sleep mode. No data transmission is possible, and the voltage regulator is switched off.

4. Modes of Operation

Figure 4-1. Modes of Operation

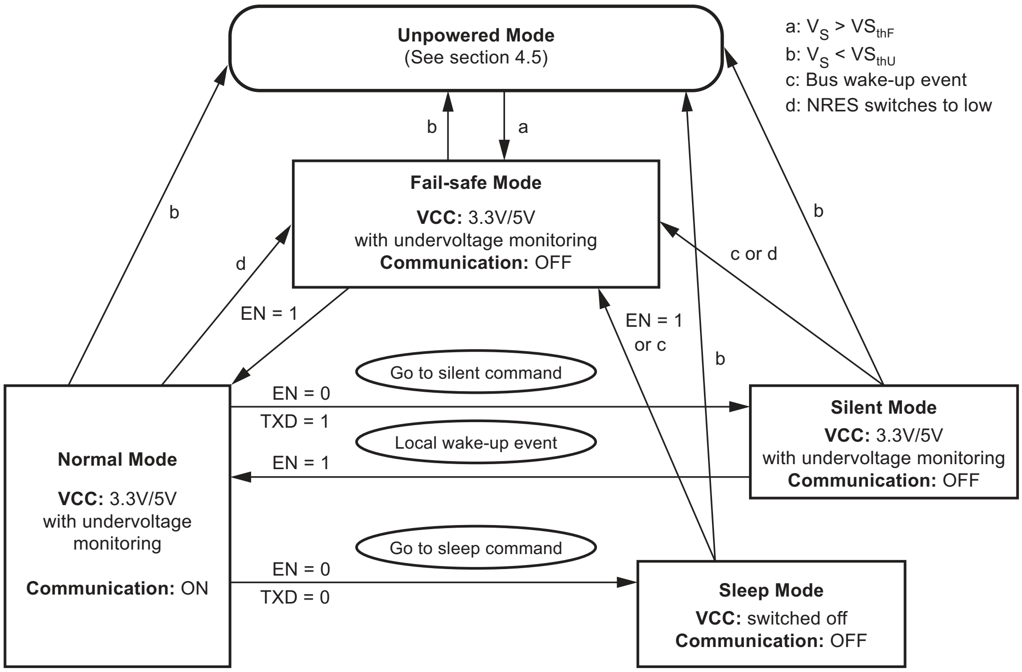


Table 4-1. Modes of Operation

Modes of Operation	Transceiver	V_{CC}	LIN
Fail safe	OFF	3.3V/5V	Recessive
Normal	ON	3.3V/5V	TXD depending
Silent	OFF	3.3V/5V	Recessive
Sleep	OFF	0V	Recessive

4.1 Normal Mode

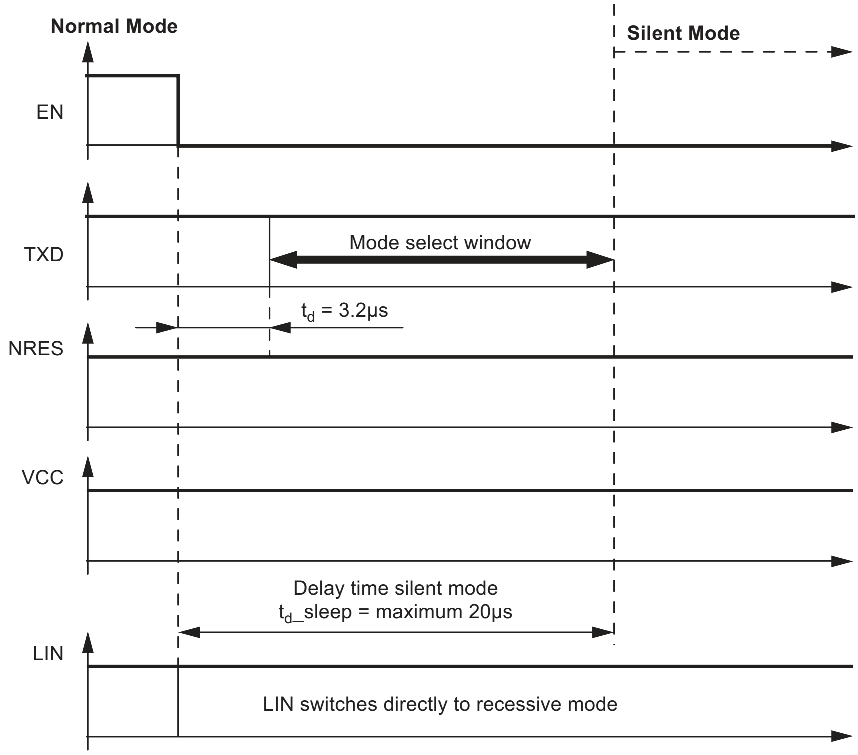
This is the normal transmitting and receiving mode of the LIN interface, in accordance with LIN specification 2.x. The V_{CC} voltage regulator operates with a 3.3V/5V output voltage, with a low tolerance of ±2% and a maximum output current of 85mA.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to fail-safe mode.

4.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into silent mode. The TXD signal has to be logic high during the mode select window (Figure 4-3 on page 8). The transmission path is disabled in silent mode. The overall supply current from V_{Batt} is a combination of the $I_{VSsilent}$ = 35µA plus the V_{CC} regulator output current I_{VCC}.

Figure 4-2. Switch to Silent Mode



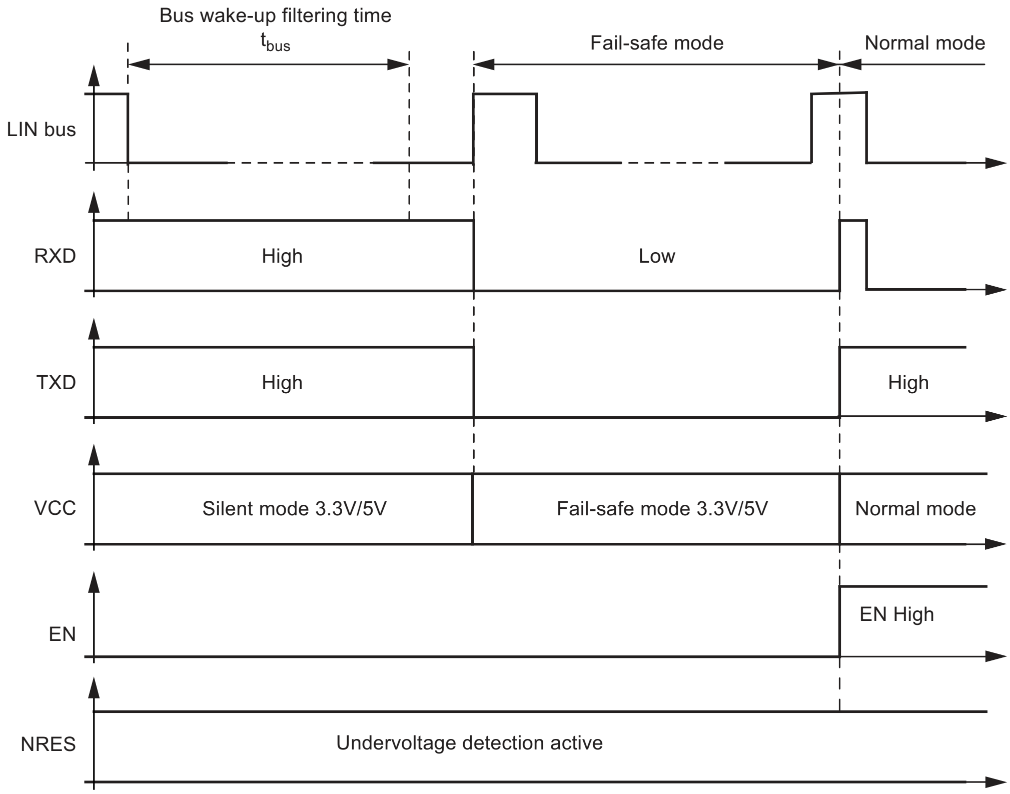
In silent mode the internal slave termination between pin LIN and pin VS is disabled to minimize the current consumption in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10µA) between pin LIN and pin VS is present. The silent mode can be activated independently from the current level on pin LIN.

If an undervoltage condition occurs, NRES is switched to low and the Atmel® ATA6629/ATA6631 changes its state to fail-safe mode.

A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and the following rising edge at pin LIN (see Figure 4-3) results in a remote wake-up request which is only possible if TXD is high. The device switches from silent mode to fail-safe mode, then the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD and TXD to interrupt the microcontroller (Figure 4-3). EN high can be used to switch directly to normal mode.

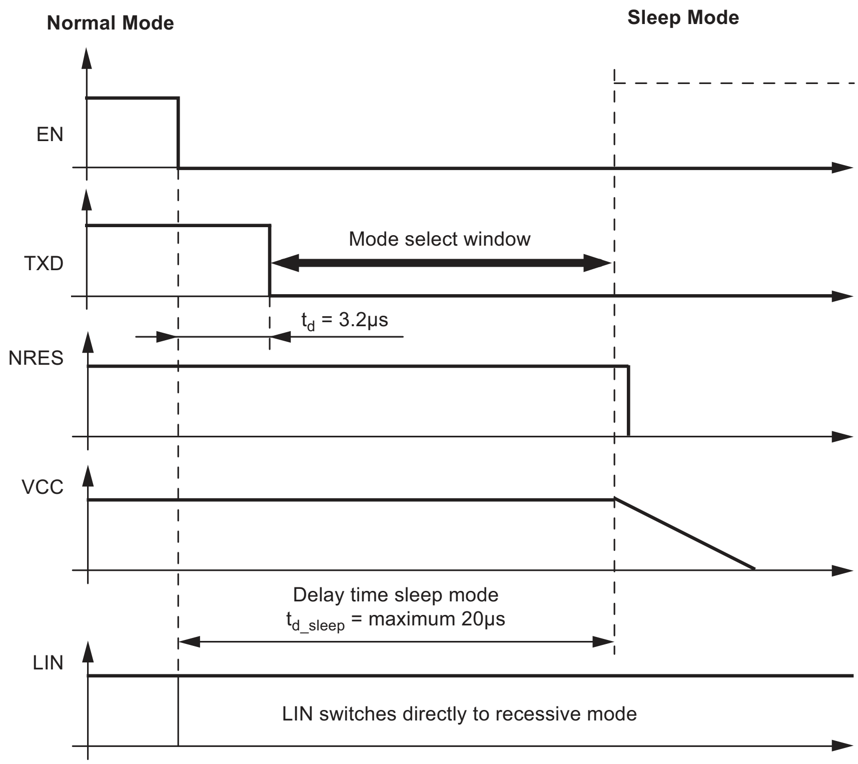
Figure 4-3. LIN Wake-up Waveform Diagram from Silent Mode



4.3 Sleep Mode

A falling edge at EN while TXD is low switches the IC into sleep mode. The TXD signal has to be logic low during the mode select window (Figure 4-5 on page 10).

Figure 4-4. Switch to Sleep Mode



In order to avoid any influence to the LIN-pin during switching into sleep mode it is possible to switch the EN up to 3.2µs earlier to low than the TXD. Therefore, the best an easiest way are two falling edges at TXD and EN at the same time.

In sleep mode the transmission path is disabled. Supply current from V_{Batt} is typically $I_{VSsleep}$ = 10µA. The V_{CC} regulator is switched off; NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled to minimize the current consumption in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10µA) between pin LIN and pin VS is present. The sleep mode can be activated independently from the current level on pin LIN.

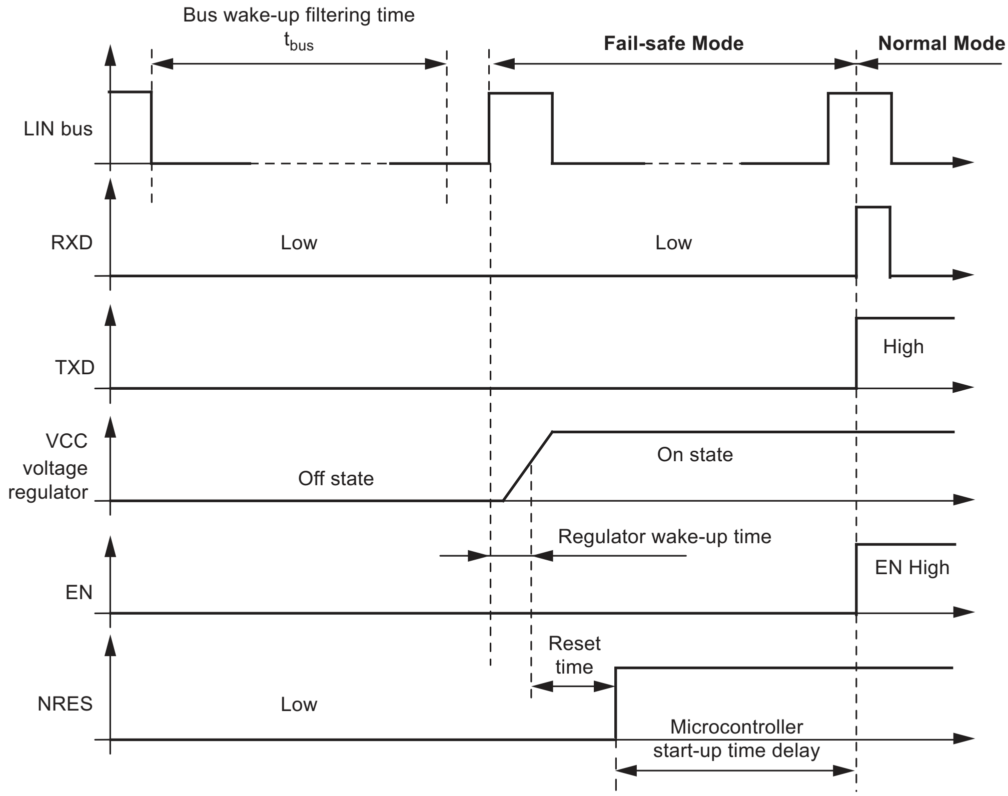
A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and a following rising edge at pin LIN results in a remote wake-up request. The device switches from sleep Mode to fail-safe mode.

The V_{CC} regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD and TXD to interrupt the microcontroller (Figure 4-5 on page 10).

EN high can be used to switch directly from sleep/silent to fail-safe mode. If EN is still high after VCC ramp up and undervoltage reset time, the IC switches to normal mode.

Figure 4-5. LIN Wake-up Diagram from Sleep Mode



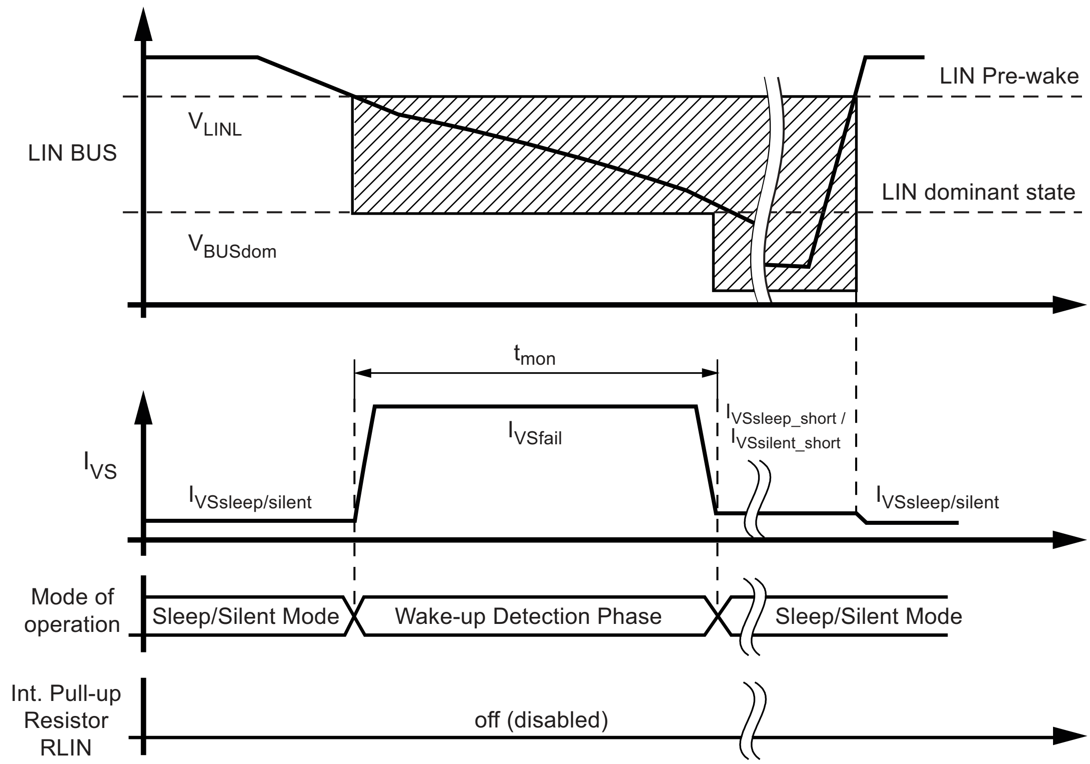
4.4 Sleep or Silent Mode: Behavior at a Floating LIN-bus or a Short Circuited LIN to GND

In sleep or in silent mode the device has a very low current consumption even during short-circuits or floating conditions on the bus. A floating bus can arise if the master pull-up resistor is missing, e.g., if it is switched off when the LIN- master is in sleep mode or even if the power supply of the master node is switched off.

In order to minimize the current consumption I_{VS} in sleep or silent mode during voltage levels at the LIN-pin below the LIN pre-wake threshold, the receiver is activated only for a specific time tmon. If t_{mon} elapses while the voltage at the bus is lower than pre-wake detection low (V_{LINL}) and higher than the LIN dominant level, the receiver is switched off again and the circuit changes back to sleep respectively silent mode. The current consumption is then $I_{VSsleep\_short}$ or $I_{VSsilent\_short}$ (typ. 10µA more than $I_{VSsleep}$ respectively $I_{VSsilent}$). If a dominant state is reached on the bus no wake-up will occur. Even if the voltage rises above the pre-wake detection high (V_{LINH}), the IC will stay in sleep respectively silent mode (see Figure 4-6 on page 11).

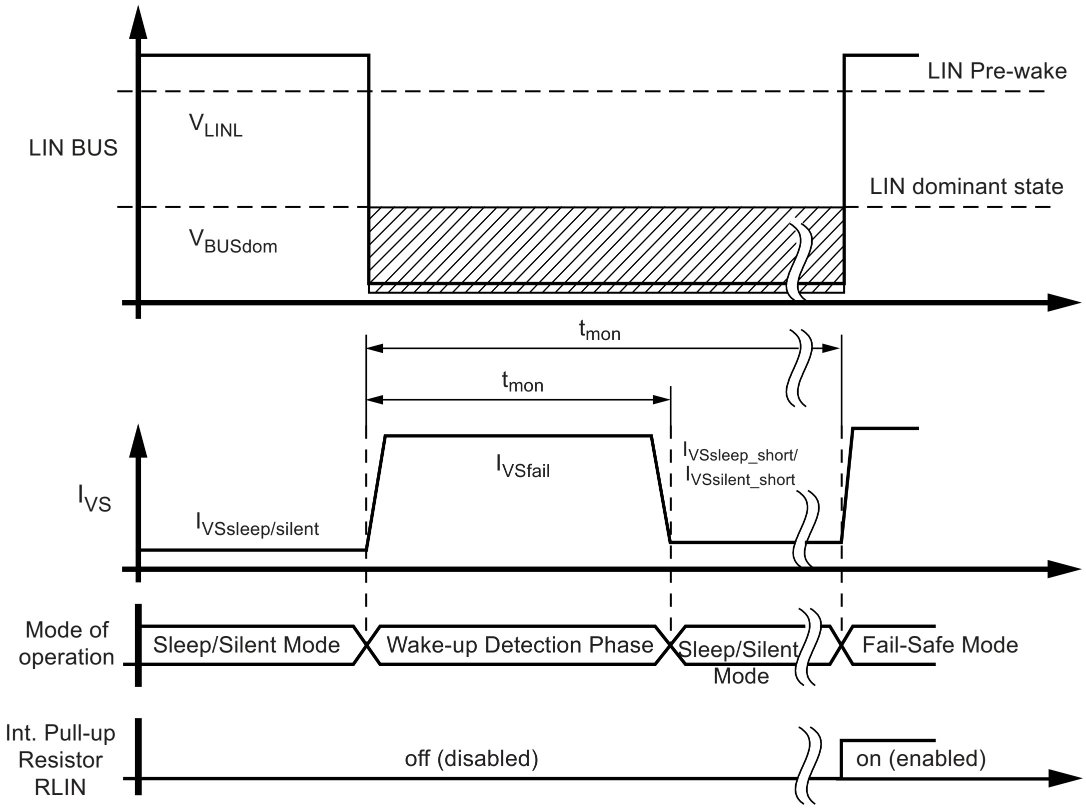
This means the LIN-bus must be above the pre-wake detection threshold V_{LINH} for a few microseconds before a new LIN wake-up is possible.

Figure 4-6. Floating LIN-bus During Sleep or Silent Mode



If the Atmel® ATA6629/ATA6631 is in sleep or silent mode and the voltage level at the LIN-bus is in dominant state ($V_{LIN} < V_{BUSdom}$) for a time period exceeding t_{mon} (during a short circuit at LIN, for example), the IC switches back to sleep mode respectively silent mode. The V_S current consumption then is $I_{VSsleep\_short}$ or $I_{VSsilent\_short}$ (typ. 10µA more than $I_{VSsleep}$ respectively $I_{VSsilent}$). After a positive edge at pin LIN the IC switches directly to fail-safe mode (see Figure 4-7 on page 12).

Figure 4-7. Short Circuit to GND on the LIN bus During Sleep- or Silent Mode



4.5 Fail-safe Mode

The device automatically switches to fail-safe mode at system power-up. The voltage regulator is switched on (see Figure 6-1 on page 15). The NRES output switches to low for t_{res} = 4ms and gives a reset to the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to normal mode. A power down of V_{Batt} ($V_S < VS_{th}$) during silent or sleep mode switches the IC into fail-safe mode after power up. A low at NRES switches the IC into fail-safe mode directly. During fail-safe mode the TXD pin is an output and signals the fail-safe source.

The LIN SBC can operate in different modes, like normal, silent or sleep mode. The functionality of these modes is described in Table 4-2.

Table 4-2. TXD, RXD Depending from Operation Modes

Different Modes	TXD	RXD
Fail-safe Mode	Signalling fail-safe sources (see Table 4-3)	
Normal Mode	Follows data transmission	
Silent Mode	High	High
Sleep Mode	Low	Low

A wake-up event from either silent or sleep mode will be signalled to the microcontroller using the two pins RXD and TXD. The coding is shown in Table 4-3.

A wake-up event will lead the IC to the fail-safe mode.

Table 4-3. Signalling Fail-safe Sources

Fail-safe Sources	TXD	RXD
LIN wake up (pin LIN)	Low	Low
VS_{th} (battery) undervoltage detection	High	Low

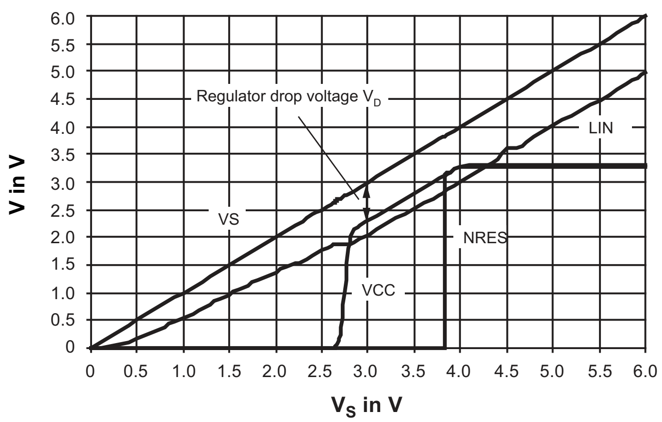
4.6 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Figure 6-1 on page 15). After VS is higher than the VS undervoltage threshold VS_{th}, the IC mode changes from unpowered mode to fail-safe mode. The VCC output voltage reaches its nominal value after t_{VCC}. This time, t_{VCC}, depends on the VCC capacitor and the load.

The NRES is low for the reset time delay t_{reset}. During this time, t_{reset}, no mode change is possible.

IF VS drops below VS_{th}, then the IC switches to unpowered mode. The behaviour of VCC, NRES and LIN is shown in Figure 4-8.

Figure 4-8. VCC versus VS for the VCC = 3.3V Regulator

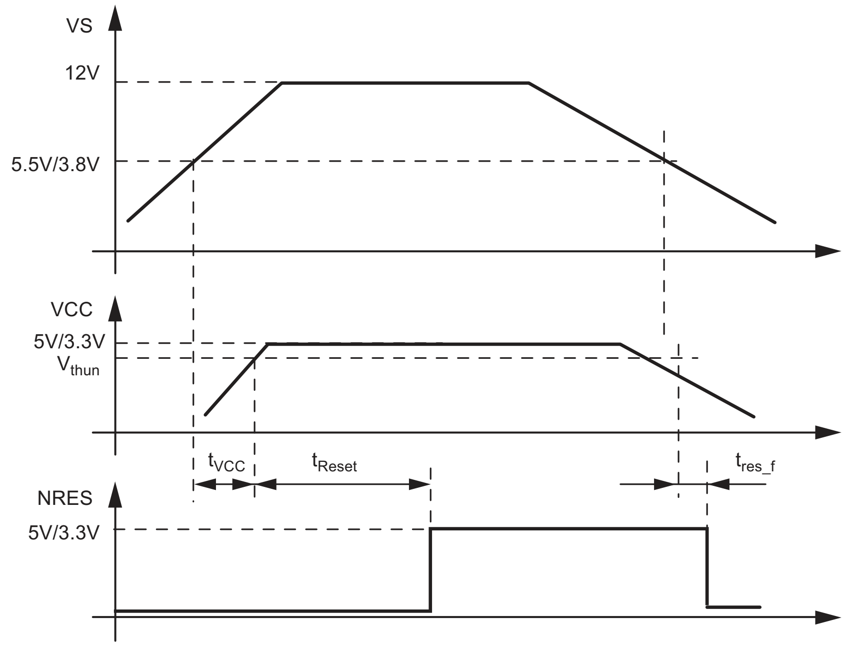


5. Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the V_{CC} regulator is working independently.
- During a short-circuit from LIN to GND the IC can be switched into sleep or Silent mode and even in this case the current consumption is lower than 30µA in sleep mode and lower than 70µA in silent mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- Sleep or silent mode: During a floating condition on the bus the IC switches back to sleep mode/silent mode automatically and thereby the current consumption is lower than 30µA/70µA.
- The reverse current is < 2µA at pin LIN during loss of V_{Batt} . This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into fail-safe mode. If the chip temperature exceeds the value T_{VCCoff}, the V_{CC} output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. Because of fail-safe mode, the V_{CC} voltage will switch on again although EN is switched off from the microcontroller.The microcontroller can then start with normal operation.
- Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- Pin RXD is set floating if V_{Batt} is disconnected.
- Pin TXD provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.
- After switching the IC into normal mode the TXD pin must be pulled to high longer than 10µs in order to activate the LIN driver. This feature prevents the bus from being driven into dominant state when the IC is switched into normal mode and TXD is low.
- If TXD is short-circuited to GND, it is possible to switch to sleep mode via ENABLE after t > tdom.

6. Voltage Regulator

Figure 6-1. V_{CC} **Voltage Regulator: Ramp Up and Undervoltage**



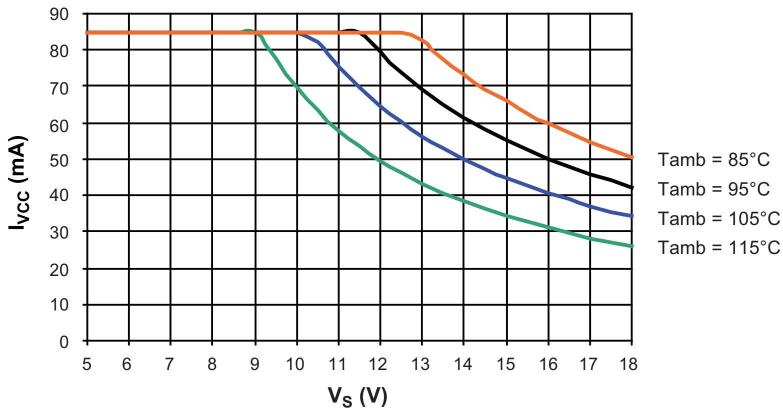
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use an electrolytic capacitor with C > 1.8µF and a ceramic capacitor with C = 100nF. The values of these capacitors can be varied by the customer, depending on the application.

With this special SO8 package (fused lead frame to pin 3) an R_{thja} of 80K/W is achieved.
Therefore, it is recommended to connect pin 3 with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the V_{CC} output current I_{VCC}, which is needed for the application.

Figure 6-2 shows the safe operating area of the Atmel® ATA6631.

Figure 6-2. Power Dissipation: Safe Operating Area: V_{CC} **Output Current versus Supply Voltage** V_S **at Different Ambient Temperatures Due to** R_{thja} **= 80K/W**



For programming purposes of the microcontroller, it is potentionally necessary to supply the V_{CC} output via an external power supply while the V_S Pin of the system basis chip is disconnected. This will not affect the system basis chip.

7. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500ms T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			+40	V
Pulse time ≤ 2 min T_a = 25°C Output current I_{VCC} ≤ 85mA	V_S			27	V
Logic pins (RxD, TxD, EN, NRES)		–0.3		+5.5	V
Output current NRES	I_{NRES}			+2	mA
LIN - DC voltage		–27		+40	V
V_{CC} - DC voltage		–0.3		+5.5	V
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND		±8			KV
ESD HBM following STM5.1 with 1.5 kΩ/100 pF - Pin VS, LIN to GND		±6			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine model ESD AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

8. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to ambient (free air)	R_{thja}			145	K/W
Special heat sink at GND (pin 3) on PCB	R_{thja}		80		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	160	170	°C
Thermal shutdown of LIN output	T_{LINoff}	150	160	170	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

9. Electrical Characteristics

$5V < V_S < 27V$, $-40°C < T_j < 150°C$; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	Vs pin								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	27	V	A
1.2	Supply current in sleep mode	Sleep mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$	VS	$I_{VSsleep}$	2	10	14	µA	A
		Sleep mode, $V_{LIN} = 0V$ Bus shorted to GND $V_S < 14V$	VS	$I_{VSsleep\_short}$	3	20	30	µA	A
1.3	Supply current in silent mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	$I_{VSsilent}$	20	35	50	µA	A
		Silent mode $V_S < 14V$ Bus shorted to GND Without load at VCC	VS	$I_{VSsilent\_short}$	25	45	70	µA	A
1.4	Supply current in normal mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	I_{VSrec}	0.3		0.8	mA	A
1.5	Supply current in normal mode	Bus dominant $V_S < 14V$ V_{CC} load current 50mA	VS	I_{VSdom}	50		53	mA	A
1.6	Supply current in fail-safe mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	I_{VSfail}	0.35		0.53	mA	A
1.7	VS undervoltage threshold	Switch to unpowered mode	VS	V_{SthU}	3.7	4.2	4.7	V	A
		Switch to fail-safe mode	VS	V_{SthF}	4.0	4.5	5	V	A
1.8	VS undervoltage hysteresis		VS	V_{Sth_hys}		0.3		V	A
2	RXD output pin								
2.1	Low level output sink current	Normal Mode $V_{LIN} = 0V$, $V_{RXD} = 0.4V$	RXD	I_{RXD}	1.3	2.5	8	mA	A
2.2	Low level output voltage	$I_{RXD} = 1mA$	RXD	V_{RXDL}			0.4	V	A
2.3	Internal resistor to V_{CC}		RXD	R_{RXD}	3	5	7	kΩ	A
3	TXD input/output pin								
3.1	Low level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High level voltage input		TXD	V_{TXDH}	2		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	$V_{TXD} = 0V$	TXD	R_{TXD}	125	250	400	kΩ	A
3.4	High level leakage current	$V_{TXD} = V_{CC}$	TXD	I_{TXD}	–3		+3	µA	A
3.5	Low level output sink current at local wake-up request	Fail-safe Mode $V_{LIN} = V_S$ $V_{WAKE} = 0V$ $V_{TXD} = 0.4V$	TXD	$I_{TXDwake}$	2	2.5	8	mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	EN input pin								
4.1	Low level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High level voltage input		EN	V_{ENH}	2		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = VCC	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	NRES open drain output pin								
5.1	Low level output voltage	V_S ≥ 5.5V I_{NRES} = 1mA	NRES	V_{NRESL}			0.14	V	A
5.2	Low level output low	10 kΩ to 5V V_{CC} = 0V	NRES	V_{NRESLL}			0.2	V	A
5.3	Undervoltage reset time	V_{VS} ≥ 5.5V C_{NRES} = 20pF	NRES	t_{Reset}	2	4	6	ms	A
5.4	Reset debounce time for falling edge	V_{VS} ≥ 5.5V C_{NRES} = 20pF	NRES	t_{res_f}	1.5		10	µs	A
5.5	Switch off leakage current	V_{NRES} = 5.5V	NRES		–3		+3	µA	A
6	VCC Voltage Regulator Atmel ATA6629								
6.1	Output voltage VCC	4V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	3.234		3.366	V	A
		4.5V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	3.234		3.366	V	C
6.2	Output voltage V_{CC} at low V_S	3V < VS < 4V	VCC	VCC_{low}	V_{VS} – V_{Drop}		3.366	V	A
6.3	Regulator drop voltage	VS > 3V, I_{VCC} = –15mA	VCC	V_{D1}			200	mV	A
6.4	Regulator drop voltage	VS > 3V, I_{VCC} = –50mA	VCC	V_{D2}		500	700	mV	A
6.5	Line regulation maximum	4V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
6.6	Load regulation maximum	5 mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
6.7	Power supply ripple rejection	10 Hz to 100kHz C_{VCC} = 10µF VS = 14V, I_{VCC} = –15mA			50			dB	D
6.8	Output current limitation	VS > 4V	VCC	I_{VCCs}	–240	–160	–85	mA	A
6.9	External load capacity	0.2Ω < ESR < 5Ω at 100kHz for phase margin ≥ 60° ESR < 0.2Ω at 100kHz for phase margin ≥ 30°	VCC	C_{load}	1.8	10		µF	D
6.10	VCC undervoltage threshold	Referred to VCC VS > 4V	VCC	V_{thunN}	2.8		3.2	V	A
6.11	Hysteresis of undervoltage threshold	Referred to VCC VS > 4V	VCC	$Vhys_{thun}$		150		mV	A
6.12	Ramp up time VS > 4V to VCC = 3.3V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	t_{VCC}		320	500	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	VCC voltage regulator Atmel ATA6631								
7.1	Output voltage VCC	5.5V < V_S < 18V (0mA to 50mA)	VCC	VCC_{nor}	4.9		5.1	V	A
		6V < V_S < 18V (0mA to 85mA)	VCC	VCC_{nor}	4.9		5.1	V	C
7.2	Output voltage V_{CC} at low V_S	4V < VS < 5.5V	VCC	VCC_{low}	$V_{VS} – V_D$		5.1	V	A
7.3	Regulator drop voltage	VS > 4V, I_{VCC} = –20mA	VCC	V_{D1}			250	mV	A
7.4	Regulator drop voltage	VS > 4V, I_{VCC} = –50mA	VCC	V_{D2}		400	600	mV	A
7.5	Regulator drop voltage	VS > 3.3V, I_{VCC} = –15mA	VCC	V_{D3}			200	mV	A
7.6	Line regulation maximum	5.5V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
7.7	Load regulation maximum	5 mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
7.8	Power supply ripple rejection	10Hz to 100kHz C_{VCC} = 10µF VS = 14V, I_{VCC} = –15mA			50			dB	D
7.9	Output current limitation	VS > 5.5V	VCC	I_{VCCs}	–240	–160	–85	mA	A
7.10	External load capacity	0.2Ω < ESR < 5Ω at 100kHz for phase margin ≥ 60°	VCC	C_{load}	1.8	10		µF	D
		ESR < 0.2Ω at 100kHz for phase margin ≥ 30°							
7.11	VCC undervoltage threshold	Referred to VCC VS > 5.5V	VCC	V_{thunN}	4.2		4.8	V	A
7.12	Hysteresis of undervoltage threshold	Referred to VCC VS > 5.5V	VCC	$Vhys_{thun}$		250		mV	A
7.13	Ramp up time VS > 5.5V to VCC = 5V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	T_{VCC}		320	500	µs	A
8	LIN bus driver: bus load conditions: load 1 (Small): 1nF, 1kΩ; load 2 (large): 10nF, 500Ω; internal pull-up RRXD = 5kΩ ; CRXD = 20pF, Load 3 (medium): 6.8nF, 660Ω characterized on samples 10.7 and 10.8 specifies the timing parameters for proper operation at 20kBit/s and 10.9 and 10.10 at 10.4kBit/s								
8.1	Driver recessive output voltage	Load1/load2	LIN	V_{BUSrec}	$0.9 \times V_S$		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
8.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
8.4	Driver dominant voltage	V_{VS} = 7V R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A
8.6	Pull–up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
8.8	LIN current limitation $V_{BUS} = V_{Batt\_max}$		LIN	I_{BUS_LIM}	40	120	200	mA	A
8.9	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V V_{Batt} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
8.10	Leakage current LIN recessive	Driver off 8V < V_{Batt} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
8.11	Leakage current when control unit disconnected from ground. loss of local ground must not affect communication in the residual network	$GND_{Device} = V_S$ V_{Batt} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
8.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Batt} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
8.13	Capacitance on pin LIN to GND		LIN	C_{LIN}			20	pF	D
9	LIN bus receiver								
9.1	Center of receiver threshold	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
9.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
9.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
9.4	Receiver input hysteresis	$V_{hys} = V_{th\_rec} - V_{th\_dom}$	LIN	V_{BUShys}	0.028 × V_S	0.1 x V_S	0.175 × V_S	V	A
9.5	Pre-wake detection LIN High level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
9.6	Pre-wake detection LIN Low level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A
10	Internal Timers								
10.1	Dominant time for wake–up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	30	90	150	µs	A
10.2	Time delay for mode change from fail-safe into normal mode via pin EN	V_{EN} = 5V	EN	t_{norm}	5	15	20	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

$5V < V_S < 27V$, $-40°C < T_j < 150°C$; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.3	Time delay for mode change from normal mode to sleep mode via pin EN	V_{EN} = 0V	EN	t_{sleep}	8	16	25	µs	A
10.4	TXD dominant time out time	V_{TXD} = 0V	TXD	t_{dom}	27	55	70	ms	A
10.5	Time delay for mode change from silent mode into normal mode via EN	V_{EN} = 5V	EN	t_{s_n}	5	15	40	µs	A
10.6	Monitoring time for wake-up over LIN bus		LIN	t_{mon}	6	10	15	ms	A
10.7	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 50µs $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				A
10.8	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 50µs $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		A
10.9	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96µs $D3 = t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
10.10	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 96µs $D4 = t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
10.11	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
11	Receiver electrical AC parameters of the LIN physical layer LIN receiver, RXD load conditions: internal pull-up; CRXD = 20pF								
11.1	Propagation delay of receiver Figure 9-1 on page 22	V_S = 7.0V to 18V $t_{rx\_pd} = max(t_{rx\_pdr}, t_{rx\_pdf})$	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	RXD	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 9-1. Definition of Bus Timing Characteristics

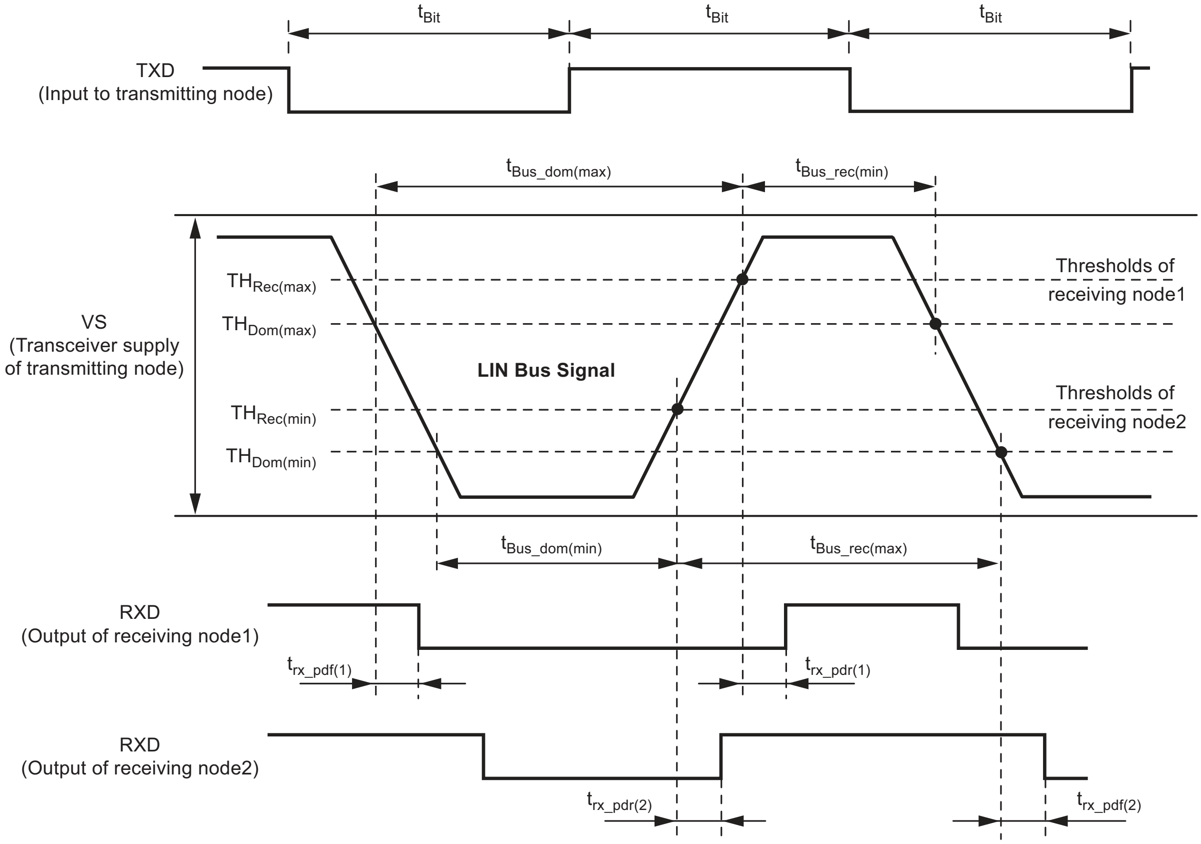
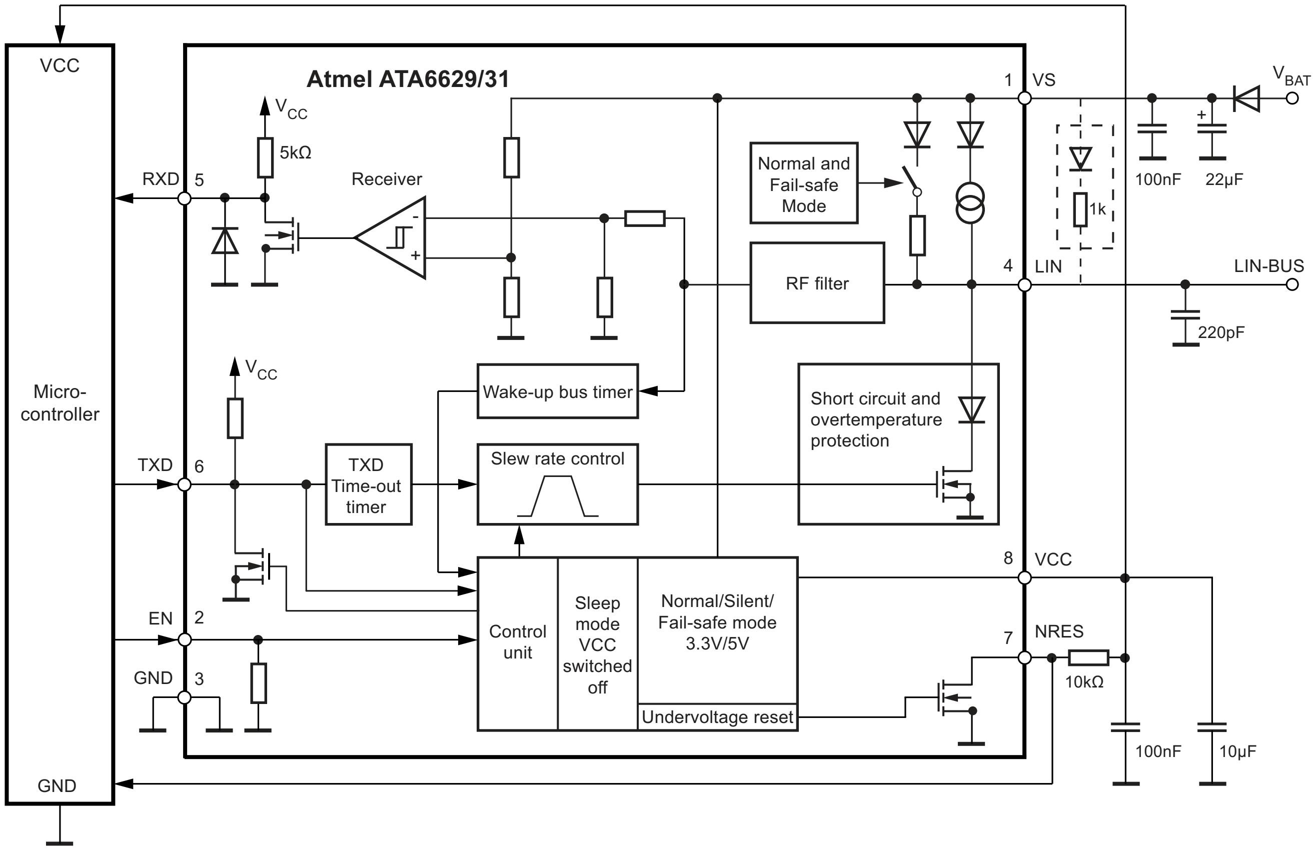


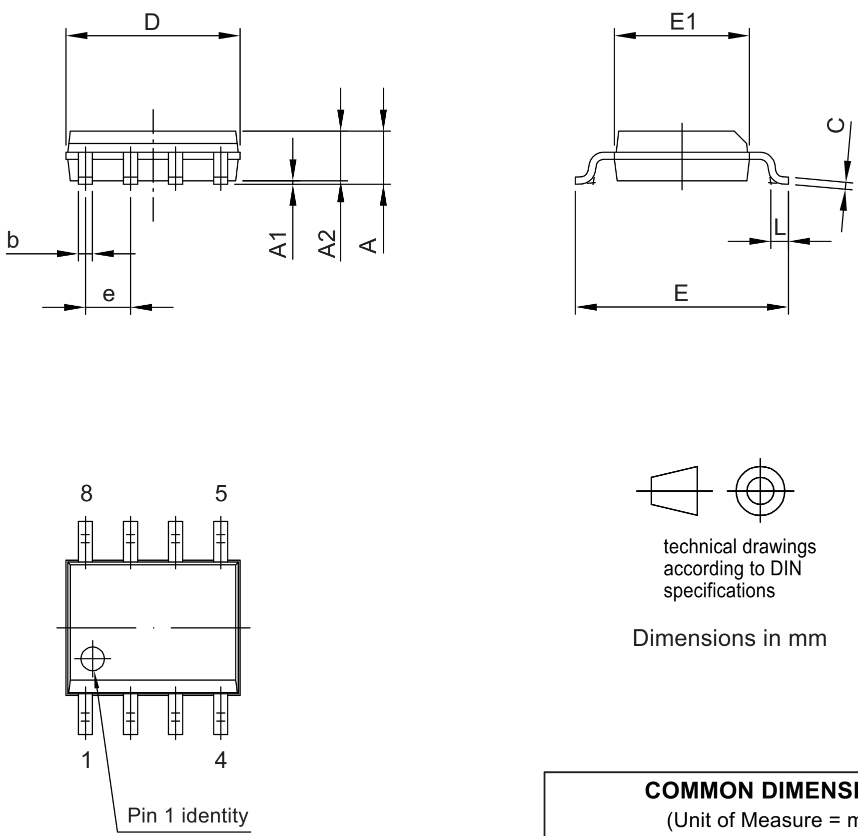
Figure 9-2. Application Circuit



10. Ordering Information

Extended Type Number	Package	Remarks
ATA6629-GAQW	SO8	3.3V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6631-GAQW	SO8	5V LIN system basis chip, Pb-free, 4k, taped and reeled

11. Package Information



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	1.5	1.65	1.8	
A1	0.1	0.15	0.25	
A2	1.4	1.47	1.55	
D	4.8	4.9	5	
E	5.8	6	6.2	
E1	3.8	3.9	4	
L	0.4	0.65	0.9	
C	0.15	0.2	0.25	
b	0.3	0.4	0.5	
e		1.27 BSC		

05/08/14

Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**TITLE** **Package: SO8**	**GPC**	**DRAWING NO.**	**REV.**
			6.543-5185.01-4	1

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9165F-AUTO-10/14	• Put datasheet in the latest template • Section 10 “Ordering Information” on page 24 updated • Section 11 “Package Information” on page 25 updated
9165E-AUTO-04/14	• Put datasheet in the latest template
9165D-AUTO-03/11	• Features on page 1 changed • Section 1 “Description” on pages 1 to 2 changed • Section 3 “Functional Description” on pages 3 to 4 changed • Section 4 “Modes of Operation” on pages 5 to 12 changed • Section 5 “Fail-safe Features” on page 13 changed • Section 6 “Voltage Regulator” on pages 14 to 15 changed • Section 7 “Absolute Maximum Ratings” on page 16 changed • Section 9 “Electrical Characteristics” on pages 17 to 23 changed
9165C-AUTO-10/10	• Section 9 “Electrical Characteristics” numbers 1.7 on page 17 and 10.3 on page 20 changed
9165B-AUTO-05/10	• Features on page 1 changed •Text under heading 3.3 changed •Text under heading 4.2 changed •Abs.Max.Rat.Table -> Values in row “ESD HBM following....” changed • El.Char.Table -> rows changed: 1.2, 1.3, 5.1, 5.2, 6.5, 6.6, 6.7, 6.8, 6.12, 7.6, 7.7, 7.8, 7.9, 7.13 • El.Char.Table -> row 8.13 added

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