# Product Datasheet

## DAC-Q28-S28-3.5M-C

### Huawei® Compatible 100Gb/s QSFP28 to 4SFP28 Breakout Direct Attach Cable Copper, Passive, 3.5m

#### FEATURES

- Compatible with IEEE 802.3bj, IEEE 802.3by and InfiniBand EDR
- Supports aggregate data rates of 100Gbps
- Optimized construction to minimize insertion loss and cross talk
- Backward compatible with existing QSFP+ connectors and cages
- Pull-to-release slide latch design
- 26AWG through 30AWG cable
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Customizable EEPROM mapping for cable signature
- RoHS compliant

#### APPLICATIONS

- Switches, servers and routers
- Data Center networks

#### STORAGE AREA NETWORKS

- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment

#### INDUSTRIAL STANDARDS

- 100G Ethernet (IEEE 802.3bj)
- 25G Ethernet (IEEE 802.3by)
- InfiniBand EDR
- SFF-8665 QSFP+ 28G 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8402 SFP+ 1X 28Gb/s Pluggable Transceiver Solution (SFP28)

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## DESCRIPTION

ATGBICS QSFP28 passive copper cable assembly feature eight differential copper pairs, providing four data transmission channels at speeds up to 28Gbps per channel, and meets 100G Ethernet,25G Ethernet and InfiniBand Enhanced Data Rate (EDR) requirements. Available in a broad range of wire gages-from 26AWG through 30AWG-this 100G copper cable assembly features low insertion loss and low cross talk.

Designed for applications in the data center, networking and telecommunications markets that require a high speed, reliable cable assembly, this next generation product shares the same mating interface with QSFP+ form factor, making it backward compatible with existing QSFP ports. QSFP28 can be used with current 10G and 14G applications with substantial signal integrity margin.

### High Speed Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| **Differential Impedance** | TDR | 90 | 100 | 110 | Ω | |
| **Insertion loss** | SDD21 | -22.48 | | | dB | At 12.8906 GHz |
| **Differential Return Loss** | SDD11 | | | See 1 | dB | At 0.05 to 4.1 GHz |
| | SDD22 | | | See 2 | dB | At 4.1 to 19 GHz |
| **Common-mode to common-mode output return loss** | SCC11<br>SCC22 | | | -2 | dB | At 0.2 to 19 GHz |
| **Differential to common mode return loss** | SCD11<br>SCD22 | | | See 3 | dB | At 0.01 to 12.89 GHz |
| | | | | See 4 | | At 12.89 to 19 GHz |
| **Differential to common Mode Conversion Loss** | SCD21-IL | | | -10 | dB | At 0.01 to 12.89 GHz |
| | | | | See 5 | | At 12.89 to 15.7 GHz |
| | | | | -6.3 | | At 15.7 to 19 GHz |

**Notes:**

1. Reflection Coefficient given by equation SDD11(dB) < -16.5 + 2 × SQRT(f), with f in GHz
2. Reflection Coefficient given by equation SDD11(dB) < -10.66 + 14 × log10(f/5.5), with f in GHz
3. Reflection Coefficient given by equation SCD11(dB) < -22 + (20/25.78) * f, with f in GHz
4. Reflection Coefficient given by equation SCD11(dB) < -15 + (6/25.78) * f, with f in GHz
5. Reflection Coefficient given by equation SCD21(dB) < -27 + (29/22) * f, with f in GHz

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## QSFP28 Pin Function Definition

| Pin | Logic | Symbol | Description |
|---|---|---|---|
| 1 | | GND | Ground |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input |
| 4 | | GND | Ground |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input |
| 7 | | GND | Ground |
| 8 | LVTTL-I | ModSelL | Module Select |
| 9 | LVTTL-I | ResetL | Module Reset |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data |
| 13 | | GND | Ground |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output |
| 16 | | GND | Ground |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output |
| 19 | | GND | Ground |
| 20 | | GND | Ground |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output |
| 23 | | GND | Ground |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output |
| 26 | | GND | Ground |
| 27 | LVTTL-O | ModPrsL | Module Present |
| 28 | LVTTL-O | IntL | Interrupt |
| 29 | | Vcc Tx | +3.3V Power supply transmitter |
| 30 | | Vcc1 | +3.3V Power supply |
| 31 | LVTTL-I | LPMode | Low Power Mode |
| 32 | | GND | Ground |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input |
| 35 | | GND | Ground |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input |
| 38 | | GND | Ground |

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## QSFP+ Pin Function Definition

| Pin | Logic | Symbol | Description |
|---|---|---|---|
| 1 | | GND | Ground |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input |
| 4 | | GND | Ground |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input |
| 7 | | GND | Ground |
| 8 | LVTTL-I | ModSelL | Module Select |
| 9 | LVTTL-I | ResetL | Module Reset |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data |
| 13 | | GND | Ground |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output |
| 16 | | GND | Ground |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output |
| 19 | | GND | Ground |
| 20 | | GND | Ground |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output |
| 23 | | GND | Ground |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output |
| 26 | | GND | Ground |
| 27 | LVTTL-O | ModPrsL | Module Present |
| 28 | LVTTL-O | IntL | Interrupt |
| 29 | | Vcc Tx | +3.3V Power supply transmitter |
| 30 | | Vcc1 | +3.3V Power supply |

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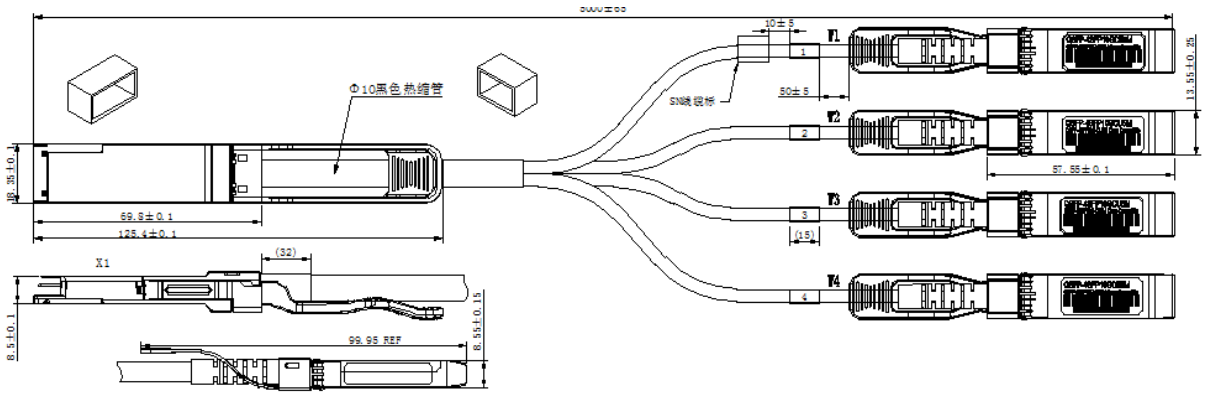
| | | | |
|---|---|---|---|
| **31** | LVTTL-I | LPMode | Low Power Mode |
| **32** | | GND | Ground |
| **33** | CML-I | Tx3p | Transmitter Non-Inverted Data Input |
| **34** | CML-I | Tx3n | Transmitter Inverted Data Input |
| **35** | | GND | Ground |
| **36** | CML-I | Tx1p | Transmitter Non-Inverted Data Input |
| **37** | CML-I | Tx1n | Transmitter Inverted Data Input |
| **38** | | GND | Ground |

## Mechanical Information

The connector is compatible with the SFF-8436 specification




| Length (m) | Cable AWG |
|---|---|
| 1 | 30 |
| 2 | 30 |
| 3 | 26/30 |
| 4 | 26 |
| 5 | 26 |

## General Product Characteristics

| Q/4SFP+ DAC Specifications | |
|---|---|
| **Number of Lanes** | Tx & Rx |
| **Channel Data Rate** | 10.3125 Gbps |
| **Operating Temperature** | 0 to + 70°C |
| **Storage Temperature** | -40 to + 85°C |
| **Supply Voltage** | 3.3 V nominal |
| **Electrical Interface** | 38 pins edge connector (QSFP+)<br>20 pins edge connector (SFP+) |
| **Management Interface** | Serial, I2C |

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## Regulatory Compliance

| Feature | Test Method | Performance |
|---|---|---|
| **Electrostatic Discharge (ESD) to the Electrical Pins** | MIL-STD-883C Method 3015.7 | Class 1 (>2000 Volts) |
| **Electromagnetic Interference (EMI)** | FCC Class B | Compliant with Standards |
| | CENELEC EN55022 Class B | |
| | CISPR22 ITE Class B | |
| **RF Immunity (RFI)** | IEC61000-4-3 | Typically Show no Measurable Effect from a 10V/m Field Swept from 80 to 1000MHz |
| **RoHS Compliance** | RoHS Directive 2011/65/EU and it's Amendment Directives （EU） 2015/863 | RoHS （EU）2015/863 compliant |
| **REACH Compliance** | REACH Regulation (EC) No 1907/2006 | REACH (EC) No 1907/2006 compliant |