S-8211E Series

BATTERY PROTECTION IC FOR 1-CELL PACK

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Rev.2.4_03

The S-8211E Series has high-accuracy voltage detections circuit and delay circuits.
The S-8211E Series is suitable for monitoring overcharge and overdischarge of 1-cell lithium ion / lithium polymer rechargeable battery pack.

■ Features

(1) High-accuracy voltage detection circuit

• Overcharge detection voltage	3.6 V to 4.5 V (5 mV step)	Accuracy ±25 mV (+25°C) Accuracy ±30 mV (–5°C to +55°C)
• Overcharge release voltage	3.5 V to 4.4 V*1	Accuracy ±50 mV
• Overdischarge detection voltage	2.0 V to 3.0 V (10 mV step)	Accuracy ±50 mV
• Overdischarge release voltage	2.0 V to 3.4 V*2	Accuracy ±100 mV

(2) Detection delay times are generated by an internal circuit (external capacitors are unnecessary) — Accuracy ±20%

(3) Wide operating temperature range — –40°C to +85°C

(4) Low current consumption

• During operation	3.0 μA typ., 5.5 μA max. (+25°C)
• During overdischarge	2.0 μA typ., 3.5 μA max. (+25°C)

(5) Output logic of CO pin is selectable. — Active “H”, Active “L”

(6) Lead-free, Sn 100%, halogen-free*3

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)

***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

***3.** Refer to “■ **Product Name Structure**” for details.

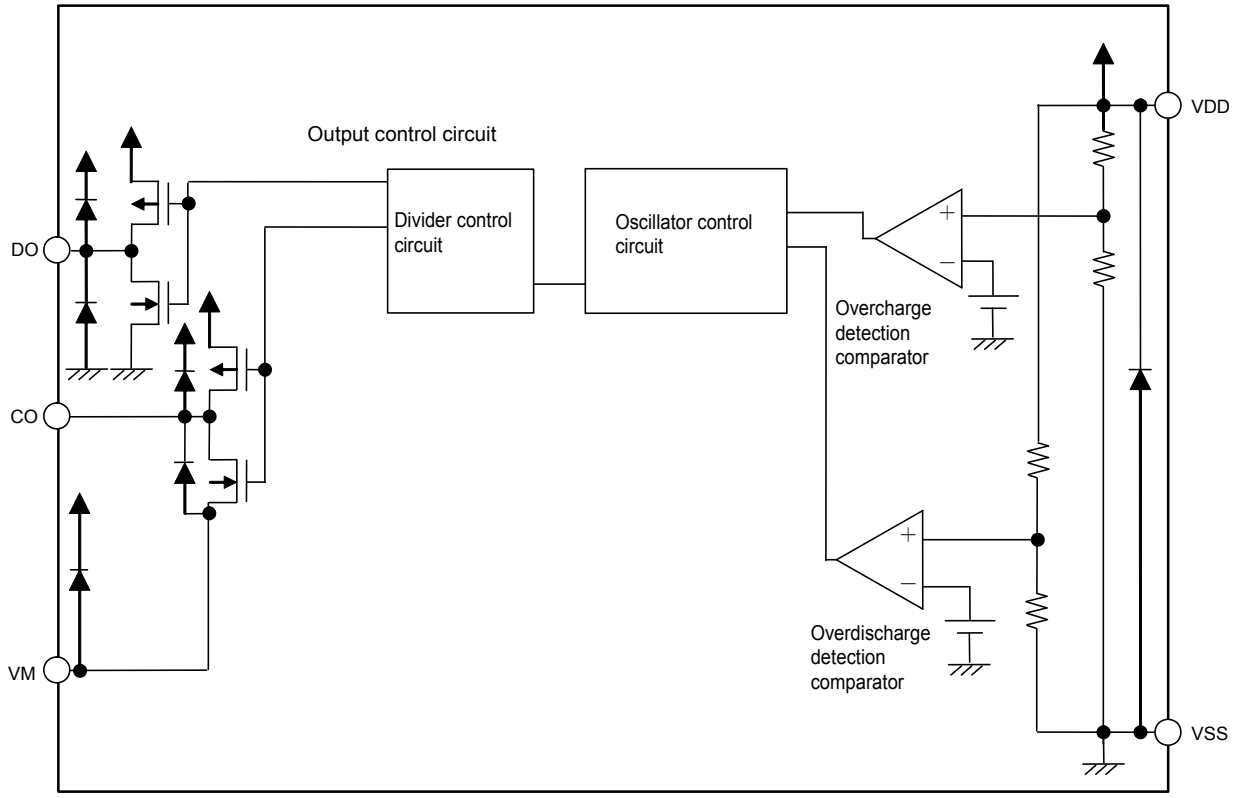
■ Applications

- Lithium-ion rechargeable battery pack
- Lithium-polymer rechargeable battery pack

■ Packages

- SOT-23-5
- SNT-6A

■ Block Diagram



Remark All diodes shown in figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product Name

S-8211E xx - xxxx U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package name (abbreviation) and IC packing specifications*1
M5T1: SOT-23-5, Tape
I6T1: SNT-6A, Tape

Serial code*2
Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product Name List

3. 1 SOT-23-5

Table 1

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Delay Time Combination*1	CO Pin Output Form
S-8211EAC-M5T1U	3.600 V	3.600 V	2.00 V	2.00 V	(1)	CMOS output active “L”
S-8211EAF-M5T1U	3.650 V	3.550 V	2.00 V	2.30 V	(2)	CMOS output active “L”
S-8211EAG-M5T1U	3.800 V	3.600 V	2.00 V	2.30 V	(2)	CMOS output active “L”
S-8211EAJ-M5T1U	4.180 V	4.180 V	2.50 V	3.00 V	(1)	CMOS output active “H”
S-8211EAK-M5T1U	3.600 V	3.600 V	2.00 V	2.30 V	(1)	CMOS output active “H”

***1.** Refer to the **Table 3** about the details of the delay time combinations (1), (2).

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

3. 2 SNT-6A

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Delay Time Combination*1	CO Pin Output Form
S-8211EAA-I6T1U	4.220 V	4.220 V	2.00 V	2.00 V	(2)	CMOS output active “L”
S-8211EAB-I6T1U	4.270 V	4.270 V	2.00 V	2.00 V	(2)	CMOS output active “L”
S-8211EAD-I6T1U	4.220 V	4.220 V	2.50 V	2.50 V	(2)	CMOS output active “L”
S-8211EAE-I6T1U	4.220 V	4.220 V	2.30 V	2.30 V	(2)	CMOS output active “L”
S-8211EAH-I6T1U	4.000 V	3.800 V	3.00 V	3.20 V	(1)	CMOS output active “L”
S-8211EAI-I6T1U	3.800 V	3.700 V	2.30 V	2.40 V	(1)	CMOS output active “L”
S-8211EAP-I6T1U	4.280 V	4.080 V	2.50 V	2.50 V	(1)	CMOS output active “L”

***1.** Refer to the **Table 3** about the details of the delay time combinations (1), (2).

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

Table 3

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]
(1)	1.2 s	150 ms
(2)	573 ms	300 ms

Remark The delay times can be changed within the range listed **Table 4**. For details, please contact our sales office.

Table 4

Delay Time	Symbol	Selection Range			Remark
Overcharge detection delay time	t_{CU}	143 ms	573 ms	1.2 s	Select a value from the left.
Overdischarge detection delay time	t_{DL}	38 ms	150 ms	300 ms	Select a value from the left.

Remark The value surrounded by bold lines is the delay time of the standard products.

■ Pin Configurations

1. SOT-23-5

SOT-23-5
Top view

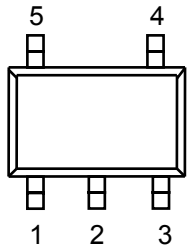


Figure 2

Table 5

Pin No.	Symbol	Description
1	VM	Negative power supply input pin for CO pin
2	VDD	Input pin for positive power supply
3	VSS	Input pin for negative power supply
4	DO	Output pin for overdischarge detection (CMOS output)
5	CO	Output pin for overcharge detection (CMOS output)

2. SNT-6A

SNT-6A
Top view

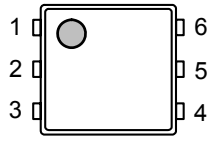


Figure 3

Table 6

Pin No.	Symbol	Description
1	NC*1	No connection
2	CO	Output pin for overcharge detection (CMOS output)
3	DO	Output pin for overdischarge detection (CMOS output)
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VM	Negative power supply input pin for CO pin

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD pin or VSS pin.

■ Absolute Maximum Ratings

Table 7

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied pin	Absolute Maximum Ratings	Unit
Input voltage between VDD pin and VSS pin		V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 12	V
VM pin input voltage		V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin output voltage		V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin output voltage		V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3	V
Power dissipation	SOT-23-5	P_D	−	600[*1]	mW
	SNT-6A		−	400[*1]	mW
Operating ambient temperature		T_{opr}	−	−40 to +85	°C
Storage temperature		T_{stg}	−	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

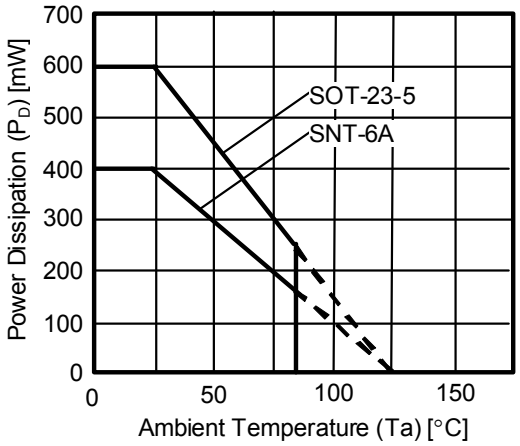


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Except Detection Delay Time (+25°C)

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE									
Overcharge detection voltage	V_{CU}	3.60 V to 4.50 V, Adjustable		V_{CU} −0.025	V_{CU}	V_{CU} +0.025	V	1	1
		3.60 V to 4.50 V, Adjustable, Ta = −5°C to +55°C*1		V_{CU} −0.03	V_{CU}	V_{CU} +0.03	V	1	1
Overcharge release voltage	V_{CL}	3.50 V to 4.40 V, Adjustable	$V_{CL} \neq V_{CU}$	V_{CL} −0.05	V_{CL}	V_{CL} +0.05	V	1	1
			$V_{CL} = V_{CU}$	V_{CL} −0.05	V_{CL}	V_{CL} +0.025	V	1	1
Overdischarge detection voltage	V_{DL}	2.00 V to 3.00 V, Adjustable		V_{DL} −0.05	V_{DL}	V_{DL} +0.05	V	2	2
Overdischarge release voltage	V_{DU}	2.00 V to 3.40 V, Adjustable	$V_{DU} \neq V_{DL}$	V_{DU} −0.10	V_{DU}	V_{DU} +0.10	V	2	2
			$V_{DU} = V_{DL}$	V_{DU} −0.05	V_{DU}	V_{DU} +0.05	V	2	2
INPUT VOLTAGE									
Operating voltage between VDD pin and VSS pin	V_{DSOP1}	−		1.5	−	8	V	−	−
INPUT CURRENT									
Current consumption during operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V		1.0	3.0	5.5	μA	3	2
Current consumption during overdischarge	I_{OPED}	V_{DD} = 1.5 V, V_{VM} = 0 V		0.3	2.0	3.5	μA	3	2
OUTPUT RESISTANCE									
CO pin resistance “H”	R_{COH}	−		2.5	5	10	kΩ	4	3
CO pin resistance “L”	R_{COL}	CO pin output logic active “H”		2.5	9	15	kΩ	4	3
		CO pin output logic active “L”		2.5	5	10	kΩ	4	3
DO pin resistance “H”	R_{DOH}	−		2.5	5	10	kΩ	5	3
DO pin resistance “L”	R_{DOL}	−		2.5	5	10	kΩ	5	3

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. Except Detection Delay Time (−40°C to +85°C [*1])

Table 9

(Ta = −40°C to +85°C [*1] unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE									
Overcharge detection voltage	V_{CU}	3.60 V to 4.50 V, Adjustable		V_{CU} − 0.060	V_{CU}	V_{CU} + 0.040	V	1	1
Overcharge release voltage	V_{CL}	3.50 V to 4.40 V, Adjustable	$V_{CL} \neq V_{CU}$	V_{CL} − 0.08	V_{CL}	V_{CL} + 0.065	V	1	1
			$V_{CL} = V_{CU}$	V_{CL} − 0.08	V_{CL}	V_{CL} + 0.04	V	1	1
Overdischarge detection voltage	V_{DL}	2.00 V to 3.00 V, Adjustable		V_{DL} − 0.11	V_{DL}	V_{DL} + 0.13	V	2	2
Overdischarge release voltage	V_{DU}	2.00 V to 3.40 V, Adjustable	$V_{DU} \neq V_{DL}$	V_{DU} − 0.15	V_{DU}	V_{DU} + 0.19	V	2	2
			$V_{DU} = V_{DL}$	V_{DU} − 0.11	V_{DU}	V_{DU} + 0.13	V	2	2
INPUT VOLTAGE									
Operating voltage between VDD pin and VSS pin	V_{DSOP1}	−		1.5	−	8	V	−	−
INPUT CURRENT									
Current consumption during operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V		0.7	3.0	6.0	μA	3	2
Current consumption during overdischarge	I_{OPED}	V_{DD} = 1.5 V, V_{VM} = 0 V		0.2	2.0	3.8	μA	3	2
OUTPUT RESISTANCE									
CO pin resistance “H”	R_{COH}	−		1.2	5	15	kΩ	4	3
CO pin resistance “L”	R_{COL}	CO pin output logic active “H”		1.2	9	27	kΩ	4	3
		CO pin output logic active “L”		1.2	5	15	kΩ	4	3
DO pin resistance “H”	R_{DOH}	−		1.2	5	15	kΩ	5	3
DO pin resistance “L”	R_{DOL}	−		1.2	5	15	kΩ	5	3

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

3. Detection Delay Time

3. 1 S-8211EAC, S-8211EAH, S-8211EAI, S-8211EAJ, S-8211EAK, S-8211EAP

Table 10

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = +25°C)								
Overcharge detection delay time	t_{CU}	–	0.96	1.2	1.4	s	6	4
Overdischarge detection delay time	t_{DL}	–	120	150	180	ms	6	4
DELAY TIME (Ta = –40°C to +85°C) *1								
Overcharge detection delay time	t_{CU}	–	0.7	1.2	2.0	s	6	4
Overdischarge detection delay time	t_{DL}	–	83	150	255	ms	6	4

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

3. 2 S-8211EAA, S-8211EAB, S-8211EAD, S-8211EAE, S-8211EAF, S-8211EAG

Table 11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = +25°C)								
Overcharge detection delay time	t_{CU}	–	458	573	687	ms	6	4
Overdischarge detection delay time	t_{DL}	–	240	300	360	ms	6	4
DELAY TIME (Ta = –40°C to +85°C) *1								
Overcharge detection delay time	t_{CU}	–	334	573	955	ms	6	4
Overdischarge detection delay time	t_{DL}	–	166	300	510	ms	6	4

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) are judged by V_{VM} + 1.0 V, and the output voltage levels "H" and "L" at DO pin (V_{DO}) are judged by V_{SS} + 1.0 V. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge Detection Voltage, Overcharge Release Voltage (Test Condition 1, Test Circuit 1)

1. 1 CO pin output logic = Active "H"

Overcharge detection voltage (V_{CU}) is defined as the voltage between the VDD pin and VSS pin at which V_{CO} goes from "L" to "H" when the voltage V1 is gradually increased from the starting condition of V1 = 3.5 V. Overcharge release voltage (V_{CL}) is defined as the voltage between the VDD pin and VSS pin at which V_{CO} goes from "H" to "L" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between overcharge detection voltage (V_{CU}) and overcharge release voltage (V_{CL}).

1. 2 CO pin output logic = Active "L"

Overcharge detection voltage (V_{CU}) is defined as the voltage between the VDD pin and VSS pin at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.5 V. Overcharge release voltage (V_{CL}) is defined as the voltage between the VDD pin and VSS pin at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between overcharge detection voltage (V_{CU}) and overcharge release voltage (V_{CL}).

2. Overdischarge Detection Voltage, Overdischarge Release Voltage (Test Condition 2, Test Circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage between the VDD pin and VSS pin at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = 3.5 V, V2 = 0 V. Overdischarge release voltage (V_{DU}) is defined as the voltage between the VDD pin and VSS pin at which V_{DO} goes from "L" to "H" when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between overdischarge release voltage (V_{DU}) and overdischarge detection voltage (V_{DL}).

3. Current Consumption during Operation (Test Condition 3, Test Circuit 2)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 3.5 V and V2 = 0 V (normal status).

4. Current Consumption during Overdischarge (Test Condition 3, Test Circuit 2)

The current consumption during overdischarge (I_{OPED}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 1.5 V, V2 = 0V (overdischarge status).

5. CO Pin Resistance "H"
(Test Condition 4, Test Circuit 3)

5. 1 CO pin output logic = Active "H"

The CO pin resistance "H" (R_{COH}) is the resistance at the CO pin under the set conditions of V1 = 4.5 V, V2 = 0 V, V3 = 4.0 V.

5. 2 CO pin output logic = Active "L"

The CO pin resistance "H" (R_{COH}) is the resistance at the CO pin under the set conditions of V1 = 3.5 V, V2 = 0 V, V3 = 3.0 V.

6. CO Pin Resistance "L"
(Test Condition 4, Test Circuit 3)

6. 1 CO pin output logic = Active "H"

The CO pin resistance "L" (R_{COL}) is the resistance at the CO pin under the set conditions of V1 = 3.5 V, V2 = 0 V, V3 = 0.5 V.

6. 2 CO pin output logic = Active "L"

The CO pin resistance "L" (R_{COL}) is the resistance at the CO pin under the set conditions of V1 = 4.5 V, V2 = 0 V, V3 = 0.5 V.

7. DO Pin Resistance "H"
(Test Condition 5, Test Circuit 3)

The DO pin "H" resistance (R_{DOH}) is the resistance at the DO pin under the set conditions of V1 = 3.5 V, V2 = 0 V, V4 = 3.0 V.

8. DO Pin Resistance "L"
(Test Condition 5, Test Circuit 3)

The DO pin "L" resistance (R_{DOL}) is the resistance at the DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.5 V.

9. Overcharge Detection Delay Time
(Test Condition 6, Test Circuit 4)

9. 1 CO pin output logic = Active "H"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "L" to "H" just after the voltage V1 momentarily increases (within 10 μs) from overcharge detection voltage (V_{CU}) −0.2 V to overcharge detection voltage (V_{CU}) +0.2 V under the set conditions of V2 = 0 V.

9. 2 CO pin output logic = Active "L"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the voltage V1 momentarily increases (within 10 μs) from overcharge detection voltage (V_{CU}) −0.2 V to overcharge detection voltage (V_{CU}) +0.2 V under the set conditions of V2 = 0 V.

10. Overdischarge Detection Delay Time
(Test Condition 6, Test Circuit 4)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the voltage V1 momentarily decreases (within 10 μs) from overdischarge detection voltage (V_{DL}) +0.2 V to overdischarge detection voltage (V_{DL}) −0.2 V under the set condition of V2 = 0 V.

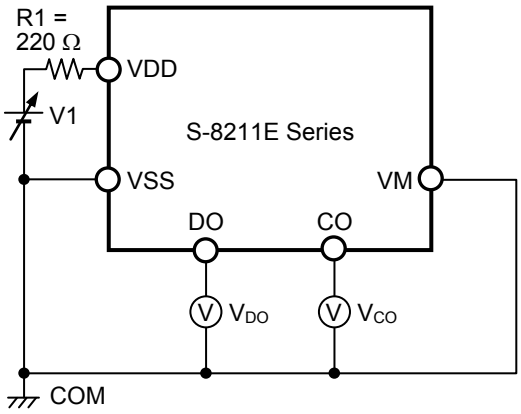


Figure 5 Test Circuit 1

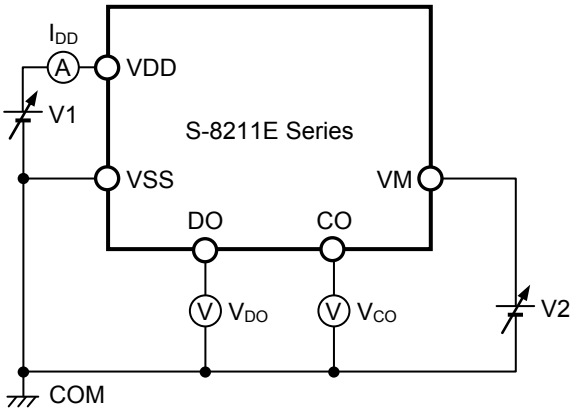


Figure 6 Test Circuit 2

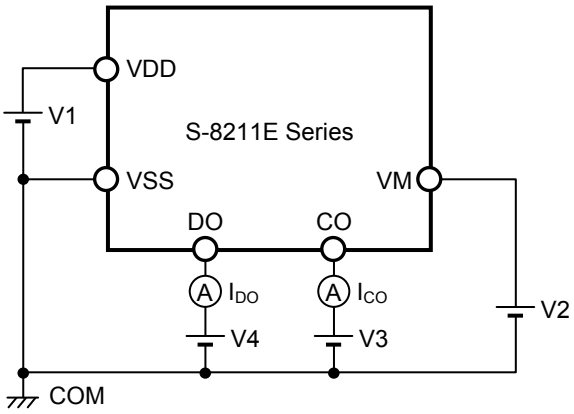


Figure 7 Test Circuit 3

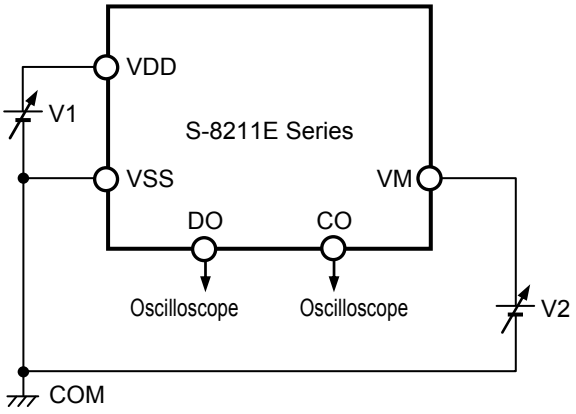


Figure 8 Test Circuit 4

■ Operation

Remark Refer to the "■ **Battery Protection IC Connection Example**".

1. Normal Status

The S-8211E Series monitors the voltage of the battery connected between the VDD and VSS pins.
In case of overdischarge detection voltage (V_{DL}) ≤ battery voltage ≤ overcharge detection voltage (V_{CU}), the output levels of CO and DO pins are as follows. This is the normal status.

Table 12

CO Pin Output Logic	CO Pin	DO Pin
Active "H"	V_{VM}	V_{DD}
Active "L"	V_{DD}	V_{DD}

2. Overcharge Status

When the battery voltage in the normal status exceeds the overcharge detection voltage (V_{CU}) during charge, and this status is held for the overcharge detection delay time (t_{CU}) or more, the output levels of CO and DO pins are as follows. This is the overcharge status.
This overcharge status is released when the battery voltage decreases to the overcharge release voltage (V_{CL}) or less.

Table 13

CO Pin Output Logic	CO Pin	DO Pin
Active "H"	V_{DD}	V_{DD}
Active "L"	V_{VM}	V_{DD}

3. Overdischarge Status

When the battery voltage in the normal status decreases than the overcharge detection voltage (V_{DL}) during discharge, and this status is held for the overdischarge detection delay time (t_{DL}) or more, the output levels of CO and DO pins are as follows. This is the overdischarge status.
This overdischarge status is released when the battery voltage increases to the overdischarge release voltage (V_{DU}) or more.

Table 14

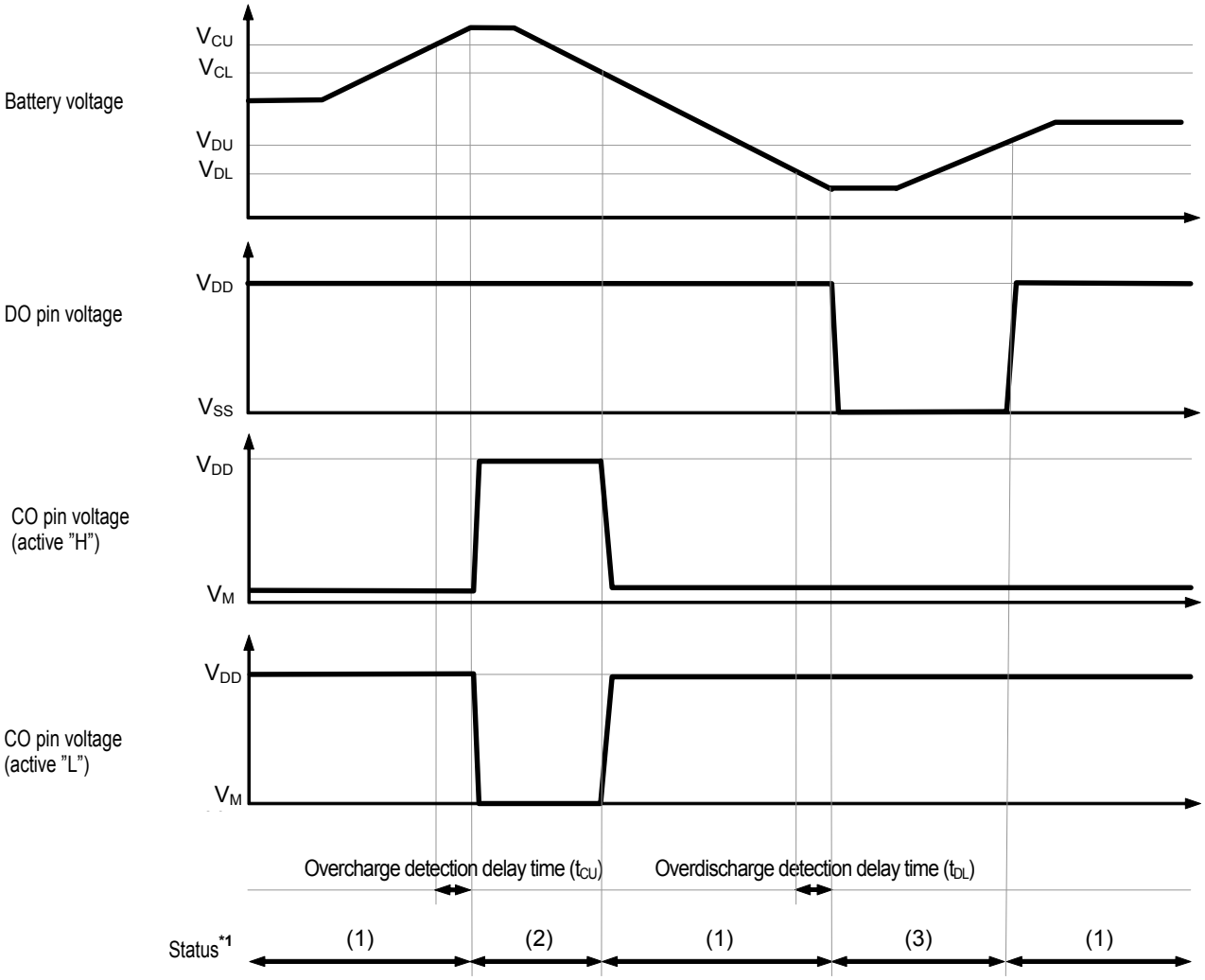
CO Pin Output Logic	CO Pin	DO Pin
Active "H"	V_{VM}	V_{SS}
Active "L"	V_{DD}	V_{SS}

4. Delay Circuit

The detection delay times are determined by dividing a clock of approximately 3.5 kHz by the counter.

■ Timing Chart

1. Overcharge Detection, Overdischarge Detection



***1.** (1) : Normal status
(2) : Overcharge status
(3) : Overdischarge status

Figure 9

■ Battery Protection IC Connection Example

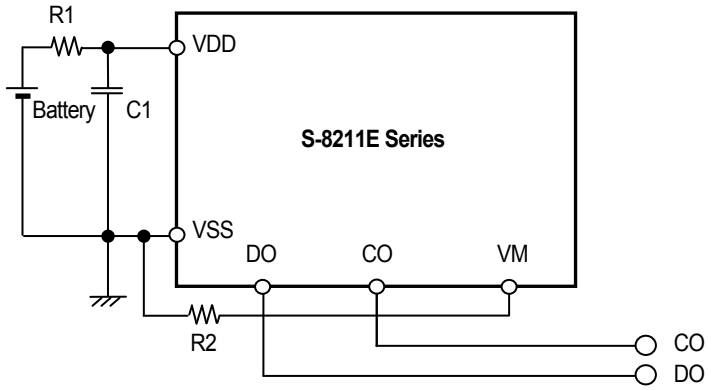


Figure 10

Table 15 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
R1	Resistor	ESD protection, For power fluctuation	100 Ω	220 Ω	330 Ω	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption. *1
C1	Capacitor	For power fluctuation	0.022 μF	0.1 μF	1.0 μF	Connect a capacitor of 0.022 μF or higher between VDD pin and VSS pin. *2
R2*3	Resistor	ESD protection	300 Ω	1 kΩ	4 kΩ	-

***1.** Insert a resistor of 100 Ω or higher as R1 for ESD protection.

***2.** If a capacitor of less than 0.022 μF is connected to C1, DO pin may oscillate. Be sure to connect a capacitor of 0.022 μF or higher to C1.

***3.** Be sure to using R2, connect the VM pin with the VSS pin.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

■ Application Circuit Examples

1. Protection circuits series multi-cells

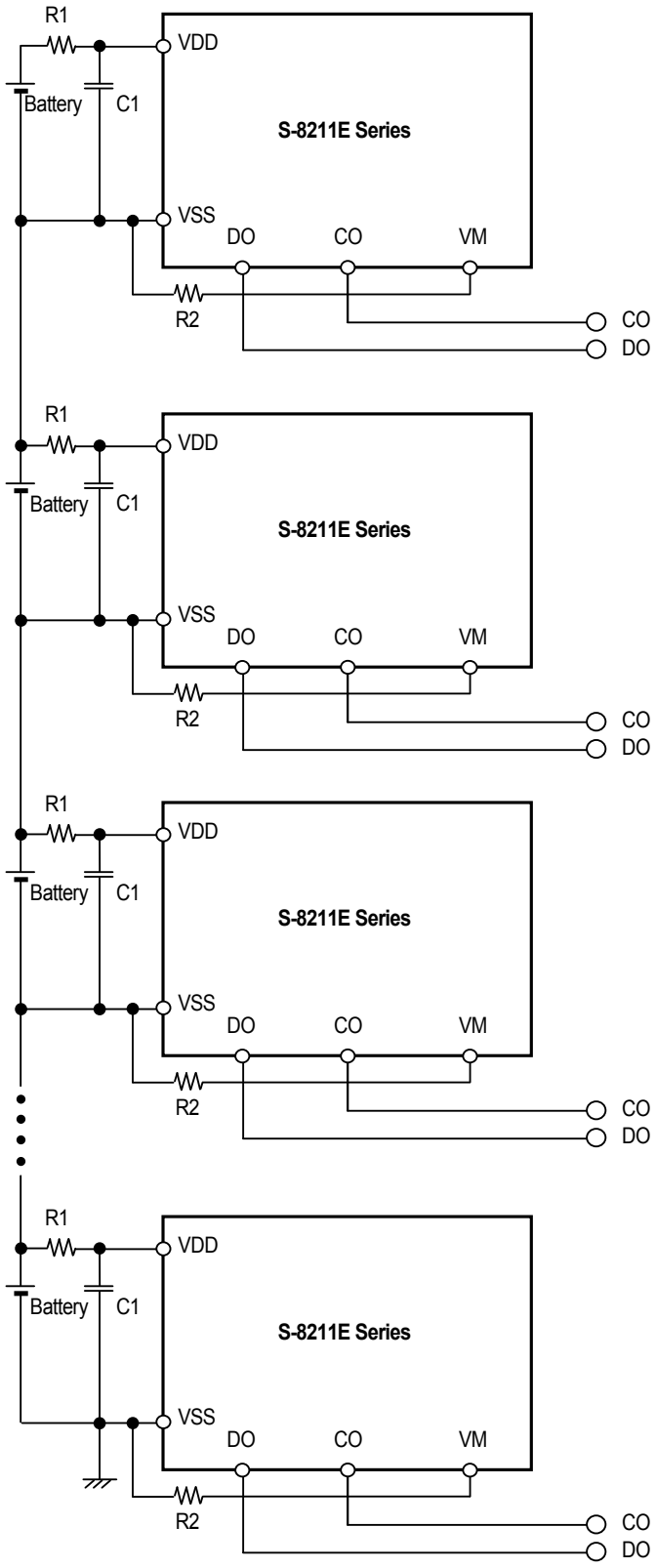


Figure 11

2. Charge cell-balance detection circuit

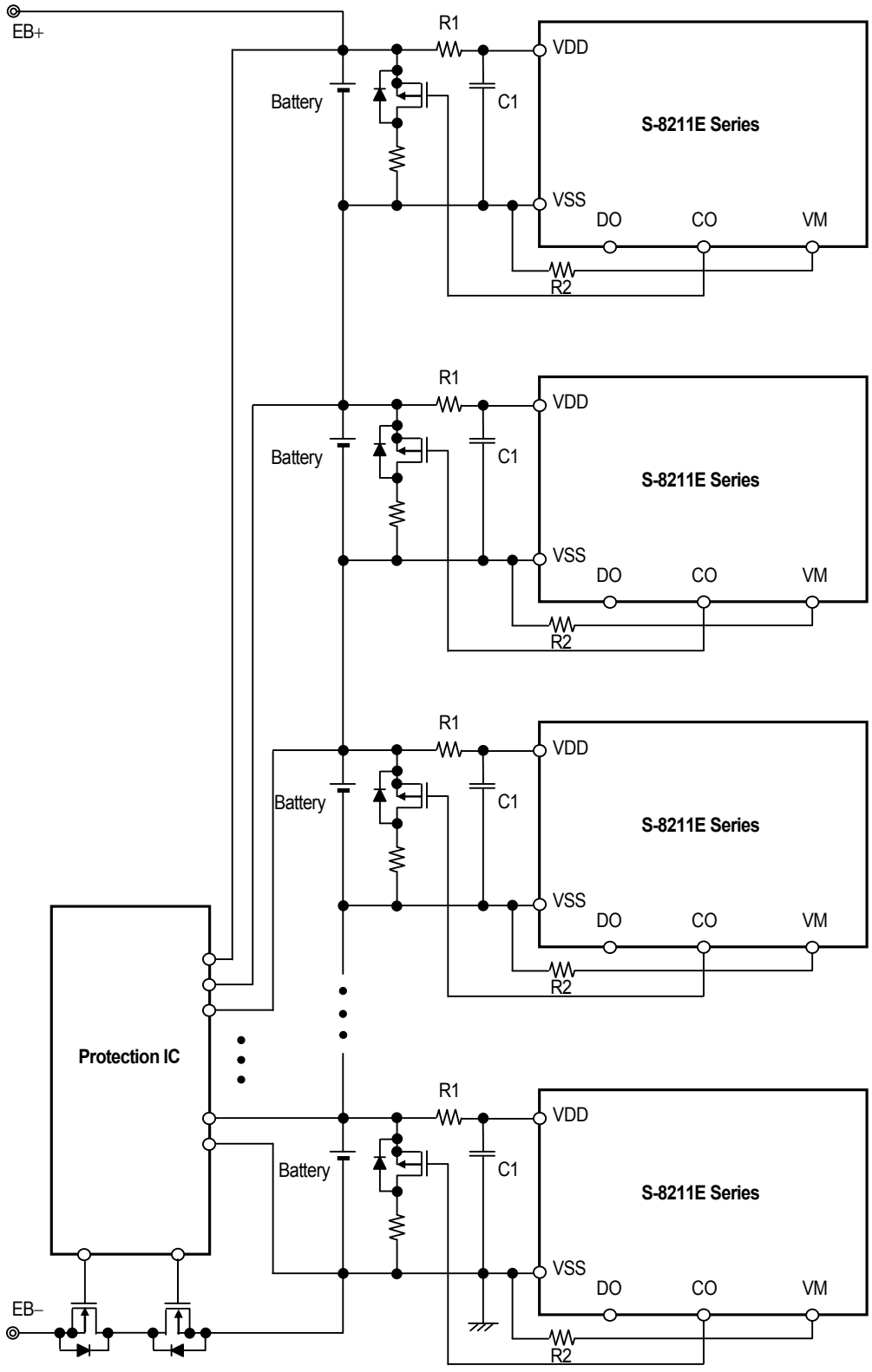


Figure 12

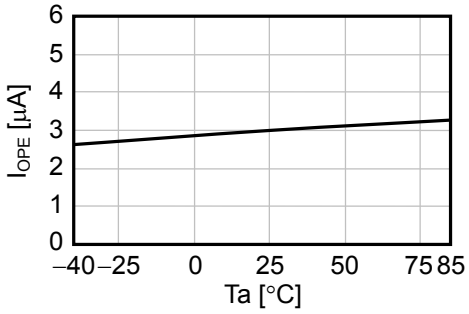
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Be sure to using R2, connect the VM pin with the VSS pin.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

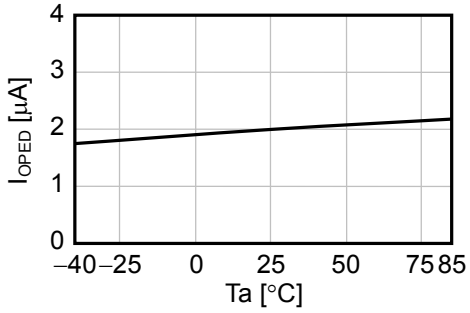
■ Characteristics (Typical Data)

1. Current Consumption

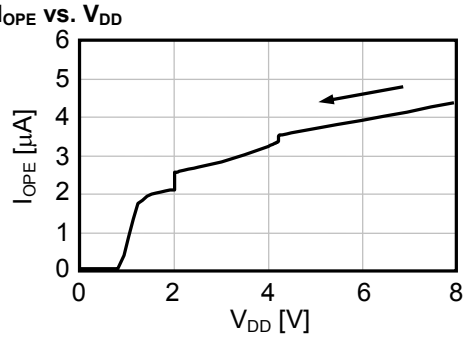
1. 1 I_{OPE} vs. Ta



1. 2 I_{OPED} vs. Ta

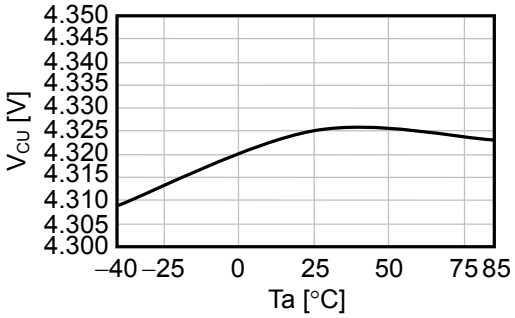


1. 3 I_{OPE} vs. V_{DD}

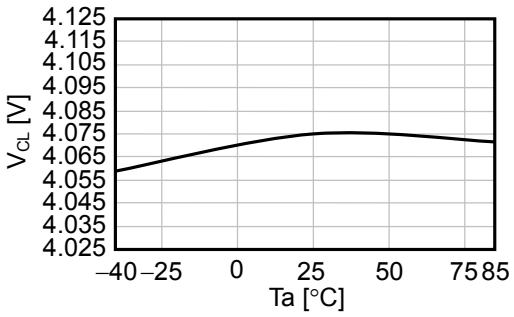


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Time

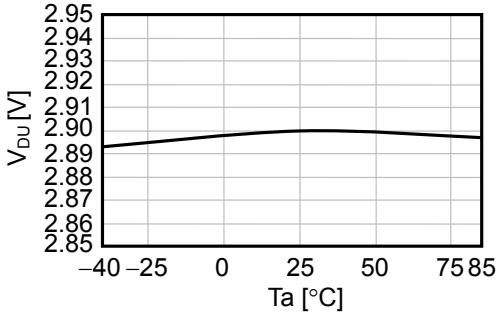
2. 1 V_{CU} vs. Ta



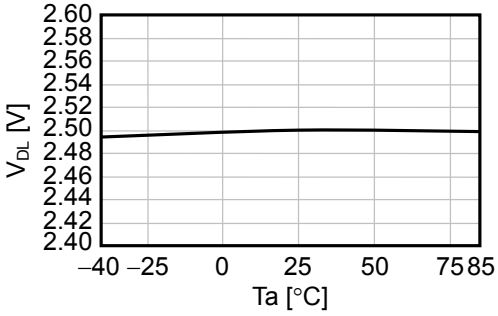
2. 2 V_{CL} vs. Ta



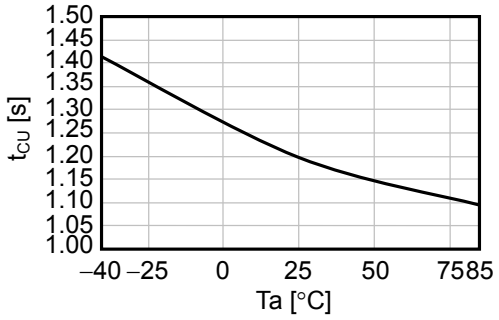
2. 3 V_{DU} vs. Ta



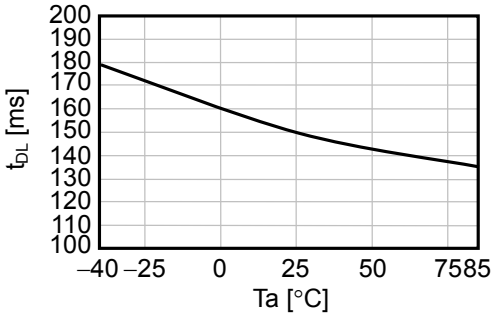
2. 4 V_{DL} vs. Ta



2. 5 t_{CU} vs. Ta

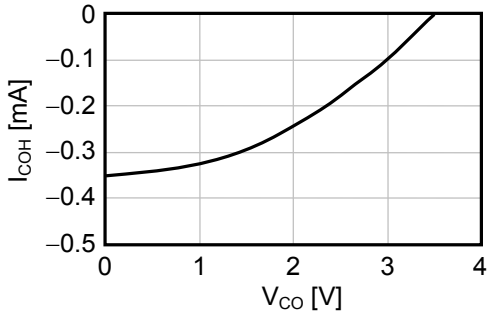


2. 6 t_{DL} vs. Ta

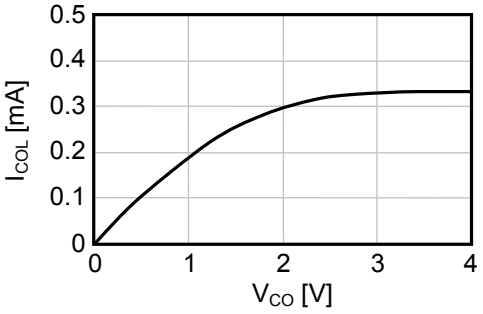


3. CO pin / DO pin

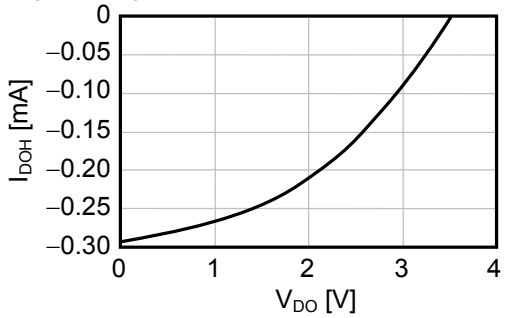
3. 1 I_{COH} vs. V_{CO}



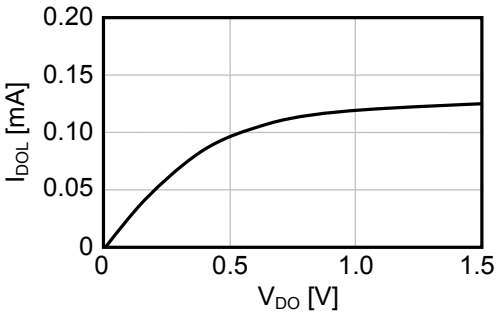
3. 2 I_{COL} vs. V_{CO}



3. 3 I_{DOH} vs. V_{DO}



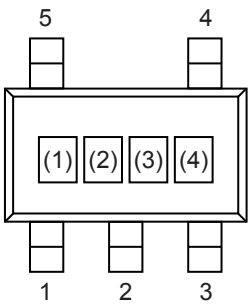
3. 4 I_{DOL} vs. V_{DO}



■ Marking Specifications

1. SOT-23-5

Top view



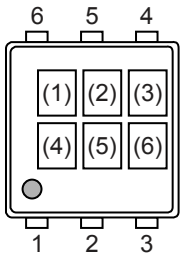
(1) to (3): Product Code (refer to **Product Name vs. Product Code**)
(4) : Lot number

Product Name vs. Product Code

Product Name	Product Code		
	(1)	(2)	(3)
S-8211EAC-M5T1U	R	3	C
S-8211EAF-M5T1U	R	3	F
S-8211EAG-M5T1U	R	3	G
S-8211EAJ-M5T1U	R	3	J
S-8211EAK-M5T1U	R	3	K

2. SNT-6A

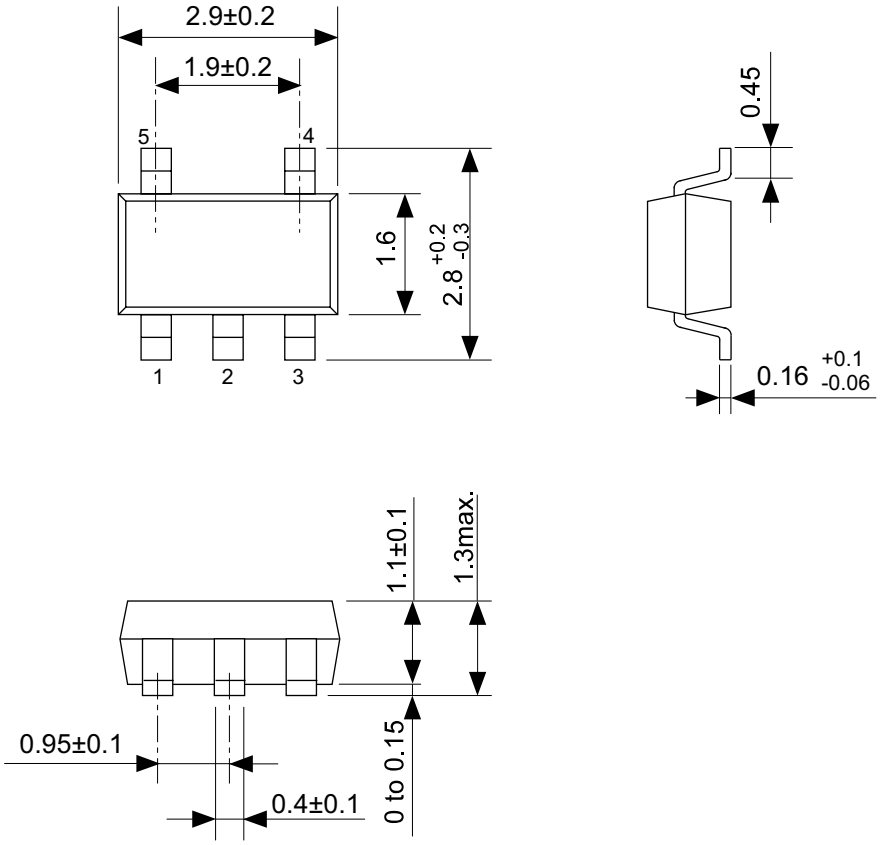
Top view



(1) to (3): Product Code (refer to **Product Name vs. Product Code**)
(4) to (6): Lot number

Product Name vs. Product Code

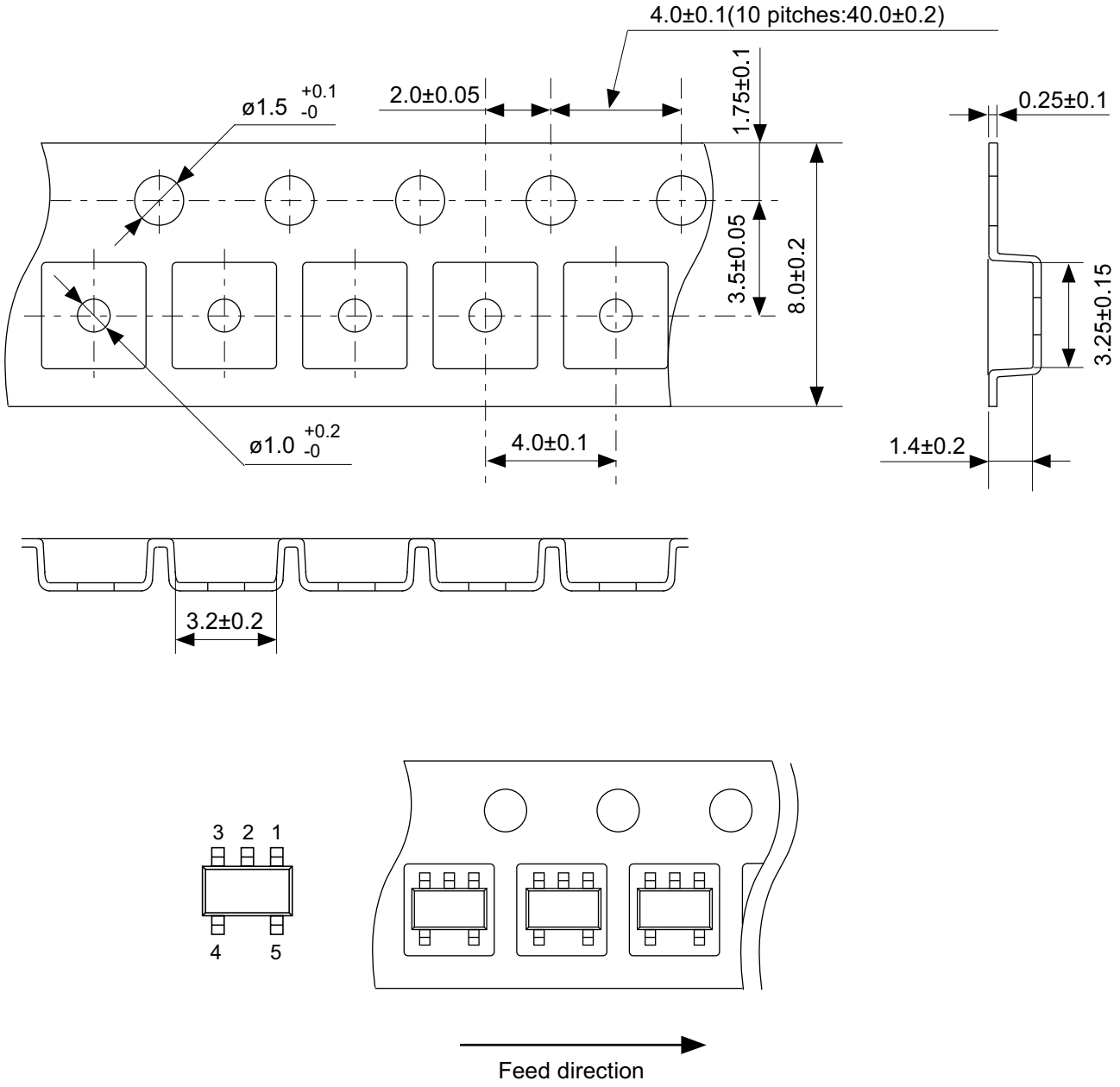
Product Name	Product Code		
	(1)	(2)	(3)
S-8211EAA-I6T1U	R	3	A
S-8211EAB-I6T1U	R	3	B
S-8211EAD-I6T1U	R	3	D
S-8211EAE-I6T1U	R	3	E
S-8211EAH-I6T1U	R	3	H
S-8211EAI-I6T1U	R	3	I
S-8211EAP-I6T1U	R	3	P



No. MP005-A-P-SD-1.3

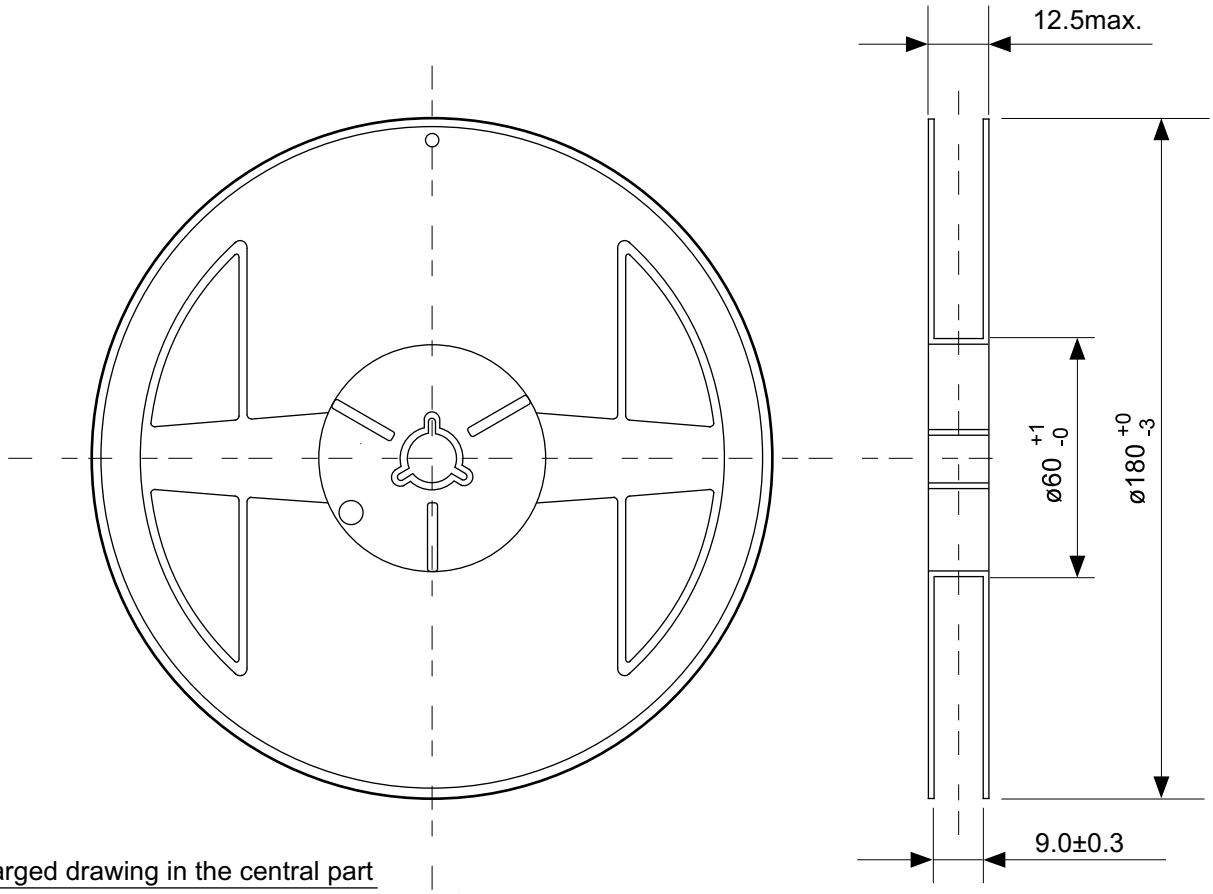
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

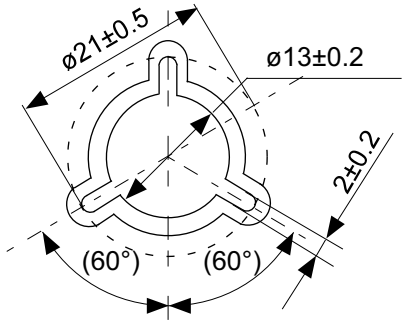


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

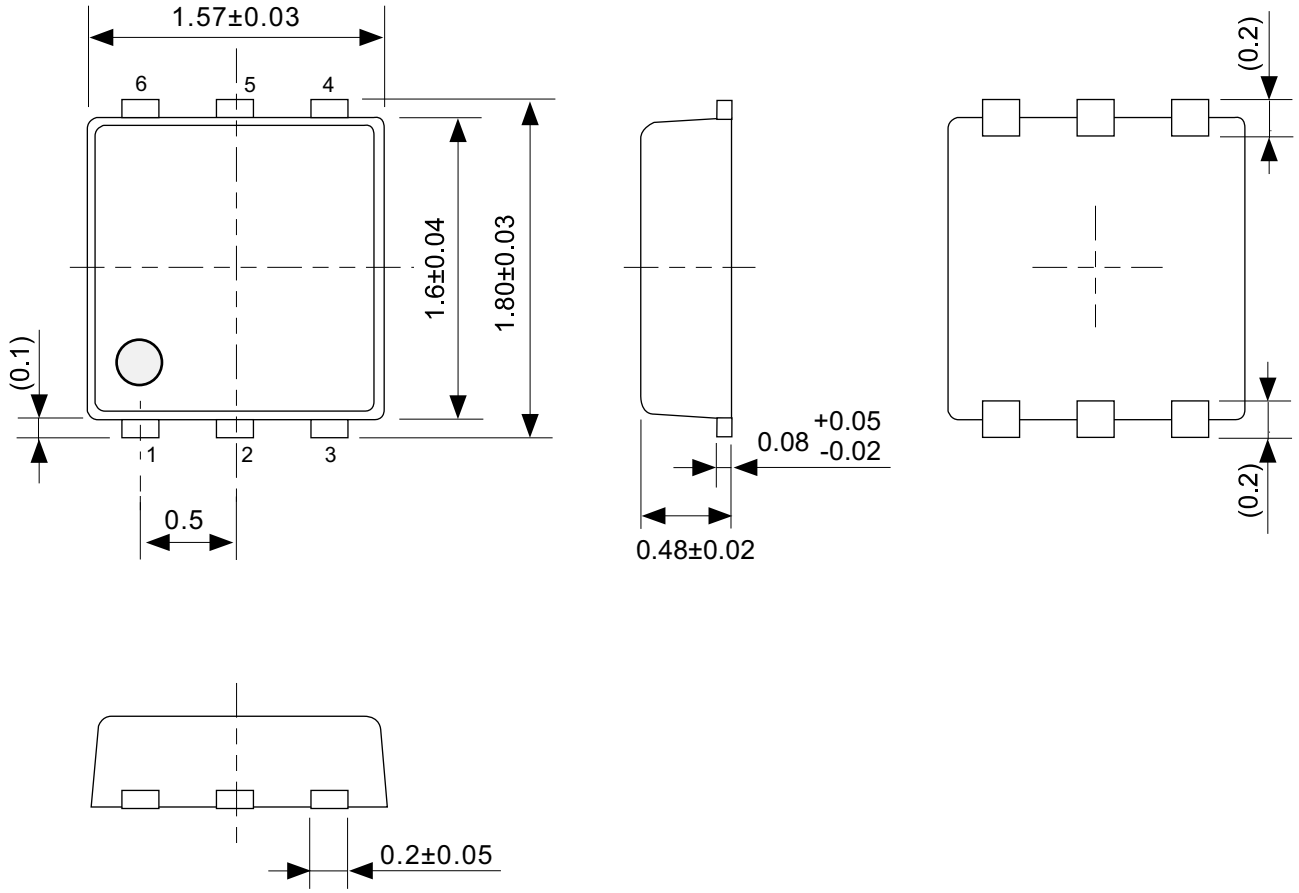


Enlarged drawing in the central part



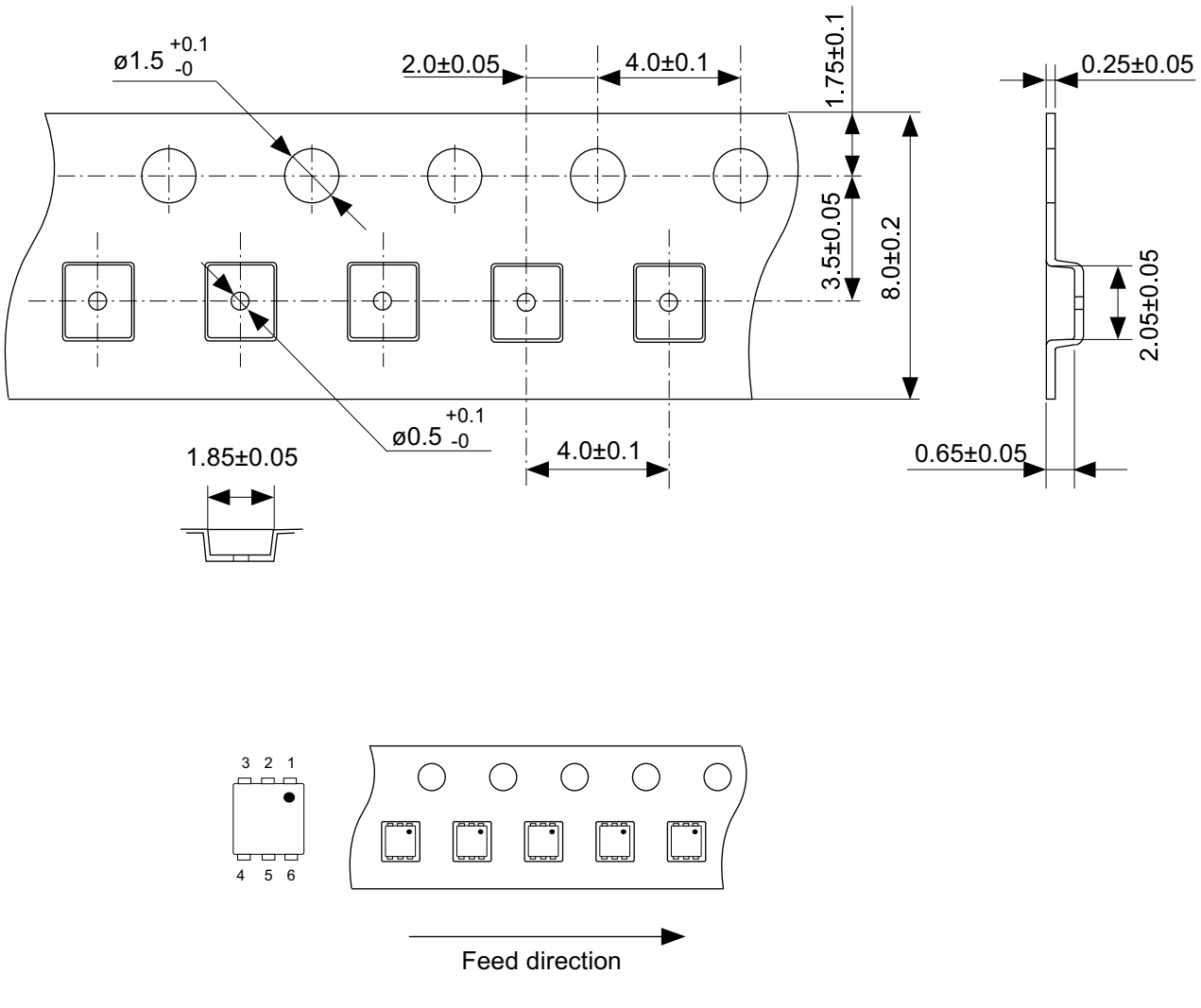
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



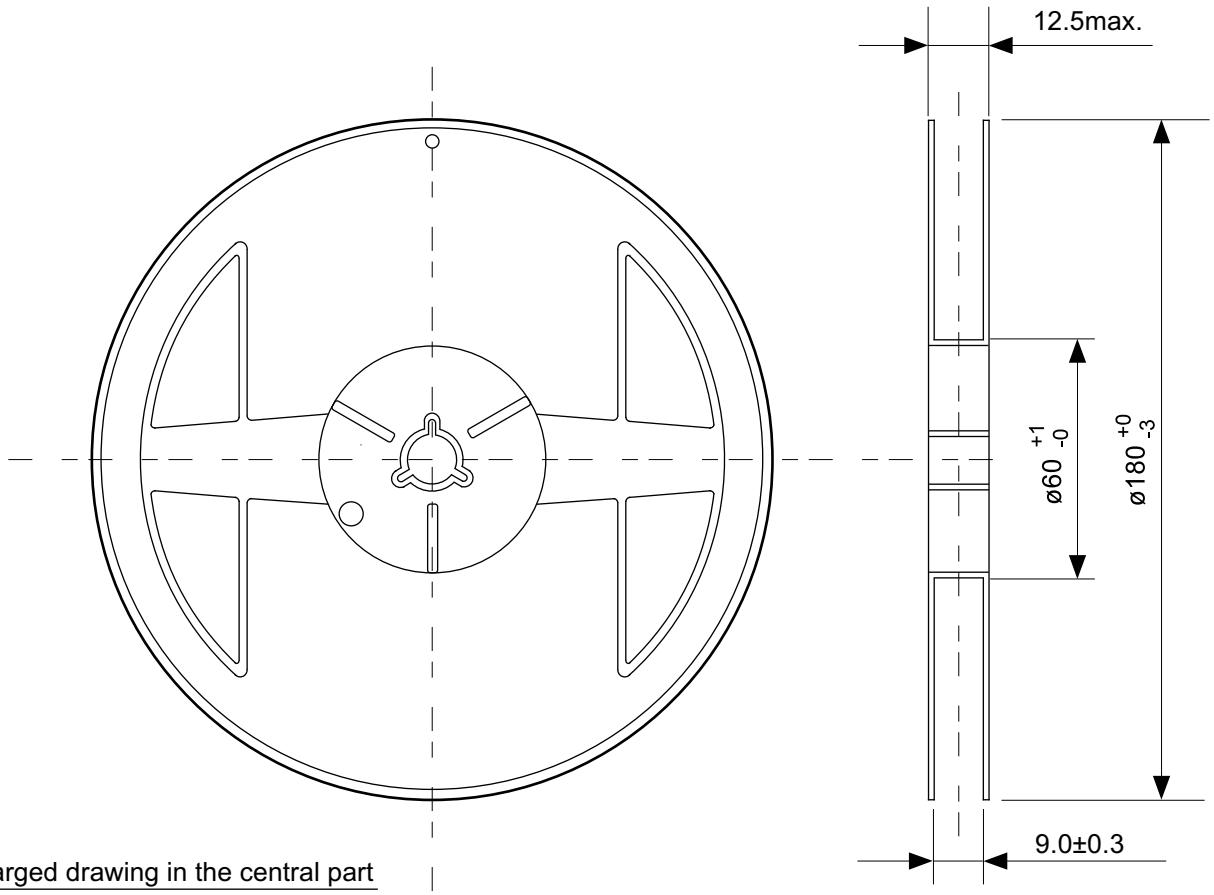
No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

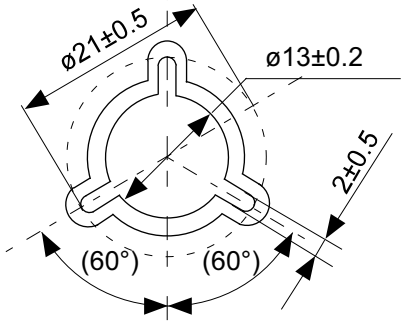


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

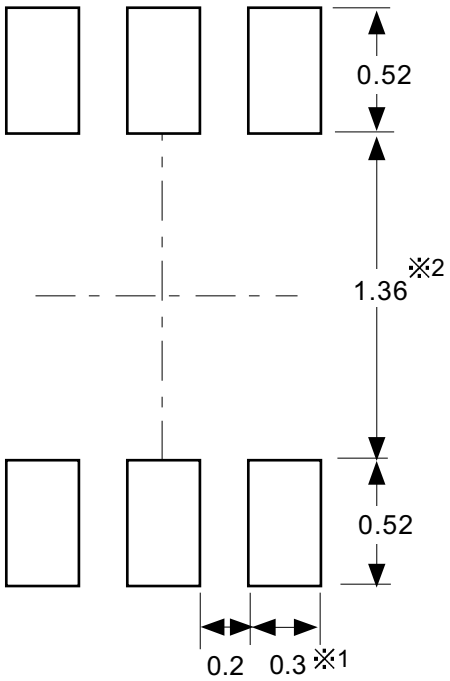


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution
1. **Do not do silkscreen printing and solder printing under the mold resin of the package.**
2. **The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
3. **Match the mask aperture size and aperture position with the land pattern.**
4. **Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意
1. **请勿在树脂型封装的下面印刷丝网、焊锡。**
2. **在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
3. **钢网的开口尺寸和开口位置请与焊盘模式对齐。**
4. **详细内容请参阅 "SNT 封装的应用指南"。**

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
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2.4-2019.07