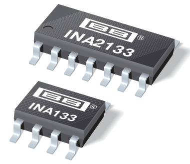
BURR - BROWN®



INA133
INA2133

For most current data sheet and other product information, visit www.burr-brown.com

High-Speed, Precision DIFFERENCE AMPLIFIERS

FEATURES

- DESIGNED FOR LOW COST
- SINGLE, DUAL VERSIONS
- LOW OFFSET VOLTAGE DRIFT: ±450µV max, ±5µV/°C max
- LOW GAIN ERROR: 0.05% max
- WIDE BANDWIDTH: 1.5MHz
- HIGH SLEW RATE: 5V/µs
- FAST SETTLING TIME: 5.5µs to 0.01%
- LOW QUIESCENT CURRENT: 950µA
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- SO-8 and SO-14 PACKAGES

APPLICATIONS

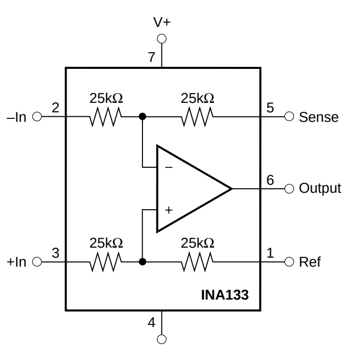
- DIFFERENTIAL INPUT AMPLIFIER BUILDING BLOCK
- DIFF IN/DIFF OUT AMPLIFIER
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN = +1/2 OR G = +2 AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT/DIFFERENTIAL LINE RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- BATTERY POWERED SYSTEMS
- LOW COST AUTOMOTIVE

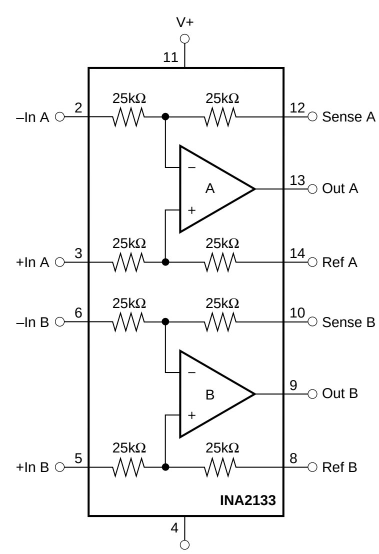
DESCRIPTION

The INA133 and INA2133 are high slew rate, unity-gain difference amplifiers consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. They operate over a wide supply range, ±2.25V to ±18V (+4.5V to +36V single supply), and input common-mode voltage range extends beyond the positive and negative supply rails.

The differential amplifier is the foundation of many commonly used circuits. The low cost INA133 and INA2133 provide this precision circuit function without using an expensive precision network.

The single version, INA133, package is the SO-8 surface mount. The dual version, INA2133, package is the SO-14 surface mount. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C. Operation is from –55°C to +125°C.





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PDS-1530A

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SBOS115

SPECIFICATIONS: V_S = ±15V

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

		INA133U INA2133U			INA133UA INA2133UA			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE(1)	RTO							
Initial(1)	V_{CM} = 0V		±150	±450		*	±900	μV
vs Temperature	T_A = –40°C to +85°C		±2	±5	See Typical Curve			μV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±10	±30		900	±50	μV/V
vs Time			0.3			*		μV/√mo
Channel Separation (dual)	dc		120			*		dB
INPUT IMPEDANCE(2)								
Differential			50			*		kΩ
Common-Mode	V_{CM} = 0V		25			*		kΩ
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range								
Positive	V_O = 0V	2(V+) –3	2(V+) –2		*	*		V
Negative	V_O = 0V	2(V–) +3	2(V–) +2		*	*		V
Common-Mode Rejection Ratio	V_{CM} = –27V to +27V, R_S = 0Ω	80	90		74	*		dB
OUTPUT VOLTAGE NOISE(3)	RTO							
f = 0.1Hz to 10Hz			2			*		μVp-p
f = 10Hz			80			*		nV/√Hz
f = 100Hz			60			*		nV/√Hz
f = 1kHz			57			*		nV/√Hz
GAIN								
Initial			1			*		V/V
Error	V_O = –14V to +13.5V		±0.02	±0.05		*	±0.1	%
vs Temperature	T_A = –40°C to +85°C		±1	±10		*	*	ppm/°C
Nonlinearity	V_O = –14V to +13.5V		±0.0001	±0.001		*	±0.002	% of FS
OUTPUT								
Voltage Output	Gain Error < 0.1%							
Positive	R_L = 10kΩ to Ground	(V+) –1.5	(V+)–1.3		*	*		V
Negative	R_L = 10kΩ to Ground	(V–) +1	(V–)+0.8		*	*		V
Positive	R_L = 100kΩ to Ground		(V+)–0.8			*		V
Negative	R_L = 100kΩ to Ground		(V–)+0.3			*		V
Current Limit, Continuous-to-Common			–25/+32			*		mA
Capacitive Load (stable operation)			1000			*		pF
FREQUENCY RESPONSE								
Small-Signal Bandwidth	–3dB		1.5			*		MHz
Slew Rate			5			*		V/μs
Settling Time: 0.1%	10V Step, C_L = 100pF		4			*		μs
0.01%	10V Step, C_L = 100pF		5.5			*		μs
Overload Recovery Time	50% Overdrive		4			*		μs
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range								
Dual Supplies		±2.25		±18	*		*	V
Single Supply		+4.5		+36	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±0.95	±1.2		*	*	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operation		–55		+125	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance θ_{JA}								
SO-8 Surface Mount			150			*		°C/W
SO-14 Surface Mount			100			*		°C/W

* Specifications the same as INA133U, INA2133U.

NOTES: (1) Includes the effects of amplifier's input bias and offset currents. (2) 25kΩ resistors are ratio matched but have ±20% absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

SPECIFICATIONS: V_S = ±5V

At T_A = +25°C, V_S = ±5V, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA133U INA2133U			INA133UA INA2133UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE(1)	RTO							
Initial(1)	V_{CM} = 0V		±300	±750		✻	±1500	µV
vs Temperature			±2			✻		µV/°C
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range								
Positive	V_O = 0V	2(V+) –3	2(V+) –2		✻	✻		V
Negative	V_O = 0V	2(V–) +3	2(V–) +2		✻	✻		V
Common-Mode Rejection Ratio	V_{CM} = –7V to +7V, R_S = 0Ω	80	90		74	✻		dB
GAIN								
Initial			1			✻		V/V
Gain Error	V_O = –4V to 3.5V		±0.02	±0.05		✻	±0.1	%
Nonlinearity	V_O = –4V to 3.5V		±0.0001	±0.001		✻	±0.002	% of FS
OUTPUT								
Voltage Output	Gain Error < 0.1%							
Positive	R_L = 10kΩ to Ground	(V+) –1.5	(V+) –1.3		✻	✻		V
Negative	R_L = 10kΩ to Ground	(V–) +1	(V–) +0.8		✻	✻		V
Positive	R_L = 100kΩ to Ground		(V+) –0.8			✻		V
Negative	R_L = 100kΩ to Ground		(V–) +0.3			✻		V
POWER SUPPLY								
Rated Voltage			±15			✻		V
Operating Voltage Range								
Dual Supplies		±2.25		±18	✻		✻	V
Single Supply		+4.5		+36	✻		✻	V
Quiescent Current (per amplifier)	I_O = 0		±0.92	±1.2		✻	✻	mA

✻ Specifications the same as INA133U, INA2133U.

NOTES: (1) Includes the effects of amplifier's input bias and offset currents.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	36V
Input Voltage Range	2 • V_S
Output Short-Circuit (to ground)(2)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) One channel per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

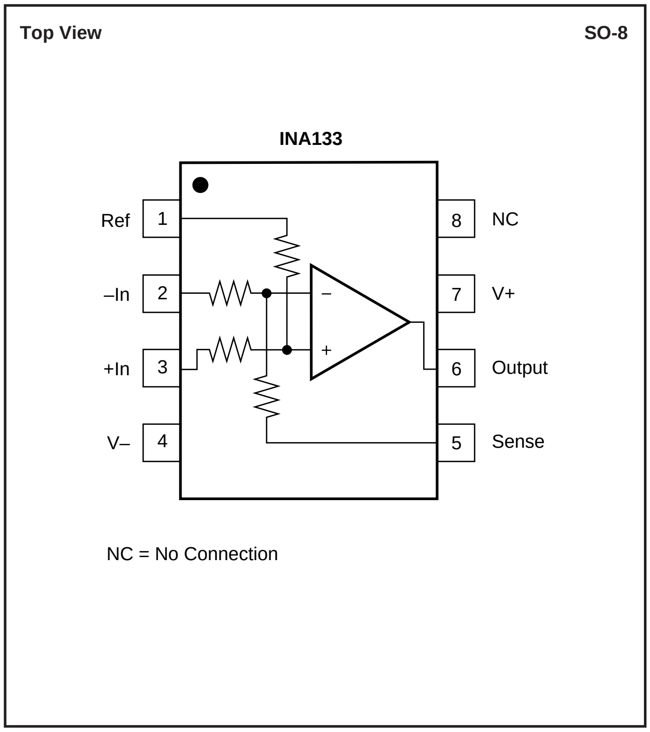
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

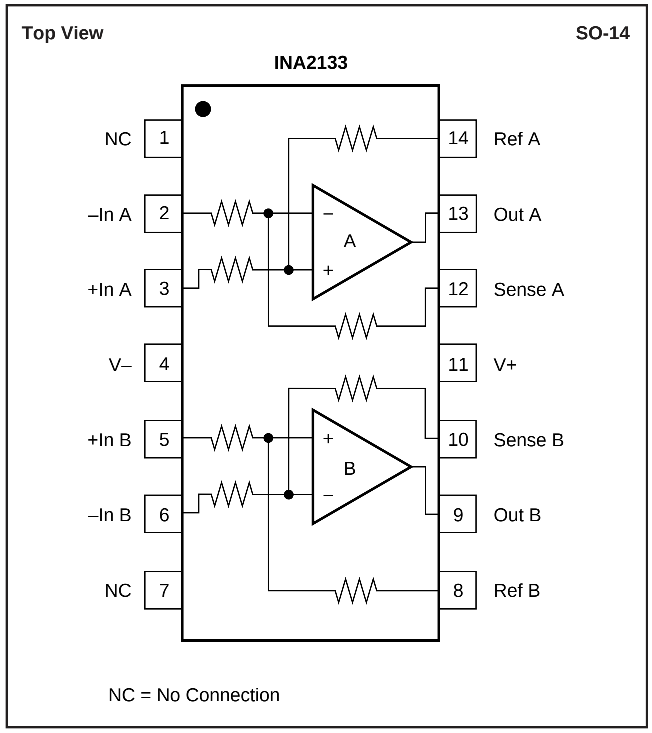
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
Single						
INA133U	SO-8 Surface Mount	182	–40°C to +85°C	INA133U	INA133U	Rails
"	"	"	"	"	INA133U/2K5	Tape and Reel
INA133UA	SO-8 Surface Mount	182	–40°C to +85°C	INA133UA	INA133UA	Rails
"	"	"	"	"	INA133UA/2K5	Tape and Reel
Dual						
INA2133U	SO-14 Surface Mount	235	–40°C to +85°C	INA2133U	INA2133U	Rails
"	"	"	"	"	INA2133U/2K5	Tape and Reel
INA2133UA	SO-14 Surface Mount	235	–40°C to +85°C	INA2133UA	INA2133UA	Rails
"	"	"	"	"	INA2133UA/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA133UA/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

PIN CONFIGURATIONS

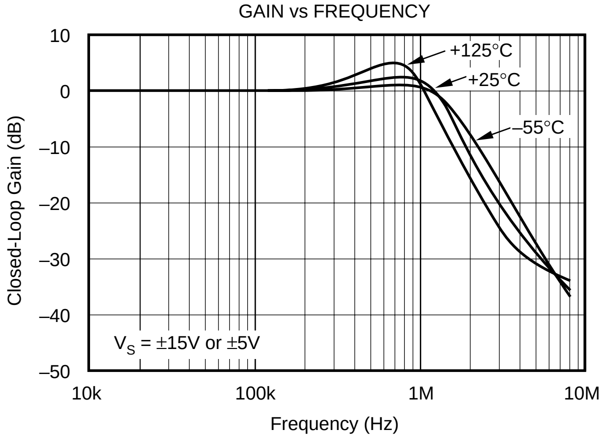




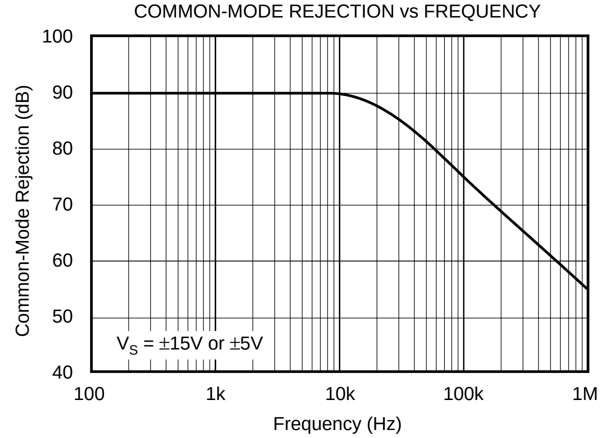
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

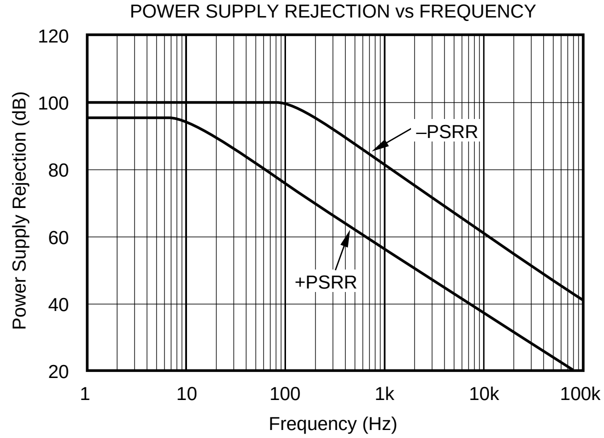
GAIN vs FREQUENCY



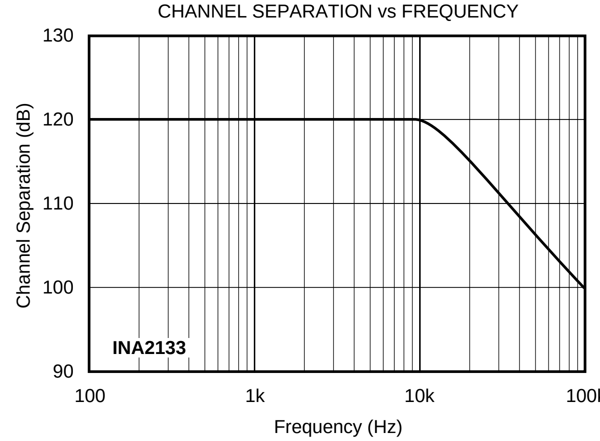
COMMON-MODE REJECTION vs FREQUENCY



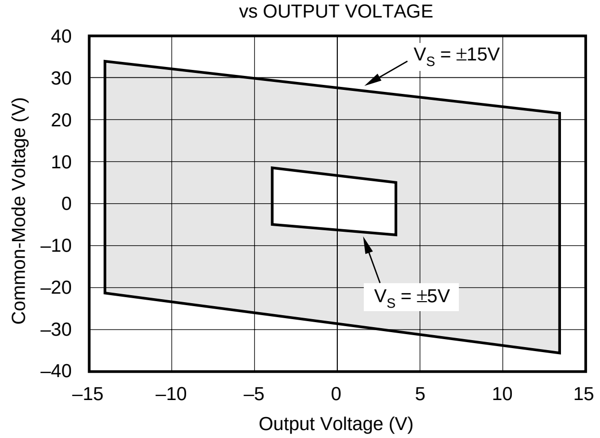
POWER SUPPLY REJECTION vs FREQUENCY



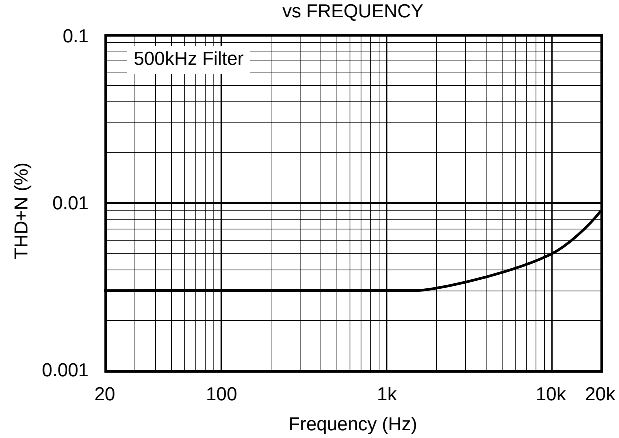
CHANNEL SEPARATION vs FREQUENCY



INPUT COMMON-MODE VOLTAGE
vs OUTPUT VOLTAGE

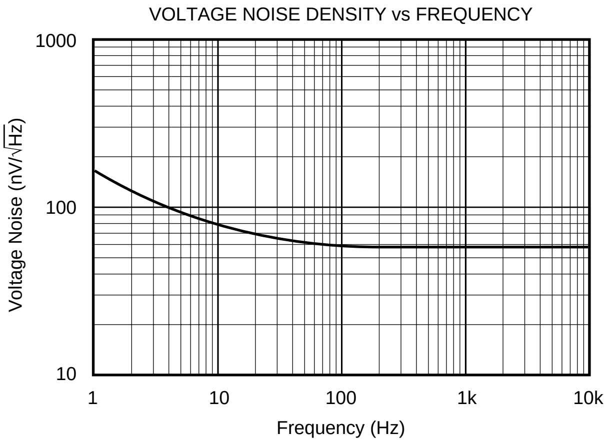


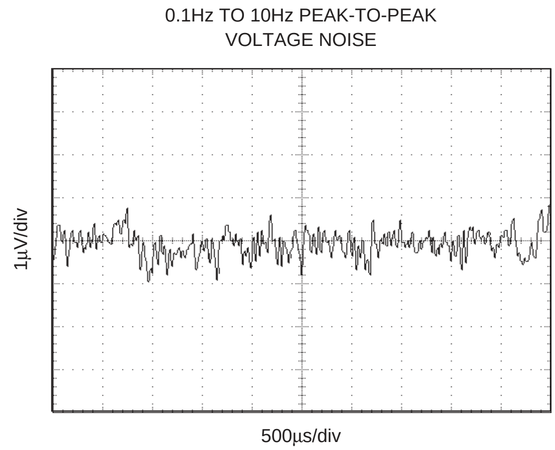
TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY

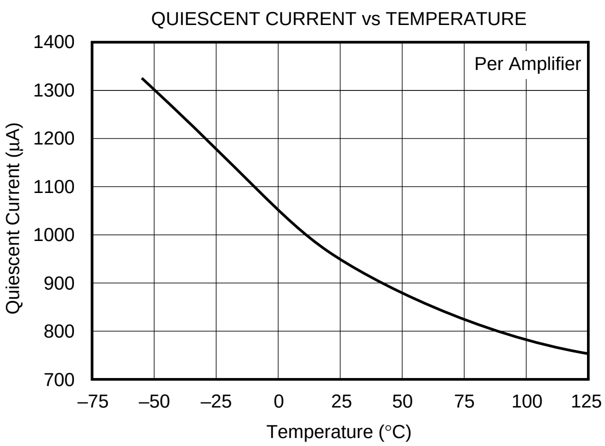


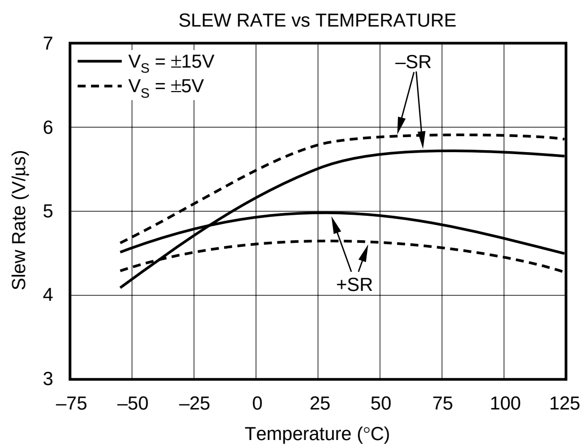
TYPICAL PERFORMANCE CURVES (CONT)

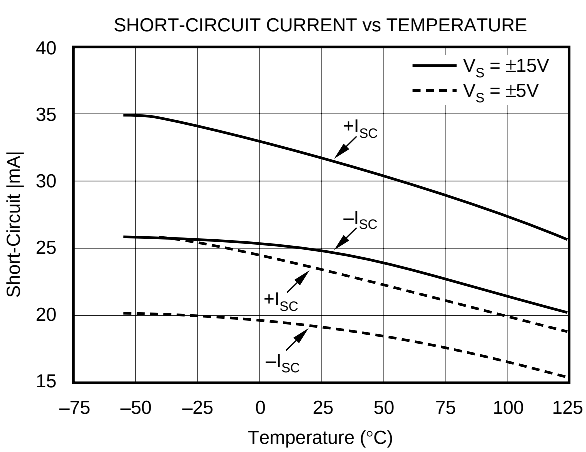
At T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

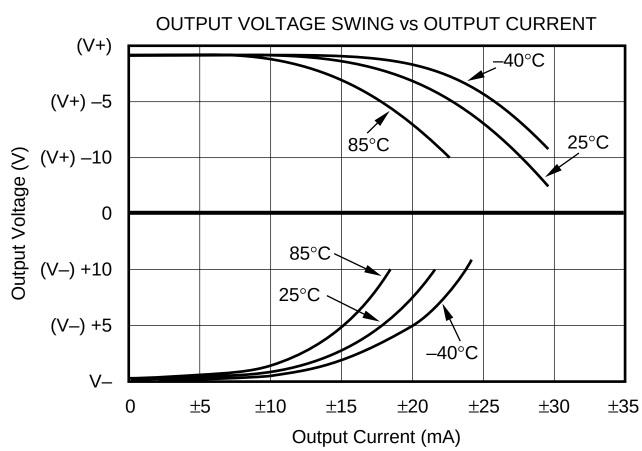








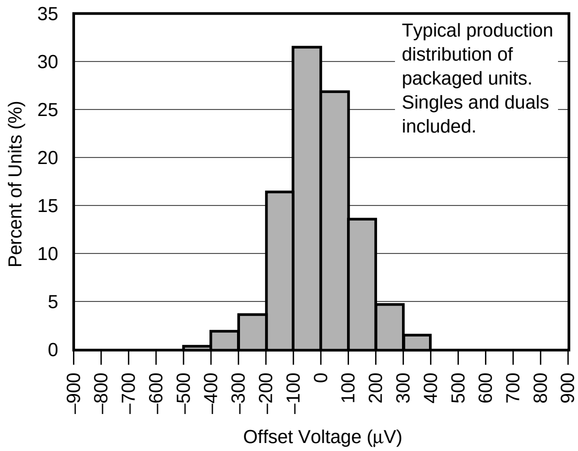




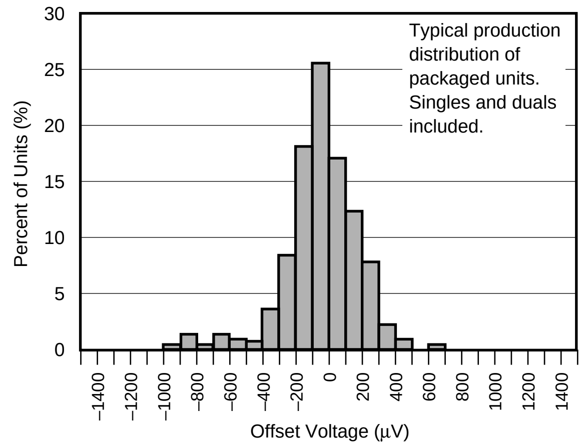
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = \pm15V$, $R_L = 10k\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.

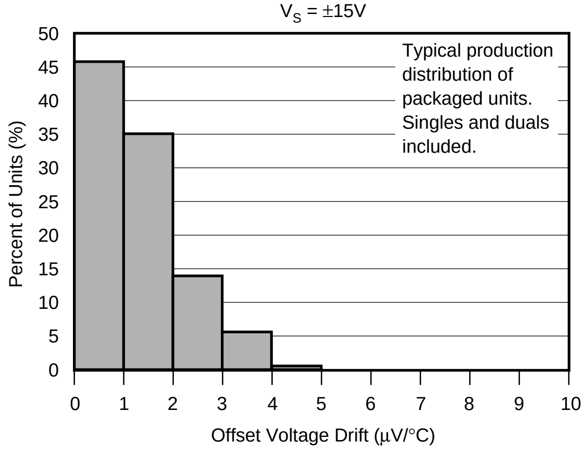
OFFSET VOLTAGE PRODUCTION DISTRIBUTION
$V_S = \pm15V$



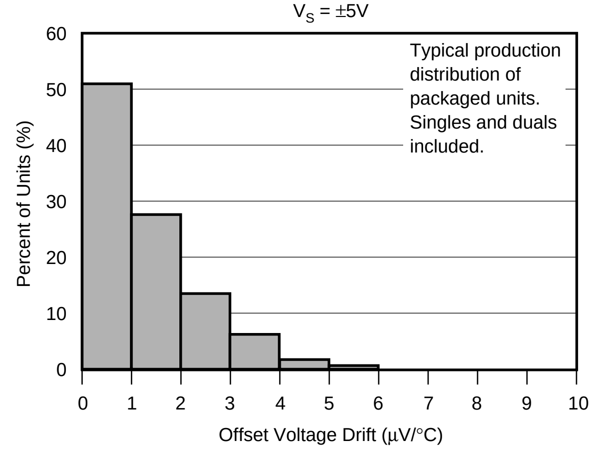
OFFSET VOLTAGE PRODUCTION DISTRIBUTION
$V_S = \pm5V$



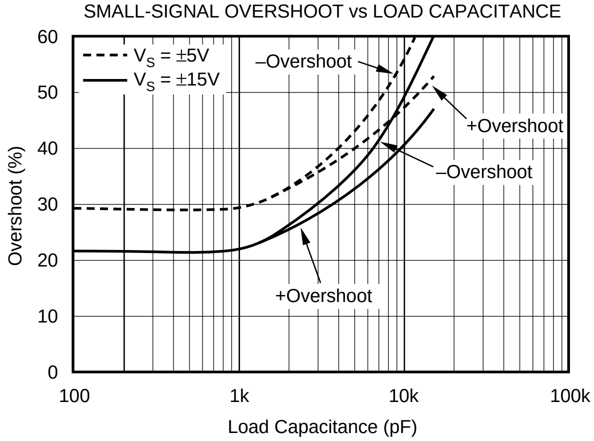
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION
$V_S = \pm15V$



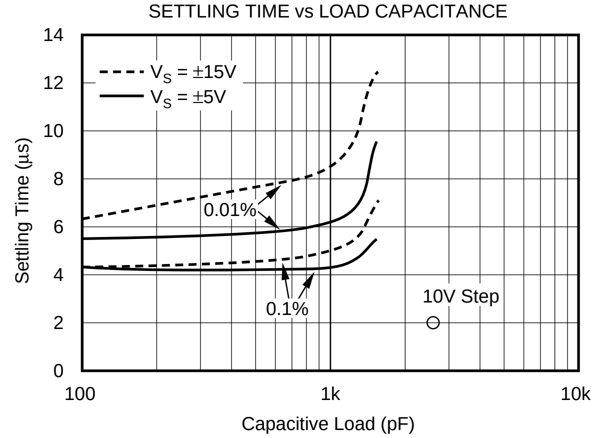
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION
$V_S = \pm5V$



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



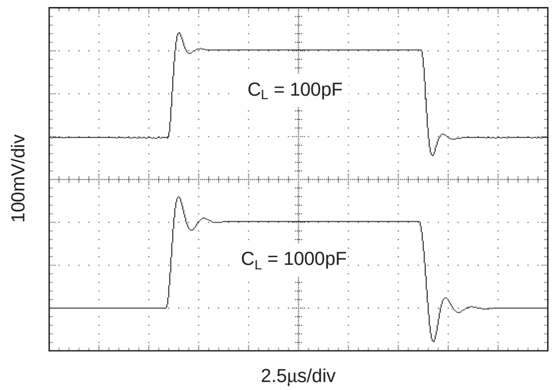
SETTLING TIME vs LOAD CAPACITANCE



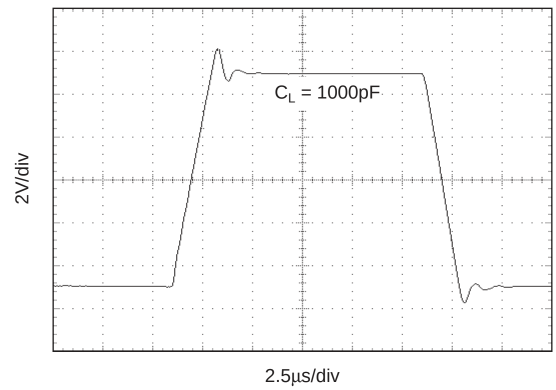
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to ground, and reference pin connected to ground, unless otherwise noted.

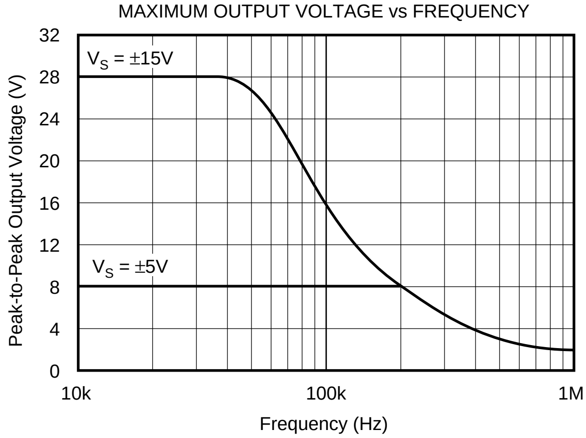
SMALL-SIGNAL STEP RESPONSE



LARGE-SIGNAL STEP RESPONSE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



APPLICATIONS INFORMATION

The INA133 and INA2133 are high-speed difference amplifiers suitable for a wide range of general purpose applications. Figure 1 shows the basic connections required for operation of the INA133. Decoupling capacitors are strongly recommended in applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 1. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 1, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB (a 10Ω mismatch degrades CMR to 74dB). If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

The INA133's internal resistors are accurately ratio trimmed to match. That is, R_1 is trimmed to match R_2 and R_3 is trimmed to match R_4. However, the absolute values may not be equal ($R_1 + R_2$ may be slightly different than $R_3 + R_4$). Thus, large series resistors on the input (greater than 250Ω), even if well matched, will degrade common-mode rejection.

Circuit board layout constraints might suggest possible variations in connections of the internal resistors. For instance, it appears that pins 1 and 3 could be interchanged. However, because of the ratio trimming technique used (see paragraph above) CMRR will be degraded. If pins 1 and 3 are interchanged, pins 2 and 5 must also be interchanged to maintain proper ratio matching.

OPERATING VOLTAGE

The INA133 and INA2133 operate from single (+4.5V to +36V) or dual (±2.25V to ±18V) supplies with excellent performance. Specifications are production tested with ±5V and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Performance Curves.

INPUT VOLTAGE

The INA133 and INA2133 can accurately measure differential signals that are above and below the supply rails. Linear common-mode range extends from 2 • (V+)–3V to 2 • (V–) +3V (nearly twice the supplies). See the typical performance curve, "Input Common-Mode Voltage vs Output Voltage."

OFFSET VOLTAGE TRIM

The INA133 and INA2133 are laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

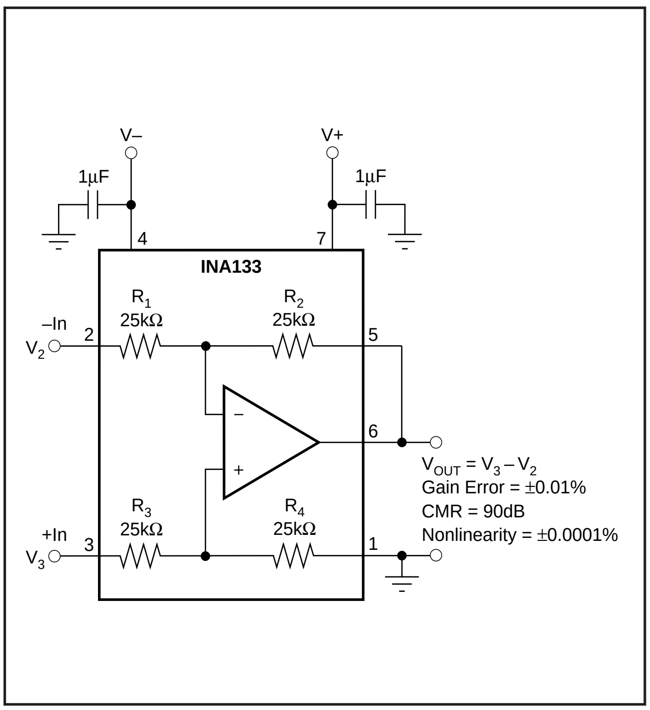


FIGURE 1. Precision Difference Amplifier (Basic Power Supply and Signal Connections).

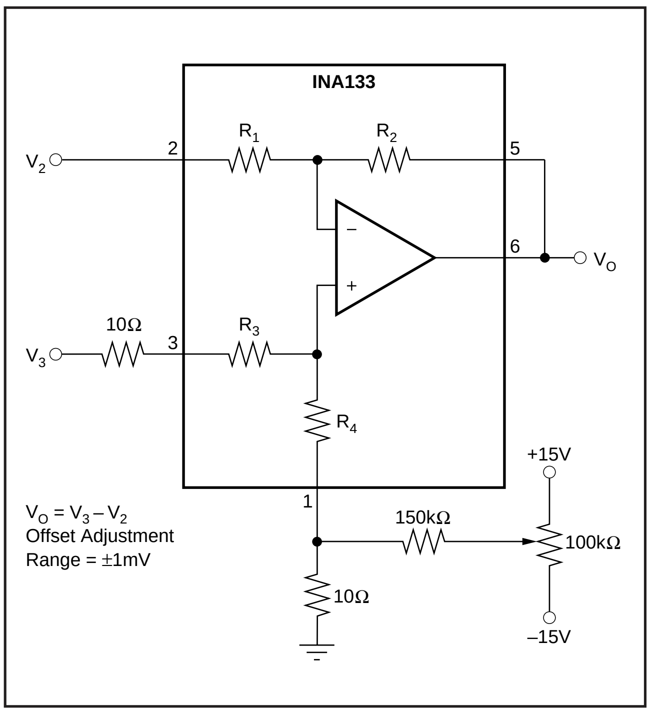
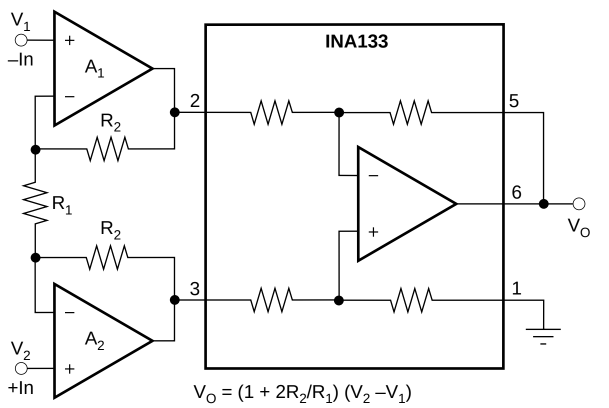


FIGURE 2. Offset Adjustment.

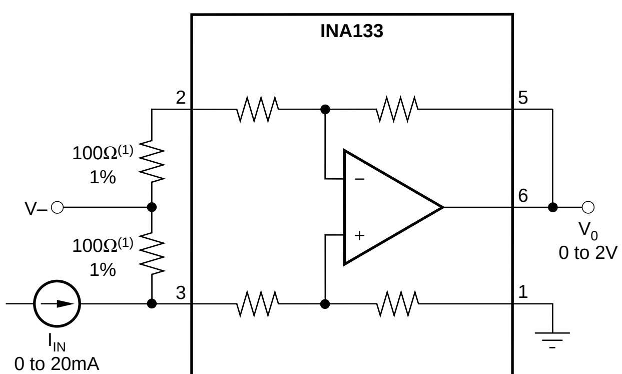
TYPICAL APPLICATIONS



The INA133 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right in the table below.

A_1, A_2	FEATURE	SIMILAR COMPLETE BURR-BROWN IA
OPA2227	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA2277	Low Offset Drift, Low Noise	INA114, INA128
OPA2130	Low Power, FET-Input (pA)	INA121
OPA2234	Single Supply, Precision, Low Power	INA122, INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122, INA126

FIGURE 3. Precision Instrumentation Amplifier.



NOTE: (1) Input series resistors should be less than 250Ω (1% max mismatch) to maintain excellent CMR. With 100Ω resistors, gain error is increased to 0.5%.

FIGURE 4. Current Receiver with Compliance to Rails.

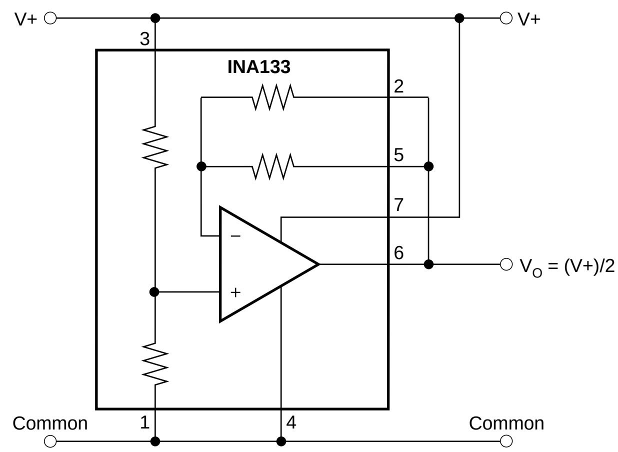


FIGURE 5. Pseudoground Generator.

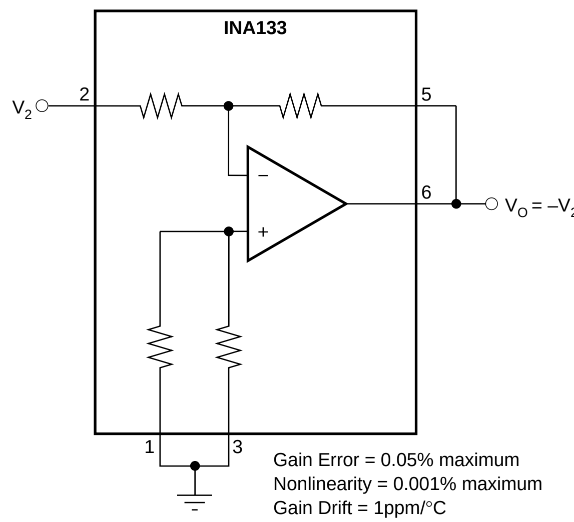


FIGURE 6. Precision Unity-Gain Inverting Amplifier.

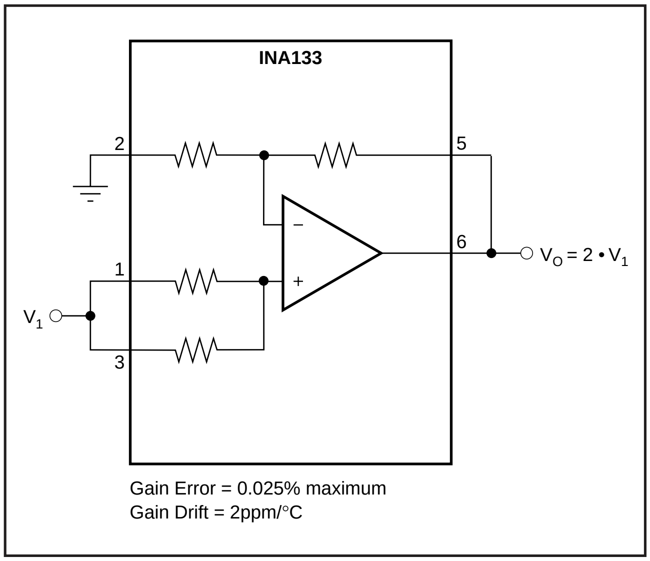


FIGURE 7. Precision Gain = 2 Amplifier.

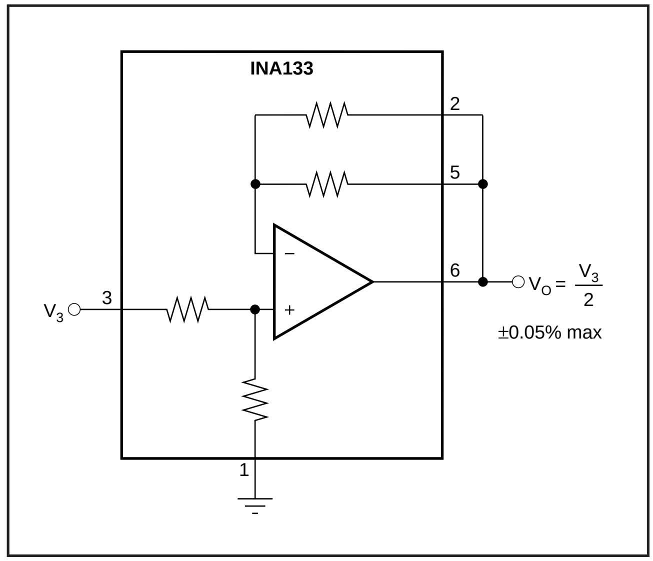


FIGURE 8. Precision Gain = 1/2 Amplifier.

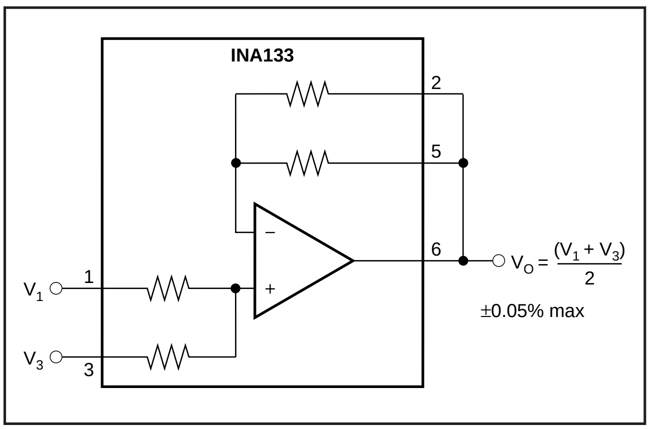


FIGURE 9. Precision Average Value Amplifier.

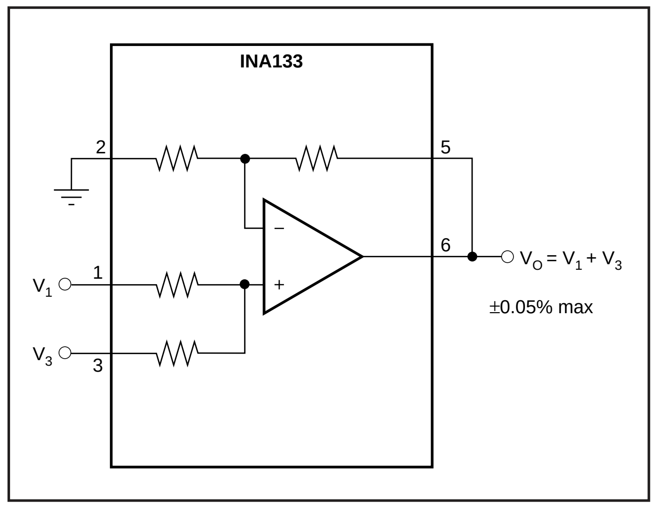


FIGURE 10. Precision Summing Amplifier.

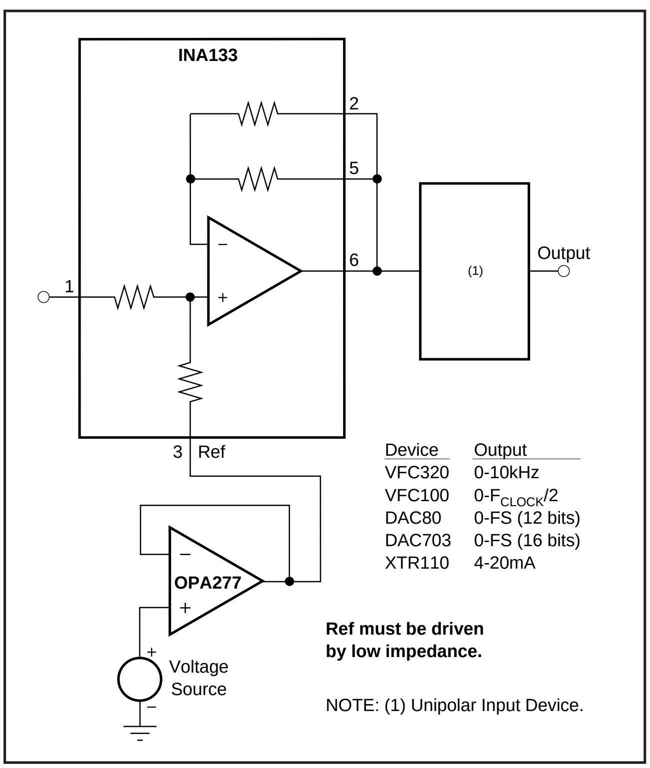


FIGURE 11. Precision Bipolar Offsetting.

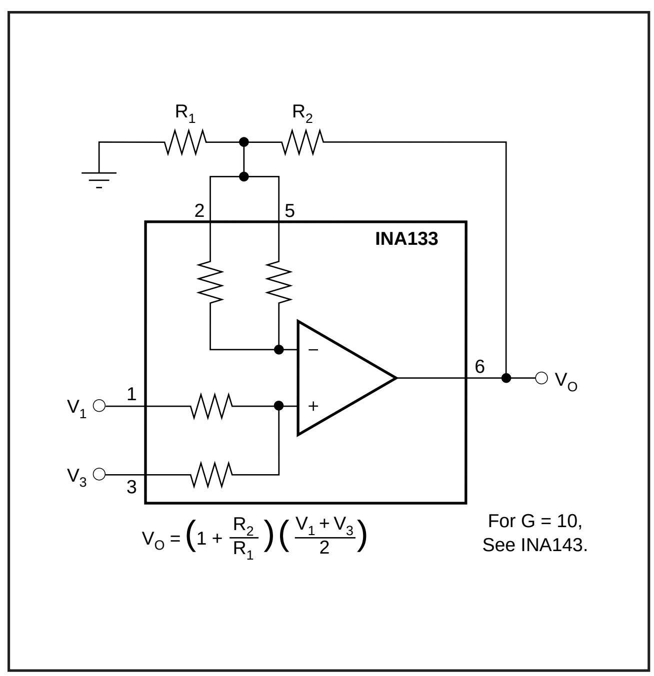


FIGURE 12. Precision Summing Amplifier with Gain.

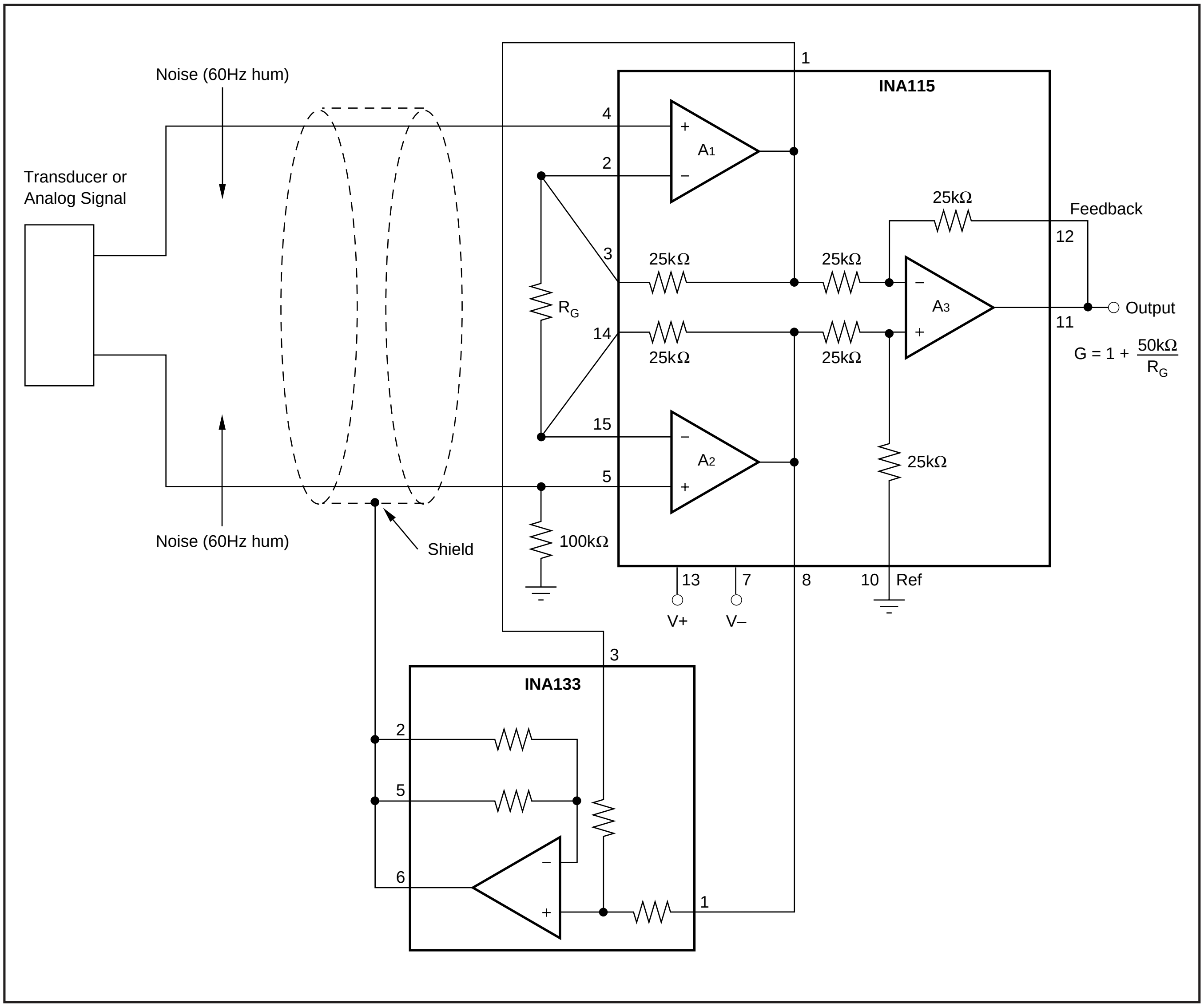


FIGURE 13. Instrumentation Amplifier Guard Drive Generator.

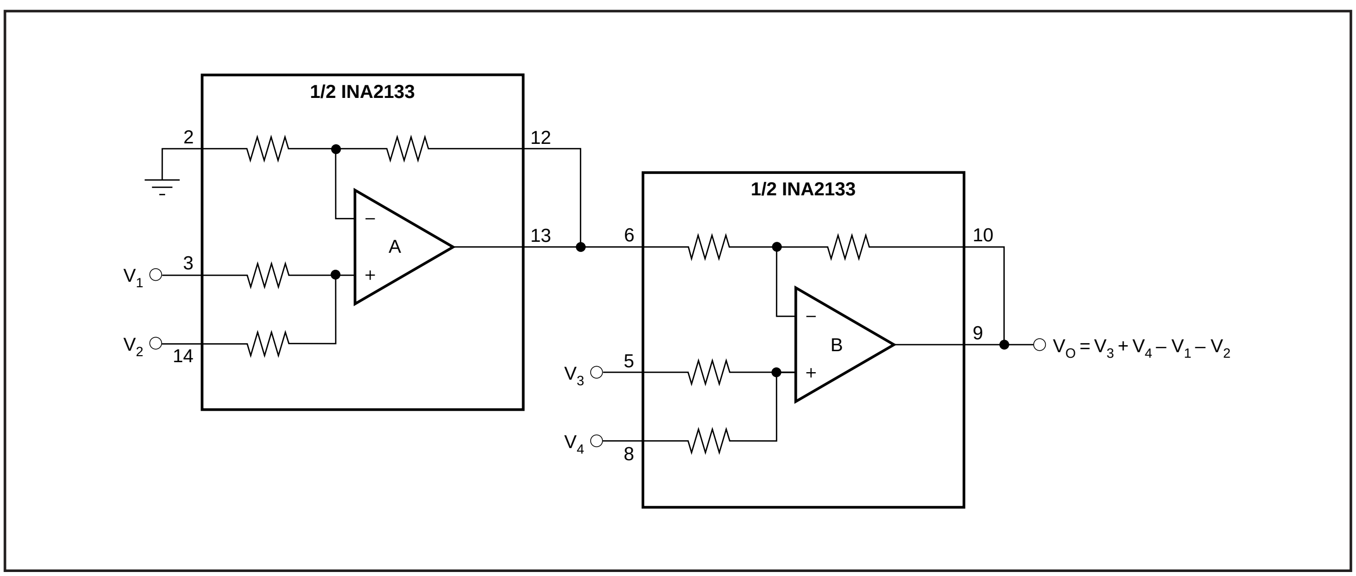


FIGURE 14. Precision Summing Instrumentation Amplifier.

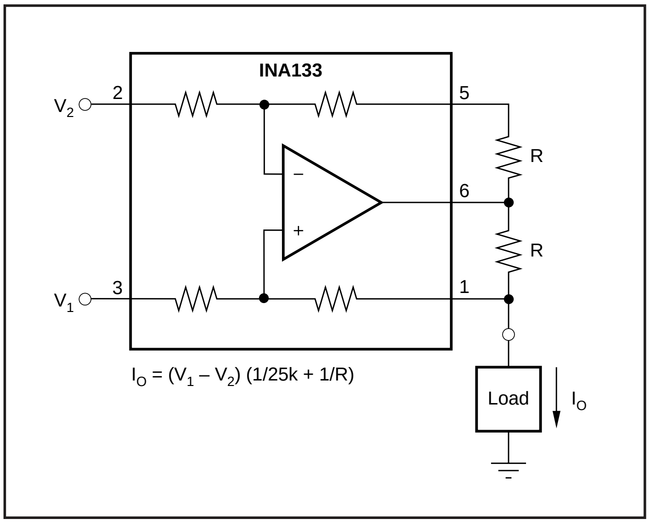


FIGURE 15. Precision Voltage-to-Current Converter with Differential Inputs.

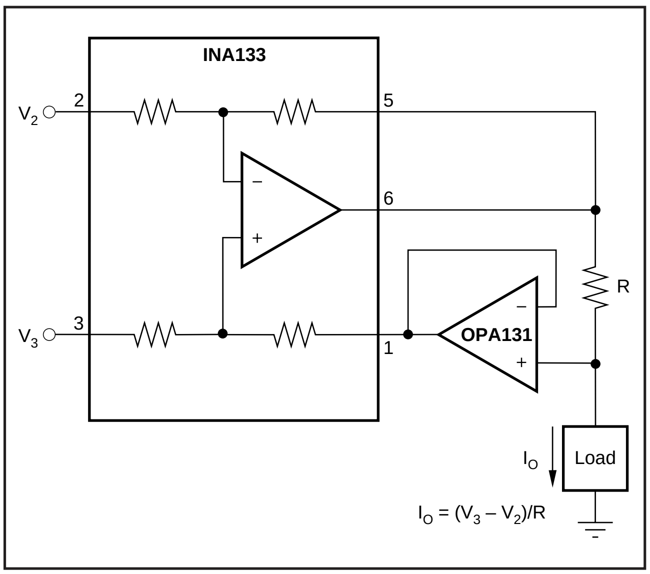


FIGURE 16. Differential Input Voltage-to-Current Converter for Low I_{OUT}.

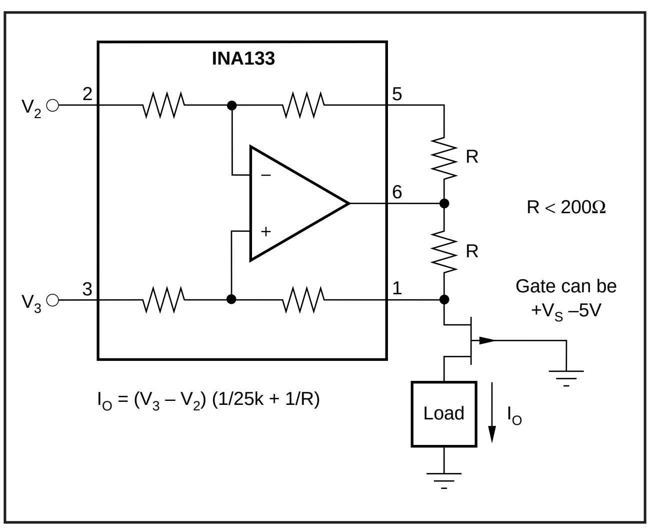


FIGURE 17. Isolating Current Source.

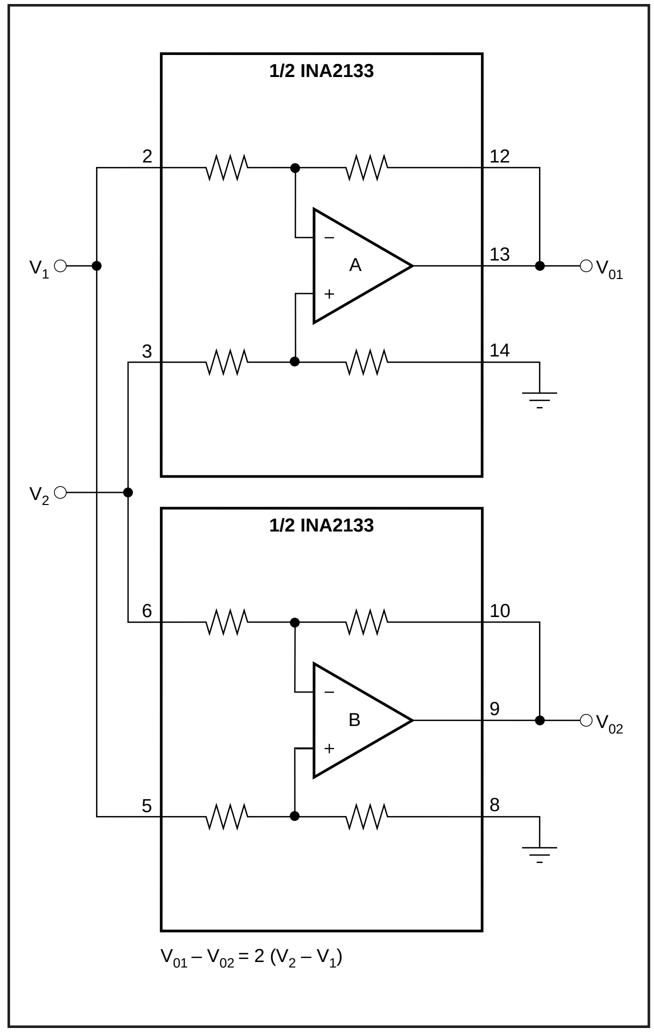


FIGURE 18. Differential Output Difference Amplifier.

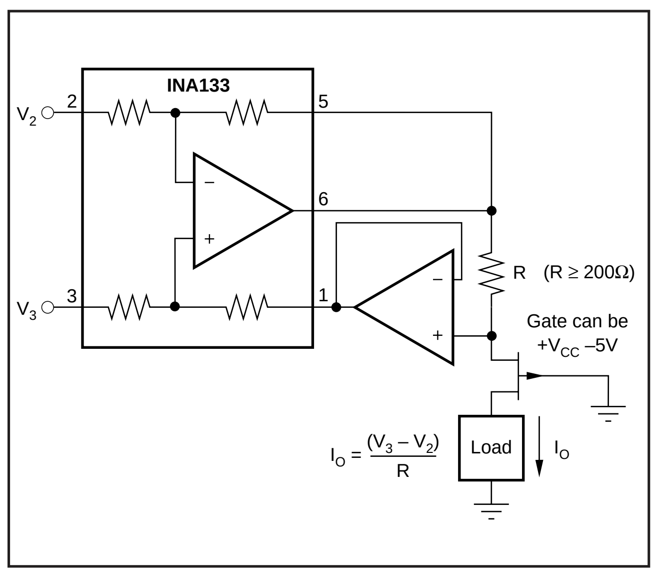


FIGURE 19. Isolating Current Source with Buffering Amplifier for Greater Accuracy.

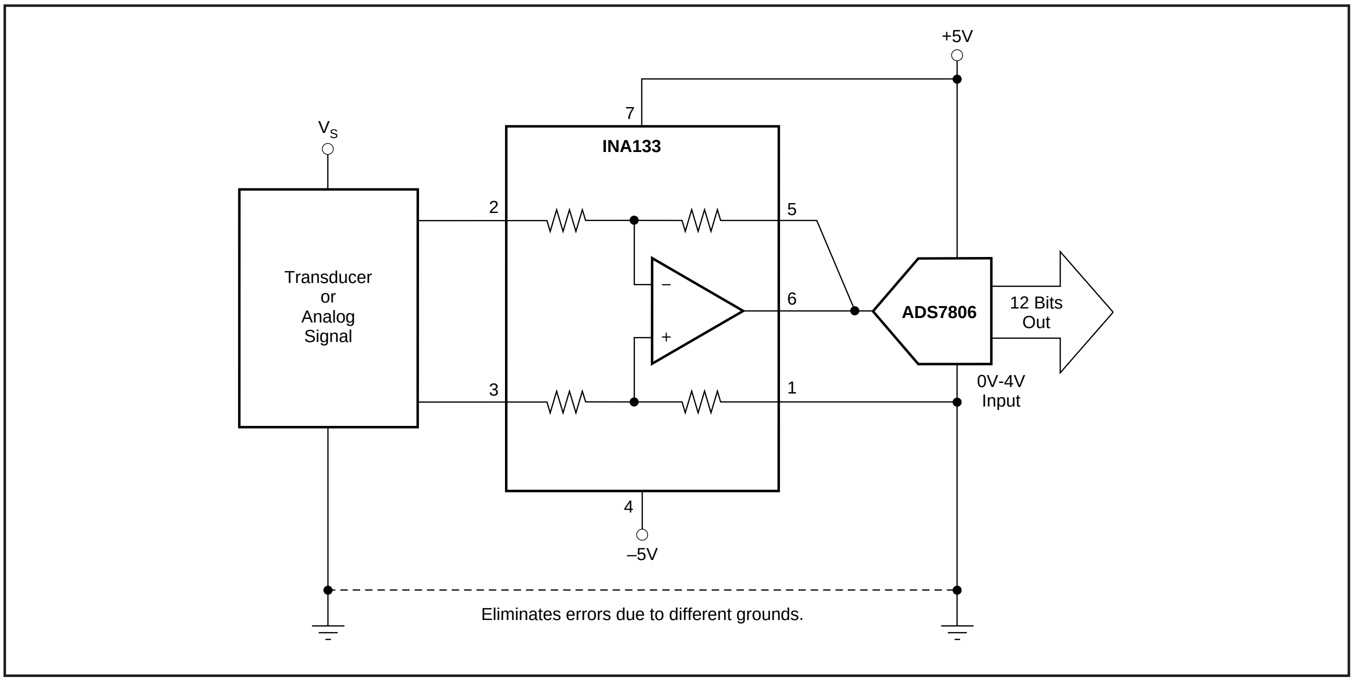


FIGURE 20. Differential Input Data Acquisition.

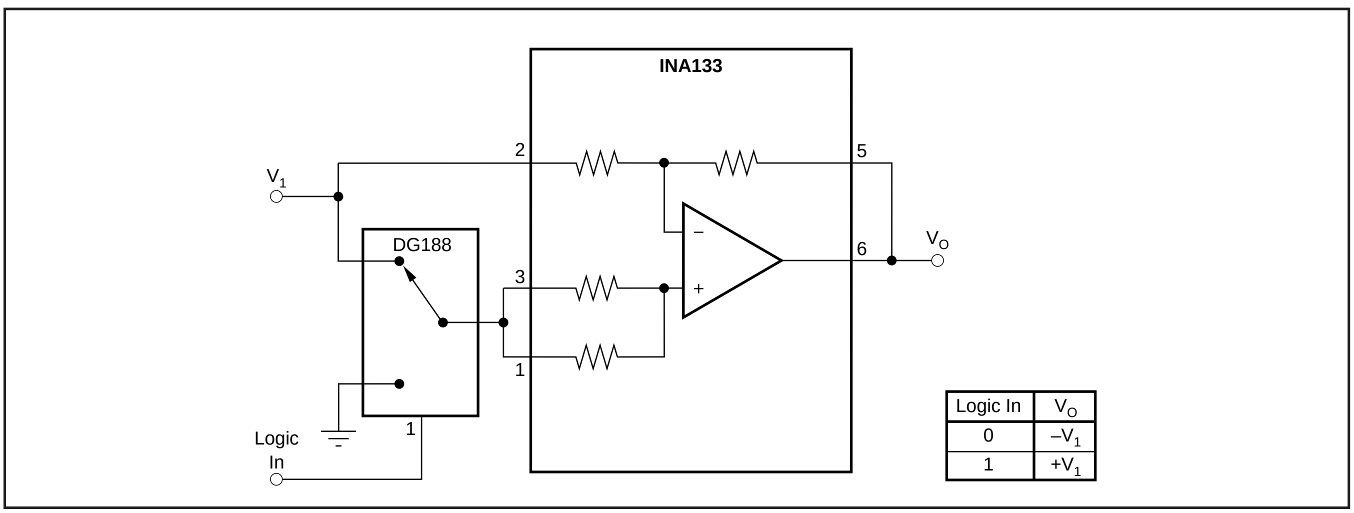


FIGURE 21. Digitally Controlled Gain of ±1 Amplifier.

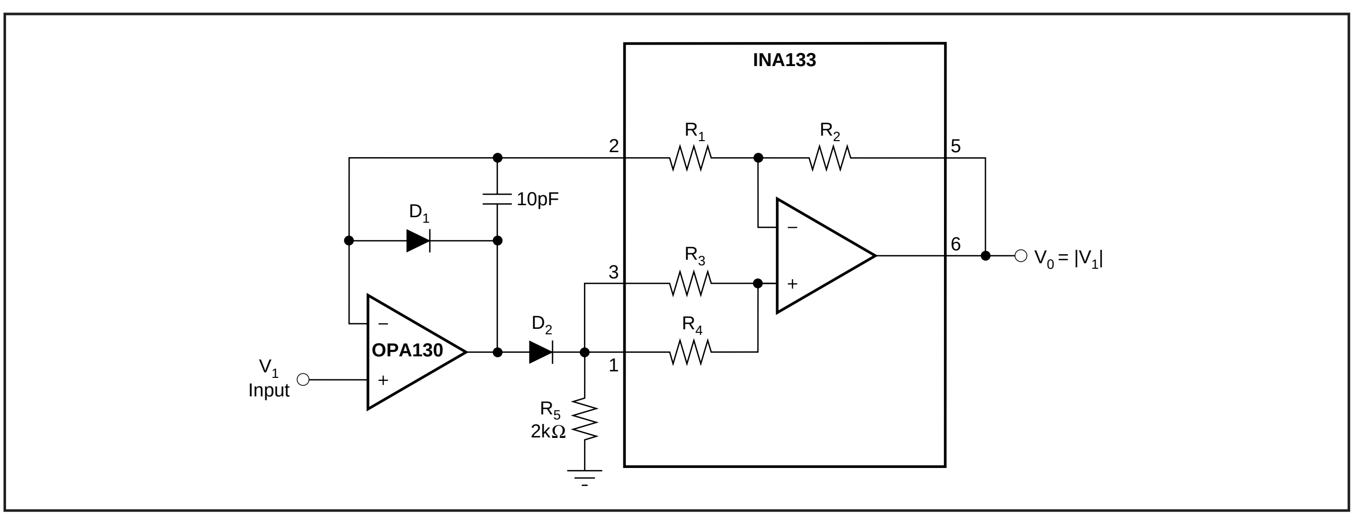


FIGURE 22. Precision Absolute Value Buffer.

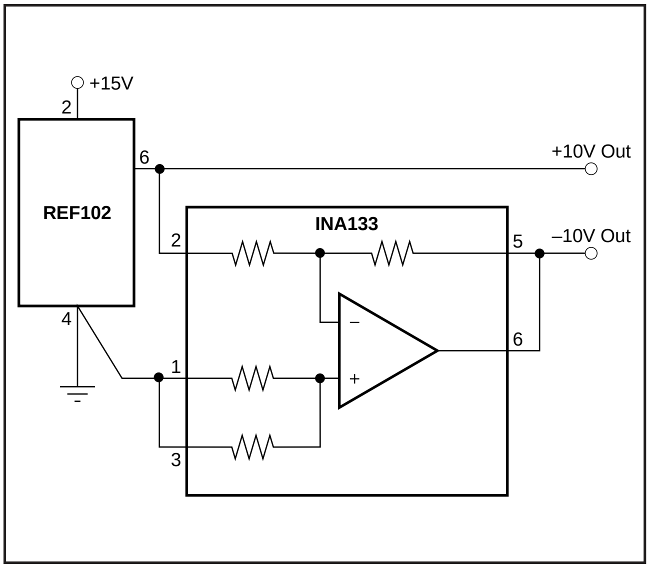


FIGURE 23. ±10V Precision Voltage Reference.

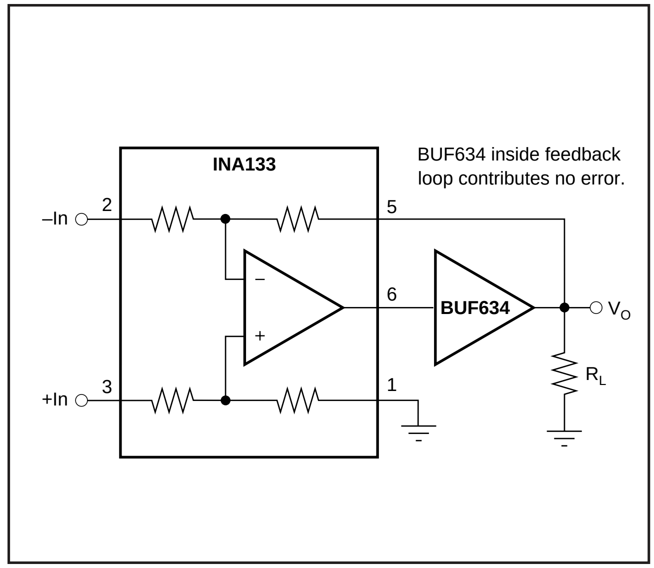


FIGURE 24. High Output Current Precision Difference Amplifier.

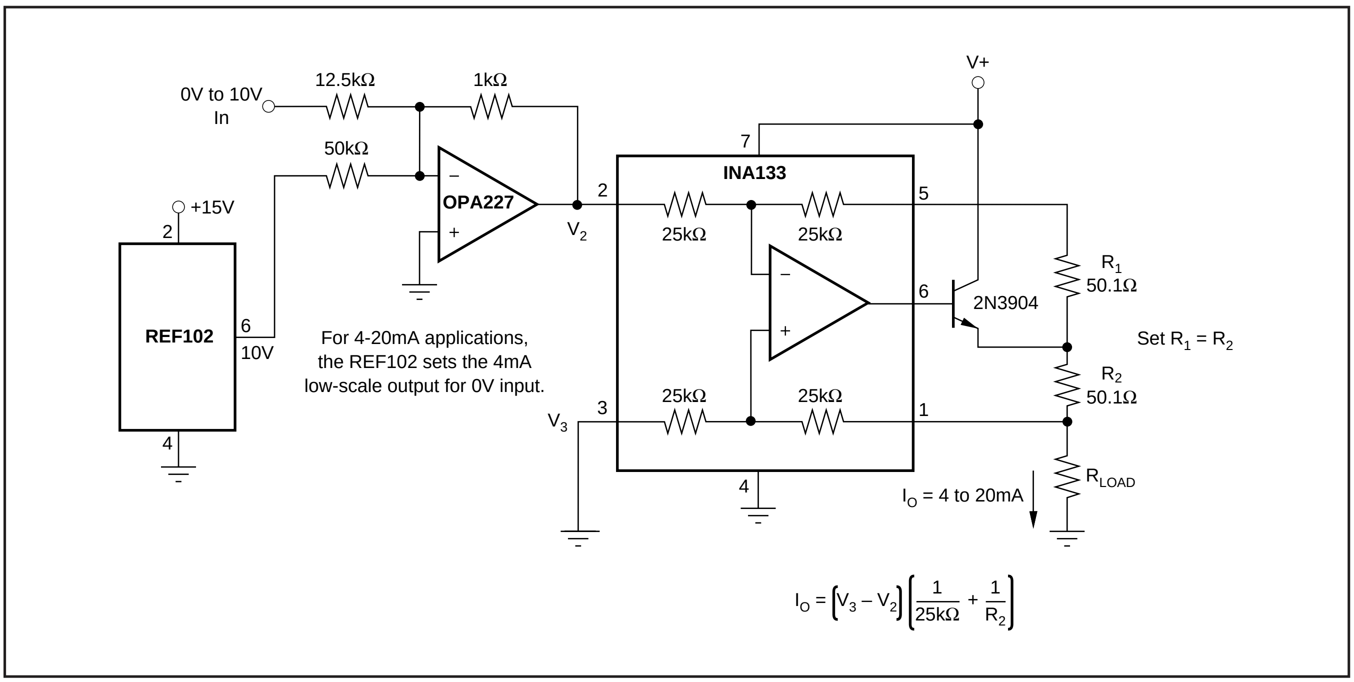


FIGURE 25. Precision Voltage-to-Current Conversion.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA133U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 133U	Samples
INA133U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 133U	Samples
INA133UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 133U A	Samples
INA133UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		INA 133U A	Samples
INA133UE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 133U	
INA2133U	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U	Samples
INA2133UA	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U A	Samples
INA2133UE4	LIFEBUY	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2133U	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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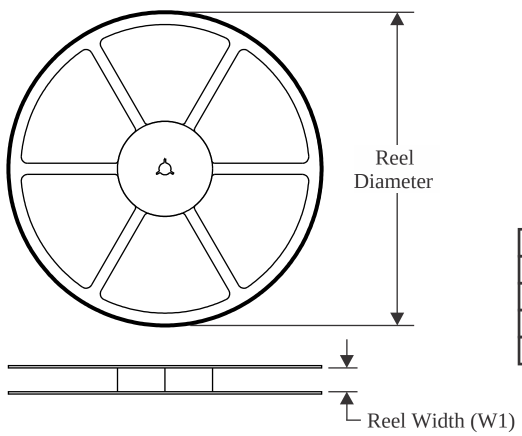
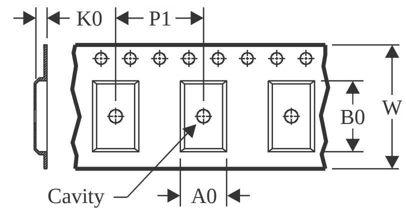
TAPE AND REEL INFORMATION

REEL DIMENSIONS

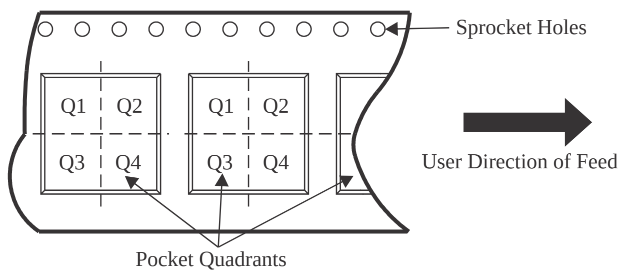


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

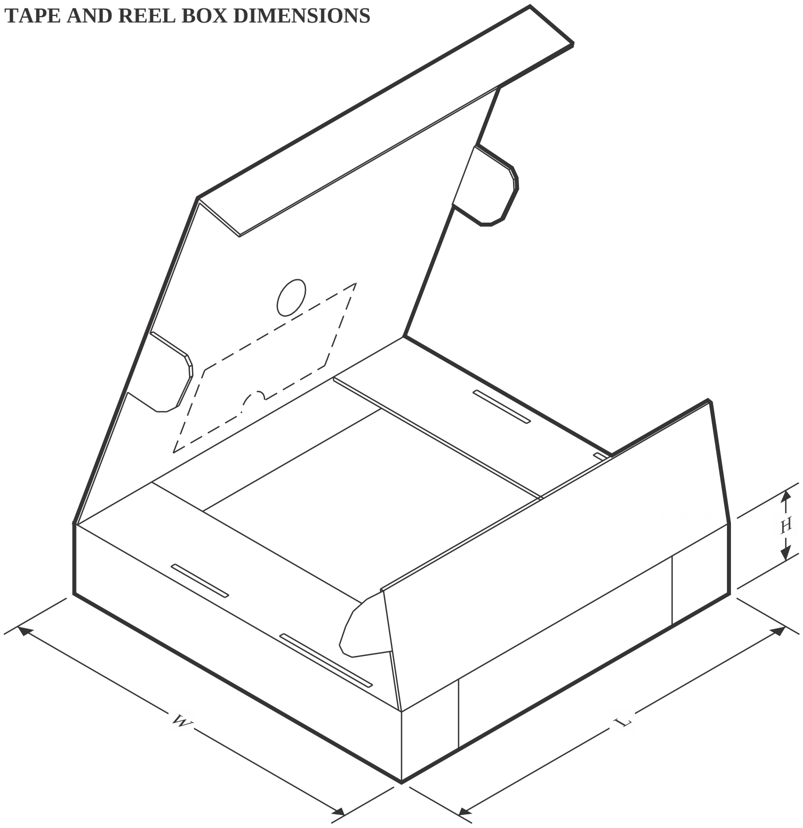
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA133U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA133UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

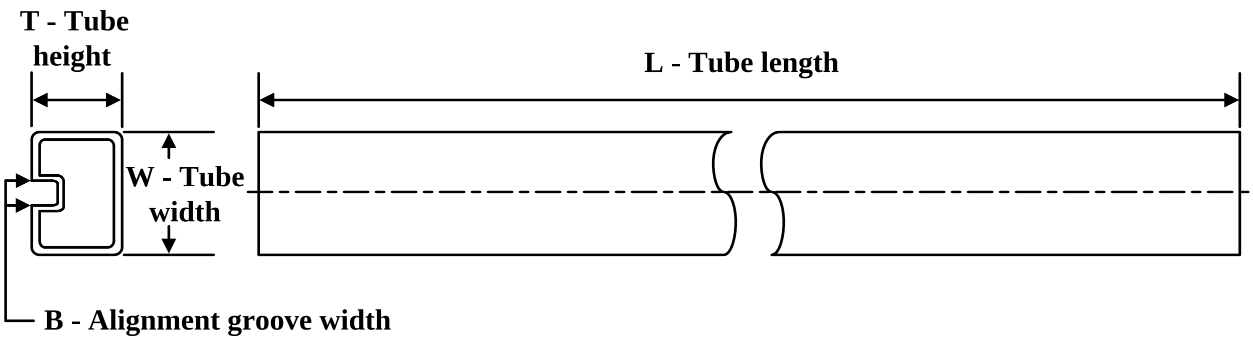
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA133U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA133UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA133U	D	SOIC	8	75	506.6	8	3940	4.32
INA133UA	D	SOIC	8	75	506.6	8	3940	4.32
INA133UE4	D	SOIC	8	75	506.6	8	3940	4.32
INA2133U	D	SOIC	14	50	506.6	8	3940	4.32
INA2133UA	D	SOIC	14	50	506.6	8	3940	4.32
INA2133UE4	D	SOIC	14	50	506.6	8	3940	4.32