DAC3283 Dual-Channel, 16-Bit, 800 MSPS, Digital-to-Analog Converter (DAC)

1 Features

- Dual, 16-Bit, 800 MSPS DACs
- 8-Bit Input LVDS Data Bus
  - Byte-Wide Interleaved Data Load
  - 8 Sample Input FIFO
  - Optional Data Pattern Checker
- Multi-DAC Synchronization
- Selectable 2x-4x Interpolation Filters
  - Stop-Band Attenuation > 85 dB
- Fs/2 and ± Fs/4 Coarse Mixer
- Digital Quadrature Modulator Correction
  - Gain, Phase and Offset Correction
- Temperature Sensor
- 3- or 4-Wire Serial Control Interface
- On-Chip 1.2-V Reference
- Differential Scalable Output: 2 to 20 mA
- Single-Carrier TM1 WCDMA ACLR: 82 dBc at f_{OUT} = 122.88 MHz
- Low Power: 1.3 W at 800 MSPS
- Space Saving Package: 48-pin 7×7mm QFN

2 Applications

- Cellular Base Stations
- Diversity Transmit
- Wideband Communications
- Digital Synthesis

3 Description

The DAC3283 is a dual-channel 16-bit 800 MSPS digital-to-analog converter (DAC) with an 8-bit LVDS input data bus with on-chip termination, optional 2x-4x interpolation filters, digital IQ compensation and internal voltage reference. The DAC3283 offers superior linearity, noise and crosstalk performance.

Input data can be interpolated by 2x or 4x through on-chip interpolating FIR filters with over 85 dB of stop-band attenuation. Multiple DAC3283 devices can be fully synchronized.

The DAC3283 allows either a complex or real output. An optional coarse mixer in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. The digital IQ compensation feature allows optimization of phase, gain and offset to maximize sideband rejection and minimize LO feed-through of an external quadrature modulator performing the final single sideband RF up-conversion.

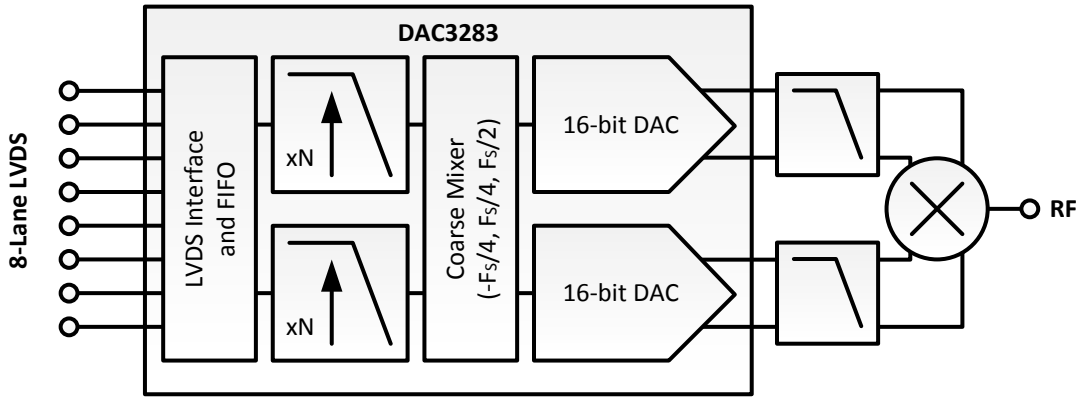
The DAC3283 is characterized for operation over the entire industrial temperature range of –40°C to 85°C and is available in a 48-pin 7×7mm QFN package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC3283	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2012) to Revision C — **Page**

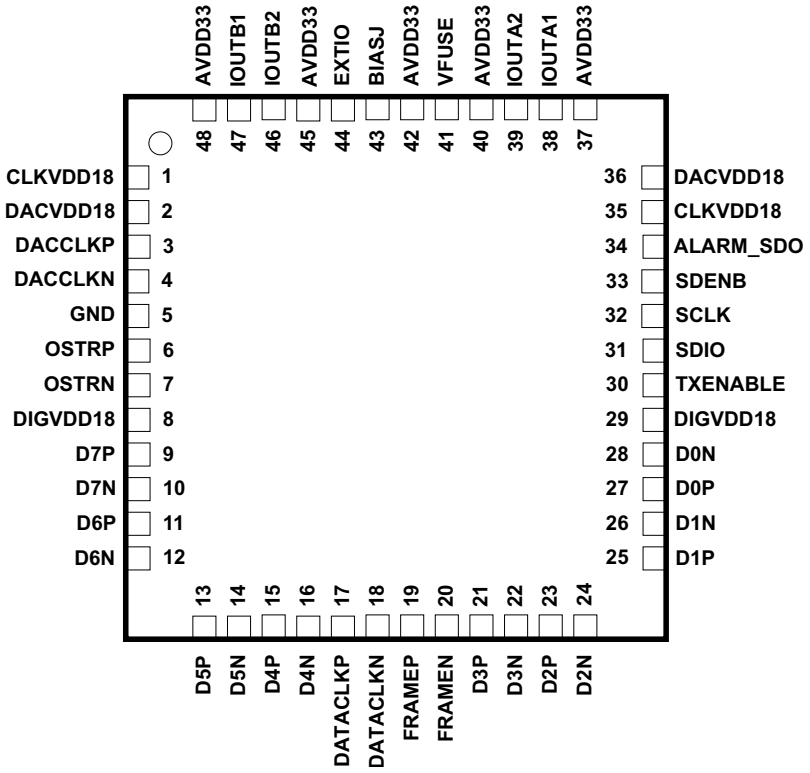
- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Moved WCDMA plots from *Typical Characteristics* to *Application Performance Plots* ... 55

Changes from Revision A (April 2010) to Revision B — **Page**

- Changed SDIO description in *Terminal Functions Table*: SDIO is bidirectional for both 3-pin mode and 4-pin mode. ... 5
- Changed *Serial Interface* section for SDIO operation: first paragraph, "data in only" to "bidirectional" ... 17
- Changed *Serial Interface* section for SDIO operation: paragraph following Figure 26, "ALARM_SDO is " to "both ALARM_SDO and SDIO are" ... 19
- Changed Figure 29 ... 20
- Added text to the *Input FIFO* section beginning at 4th paragraph after Figure 29 ... 20
- Changed Figure 30 ... 21
- Added config19 - multi_sync_sel to *FIFO Modes of Operation* section. ... 22
- Changed Table 3 ... 22
- Added *Dual Sync Souces Mode* and *Single Sync Source Mode* sections ... 22
- Changed the *Data Pattern Checker* section ... 24
- Changed Figure 35 ... 25
- Changed the *DATACLK Monitor* section ... 25
- Changed –3.75 to +3.75 degrees to –7.125 to +7.125 degrees in *Quadrature Modulation Correction (QMC)* section ... 31
- Changed CONFIG31 default from 0x52 to 0x12 ... 40
- Changed Register CONFIG0 Bit 7 to Reserved, also changed Bit 5 function to Allows the FRAME input to reset the FIFO write pointer when asserted. Changed Bit 4 function first sentence to Allows the FRAME or OSTR signal to reset the FIFO read pointer when asserted. ... 41
- Changed in Register CONFIG2 Bit 4, Function description from Normal FIFO_ISTR to Normal FRAME ... 42

6 Pin Configuration and Functions

RGZ (VQFN) Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD33	37, 40, 42, 45, 48	I	Analog supply voltage. (3.3 V)
ALARM_SDO	34	O	1.8V CMOS output for ALARM condition. The ALARM output functionality is defined through the CONFIG6 register. Default polarity is active low, but can be changed to active high via CONFIG0 **alarm_pol** control bit. Optionally, it can be used as the uni-directional data output in 4-pin serial interface mode (CONFIG 23 **sif4_ena** = '1').
BIASJ	43	O	Full-scale output current bias. For 20mA full-scale output current, connect a 960Ω resistor to GND.
CLKVDD18	1, 35	I	Internal clock buffer supply voltage. (1.8 V) It is recommended to isolate this supply from DACVDD18 and DIGVDD18.
D[7..0]P	9, 11, 13, 15, 21, 23, 25, 27	I	LVDS positive input data bits 0 through 7. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR) with two data transfers per DATACKP/N clock cycle. Dual channel 16-bit data is transferred byte-wide on this single 8-bit data bus using FRAMEP/N as a frame strobe indicator. D7P is most significant data bit (MSB) – pin 9 D0P is least significant data bit (LSB) – pin 27 The order of the bus can be reversed via CONFIG19 **rev** bit.
D[7..0]N	10, 12, 14, 16, 22, 24, 26, 28	I	LVDS negative input data bits 0 through 15. (See D[7:0]P description above) D7N is most significant data bit (MSB) – pin 10 D0N is least significant data bit (LSB) – pin 28
DACCLKP	3	I	Positive external LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18/2.
DACCLKN	4	I	Complementary external LVPECL clock input for DAC core. (see the DACCLKP description)
DACVDD18	2, 36	I	DAC core supply voltage. (1.8 V) It is recommended to isolate this supply from CLKVDD18 and DIGVDD18.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DATACLKP	17	I	LVDS positive input data clock. This positive/negative pair has an internal 100 Ω termination resistor. Input data D[7:0]P/N is latched on both edges of DATACLKP/N (Double Data Rate) with two data transfers input per DATACLKP/N clock cycle.
DATACLKN	18	I	LVDS negative input data clock. (See DATACLKP description)
DIGVDD18	8, 29	I	Digital supply voltage. (1.8V) It is recommended to isolate this supply from CLKVDD18 and DACVDD18.
EXTIO	44	I/O	Used as external reference input when internal reference is disabled through CONFIG25 **extref_ena** = '1'. Used as internal reference output when CONFIG25 **extref_ena** = '0' (default). Requires a 0.1µF decoupling capacitor to AGND when used as reference output.
FRAMEP	19	I	LVDS frame indicator positive input. This positive/negative pair has an internal 100Ω termination resistor. This signal is captured with the rising edge of DATACLKP/N and used to indicate the beginning of the frame. It is also used as a reset signal by the FIFO. The FRAMEP/N signal should be edge-aligned with D[7:0]P/N.
FRAMEN	20	I	LVDS frame indicator negative input. (See the FRAMEN description)
GND	5, Thermal Pad	I	Pin 5 and the Thermal Pad located on the bottom of the QFN package is ground for all supplies.
IOUTA1	38	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current sink and the most positive voltage on the IOUTA1 pin.
IOUTA2	39	O	A-Channel DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0 mA sink and the most positive voltage on the IOUTA2 pin.
IOUTB1	47	O	B-Channel DAC current output. Refer to IOUTA1 description above.
IOUTB2	46	O	B-Channel DAC complementary current output. Refer to IOUTA2 description above.
OSTRP	6	I	LVPECL output strobe positive input. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left floating.
OSTRN	7	I	LVPECL output strobe negative input. (See the OSTRP description)
SCLK	32	I	1.8V CMOS serial interface clock. Internal pull-down.
SDENB	33	I	1.8V CMOS active low serial data enable, always an input to the DAC3283. Internal pull-up.
SDIO	31	I/O	1.8V CMOS serial interface data. Bi-directional in both 3-pin mode (default) and 4-pin mode. Internal pull-down.
TXENABLE	30	I	1.8V CMOS active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pull-down.
VFUSE	41	I	Digital supply voltage. (1.8V) This supply pin is also used for factory fuse programming. **Connect to DACVDD18 pins for normal operation.**

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	DACDVDD18 (2)	–0.5	2.3	V
	DIGVDD18 (2)	–0.5	2.3	V
	CLKVDD18 (2)	–0.5	2.3	V
	VFUSE (2)	–0.5	2.3	V
	AVDD33 (2)	–0.5	4	V
Terminal voltage range	CLKVDD18 to DIGDVDD18	–0.5	0.5	V
	DACVDD18 TO DIGVDD18	–0.5	0.5	V
	D[7..0]P ,D[7..0]N, DATACLKP, DATACLKN, FRAMEP, FRAMEN (2)	–0.5	DIGVDD18 + 0.5	V
	DACCLKP, DACCLKN, OSTRP, OSTRN (2)	–0.5	CLKVDD18 + 0.5	V
	ALARM_SDO, SDIO, SCLK, SDENB, TXENABLE (2)	–0.5	DIGCLKVDD18 + 0.5	V
	IOUTA1/B1, IOUTA2/B2 (2)	–1.0	AVDD33 + 0.5	V
	EXTIO, BIASJ (2)	–0.5	AVDD33 + 0.5	V
Peak input current (any input)			20	mA
Peak total input current (all inputs)			–30	mA
Operating free-air temperature range, T_A: DAC3283		–40	85	°C
Storage temperature range, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	1.8-V DAC core supply voltage, DACDVDD18	1.7	1.8	1.9	V
	1.8-V digital supply voltage, DIGVDD18	1.7	1.8	1.9	V
	1.8-V internal clock buffer supply voltage, CLKVDD18	1.7	1.8	1.9	V
	3.3-V analog supply voltage, AVDD33	3.0	3.3	3.6	V

7.4 Thermal Information

THERMAL METRIC (1)		RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics – DC Specifications

over operating free-air temperature range, nominal supplies, IOUTFS = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			16			Bits
DC ACCURACY						
DNL	Differential nonlinearity	1 LSB = IOUTFS/2^{16}		±2		LSB
INL	Integral nonlinearity			±4		
ANALOG OUTPUT						
	Coarse gain linearity			±0.04		LSB
	Offset error	Mid code offset		±0.01		%FSR
	Gain error	With external reference		±2		%FSR
		With internal reference		±2		%FSR
	Gain mismatch	With internal reference	–2		2	%FSR
	Minimum full scale output current	Nominal full-scale current, IOUTFS = 16 x IBIAS current.		2		mA
	Maximum full scale output current			20		mA
	Output compliance range (1)	IOUTFS = 20 mA	AVDD –0.5V		AVDD +0.5V	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
REFERENCE OUTPUT						
V_{ref}	Reference output voltage		1.14	1.2	1.26	V
	Reference output current (2)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage range	External reference mode	0.1	1.2	1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth			472		kHz
	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift	With external reference		±1		ppm of FSR/°C
	Gain drift	With internal reference		±15		ppm of FSR/°C
				±30		
	Reference voltage drift			±8		ppm/°C
POWER SUPPLY						
	AVDD33		3.0	3.3	3.6	V
	DACVDD18, DIGVDD18, CLKVDD18		1.7	1.8	1.9	V
$I_{(AVDD33)}$	Analog supply current	Mode 1 (below)		149		mA
$I_{(DIGDVDD)}$	Digital supply current			340		mA
$I_{(DACVDD18)}$	DAC supply current			55		mA
$I_{(CLKVDD18)}$	Clock supply current			37		mA
P	Power dissipation	Mode 1: f_{DAC} = 800MSPS, 4x interpolation, Fs/4 mixer on, QMC on		1300	1450	mW
		Mode 2: f_{DAC} = 491.52MSPS, 2x interpolation, Mixer off, QMC on		1000		mW
		Mode 3: Sleep mode f_{DAC} = 800MSPS, 4x interpolation, Fs/4 mixer on, CONFIG24 **sleepa, sleepb** set = 1		750		mW
		Mode 4: Power-Down mode No clock, static data pattern, CONFIG23 **clkpath_sleep_a, clkpath_sleepb** set = 1 CONFIG24 **clkrecv_sleep, sleepa, sleepb** set = 1		7	18	mW
PSRR	Power supply rejection ratio	DC tested		±0.2		%FSR/V
T	Operating range		–40	25	85	°C

(1) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC3283 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(2) Use an external buffer amplifier with high impedance input to drive any external load.

7.6 Electrical Characteristics – AC Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT(1)						
f_{DAC}	Maximum DAC output update rate	1x Interpolation	312.5			MSPS
		2x Interpolation	625			
		4x Interpolation	800			
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10.4		ns
t_{pd}	Output propagation delay	DAC outputs are updated on the falling edge of DAC clock. Does not include digital latency (see below).		2		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			220		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%			220		ps
Power-up time	DAC wake-up time	IOUT current settling to 1% of IOUTFS. Measured from SDENB rising edge; Register CONFIG24, toggle **sleepa** from 1 to 0.		90		µs
	DAC sleep time	IOUT current settling to less than 1% of IOUTFS. Measured from SDENB rising edge; Register CONFIG24, toggle **sleepa** from 0 to 1.		90		
	Digital latency	1x Interpolation		59		DAC clock cycles
		2x Interpolation		139		
		4x Interpolation		290		
		QMC		24		
AC PERFORMANCE(2)						
SFDR	Spurious free dynamic range (0 to f_{DAC}/2)Tone at 0 dBFS	f_{DAC} = 800 MSPS, f_{OUT} = 20.1 MHz		85		dBc
		f_{DAC} = 800 MSPS, f_{OUT} = 50.1 MHz		76		
		f_{DAC} = 800 MSPS, f_{OUT} = 70.1 MHz		72		
IMD3	Third-order two-tone intermodulation distortion Each tone at –12 dBFS	f_{DAC} = 800 MSPS, f_{OUT} = 30 ± 0.5 MHz		93		dBc
		f_{DAC} = 800 MSPS, f_{OUT} = 50 ± 0.5 MHz		90		
		f_{DAC} = 800 MSPS, f_{OUT} = 100 ± 0.5 MHz		86		
NSD	Noise spectral density tone at 0dBFS	f_{DAC} = 800 MSPS, f_{OUT} = 10.1 MHz		162		dBc/Hz
		f_{DAC} = 800 MSPS, f_{OUT} = 80.1 MHz		160		
WCDMA(3)	Adjacent channel leakage ratio, single carrier	f_{DAC} = 737.28 MSPS, f_{OUT} = 30.72MHz		85		dBc
		f_{DAC} = 737.28 MSPS, f_{OUT} = 153.6MHz		81		
	Alternate channel leakage ratio, single carrier	f_{DAC} = 737.28 MSPS, f_{OUT} = 30.72MHz		91		dBc
		f_{DAC} = 737.28 MSPS, f_{OUT} = 153.6MHz		85		
	Channel isolation	f_{DAC} = 800 MSPS, f_{OUT} = 10MHz		84		dBc

(1) Measured single-ended into 50Ω load.
(2) 4:1 transformer output termination, 50Ω doubly terminated load
(3) Single carrier, W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at f_{OUT}, PAR = 12dB. TESTMODEL 1, 10 ms

7.7 Electrical Characteristics – Digital Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS INTERFACE:D[7:0]P/N, DATACLKP/N, FRAMEP/N (1)						
f_{DATA}	Input data rate	Byte-wide DDR format DATACLK frequency = 625 MHz			312.5	MSPS
f_{BUS}	Byte-wide LVDS data transfer rate				1250	MSPS
$V_{A,B+}$	Logic high differential input voltage threshold		150	400		mV
$V_{A,B-}$	Logic low differential input voltage threshold		–150	–400		mV
V_{COM}	Input common mode		0.9	1.2	1.5	V
Z_T	Internal termination		85	110	135	Ω
C_L	LVDS Input capacitance			2		pF
TIMING LVDS INPUTS: DATACLKP/N DOUBLE EDGE LATCHING – See Figure 40						
$t_{s(DATA)}$	Setup time, D[7:0]P/N and FRAMEP/N, valid to either edge of DATACLKP/N	FRAMEP/N latched on rising edge of DATACLKP/N only	–25			ps
$t_{h(DATA)}$	Hold time, D[7:0]P/N and FRAMEP/N, valid after either edge of DATACLKP/N	FRAMEP/N latched on rising edge of DATACLKP/N only	375			ps
$t_{(FRAME)}$	FRAMEP/N pulse width	$f_{DATACLK}$ is DATACLK frequency in MHz	$1/2f_{DATACLK}$			ns
$t_{\_align}$	Maximum offset between DATACLKP/N and DACCLKP/N rising edges	FIFO bypass mode only f_{DACCLK} is DACCLK frequency in MHz			$1/2f_{DACCLK}$ –0.55	ns
CLOCK INPUT (DACCLKP/N)						
	Duty cycle		40%		60%	
	Differential voltage (2)		0.4	1.0		V
	DACCLKP/N Input Frequency				800	MHz
OUTPUT STROBE (OSTRP/N)						
f_{OSTR}	Frequency	$f_{OSTR} = f_{DACCLK} / (n \times 8 \times Interp)$ where n is any positive integer f_{DACCLK} is DACCLK frequency in MHz			f_{DACCLK} / (8 x interp)	
	Duty cycle		40%		60%	
	Differential voltage		0.4	1.0		V
TIMING OSTRP/N INPUT: DACCLKP/N RISING EDGE LATCHING						
$t_{s(OSTR)}$	Setup time, OSTRP/N valid to rising edge of DACCLKP/N			200		ps
$t_{h(OSTR)}$	Hold time, OSTRP/N valid after rising edge of DACCLKP/N			200		ps
CMOS INTERFACE: ALARM_SDO, SDIO, SCLK, SDENB, TXENABLE						
V_{IH}	High-level input voltage		1.25			V
V_{IL}	Low-level input voltage				0.54	V
I_{IH}	High-level input current		–40		40	µA
I_{IL}	Low-level input current		–40		40	µA
CI	CMOS input capacitance			2		pF
V_{OH}	ALARM_SDO, SDIO	I_{load} = –100 µA	DIGVDD18 –0.2			V
		I_{load} = –2mA	0.8 x DIGVDD18			V
V_{OL}	ALARM_SDO, SDIO	I_{load} = 100 µA			0.2	V
		I_{load} = 2 mA			0.5	V

(1) See LVDS INPUTS section for terminology.
(2) Driving the clock input with a differential voltage lower than 1V will result in degraded performance.

7.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SERIAL PORT TIMING – See Figure 26 and Figure 27						
$t_{s(SDENB)}$	Setup time, SDENB to rising edge of SCLK		20			ns
$t_{s(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK		10			ns
$t_{h(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK		5			ns
$t_{(SCLK)}$	Period of SCLK	Register CONFIG5 read (temperature sensor read)	1			µs
		All other registers	100			ns
$t_{(SCLKH)}$	High time of SCLK	Register CONFIG5 read (temperature sensor read)	0.4			µs
		All other registers	40			ns
$t_{(SCLKL)}$	Low time of SCLK	Register CONFIG5 read (temperature sensor read)	0.4			µs
		All other registers	40			ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			10		ns

7.9 Typical Characteristics

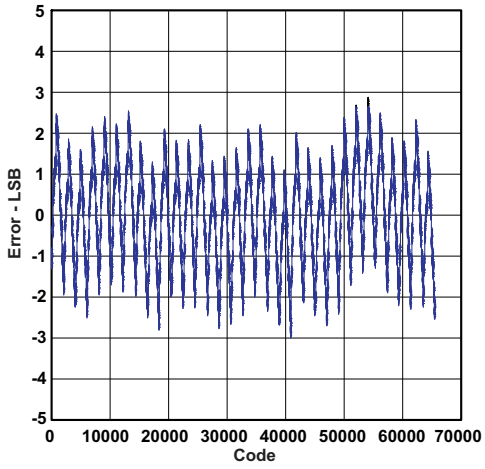


Figure 1. Integral Non-Linearity

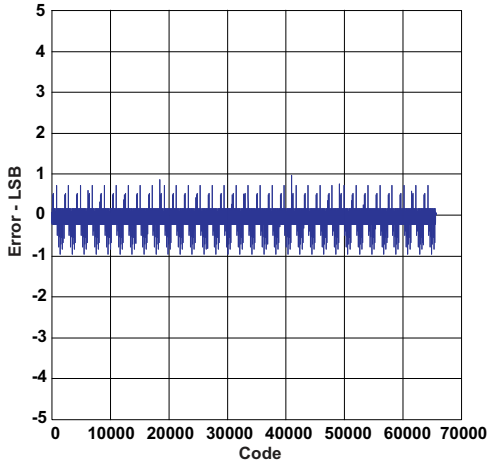


Figure 2. Differential Non-Linearity

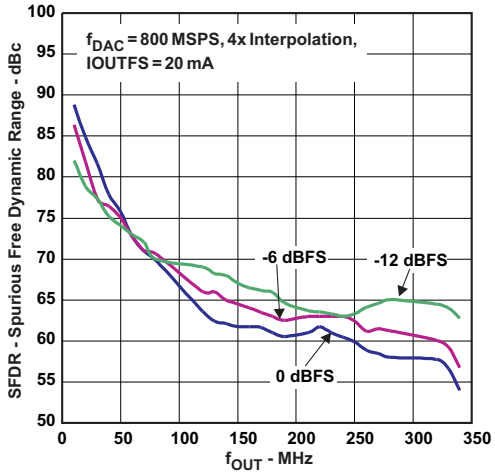


Figure 3. Spurious Free Dynamic Range vs Input Scale

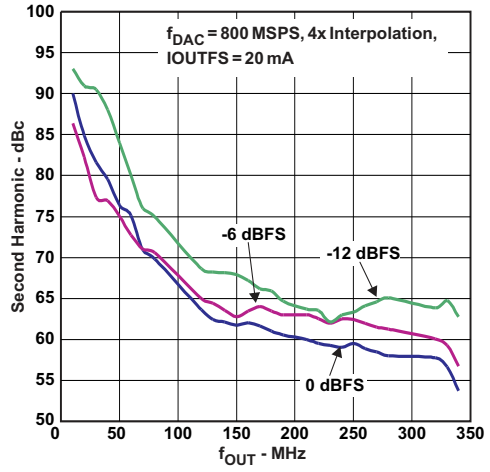


Figure 4. Second Harmonic vs Input Scale

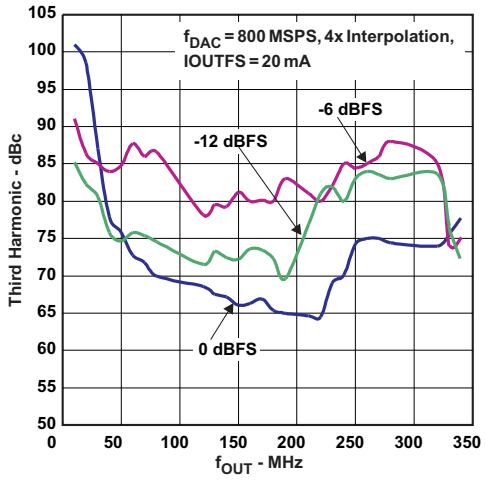


Figure 5. Third Harmonic vs Input Scale

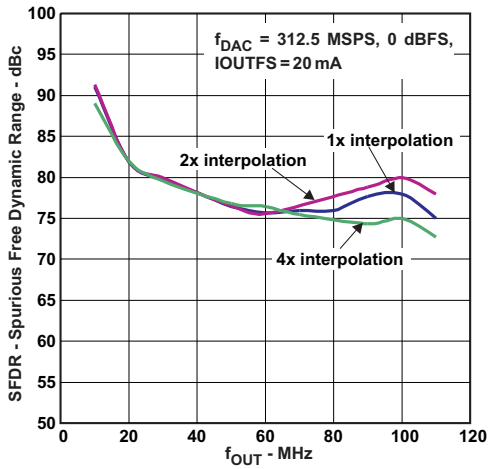


Figure 6. Spurious Free Dynamic Range vs Interpolation

Typical Characteristics (continued)

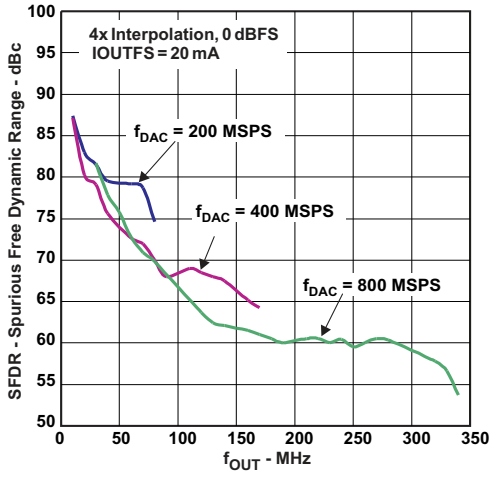


Figure 7. Spurious Free Dynamic Range vs f_{DAC}

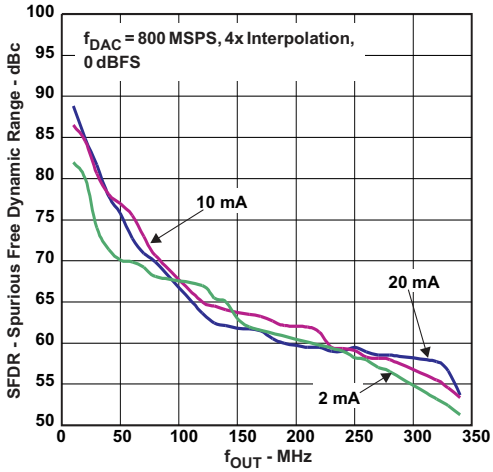


Figure 8. Spurious Free Dynamic Range vs IOUTFS

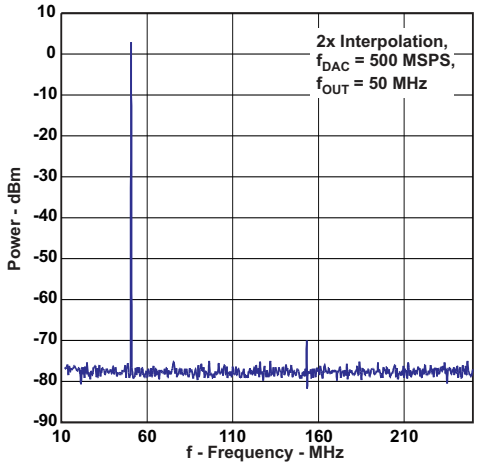


Figure 9. Single Tone Spectral Plot

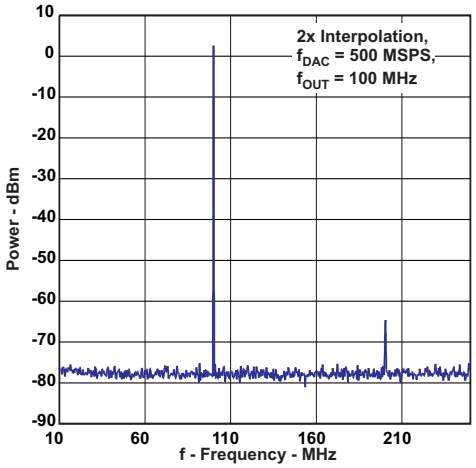


Figure 10. Single Tone Spectral Plot

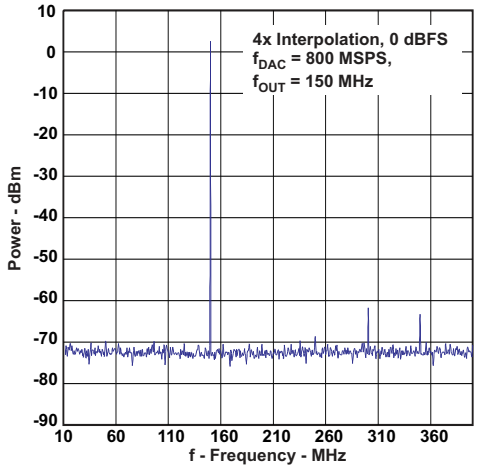


Figure 11. Single Tone Spectral Plot

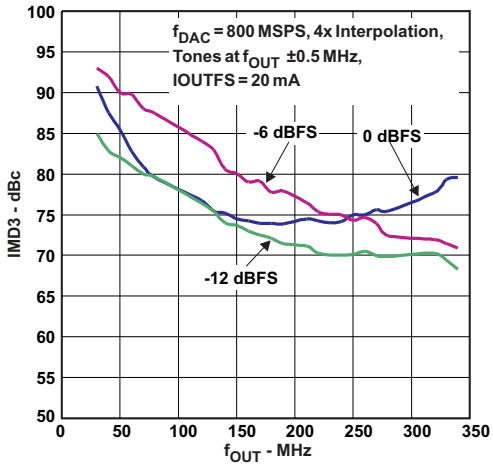


Figure 12. IMD3 vs Input Scale

Typical Characteristics (continued)

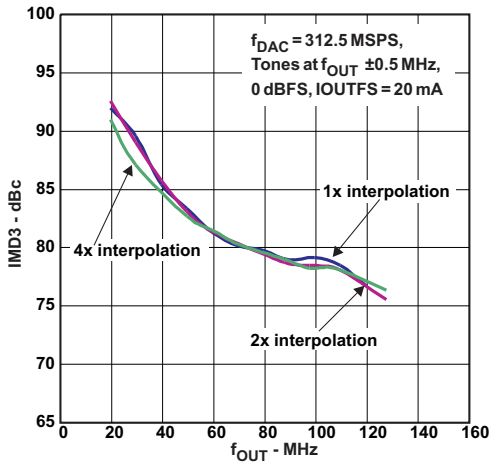


Figure 13. IMD3 vs Interpolation

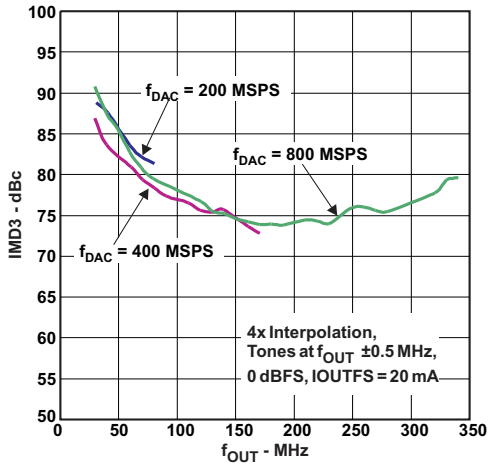


Figure 14. IMD3 vs f_{DAC}

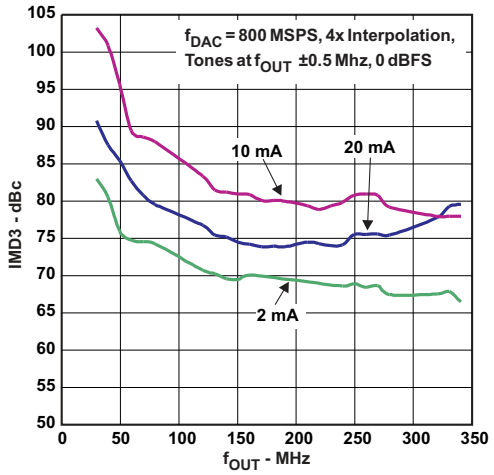


Figure 15. IMD3 vs IOUTFS

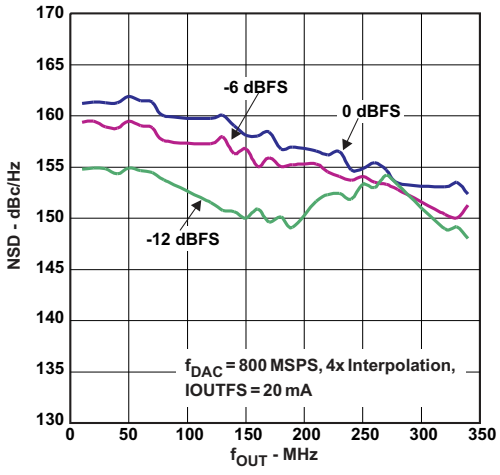


Figure 16. NSD vs Input Scale

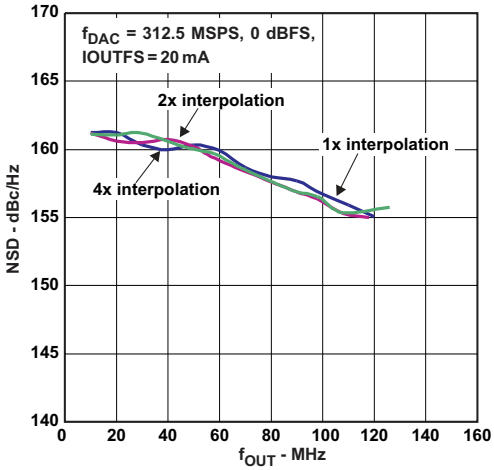


Figure 17. NSD vs Interpolation

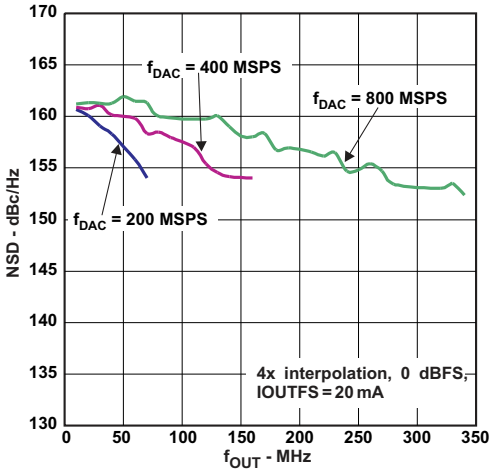


Figure 18. NSD vs f_{DAC}

Typical Characteristics (continued)

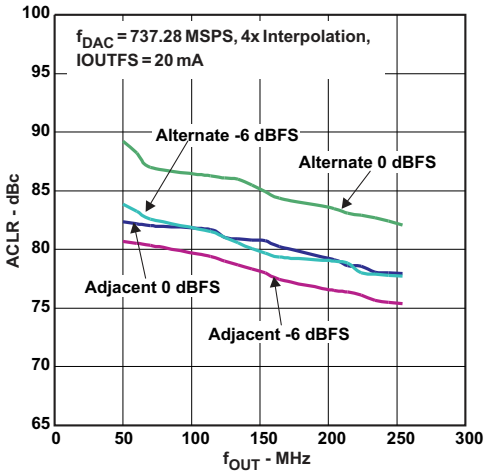


Figure 19. Single Carrier WCDMA ACLR vs Input Scale

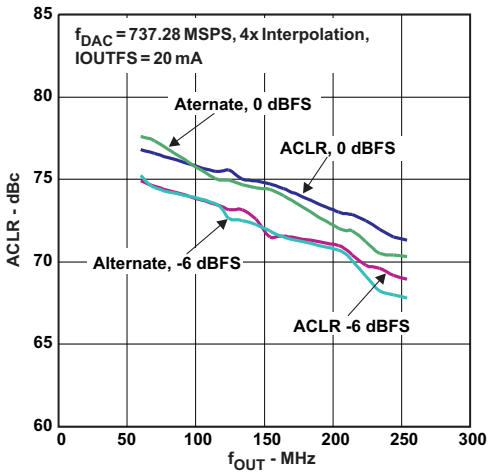


Figure 20. Four Carrier WCDMA ACLR vs Input Scale

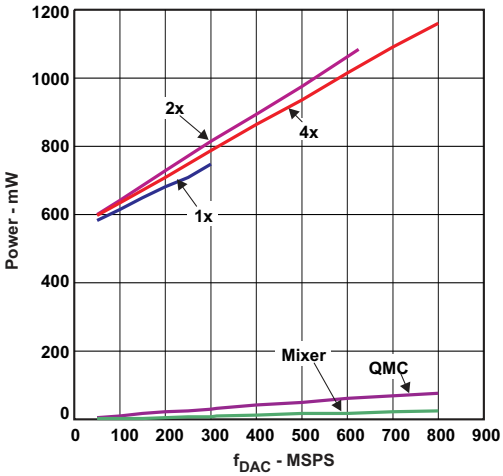


Figure 21. Power vs f_{DAC}

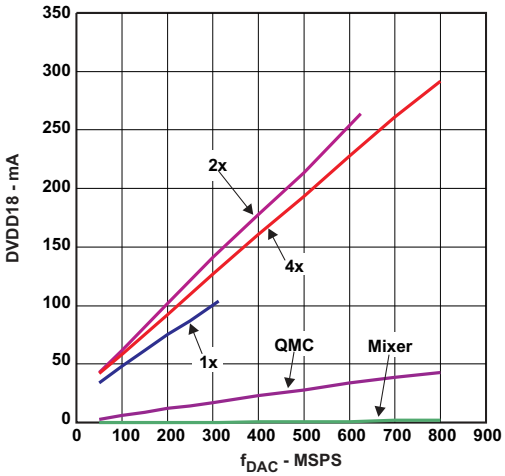


Figure 22. DVDD18 vs f_{DAC}

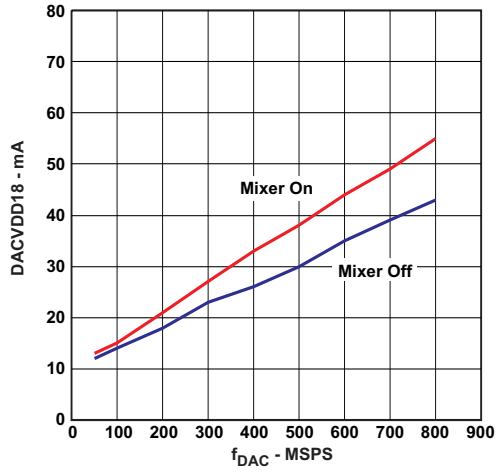


Figure 23. DACVDD18 vs f_{DAC}

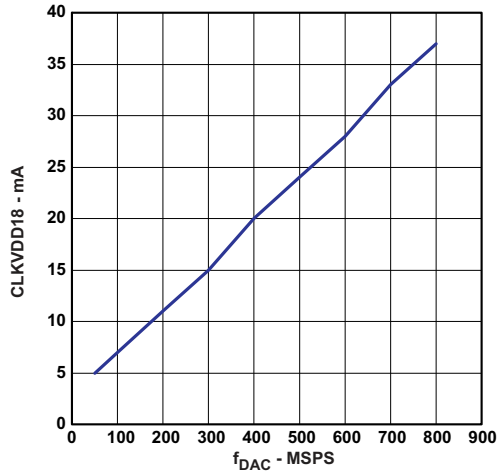


Figure 24. CLKVDD18 vs f_{DAC}

Typical Characteristics (continued)

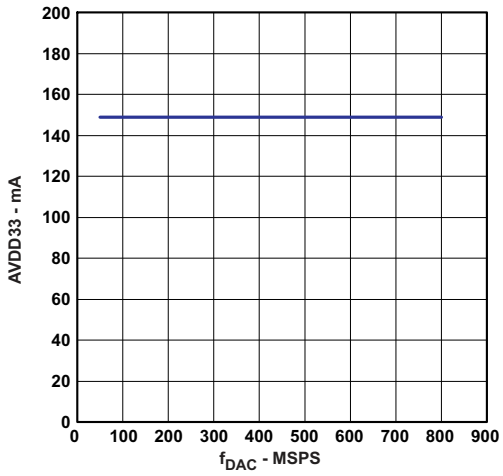


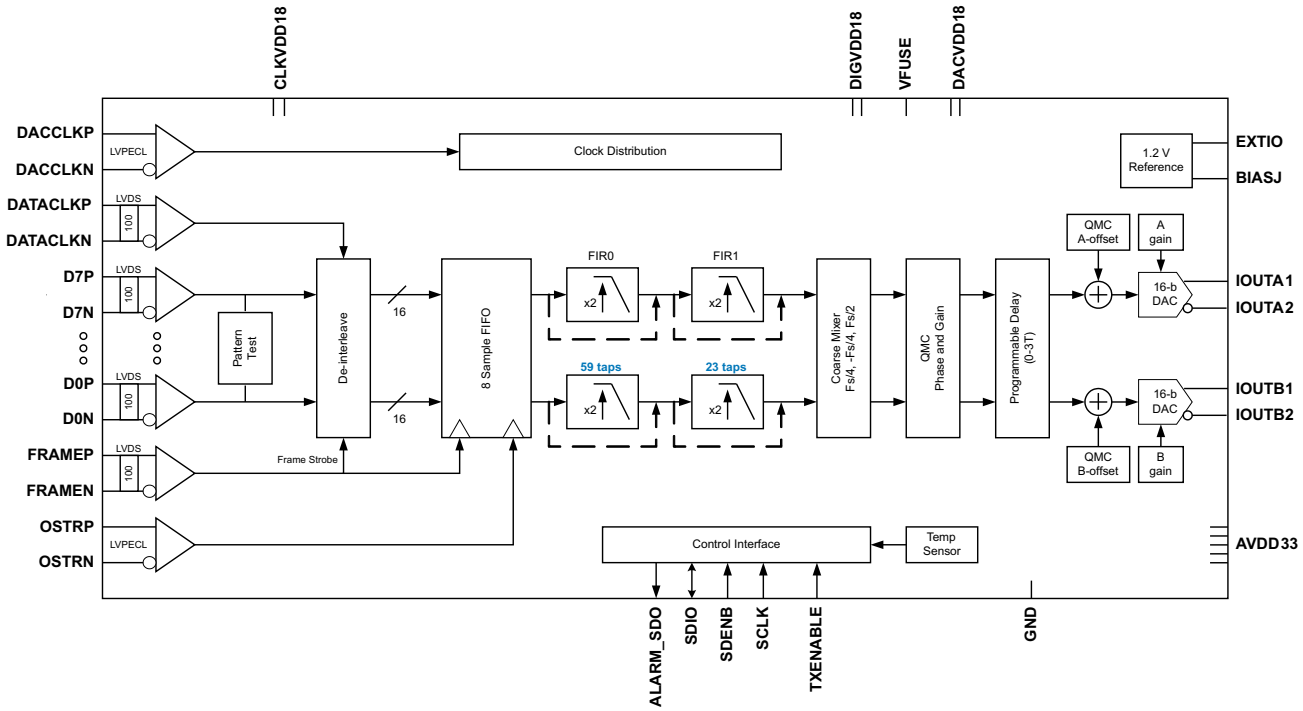
Figure 25. AVDD33 vs f_{DAC}

8 Detailed Description

8.1 Overview

The DAC3283 is a dual-channel 16-bit 800 MSPS digital-to-analog converter (DAC) with an 8-bit LVDS input data bus with on-chip termination, optional 2x-4x interpolation filters, digital IQ compensation and internal voltage reference. Input data can be interpolated by 2x or 4x through on-chip interpolating FIR filters with over 85 dB of stop-band attenuation. Multiple DAC3283 devices can be fully synchronized. The DAC3283 allows either a complex or real output. An optional coarse mixer in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. The digital IQ compensation feature allows optimization of phase, gain and offset to maximize sideband rejection and minimize LO feed-through of an external quadrature modulator performing the final single sideband RF up-conversion.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Definition Of Specifications

8.3.1.1 Adjacent Carrier Leakage Ratio (ACLR)

Defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

8.3.1.2 Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR)

Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

8.3.1.3 Differential Nonlinearity (DNL)

Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Feature Description (continued)

8.3.1.4 Gain Drift

Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

8.3.1.5 Gain Error

Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

8.3.1.6 Integral Nonlinearity (INL)

Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

8.3.1.7 Intermodulation Distortion (IMD3, IMD)

The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

8.3.1.8 Offset Drift

Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

8.3.1.9 Offset Error

Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

8.3.1.10 Output Compliance Range

Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

8.3.1.11 Reference Voltage Drift

Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

8.3.1.12 Spurious Free Dynamic Range (SFDR)

Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

8.3.1.13 Noise Spectral Density (NSD)

Noise Spectral Density (NSD): Defined as the difference of power (in dBc) between the output tone signal power and the noise floor of 1Hz bandwidth within the first Nyquist zone.

8.4 Device Functional Modes

8.4.1 Serial Interface

The serial port of the DAC3283 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC3283. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by **sif4_ena** in register **CONFIG23**. In both configurations, SCLK is the serial interface input clock and SDENB is serial interface enable. For 3 pin configuration, SDIO is a bidirectional pin for both data in and data out. For 4 pin configuration, SDIO is bidirectional and ALARM_SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK.

Device Functional Modes (continued)

Each read/write operation is framed by signal SDENB (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. Table 1 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

Table 1. Instruction Byte of the Serial Interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC3283 and a low indicates a write operation to DAC3283.

[N1:N0] Identifies the number of data bytes to be transferred per Table 2. Data is transferred MSB first.

Table 2. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4:A0] Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the DAC3283 MSB first and counts down for each byte.

Figure 26 shows the serial interface timing diagram for a DAC3283 write operation. SCLK is the serial interface clock input to DAC3283. Serial data enable SDENB is an active low input to DAC3283. SDIO is serial data in. Input data to DAC3283 is clocked on the rising edges of SCLK.

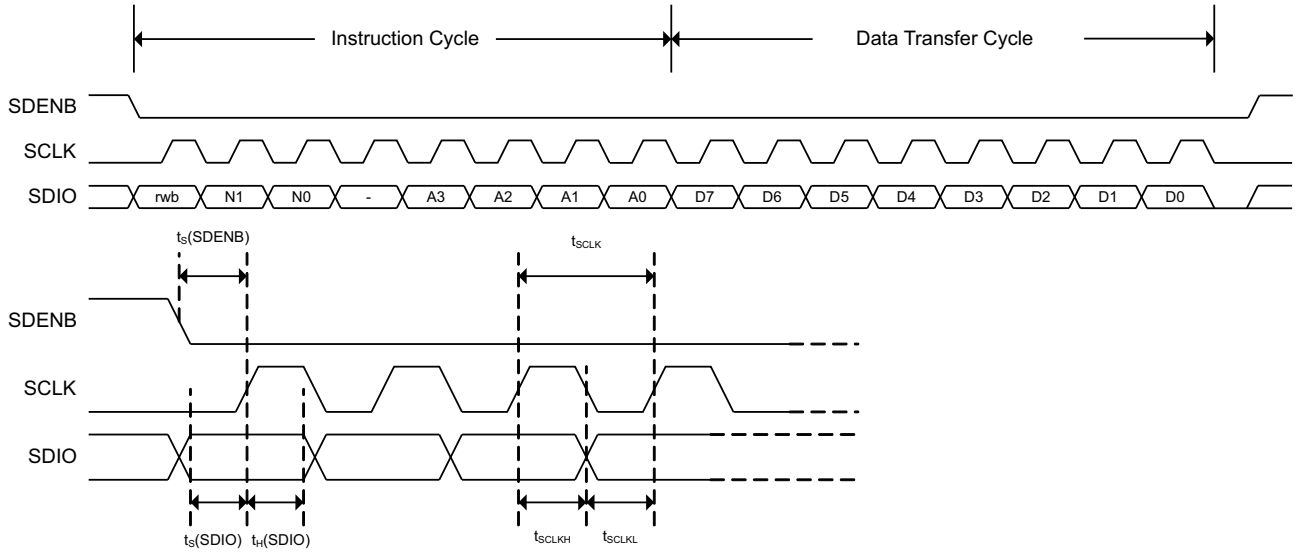


Figure 26. Serial Interface Write Timing Diagram

Figure 27 shows the serial interface timing diagram for a DAC3283 read operation. SCLK is the serial interface clock input to DAC3283. Serial data enable SDENB is an active low input to DAC3283. SDIO is serial data in during the instruction cycle. In 3 pin configuration, SDIO is data out from DAC3283 during the data transfer cycle(s), while ALARM_SDO is in a high-impedance state. In 4 pin configuration, both ALARM_SDO and SDIO are data out from DAC3283 during the data transfer cycle(s). At the end of the data transfer, ALARM_SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when it will 3-state.

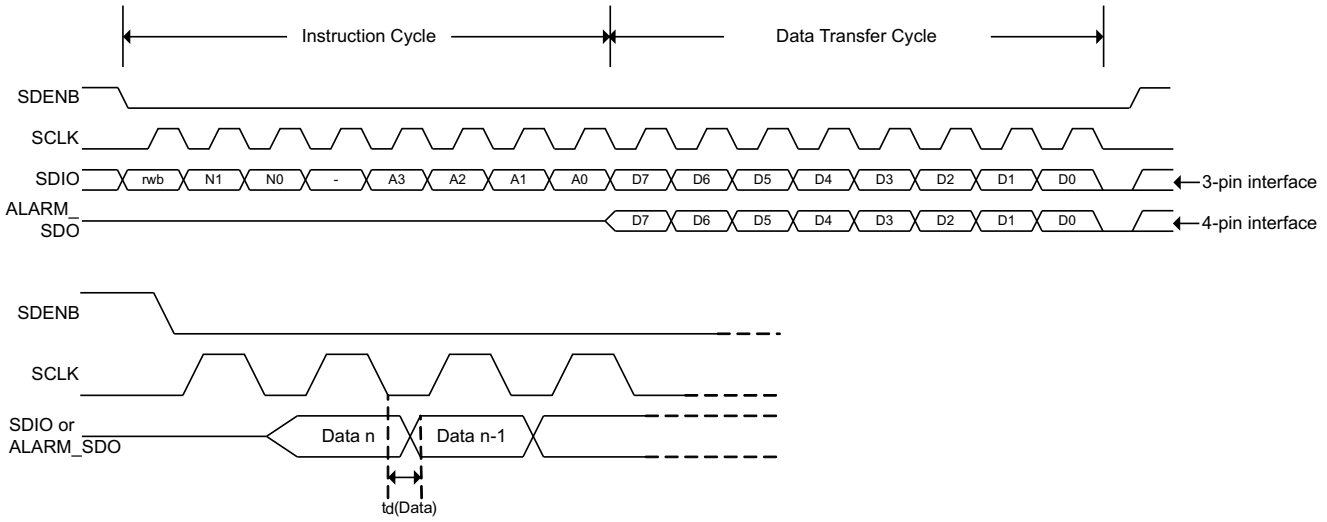


Figure 27. Serial Interface Read Timing Diagram

8.4.2 Data Interface

The DAC3283 has a single 8-bit LVDS bus that accepts dual, 16-bit data input in byte-wide format. Data into the DAC3283 is formatted according to the diagram shown in Figure 28 where index 0 is the data LSB and index 15 is the data MSB. The data is sampled by DATACLK, a double data rate (DDR) clock.

The FRAME signal is required to indicate the beginning of a frame. The frame signal can be either a pulse or a periodic signal where the frame period corresponds to 8 samples. The pulse-width ($t_{(FRAME)}$) needs to be at least equal to ½ of the DATACLK period. FRAME is sampled by a rising edge in DATACLK.

The setup and hold requirements listed in the specifications tables must be met to ensure proper sampling.

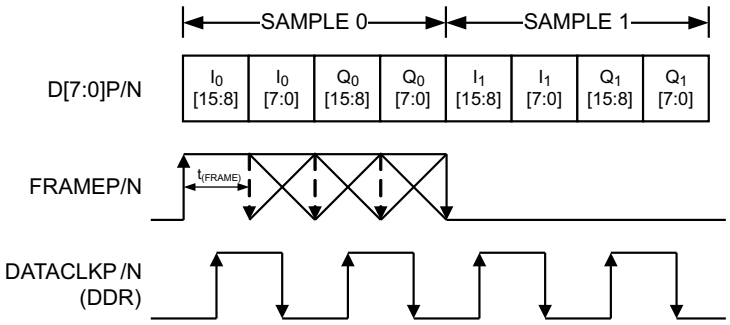


Figure 28. Byte-Wide Data Transmission Format

8.4.3 Input FIFO

The DAC3283 includes a 2-channel, 16-bits wide and 8-samples deep input FIFO which acts as an elastic buffer. The purpose of the FIFO is to absorb any timing variations between the input data and the internal DAC data rate clock such as the ones resulting from clock-to-data variations from the data source.

Figure 29 shows a simplified block diagram of the FIFO.

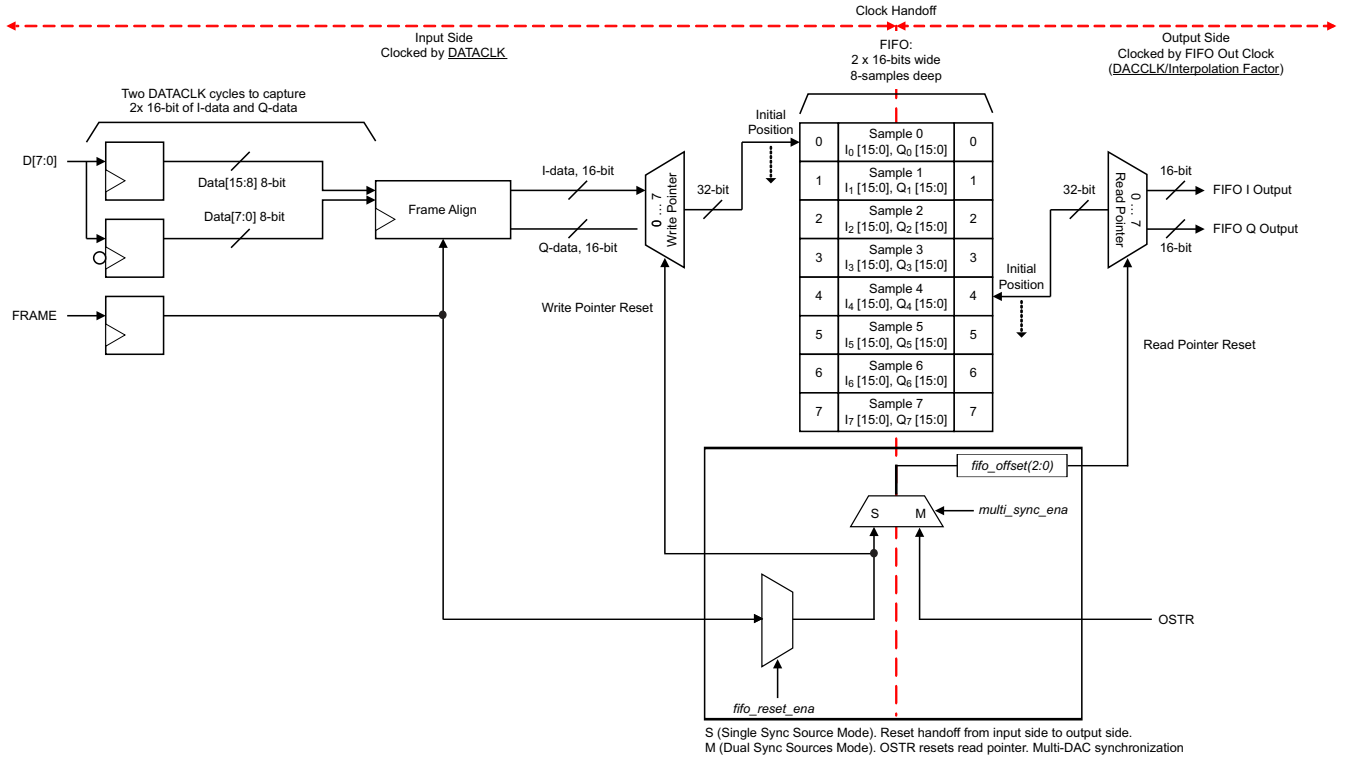


Figure 29. DAC3283 FIFO Block Diagram

Data is written to the device 8-bits at a time on the rising and falling edges of DATACLK. In order to form a complete 32-bit wide sample (16-bit I-data and 16-bit Q-data) two DATACLK periods are required as shown in Figure 30. Each 32-bit wide sample is written into the FIFO at the address indicated by the write pointer. Similarly, data from the FIFO is read by the FIFO Out Clock 32-bits at a time from the address indicated by the read pointer. The FIFO Out Clock is generated internally from the DACCLK signal and its rate is equal to DACCLK/Interpolation. Each time a FIFO write or FIFO read is done the corresponding pointer moves to the next address.

The reset position for the FIFO read and write pointers is set by default to addresses 0 and 4 as shown in Figure 29. This offset gives optimal margin within the FIFO. The default read pointer location can be set to another value using fifo_offset(2:0) in register CONFIG3. Under normal conditions data is written-to and read-from the FIFO at the same rate and consequently the write and read pointer gap remains constant. If the FIFO write and read rates are different, the corresponding pointers will be cycling at different speeds which could result in pointer collision. Under this condition the FIFO attempts to read and write data from the same address at the same time which will result in errors and thus must be avoided.

The FRAME signal besides acting as a frame indicator can also used to reset the FIFO pointers to their initial location. Unlike Data, the FRAME signal is latched only on the rising edges of DATACLK. When a rising edge occurs on FRAME, the pointers will return to their original position. The write pointer is always set back to position 0 upon reset. The read pointer reset position is determined by fifo_offset (address 4 by default).

Similarly, the read pointer sync source is selected by multi_sync_sel (CONFIG19). Either the FRAME or OSTR signal can be set to reset the read pointer. If FRAME is used to reset the read pointer, the FIFO Out Clock will recapture the FRAME signal to reset the read pointer. This clock domain transfer (DATACLK to FIFO Out Clock) results in phase ambiguity of the reset signal. This limits the precise control of the output timing and makes full synchronization of multiple devices difficult.

To alleviate this, the device offers the alternative of resetting the FIFO read pointer independently of the write pointer by using the OSTR signal. The OSTR signal is sampled by DACCLK and must satisfy the timing requirements in the specification table. In order to minimize the skew it is recommended to use the same clock distribution device such as Texas Instruments CDCE62005 to provide the DACCLK and OSTR signals to all the DAC3283 devices in the system. Swapping the polarity of the DACCLK output with respect to the OSTR output establishes proper phase relationship.

The FIFO pointers reset procedure can be done periodically or only once during initialization as the pointers automatically return to the initial position when the FIFO has been filled. To reset the FIFO periodically, it is necessary to have FRAME and OSTR signals to repeat at multiple of 8 FIFO samples. To disable FIFO reset, set fifo_reset_ena and multi_sync_ena (CONFIG0) to 0.

The frequency limitation for the FRAME signal is the following:

$f_{SYNC} = f_{DATACLK}/(n \times 16)$ where n = 1, 2, ...

The frequency limitation for the OSTR signal is the following:

$f_{OSTR} = f_{DAC}/(n \times \text{interpolation} \times 8)$ where n = 1, 2, ...

The frequencies above are at maximum when n = 1. This is when FRAME and OSTR have a rising edge transition every 8 FIFO samples. The occurrence can be made less frequently by setting n > 1, for example, every n x 8 FIFO samples.

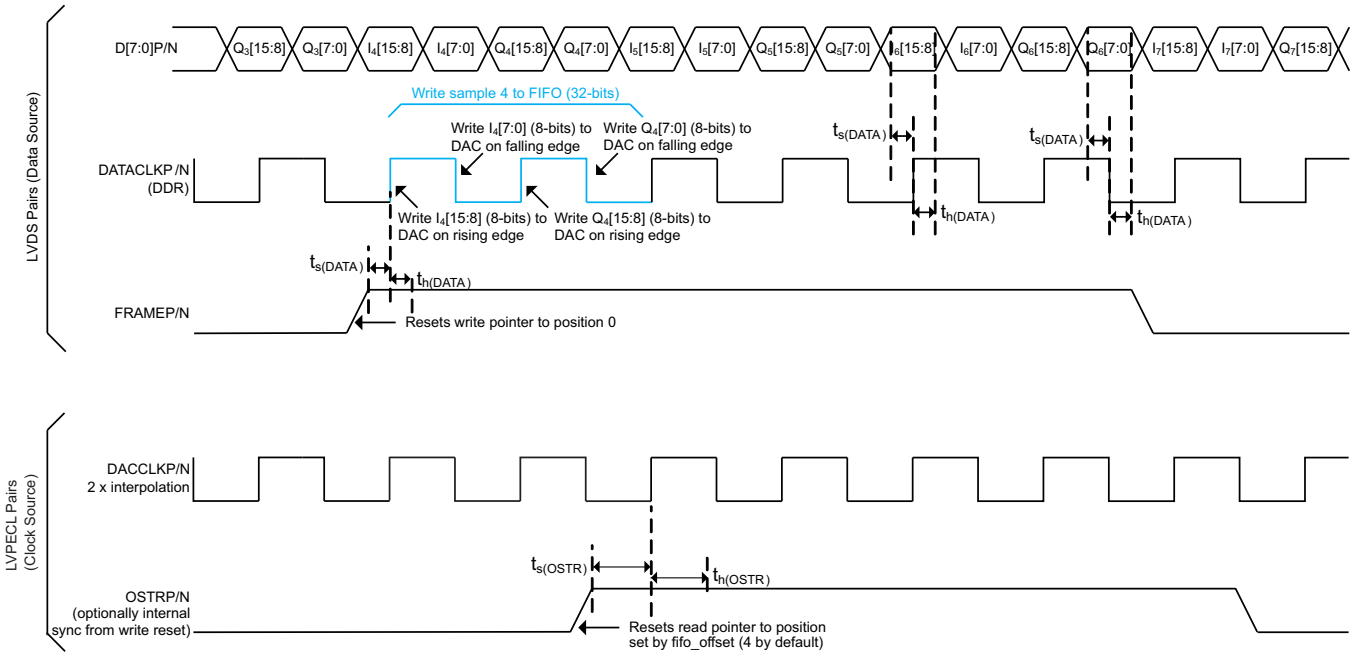


Figure 30. FIFO Write Description

8.4.4 FIFO Alarms

The FIFO only operates correctly when the write and read pointers are positioned properly. If either pointer over or under runs the other, samples will be duplicated or skipped. To prevent this, register CONFIG7 can be used to track three FIFO related alarms:

- alarm_fifo_2away. Occurs when the pointers are within two addresses of each other.
- alarm_fifo_1away. Occurs when the pointers are within one address of each other.
- alarm_fifo_collision. Occurs when the pointers are equal to each other.

These three alarm events are generated asynchronously with respect to the clocks and can be accessed either through CONFIG7 or through the ALARM_SDO pin.

8.4.5 FIFO Modes of Operation

The DAC3283 FIFO can be completely bypassed through registers *config0* and *config19*. The register configuration for each mode is described in Table 3.

Register	Control Bits
config0	fifo_ena, fifo_reset_ena, multi_sync_ena
config19	multi_sync_sel

Table 3. FIFO Operation Modes

	Config1 FIFO Bits			*Config19*
FIFO Mode	**fifo_ena**	**fifo_reset_ena**	**multi_sync_ena**	**multi_sync_sel**
Dual Sync Sources	1	1	1	0
Single Sync Source	1	1	1	1
Bypass	0	X	X	X

8.4.5.1 Dual Sync Souces Mode

This is the recommended mode of operation for those applications that require precise control of the output timing. In Dual Sync Sources mode, the FIFO write and read pointers are reset independently. The FIFO write pointer is reset using the LVDS FRAME signal, and the FIFO read pointer is reset using the LVPECL OSTR signal. This allows LVPECL OSTR signal to control the phase of the output for either a single chip or multiple chips. Multiple devices can be fully synchronized in this mode.

8.4.5.2 Single Sync Source Mode

In Single Sync Source mode, the FIFO write and read pointers are reset from the LVDS FRAME signal. This mode has a possibility of up to 2 DAC clocks offset between the outputs of multiple devices (The DAC outputs of the same device maintain the same phase). Applications requiring exact output timing control will need Dual Sync Sources mode instead of Single Sync Source mode. A rising edge for FIFO and clock divider sync is recommended. Periodic sync signal is not recommended due to non-deterministic latency of the sync signal through the clock domain transfer.

8.4.5.3 Bypass Mode

In FIFO bypass mode, the FIFO block is not used. As a result the input data is handed off from the DATACLK to the DACCLK domain without any compensation. In this mode the relationship between DATACLK and DACCLK (t_{align}) is critical and used as a synchronizing mechanism for the internal logic. Due to the t_{align} constraint it is highly recommended that a clock synchronizer device such as Texas Instruments' CDCM7005 or CDCE62005 is used to provide both clock inputs. In bypass mode the pointers have no effect on the data path or handoff.

8.4.6 Multi-Device Operation

In various applications, such as multi antenna systems where the various transmit channels information is correlated, it is required that multiple DAC devices are completely synchronized such that their outputs are phase aligned. The DAC3283 architecture supports this mode of operation.

8.4.6.1 Multi-Device Synchronization: Dual Sync Sources Mode

For single or multi-device synchronization it is important that delay differences in the data are absorbed by the device so that latency through the device remains the same. Furthermore, to guarantee that the outputs from each DAC are phase aligned it is necessary that data is read from the FIFO of each device simultaneously. In the DAC3283 this is accomplished by operating the multiple devices in Dual Sync Sources mode. In this mode the additional OSTR signal is required by each DAC3283 to be synchronized.

Data into the device is input as LVDS signals from one or multiple baseband ASICs or FPGAs. Data into the multiple DAC devices can experience different delays due to variations in the digital source output paths or board level wiring. These different delays can be effectively absorbed by the DAC3283 FIFO so that all outputs are phase aligned correctly.

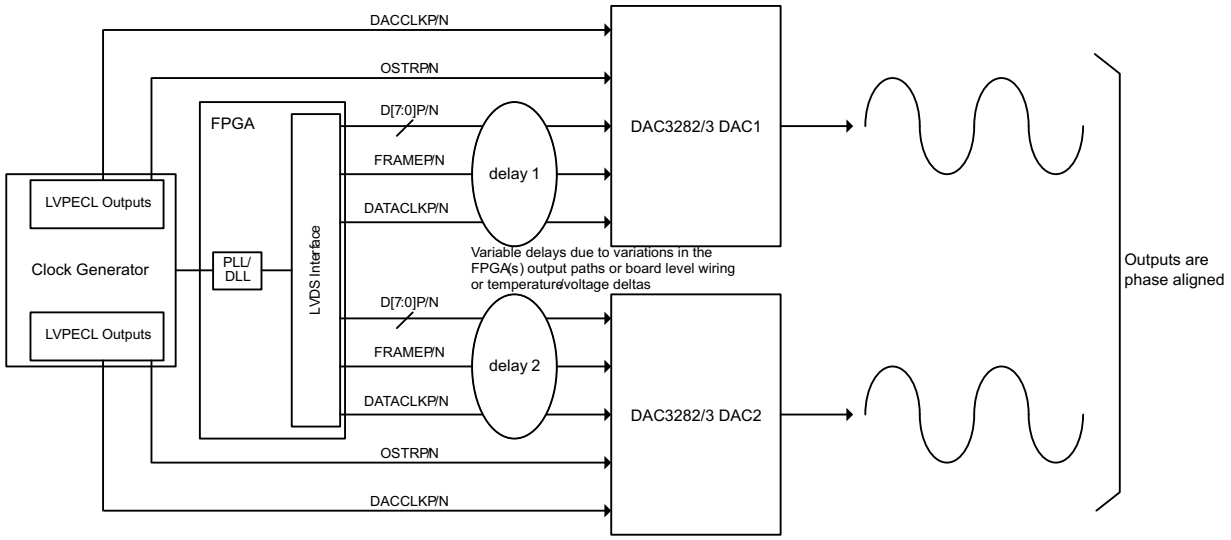


Figure 31. Synchronization System in Dual Sync Sources Mode

For correct operation both OSTR and DACCLK must be generated from the same clock domain. The OSTR signal is sampled by DACCLK and must satisfy the timing requirements in the specifications table. If the clock generator does not have the ability to delay the DACCLK to meet the OSTR timing requirement, the polarity of the DACCLK outputs can be swapped with respect to the OSTR ones to create 180 degree phase delay of the DACCLK. This may help establish proper setup and hold time requirement of the OSTR signal.

Careful board layout planning must be done to ensure that the DACCLK and OSTR signals are distributed from device to device with the lowest skew possible as this will affect the synchronization process. In order to minimize the skew across devices it is recommended to use the same clock distribution device to provide the DACCLK and OSTR signals to all the DAC devices in the system.

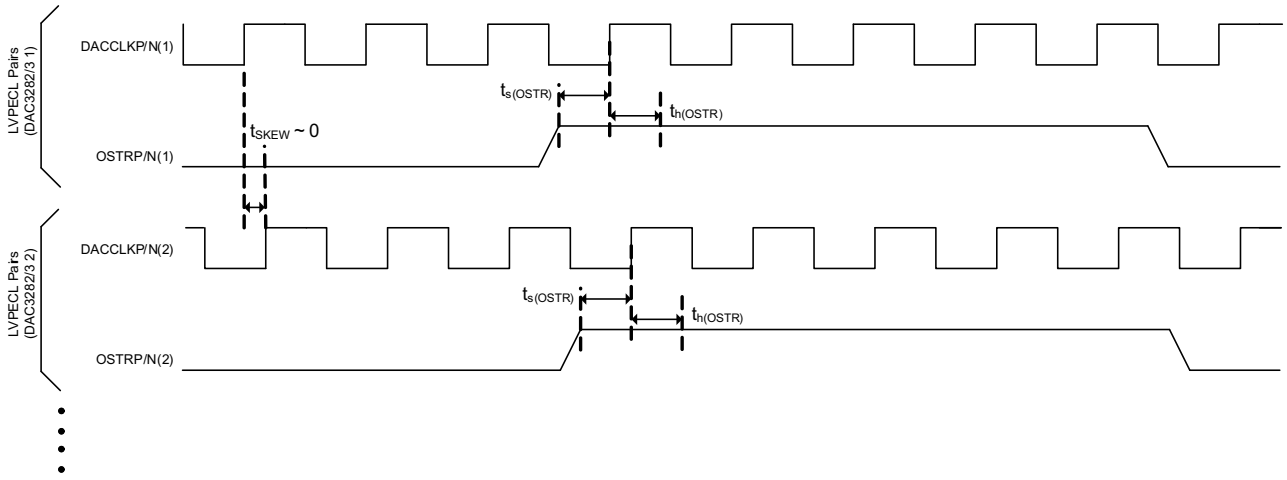


Figure 32. Timing Diagram for LVPECL Synchronization Signals

The following steps are required to ensure the devices are fully synchronized. The procedure assumes all the DAC3283 devices have a DACCLK and OSTR signal and the following steps must be carried out on each device.

- Start-up the device as described in the power-up sequence. Set the DAC3283 in Dual Sync Sources mode and select OSTR as the FIFO output pointer sync source and clock divider sync source (*multi_sync_sel* in register *config19*).
- Sync the clock divider and FIFO pointers.

- Verify there are no FIFO alarms either through register *config7* or through the ALARM_SDO pin.

After these steps all the DAC3283 outputs will be synchronized.

8.4.6.2 Multi-Device Operation: Single Sync Source Mode

In Single Sync Source mode, the FIFO write and read pointers are reset from the same FRAME source. Although the FIFO in this mode can still absorb the data delay differences due to variations in the digital source output paths or board level wiring, it is impossible to guarantee data will be read from the FIFO of different devices simultaneously thus preventing exact phase alignment.

The FIFO read pointer reset is handoff between the two clock domains (DATACLK and FIFO OUT CLOCK) by simply re-sampling the write pointer reset. Since the two clocks are asynchronous there is a small but distinct possibility of a meta-stablility during the pointer handoff. This meta-stability can cause the outputs of the multiple devices to slip by up to 2 DAC clock cycles.

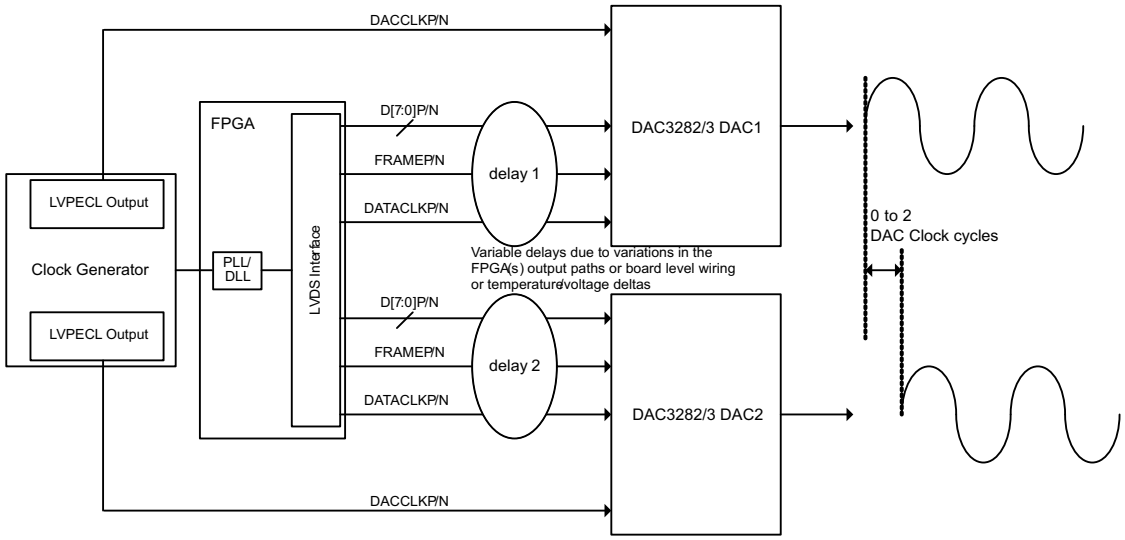


Figure 33. Multi-Device Operation in Single Sync Source Mode

8.4.7 Data Pattern Checker

The DAC3283 incorporates a simple pattern checker test in order to determine errors in the data interface. The main cause of failures is setup/hold timing issues. The test mode is enabled by asserting *iotest_ena* in register *config1*. In test mode the analog outputs are deactivated regardless of the state of TXENABLE.

The data pattern key used for the test is 8 words long and is specified by the contents of *iotest_pattern[0:7]* in registers *config9* through *config16*. The data pattern key can be modified by changing the contents of these registers.

The first word in the test frame is determined by a rising edge transition in FRAME. At this transition, the *pattern0* word should be input to the data pins. Patterns 1 through 7 should follow sequentially on each edge of DATACLK (rising and falling). The sequence should be repeated until the pattern checker test is disabled by setting *iotest_ena* back to “0”. It is not necessary to have a rising FRAME edge aligned with every *pattern0* word, just the first one to mark the beginning of the series.

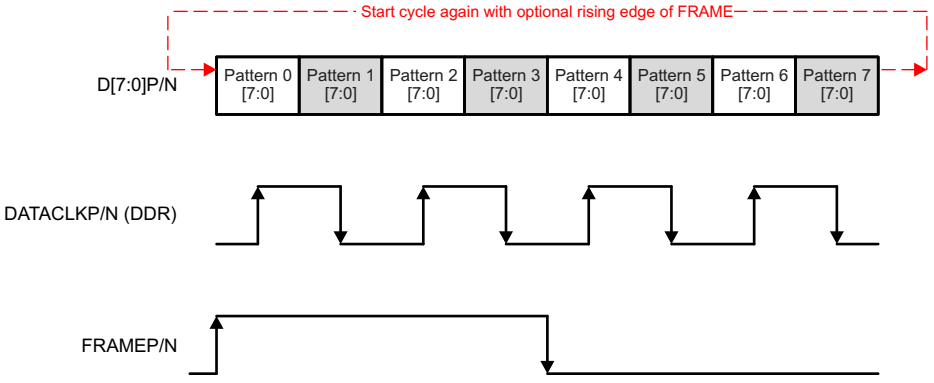


Figure 34. IO Pattern Checker Data Transmission Format

The test mode determines if the 8-bit LVDS data D[7:0]P/N of all the patterns were received correctly by comparing the received data against the data pattern key. If any of the 8-bit data D[7:0]P/N were received incorrectly, the corresponding bits in *iotest_results(7:0)* in register *config8* will be set to “1” to indicate bit error location. Furthermore, the error condition will trigger the *alarm_from_iotest* bit in register *config7* to indicate a general error in the data interface. When data pattern checker mode is enabled, this alarm in register *config7*, bit 3 is the only valid alarm. Other alarms in register *config7* are not valid and can be disregarded.

For instance, pattern0 is programmed to the default of 0x7A. If the received Pattern 0 is 0x7B, then bit 0 in *iotest_results(7:0)* will be set to “1” to indicate an error in bit 0 location. The *alarm_from_iotest* will also be set to “1” to report the data transfer error. The user can then narrow down the error from the bit location information and implement the fix accordingly.

The alarms can be cleared by writing 0x00 to *iotest_results(7:0)* and "0" to *alarm_from_iotest* through the serial interface. The serial interface will read back 0s if there are no errors or if the errors are cleared. The corresponding alarm bit will remain a "1" if the errors remain.

It is recommended to enable the pattern checker and then run the pattern sequence for 100 or more complete cycles before clearing the *iotest_results(7:0)* and *alarm_from_iotest*. This will eliminate the possibility of false alarms generated during the setup sequence.

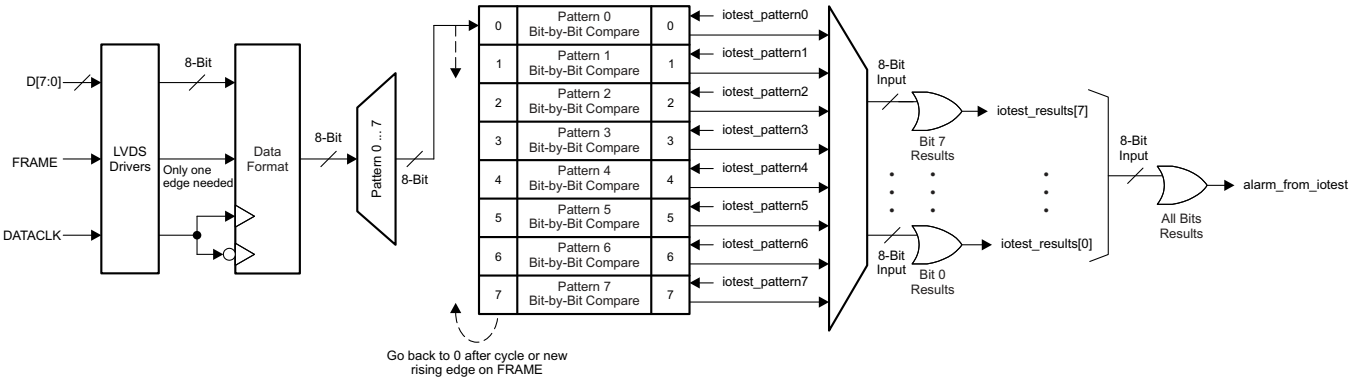


Figure 35. DAC3283 Pattern Check Block Diagram

8.4.8 DATACLK Monitor

The DAC3283 incorporates a clock monitor to determine if DATACLK is present. A missing DATACLK may result in unexpected DAC outputs. As shown in Figure 36, the clock monitor circuit is a simple counter circuit. It is reset on each rising edge of DATACLK, and counts up with each rising edge of FIFOOUT_CLK. The output of the counter has two latches: clk_alarm latch and tx_off latch. If the missing DATACLK is registered by the clock monitor circuit after the counter reached the count of four, it will send a pulse to the two latches, which issue two alarms, respectively.

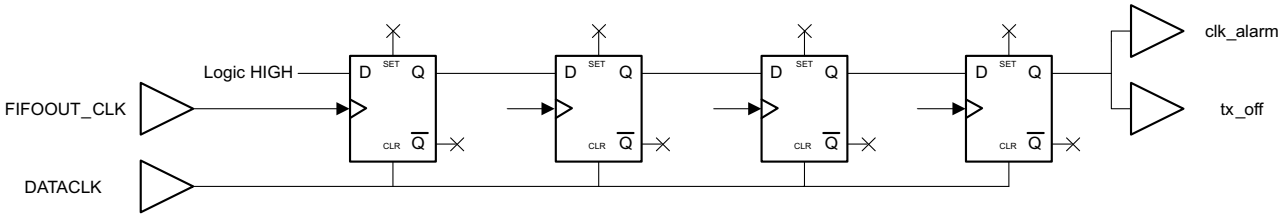


Figure 36. DATACLK Monitor Circuit

CIRCUIT	FUNCTIONS	REGISTER LOCATION	STATE	DESCRIPTION
clk_alarm latch	clk_alarm_mask	CONFIG17, bit4 read/write	1	masks the alarm signal to the CMOS ALARM_SDO
			0	unmasks the alarm signal to the CMOS ALARM_SDO
	clk_alarm_ena	CONFIG17, bit1 read/write	1	clears the latch and enables the clock loss monitoring
			0	holds the latch at reset at all times
	clk_alarm	VERSION31, bit7 read-only	1	indicates clock loss event
			0	indicates normal operation
tx_off latch	tx_off_mask	CONFIG17, bit3 read/write	1	masks the alarm signal to the CMOS ALARM_SDO
			0	unmasks the alarm signal to the CMOS ALARM_SDO
	tx_off_ena	CONFIG17, bit0 read/write	1	clears the latch and enables the clock loss monitoring
			0	holds the latch at reset at all times
	tx_off	VERSION31, bit6 read-only	1	indicates output disabled event
			0	indicates normal operation

The purpose of the clk_alarm latch is to register the loss of DATACLK event. Upon the event, the latch will issue a read-only clk_alarm alarm. This latch can be held reset at all time by setting clk_alarm_ena = '0' at all time.

The purpose of the tx_off latch is to disable the output when the DATACLK is lost. Upon the event, the latch will issue a read-only tx_off alarm. When this alarm is set, the DAC3283 outputs are automatically disabled by setting output data to mid-scale. This latch can be held reset at all time by setting tx_off_ena = '0' at all time.

Both alarms are set by default to trigger the ALARM_SDO pin in 3-pin SPI mode. By writing clk_alarm_mask and tx_off_mask to '1', the ALARM_SDO will ignore these two alarms. This may be useful if the ALARM_SDO is needed to report other critical alarms in the interrupt routine.

These two latches can be held reset at all times, effectively ignoring any clock monitor output, by setting clk_alarm_ena and tx_off_ena to '0". When a '0' is written to either of these two register bits, it will force the latch output low. For the latches to report an error, the clk_monitor_ena and tx_off_ena must be written to a '0' and then a '1'.

The clock monitoring function is implemented as follows:

1. Power up the device using the recommended power-up sequence.
   (a) Configure the device using the SPI bus.
   (b) Provide both the DATACLK and DACCLK.
2. Reset the clock monitor circuit and the latches by writing clk_alarm_ena and tx_off_ena a ‘0”, and then ‘1’ in CONFIG17.
3. Unmask the alarms by setting clk_alarm_mask and tx_off_mask to ‘0’ in CONFIG17.

If the DATACLK is interrupted, the ALARM_SDO pin will transition to indicate error. The interrupt service routine can check the following:

1. Read clk_alarm and tx_off in CONFIG31 and other alarms in CONFIG7 to determine the error that triggered the alarm.
2. If clk_alarm and tx_off alarms are set in CONFIG31, then DATACLK was interrupted and the DAC outputs should be set to mid-scale.
3. Implement system check to recover the DATACLK.
4. Reset the clock monitor circuit and clk_alarm latch by writing clk_alarm_ena a ‘0”, and then ‘1’ in CONFIG17.
5. Read clk_alarm in CONFIG31 to verify if the clock loss event has not re-triggered the alarm.
6. Once the clock monitor indicates the DATACLK is stable, resynchronize the FIFO. See Power-Up Sequence section for detail.
7. Reset the transmit disable latch by writing tx_off_ena a ‘0”, and then ‘1’ in CONFIG17. This will re-enable the DAC to output actual data.

NOTE

The ALARM_SDO pin in 4-pin SPI mode functions as SPI register data output. The system will need to poll VERSION31 alarms frequently in order to detect the DATACLK interruption errors.

8.4.9 FIR Filters

Figure 37 and Figure 38 show the magnitude spectrum response for the FIR0 and FIR1 interpolating half-band filters where f_{IN} is the input data rate to the FIR filter. Figure 39 and Figure 40 show the composite filter response for 2x and 4x interpolation. The transition band for all the interpolation settings is from 0.4 to 0.6 x f_{DATA} (the input data rate to the device) with < 0.002dB of pass-band ripple and > 85dB stop-band attenuation.

The filter taps for all digital filters are listed in Table 4.

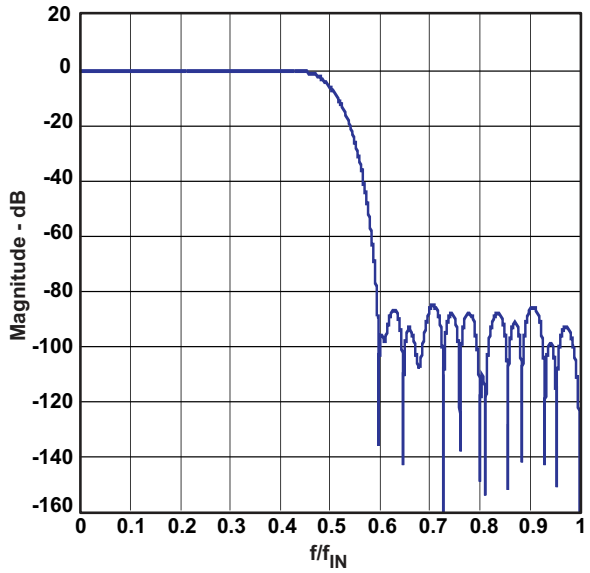


Figure 37. Magnitude Spectrum for FIR0

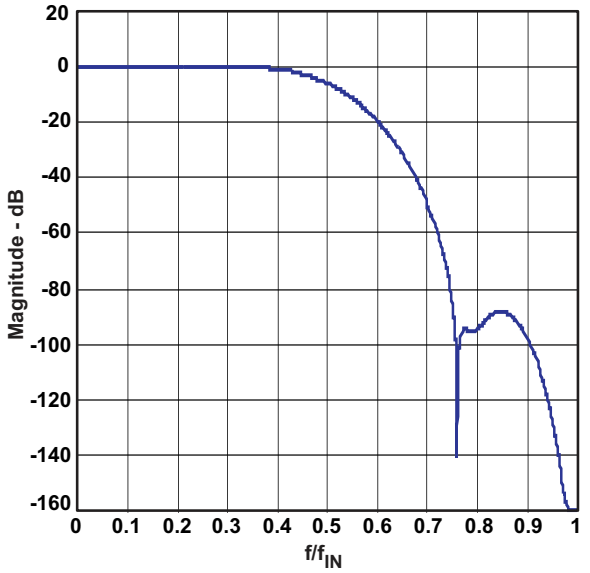


Figure 38. Magnitude Spectrum for FIR1

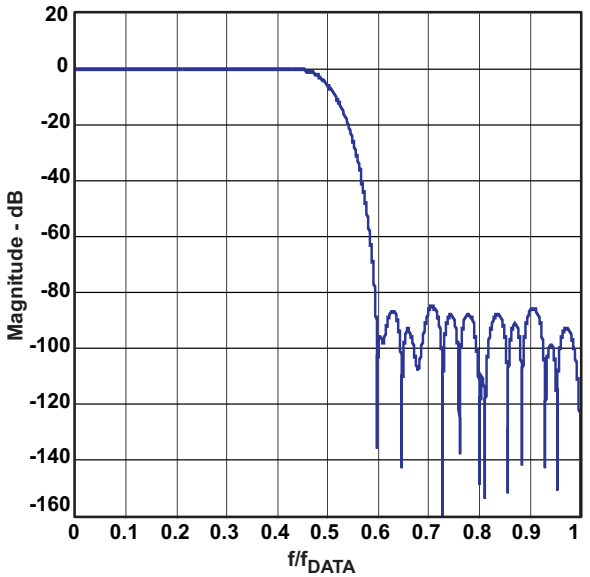


Figure 39. 2x Interpolation Composite Response

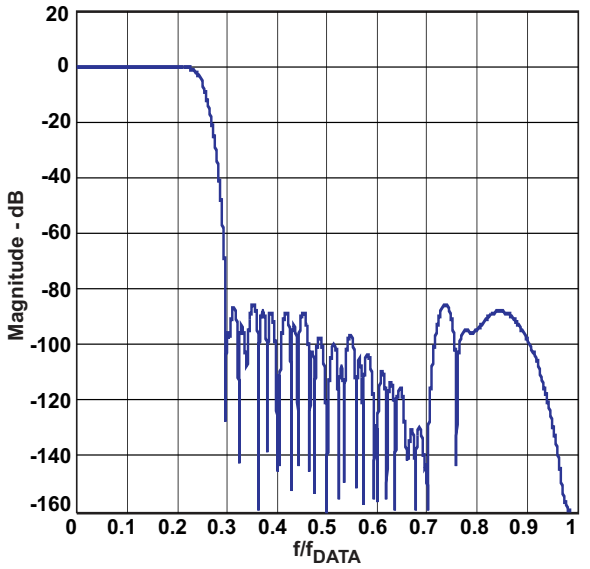


Figure 40. 4x Interpolation Composite Response

Table 4. FIR Filter Coefficients

FIR0 2x Interpolating Half-band Filter		FIR1 2x Interpolating Half-Band Filter
59 Taps		23 Taps
4	4	–2
0	0	0
–12	–12	17
0	0	0
28	28	–75
0	0	0
–58	–58	238
0	0	0
108	108	–660
0	0	0
–188	–188	2530
0	0	**4096**(1)
308	308	2530
0	0	0
–483	–483	–660
0	0	0
734	734	238
0	0	0
–1091	–1091	–75
0	0	0
1607	1607	17
0	0	0
–2392	–2392	–2
0	0	
3732	3732	
0	0	
–6681	–6681	
0	0	
20768	20768	
32768(1)		

(1) Center taps are highlighted in **BOLD.**

8.4.10 Coarse Mixer

The DAC3283 has a coarse mixer block capable of shifting the input signal spectrum by the fixed mixing frequencies $f_S/2$ or $f_S/4$. The coarse mixing function is built into the interpolation filters and thus FIR0 (2x interpolation) or FIR0 and FIR1 (4x interpolation) must be enabled to use it.

Treating channels A and B as a complex vector of the form I(t) + *j* Q(t), where I(t) = A(t) and Q(t) = B(t), the outputs of the coarse mixer, $A_{OUT}(t)$ and $B_{OUT}(t)$ are equivalent to:

$$A_{OUT}(t) = A(t)\cos(2\pi f_{CMIX}t) - B(t)\sin(2\pi f_{CMIX}t)$$
$$B_{OUT}(t) = A(t)\sin(2\pi f_{CMIX}t) + B(t)\cos(2\pi f_{CMIX}t)$$

where f_{CMIX} is the fixed mixing frequency selected by mixer_func(1:0). For $f_S/2$, $+f_S/4$ and $-f_S/4$ the above operations result in the simple mixing sequences shown in Table 5.

Table 5. Coarse Mixer Sequences

Mode	mixer_func(1:0)	Mixing Sequence
Normal (Low Pass, No Mixing)	00	A_{OUT} = { +A, +A , +A, +A } B_{OUT} = { +B, +B , +B, +B }
$f_S/2$	01	A_{OUT} = { +A, –A , +A, –A } B_{OUT} = { +B, -B , +B, -B }
$+f_S/4$	10	A_{OUT} = { +A, -B , –A, +B } B_{OUT} = { +B, +A , –B, –A }
$–f_S/4$	11	A_{OUT} = { +A, +B , –A, –B } B_{OUT} = { +B, –A , –B, +A }

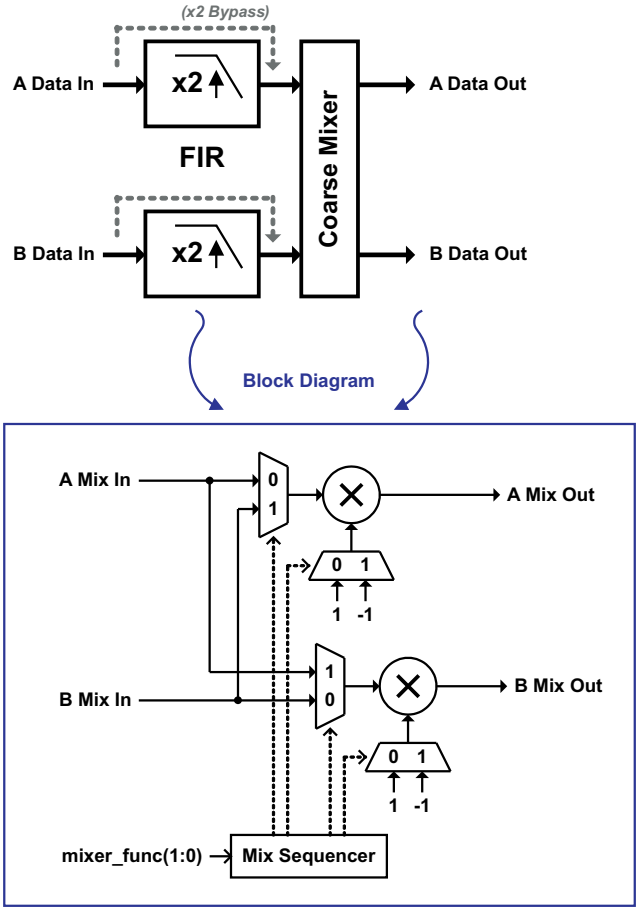


Figure 41. Coarse Mixers Block Diagram

The coarse mixer in the DAC3283 treats the A and B inputs as complex input data and for most mixing frequencies produces a complex output. Only when the mixing frequency is set to $f_S/2$ the A and B channels can be maintained isolated as shown in Table 5. In this case, the two channels are upconverted as independent signals. By setting the mixer to $f_S/2$ the interpolation filter outputs are inverted thus behaving as a high-pass filter.

Table 6. Dual-Channel Real Upconversion Options

FIR MODE	INPUT FREQUENCY(1)	OUTPUT FREQUENCY(1)	SIGNAL BANDWIDTH(1)	SPECTRUM INVERTED?
Low Pass	0.0 to 0.4 × f_{DATA}	0.0 to 0.4 × f_{DATA}	0.4 × f_{DATA}	No
High Pass	0.0 to 0.4 × f_{DATA}	0.6 to 1.0 × f_{DATA}	0.4 × f_{DATA}	Yes

(1) f_{DATA} is the input data rate of each channel after de-interleaving.

8.4.11 Quadrature Modulation Correction (QMC)

The Quadrature Modulator Correction (QMC) block provides a means for adjusting the gain and phase of the complex signal. At a quadrature modulator output, gain and phase imbalances result in an undesired sideband signal.

The block diagram for the QMC is shown in Figure 42. The QMC block contains 3 programmable parameters: qmc_gaina(10:0), qmc_gainb(10:0) and qmc_phase(9:0).

Registers qmc_gaina(10:0) and qmc_gainb(10:0) control the I and Q path gains and are 11 bit values with a range of 0 to approximately 2. This value is used to scale the signal range. Register qmc_phase(9:0) controls the phase imbalance between I and Q and is a 10-bit value that ranges from –1/8 to approximately +1/8. This value is multiplied by each Q sample then summed into the I sample path. This operation is a simplified approximation of a true phase rotation and covers the range from –7.125 to +7.125 degrees in 1024 steps.

A write to register CONFIG27 is required to load the gain and phase values (CONFIG27-CONFIG30) into the QMC block simultaneously. When updating the gain and/or phase values CONFIG27 should be written last. Programming any of the other three registers will not affect the gain and phase settings.

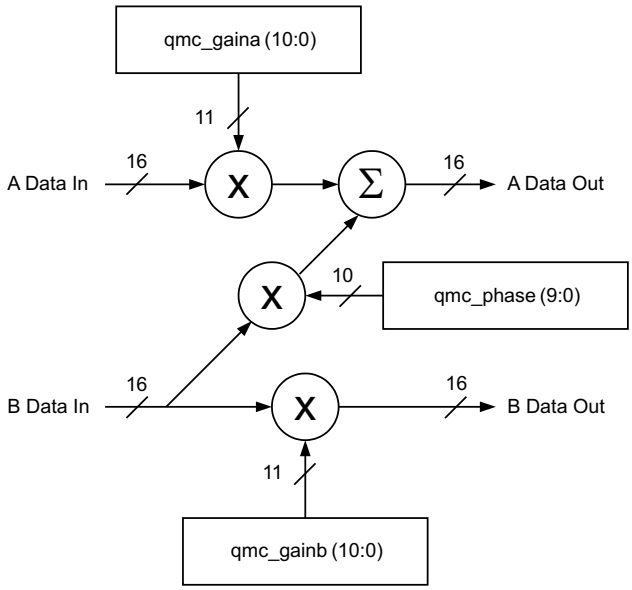


Figure 42. QMC Block Diagram

8.4.12 Digital Offset Control

The qmc_offseta(12:0) and qmc_offsetb(12:0) values in registers CONFIG20 through CONFIG23 can be used to independently adjust the A and B path DC offsets. Both offset values are in represented in 2s-complement format with a range from –4096 to 4095.

Note that a write to register CONFIG20 is required to load the values of all four qmc_offset registers (CONFIG20-CONFIG23) into the offset block simultaneously. When updating the offset values CONFIG20 should be written last. Programming any of the other three registers will not affect the offset setting.

The offset value adds a digital offset to the digital data before digital-to-analog conversion. Since the offset is added directly to the data it may be necessary to back off the signal to prevent saturation. Both data and offset values are LSB aligned.

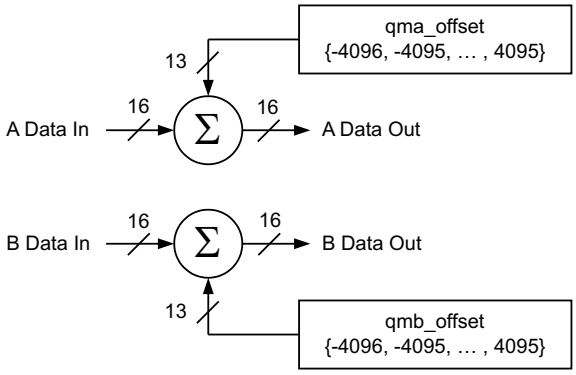


Figure 43. Digital Offset Block Diagram

8.4.13 Temperature Sensor

The DAC3283 incorporates a temperature sensor block which monitors the temperature by measuring the voltage across 2 transistors. The voltage is converted to an 8-bit digital word using a successive-approximation (SAR) analog to digital conversion process. The result is scaled, limited and formatted as a twos complement value representing the temperature in degrees Celsius.

The sampling is controlled by the serial interface signals SDENB and SCLK. If the temperature sensor is enabled (tsense_ena = 1 in register CONFIG24) a conversion takes place each time the serial port is written or read. The data is only read and sent out by the digital block when the temperature sensor is read in register CONFIG5. The conversion uses the first eight clocks of the serial clock as the capture and conversion clock, the data is valid on the falling eighth SCLK. The data is then clocked out of the chip on the rising edge of the ninth SCLK. No other clocks to the chip are necessary for the temperature sensor operation. As a result the temperature sensor is enabled even when the device is in sleep mode.

In order for the process described above to operate properly, the serial port read from CONFIG5 must be done with an SCLK period of at least 1µs. If this is not satisfied the temperature sensor accuracy is greatly reduced.

8.4.14 Sleep Modes

The DAC3283 features independent sleep control of each DAC (sleepa and sleepb), their corresponding clock path (clkpath_sleep_a and clkpath_sleep_b) as well as the clock input receiver of the device (clkrecv_sleep). The sleep control of each of these components is done through the SIF interface and is enabled by setting a 1 to the corresponding sleep register.

Complete power down of the device is set by setting all of these components to sleep. Under this mode the supply power consumption is reduced to 15mW. Power-up time in this case will be in the milliseconds range. Alternatively for those applications were power-up and power-down times are critical it is recommended to only set the DACs to sleep through the sleepa and sleepb registers. In this case both the sleep and wake-up times are only 90µs.

8.4.15 LVPECL Inputs

Figure 44 shows an equivalent circuit for the DAC input clock (DACCLP/N) and the output strobe clock (OSTRP/N).

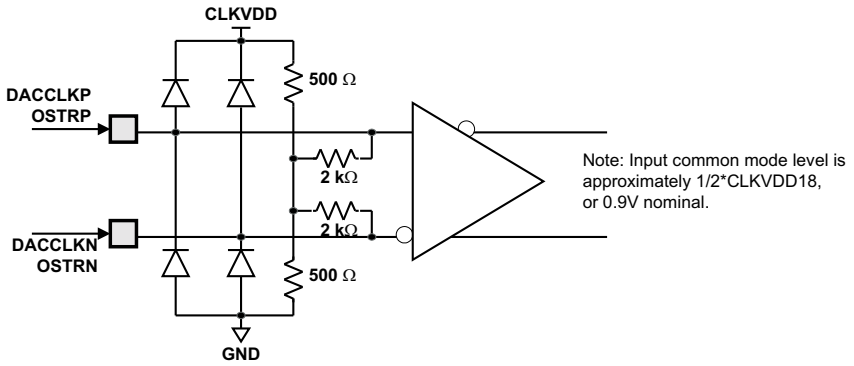


Figure 44. DACCLKP/N and OSTRP/N Equivalent Input Circuit

Figure 45 shows the preferred configuration for driving the CLKIN/CLKINC input clock with a differential ECL/PECL source.

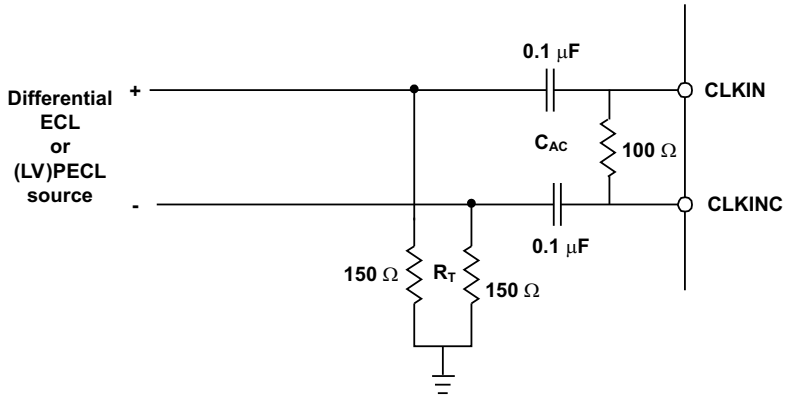


Figure 45. Preferred Clock Input Configuration with a Differential ECL/PECL Clock Source

8.4.16 LVDS INPUTS

The D[7:0]P/N, DATACLKP/N and FRAMEP/N LVDS pairs have the input configuration shown in Figure 46. Figure 47 shows the typical input levels and common-move voltage used to drive these inputs.

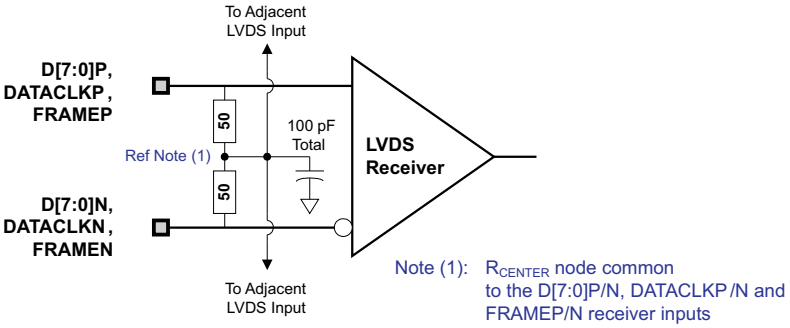


Figure 46. D[7:0]P/N, DATACLKP/N and FRAMEP/N LVDS Input Configuration

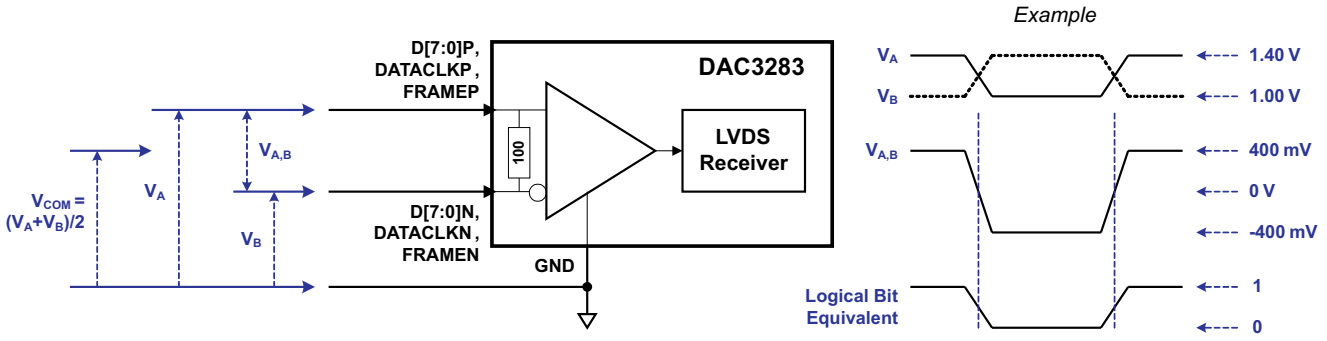


Figure 47. LVDS Data (D[7:0]P/N, DATACLKP/N, FRAMEP/N Pairs) Input Levels

Table 7. Example LVDS Data Input Levels

APPLIED VOLTAGES		RESULTING DEFERENTIAL VOLTAGE	RESULTING COMMON-MODE VOLTAGE	LOGICAL BIT BINARY EQUIVALENT
V_A	V_B	$V_{A,B}$	V_{COM}	
1.4 V	1.0 V	400 mV	1.2 V	1
1.0 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1.0 V	1
0.8 V	1.2 V	–400 mV		0

8.4.17 CMOS Digital Inputs

Figure 48 shows a schematic of the equivalent CMOS digital inputs of the DAC3283. SDIO, SCLK and TXENABLE have pull-down resistors while SDENB has a pull-up resistors internal to the DAC3283. See the specification table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 100kΩ.

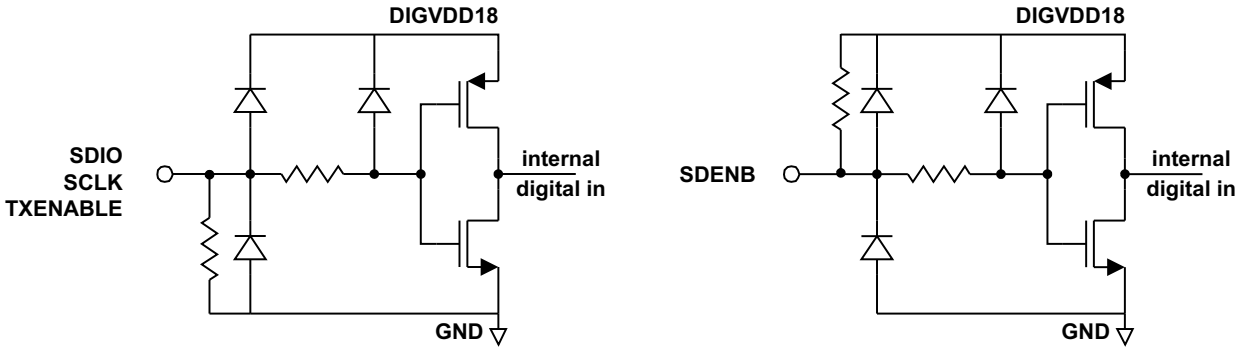


Figure 48. CMOS/TTL Digital Equivalent Input

8.4.18 Reference Operation

The DAC3283 uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUTFS = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS}$$

Each DAC has a 4-bit coarse gain control via **coarse_daca(3:0)** and **coarse_dacb (3:0)** in the CONFIG4 register. Using gain control, the IOUTFS can be expressed as::

$$IOUTAFS = (DACA\_gain + 1) \times I_{BIAS} = (DACA\_gain + 1) \times V_{EXTIO} / R_{BIAS}$$

$$IOUTBFS = (DACB\_gain + 1) \times I_{BIAS} = (DACB\_gain + 1) \times V_{EXTIO} / R_{BIAS}$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2V. This reference is active when **extref_ena** = '0' in CONFIG25. An external decoupling capacitor C_{EXT} of 0.1µF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100nA. The internal reference can be disabled and overridden by an external reference by setting the CONFIG25 extref_ena control bit. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20mA down to 2mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20dB.

8.4.19 DAC Transfer Function

The CMOS DAC's consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20mA. Differential current switches direct the current to either one of the complementary output nodes IOUT1 or IOUT2. (DACA = IOUTA1 or IOUTA2 and DACB = IOUTB1 or IOUTB2.) Complementary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (+1.2V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times IBIAS.

The relation between IOUT1 and IOUT2 can be expressed as:

IOUT1 = – IOUTFS – IOUT2

Current flowing into a node is denoted as – current and current flowing out of a node as + current. Since the output stage is a current sink the current can only flow from AVDD into the IOUT1 and IOUT2 pins. The output current flow in each pin driving a resistive load can be expressed as:

IOUT1 = IOUTFS × (65535 – CODE) / 65536

IOUT2 = IOUTFS × CODE / 65536

where CODE is the decimal representation of the DAC data input word.

For the case where IOUT1 and IOUT2 drive resistor loads R_L directly, this translates into single ended voltages at IOUT1 and IOUT2:

VOUT1 = AVDD – | IOUT1 | × R_L

VOUT2 = AVDD – | IOUT2 | × R_L

Assuming that the data is full scale (65536 in offset binary notation) and the R_L is 25 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as:

VOUT1 = AVDD – | –0 mA | × 25 Ω = 3.3 V

VOUT2 = AVDD – | –20 mA | × 25 Ω = 2.8 V

VDIFF = VOUT1 – VOUT2 = 0.5 V

Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

8.4.20 Analog Current Outputs

Figure 49 shows a simplified schematic of the current source array output with corresponding switches. Differential switches direct the current of each individual NMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referenced to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD – 0.5 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC3283 device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD + 0.5 V. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral non-linearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.

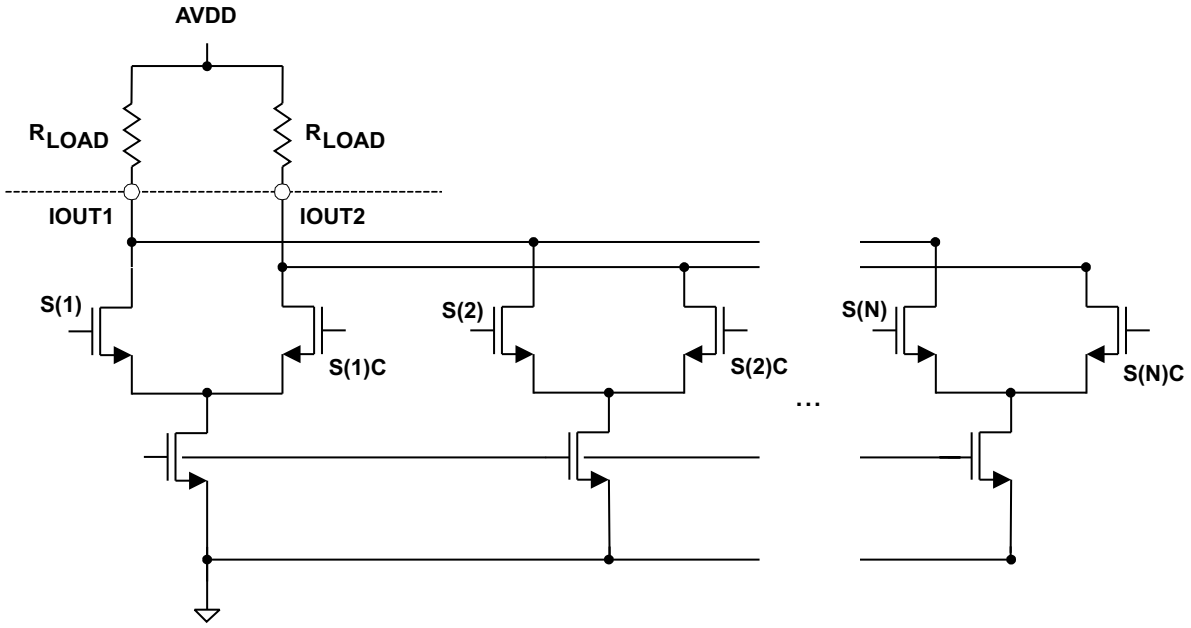


Figure 49. Equivalent Analog Current Output

The DAC3283 can be easily configured to drive a doubly terminated 50Ω cable using a properly selected RF transformer. Figure 50 and Figure 51 show the 50Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer has to be connected to AVDD to enable a dc current flow. Applying a 20 mA full-scale output current would lead to a 0.5 V_{PP} for a 1:1 transformer, and a 1 V_{PP} output for a 4:1 transformer. The low dc-impedance between IOUT1 or IOUT2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1 V_{PP} output for the 4:1 transformer results in an output between AVDD + 0.5 V and AVDD – 0.5 V.

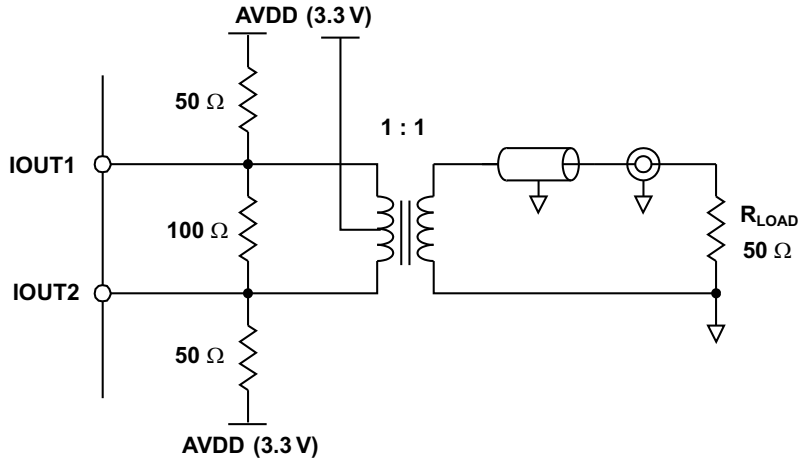


Figure 50. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

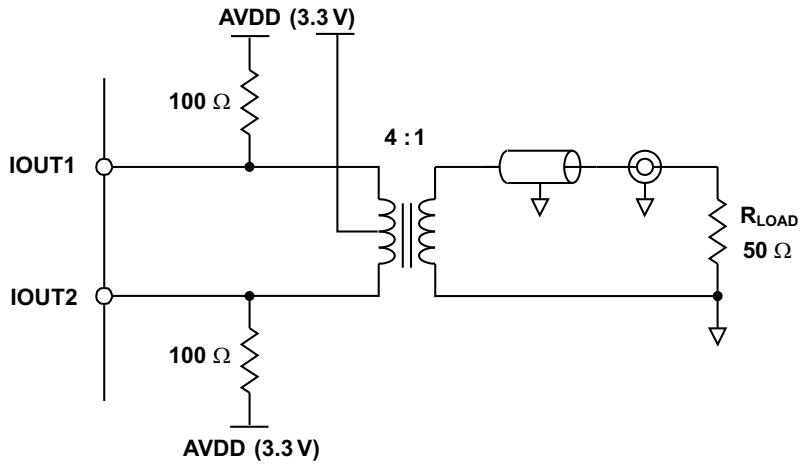


Figure 51. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

8.4.21 Passive Interface to Analog Quadrature Modulators

A common application in communication systems is to interface the DAC to an IQ modulator like the TRF3703 family of modulators from Texas Instruments. The input of the modulator is generally of high impedance and requires a specific common-mode voltage. A simple resistive network can be used to maintain 50Ω load impedance for the DAC3283 and also provide the necessary common-mode voltages for both the DAC and the modulator.

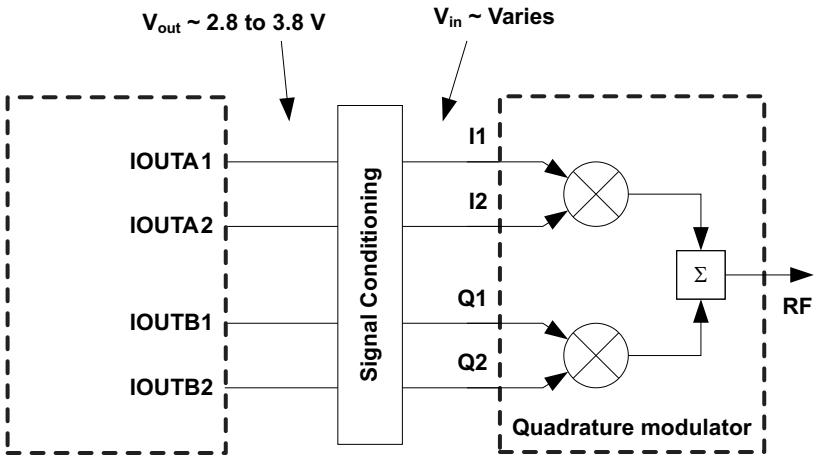


Figure 52. DAC to Analog Quadrature Modulator Interface

The DAC3283 has a maximum 20mA full-scale output and a voltage compliance range of AVDD ± 0.5 V. The TRF3703 IQ modulator family can be operated at three common-mode voltages: 1.5V, 1.7V, and 3.3V.

Figure 53 shows the recommended passive network to interface the DAC3283 to the TRF3703-17 which has a common mode voltage of 1.7V. The network generates the 3.3V common mode required by the DAC output and 1.7V at the modulator input, while still maintaining 50Ω load for the DAC.

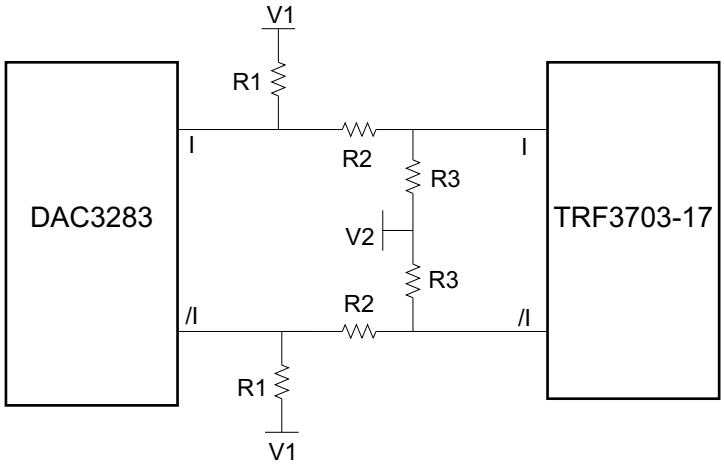


Figure 53. DAC3283 to TRF3703-17 Interface

If V1 is set to 5V and V2 is set to -5V, the corresponding resistor values are R1 = 57Ω, R2 = 80Ω, and R3 = 336Ω. The loss developed through R2 is about –1.86 dB. In the case where there is no –5V supply available and V2 is set to 0V, the resistor values are R1 = 66Ω, R2 = 101Ω, and R3 = 107Ω. The loss with these values is –5.76dB.

Figure 54 shows the recommended network for interfacing with the TRF3703-33 which requires a common mode of 3.3V. This is the simplest interface as there is no voltage shift. Because there is no voltage shift there is any loss in the network. With V1 = 5V and V2 = 0V, the resistor values are R1 = 66Ω and R3 = 208Ω.

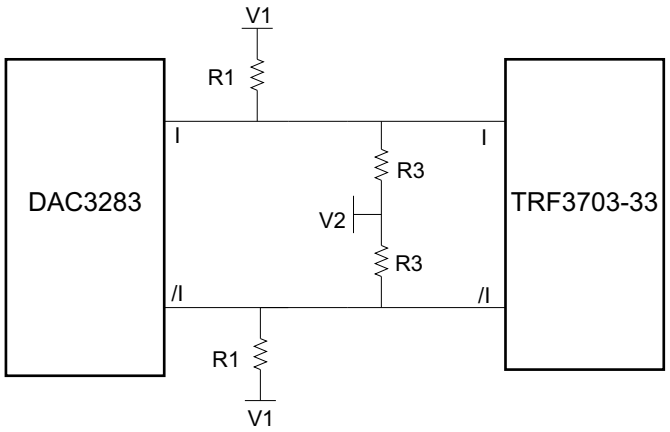


Figure 54. DAC3283 to TRF3703-33 Interface

In most applications, a baseband filter is required between the DAC and the modulator to eliminate the DAC images. This filter can be placed after the common-mode biasing network. For the DAC to modulator network shown in Figure 55, R2 and the filter load R4 need to be considered into the DAC impedance. The filter has to be designed for the source impedance created by the resistor combination of R3 // (R2+R1). The effective impedance seen by the DAC is affected by the filter termination resistor resulting in R1 // (R2+R3 // (R4/2)).

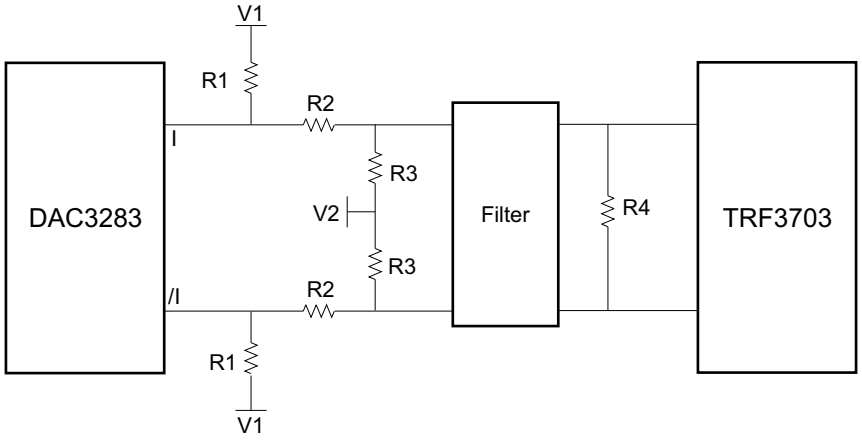


Figure 55. DAC3283 to Modulator Interface with Filter

Factoring in R4 into the DAC load, a typical interface to the TRF3703-17 with V1 = 5V and V2 = 0V results in the following values: R1 = 72Ω, R2 = 116Ω, R3 = 124Ω and R4 = 150Ω. This implies that the filter needs to be designed for 75Ω input and output impedance (single-ended impedance). The common mode levels for the DAC and modulator are maintained at 3.3V and 1.7V and the DAC load is 50Ω. The added load of the filter termination causes the signal to be attenuated by –10.8 dB.

A filter can be implemented in a similar manner to interface with the TRF3703-33. In this case it is much simpler to balance the loads and common mode voltages due to the absence of R2. An added benefit is that there is no loss in this network. With V1 = 5V and V2 = 0V the network can be designed such that R1 = 115Ω, R3 = 681Ω, and R4 = 200Ω. This results in a filter impedance of R1 // R2=100Ω, and a DAC load of R1 // R3 // (R4/2) which is equal to 50Ω. R4 is a differential resistor and does not affect the common mode level created by R1 and R3. The common-mode voltage is set at 3.3 V for a full-scale current of 20mA.

For more information on how to interface the DAC3283 to an analog quadrature modulator please refer to the application reports *Passive Terminations for Current Output DACs* (SLAA399) and *Design of Differential Filters for High-Speed Signal Chains* (SLWA053).

8.5 Register Maps

Table 8. Register Map

Name	Address	Default	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
CONFIG0	0x00	0x70	reserved	fifo_ena	fifo_reset_ena	multi_sync_ena	alarm_out_ena	alarm_pol	mixer_func(1:0)	
CONFIG1	0x01	0x11	qmc_offset_ena	qmc_correct_ena	fir0_ena	fir1_ena	unused	iotest_ena	unused	twos
CONFIG2	0x02	0x00	unused	unused	sif_sync	sif_sync_ena	unused	unused	output_delay(1:0)	
CONFIG3	0x03	0x10	64cnt_ena	unused	unused	fifo_offset(2:0)			alarm_ 2away_ena	alarm_ 1away_ena
CONFIG4	0x04	0xFF	coarse_daca(3:0)				coarse_dacb(3:0)			
CONFIG5	0x05	N/A	tempdata(7:0)							
CONFIG6	0x06	0x00	unused	alarm_mask(6:0)						
CONFIG7	0x07	0x00	unused	alarm_from_ zerochk	alarm_fifo_ collision	reserved	alarm_from_ iotest	unused	alarm_fifo_ 2away	alarm_fifo_ 1away
CONFIG8	0x08	0x00	iotest_results(7:0)							
CONFIG9	0x09	0x7A	iotest_pattern0(7:0)							
CONFIG10	0x0A	0xB6	iotest_pattern1(7:0)							
CONFIG11	0x0B	0xEA	iotest_pattern2(7:0)							
CONFIG12	0x0C	0x45	iotest_pattern3(7:0)							
CONFIG13	0x0D	0x1A	iotest_pattern4(7:0)							
CONFIG14	0x0E	0x16	iotest_pattern5(7:0)							
CONFIG15	0x0F	0xAA	iotest_pattern6(7:0)							
CONFIG16	0x10	0xC6	iotest_pattern7(7:0)							
CONFIG17	0x11	0x24	reserved	reserved	reserved	clk_alarm_mask	tx_off_mask	reserved	clk_alarm_ena	tx_off_ena
CONFIG18	0x12	0x02	reserved			reserved	daca_ complement	dacb_ complement	clkdiv_sync_ena	unused
CONFIG19	0x13	0x00	bequalsa	aequalsb	reserved	unused	unused	unused	multi_sync_sel	rev
CONFIG20	0x14	0x00	qmc_offseta(7:0)							
CONFIG21	0x15	0x00	qmc_offsetb(7:0)							
CONFIG22	0x16	0x00	qmc_offseta(12:8)					unused	unused	unused
CONFIG23	0x17	0x00	qmc_offsetb(12:8)					sif4_ena	clkpath_sleep_a	clkpath_sleep_b
CONFIG24	0x18	0x83	tsense_ena	clkrecv_sleep	unused	reserved	sleepb	sleepa	reserved	reserved
CONFIG25	0x19	0x00	reserved					extref_ena	reserved	reserved
CONFIG26	0x1A	0x00	reserved		reserved		unused	reserved		
CONFIG27	0x1B	0x00	qmc_gaina(7:0)							
CONFIG28	0x1C	0x00	qmc_gainb(7:0)							
CONFIG29	0x1D	0x00	qmc_phase(7:0)							
CONFIG30	0x1E	0x24	qmc_phase(9:8)		qmc_gaina(10:8)			qmc_gainb(10:8)		
CONFIG31	0x1F	0x12	clk_alarm	tx_off	version(5:0)					

8.5.1 CONFIG0 (address = 0x00) [reset = 0x70]

Figure 56. CONFIG0

7	6	5	4	3	2	1	0
Reserved	fifo_ena	fifo_reset_ena	multi_sync_ena	alarm_out_ena	alarm_pol	mixer_func(1:0)	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. CONFIG0 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved for factory use.
6	fifo_ena	R/W	1	When asserted the FIFO is enabled. When the FIFO is bypassed DACCCLKP/N and DATACLKP/N must be aligned to within t_align.
5	fifo_reset_ena	R/W	1	Allows the FRAME input to reset the FIFO write pointer when asserted
4	multi_sync_ena	R/W	1	Allows the FRAME or OSTR signal to reset the FIFO read pointer when asserted. This selection is determined by multi_sync_sel in register CONFIG19.
3	alarm_out_ena	R/W	0	When asserted the ALARM_SDO pin becomes an output. The functionality of this pin is controlled by the CONFIG6 alarm_mask setting.
2	alarm_pol	R/W	0	This bit changes the polarity of the ALARM signal. (0=negative logic, 1=positive logic)
1:0	mixer_func(1:0)	R/W	00	Controls the function of the mixer block.

Mode	mixer_func(1:0)
Normal	00
High Pass (Fs/2)	01
Fs/4	10
–Fs/4	11

8.5.2 CONFIG1 (address = 0x01) [reset = 0x11]

Figure 57. CONFIG1

7	6	5	4	3	2	1	0
qmc_offset_ena	qmc_correct_ena	fir0_ena	fir1_ena	Unused	iotest_ena	Unused	twos
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. CONFIG1 Field Descriptions

Bit	Field	Type	Reset	Description
7	qmc_offset_ena	R/W	0	When asserted the QMC offset correction circuitry is enabled.
6	qmc_correct_ena	R/W	0	When asserted the QMC phase and gain correction circuitry is enabled.
5	fir0_ena	R/W	0	When asserted FIR0 is activated enabling 2x interpolation.
4	fir1_ena	R/W	1	When asserted FIR1 is activated enabling 4x interpolation. **fir0_ena must be set to '1' for 4x interpolation.**
3	Unused	R/W	0	Reserved for factory use.
2	iotest_ena	R/W	0	When asserted enables the data pattern checker operation.
1	Unused	R/W	0	Reserved for factory use.
0	twos	R/W	1	When asserted the inputs are expected to be in 2's complement format. When de-asserted the input format is expected to be offset-binary.

8.5.3 CONFIG2 (address = 0x02) [reset = 0x00]

Figure 58. CONFIG2

7	6	5	4	3	2	1	0
Unused	Unused	sif_sync	sif_sync_ena	Unused	Unused	out_delay	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. CONFIG2 Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	R/W	0	Reserved for factory use.
6	Unused	R/W	0	Reserved for factory use.
5	sif_sync	R/W	0	Serial interface created sync signal. Set to '1' to cause a sync and then clear to '0' to remove it.
4	sif_sync_ena	R/W	0	When asserted this bit allows the SIF sync to be used. Normal FRAME signals are ignored.
3	Unused	R/W	0	Reserved for factory use.
2	Unused	R/W	0	Reserved for factory use.
1:0	output_delay(1:0)	R/W	00	Delays the output to the DACs from 0 to 3 DAC clock cycles.

8.5.4 CONFIG3 (address = 0x03) [reset = 0x10]

Figure 59. CONFIG3

7	6	5	4	3	2	1	0
64cnt_ena	Unused	Unused	fifo_offset(2:0)			alarm_2away_ena	alarm_1away_ena
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. CONFIG3 Field Descriptions

Bit	Field	Type	Reset	Description
7	64cnt_ena	R/W	0	This enables resetting the alarms after 64 good samples with the goal of removing unnecessary errors. For instance, when checking setup/hold through the pattern checker test, there may initially be errors. Setting this bit removes the need for a SIF write to clear the alarm register.
6	Unused	R/W	0	Reserved for factory use.
5	Unused	R/W	0	Reserved for factory use.
4:2	fifo_offset(2:0)	R/W	100	This is the default FIFO read pointer position after the FIFO read pointer has been synced. With this value the initial difference between write and read pointers can be controlled. This may be helpful in controlling the delay through the device.
1	alarm_2away_ena	R/W	0	When asserted alarms from the FIFO that represent the write and read pointers being 2 away are enabled.
0	alarm_1away_ena	R/W	0	When asserted alarms from the FIFO that represent the write and read pointers being 1 away are enabled.

8.5.5 CONFIG4 (address = 0x04) [reset = 0xFF]

Figure 60. CONFIG4

7	6	5	4	3	2	1	0
coarse_daca(3:0)				coarse_dach(3:0)			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. CONFIG4 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	coarse_daca(3:0)	R/W	1111	Scales the DACA output current in 16 equal steps. $\frac{V_{EXTIO}}{Rbias} \times (coarse\_daca/b + 1)$
3:0	coarse_dach(3:0)	R/W	1111	Scales the DACB output current in 16 equal steps.

8.5.6 CONFIG5 (address = 0x05) READ ONLY

Figure 61. CONFIG5

7	6	5	4	3	2	1	0
tempdata							
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. CONFIG5 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	tempdata	R	N/A	This is the output from the chip temperature sensor. The value of this register in two's complement format represents the temperature in degrees Celsius. **This register must be read with a minimum SCLK period of 1µs.** (Read Only)

8.5.7 CONFIG6 (address =0x06) [reset = 0x00]

Figure 62. CONFIG6

7	6	5	4	3	2	1	0
Unused	alarm_mask						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. CONFIG6 Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	R/W	0	Reserved for factory use.
6:0	alarm_mask	R/W	0000000	These bits control the masking of the alarm outputs. This means that the ALARM_SDO pin will not be asserted if the appropriate bit is set. The alarm will still show up in the CONFIG7 bits. (0=not masked, 1= masked).

alarm_mask	Masked Alarm
6	alarm_from_zerochk
5	alarm_fifo_collision
4	reserved
3	alarm_from_iotest
2	not used (expansion)
1	alarm_fifo_2away
0	alarm_fifo_1away

8.5.8 CONFIG7 (address = 0x07) [reset = 0x00] (WRITE TO CLEAR)

Figure 63. CONFIG7

7	6	5	4	3	2	1	0
Unused	alarm_from_ zerochk	alarm_fifo_ collision	Reserved	alarm_from_ iotest	Unused	alarm_fifo_ 2away	alarm_fifo_ 1away
W	W	W	W	W	W	W	W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. CONFIG7 Field Descriptions

Bit	Field	Type	Reset	Description
7	Unused	W	0	Reserved for factory use.
6	alarm_from_zerochk	W	0	This alarm indicates the 8-bit FIFO write pointer address has an all zeros patterns. Due to pointer address being a shift register, this is not a valid address and will cause the write pointer to be stuck until the next sync. This error is typically caused by timing error or improper power start-up sequence. If this alarm is asserted, resynchronization of FIFO is necessary. Refer to the Power-Up Sequence section for more detail.
5	alarm_fifo_collision	W	0	Alarm occurs when the FIFO pointers over/under run each other.
4	Reserved	W	0	Reserved for factory use.
3	alarm_from_iotest	W	0	This is asserted when the input data pattern does not match the pattern in the iotest_pattern registers.
2	Unused	W	0	Reserved for factory use.
1	alarm_fifo_2away	W	0	Alarm occurs with the read and write pointers of the FIFO are within 2 addresses of each other.
0	alarm_fifo_1away	W	0	Alarm occurs with the read and write pointers of the FIFO are within 1 address of each other.

8.5.9 CONFIG8 (address = 0x08) [reset = 0x00] (WRITE TO CLEAR)

Figure 64. CONFIG8

7	6	5	4	3	2	1	0
iotest_results							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. CONFIG8 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_results	R/W	0x00	The values of these bits tell which bit in the byte-wide LVDS bus failed during the pattern checker test.

8.5.10 CONFIG9 (address = 0x09) [reset = 0x7A]

Figure 65. CONFIG9

7	6	5	4	3	2	1	0
iotest_pattern0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. CONFIG9 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern0	R/W	0x7A	This is dataword0 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.11 CONFIG10 (address = 0x0A) [reset = 0xB6]

Figure 66. CONFIG10

7	6	5	4	3	2	1	0
iotest_pattern1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. CONFIG10 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern1	R/W	0xB6	This is dataword1 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.12 CONFIG11 (address = 0x0B) [reset = 0xEA]

Figure 67. CONFIG11

7	6	5	4	3	2	1	0
iotest_pattern2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. CONFIG11 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern2	R/W	0xB6	This is dataword2 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.13 CONFIG12 (address =0x0C) [reset = 0x45]

Figure 68. CONFIG12

7	6	5	4	3	2	1	0
iotest_pattern3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. CONFIG12 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern3	R/W	0x45	This is dataword3 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.14 CONFIG13 (address =0x0D) [reset = 0x1A]

Figure 69. CONFIG13

7	6	5	4	3	2	1	0
iotest_pattern4							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. CONFIG13 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern4	R/W	0x1A	This is dataword4 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.15 CONFIG14 Register Name (address = 0x0E) [reset = 0x16]

Figure 70. CONFIG14

7	6	5	4	3	2	1	0
iotest_pattern5							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. CONFIG14 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern5	R/W	0x16	This is dataword5 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.16 CONFIG15 Register Name (address = 0x0F) [reset = 0xAA]

Figure 71. CONFIG15

7	6	5	4	3	2	1	0
iotest_pattern6							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. CONFIG15 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern6	R/W	0xAA	This is dataword6 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.17 CONFIG16 (address = 0x10) [reset = 0xV6]

Figure 72. CONFIG16

7	6	5	4	3	2	1	0
iotest_pattern7							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. CONFIG16 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	iotest_pattern7	R/W	0xC6	This is dataword7 in the IO test pattern. It is used with the seven other words to test the input data.

8.5.18 CONFIG17 (address = 0x11) [reset = 0x24]

Figure 73. CONFIG17

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	clk_alarm_mask	tx_off_mask	Reserved	clk_alarm_ena	tx_off_ena
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. CONFIG17 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved for factory use.
6	Reserved	R/W	0	Reserved for factory use.
5	Reserved	R/W	1	Reserved for factory use.
4	clk_alarm_mask	R/W	0	This bit controls the masking of the clock monitor alarm. This means that the ALARM_SDO pin will not be asserted. The alarm will still show up in the clk_alarm bit. (0=not masked, 1= masked).
3	tx_off_mask	R/W	0	This bit control the masking of the transmit enable alarm. This means that the ALARM_SDO pin will not be asserted. The alarm will still show up in the tx_off bit. (0=not masked, 1= masked).
2	Reserved	R/W	1	Reserved for factory use.
1	clk_alarm_ena	R/W	0	When asserted the DATACLK monitor alarm is enabled.
0	tx_off_ena	R/W	0	When asserted a clk_alarm event will automatically disable the DAC outputs by setting them to midscale.

8.5.19 CONFIG18 (address = 0x12) [reset = 0x02]

Figure 74. CONFIG18

7	6	5	4	3	2	1	0
Reserved				daca_complement	dacb_complement	clkdiv_sync_ena	Unused
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. CONFIG18 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R/W	0000	Reserved for factory use.
3	daca_complement	R/W	0	When asserted the output to the DACA is complemented. This allows to effectively change the + and – designations of the LVDS data lines.
2	dacb_complement	R/W	0	When asserted the output to the DACB is complemented. This allows to effectively change the + and – designations of the LVDS data lines.
1	clkdiv_sync_ena	R/W		Enables the syncing of the clock divider using the OSTR signal or the FRAME signal passed through the FIFO. This selection is determined by multi_sync_sel in register CONFIG19. The internal divided-down clocks will be phase aligned after syncing. See Power-Up Sequence section for more detail.
0	Unused	R/W	0	Reserved for factory use.

8.5.20 CONFIG19 (address = 0x13) [reset = 0x00]

Figure 75. CONFIG19

7	6	5	4	3	2	1	0
bequalsa	aequalsb	Reserved	Unused	Unused	Unused	multi_sync_sel	rev
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. CONFIG19 Field Descriptions

Bit	Field	Type	Reset	Description
7	bequalsa	R/W	0	When asserted the DACA data is driven onto DACB.
6	aequalsb	R/W	0	When asserted the DACB data is driven onto DACA.
5	Reserved	R/W	0	Reserved for factory use.
4	Unused	R/W	0	Reserved for factory use.
3	Unused	R/W	0	Reserved for factory use.
2	Unused	R/W	0	Reserved for factory use.
1	multi_sync_sel	R/W	0	Selects the signal source for multiple device and clock divider synchronization. **multi_sync_sel** – **Sync Source** 0 – OSTR 1 – FRAME through FIFO handoff
0	rev	R/W	0	Reverse the input bits for the data word. MSB becomes LSB.

8.5.21 CONFIG20 (address = 0x14) [reset = 0x00] (CAUSES AUTOSYNC)

Figure 76. CONFIG20

7	6	5	4	3	2	1	0
qmc_offseta							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. CONFIG20 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	qmc_offseta	R/W	0x00	Lower 8 bits of the DAC A offset correction. The offset is measured in DAC LSBs. **Writing this register causes an autosync to be generated. This loads the values of all four qmc_offset registers (CONFIG20-CONFIG23) into the offset block at the same time. When updating the offset values CONFIG20 should be written last. Programming any of the other three registers will not affect the offset setting.**

8.5.22 CONFIG21 (address = 0x15) [reset = 0x00]

Figure 77. CONFIG21

7	6	5	4	3	2	1	0
qmc_offsetb							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. CONFIG21 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	qmc_offsetb	R/W	0x00	Lower 8 bits of the DAC B offset correction. The offset is measured in DAC LSBs.

8.5.23 CONFIG22 (address = 0x16) [reset = 0x00]

Figure 78. CONFIG22

7	6	5	4	3	2	1	0
qmc_offseta					Unused	Unused	Unused
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. CONFIG22 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	qmc_offseta	R/W	00000	Upper 5 bits of the DAC A offset correction.
2	Unused	R/W	0	Reserved for factory use.
1	Unused	R/W	0	Reserved for factory use.
0	Unused	R/W	0	Reserved for factory use.

8.5.24 CONFIG23 (address = 0x17) [reset = 0x00]

Figure 79. CONFIG23

7	6	5	4	3	2	1	0
qmc_offsetb(12:8)					sif4_ena	clkpath_sleep_a	clkpath_sleep_b
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. CONFIG23 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	qmc_offsetb(12:8)	R/W	00000	Upper 5 bits of the DAC B offset correction.
2	sif4_ena	R/W	0	When asserted the SIF interface becomes a 4 pin interface. The ALARM pin is turned into a dedicated output for the reading of data.
1	clkpath_sleep_a	R/W	0	When asserted puts the clock path through DAC A to sleep. This is useful for sleeping individual DACs. Even if the DAC is asleep the clock needs to pass through it for the logic to work. However, if the chip is being put into a power down mode, then all parts of the DAC can be turned off.
0	clkpath_sleep_b	R/W	0	When asserted puts the clock path through DAC B to sleep.

8.5.25 CONFIG24 (address = 0x18) [reset = 0x83]

Figure 80. CONFIG24

7	6	5	4	3	2	1	0
tsense_ena	clkrecv_sleep	Unused	Reserved	sleepb	sleepa	Reserved	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. CONFIG24 Field Descriptions

Bit	Field	Type	Reset	Description
7	tsense_ena	R/W	1	Turns on the temperature sensor when asserted.
6	clkrecv_sleep	R/W	0	When asserted the clock input receiver gets put into sleep mode. This also affects the OSTR receiver.
5	Unused	R/W	0	Reserved for factory use.
4	Reserved	R/W	0	Reserved for factory use.
3	sleepb	R/W	0	When asserted DACB is put into sleep mode.
2	sleepa	R/W	0	When asserted DACA is put into sleep mode.
1	Reserved	R/W	1	Reserved for factory use.
0	Reserved	R/W	1	Reserved for factory use.

8.5.26 CONFIG25 (address = 0x19) [reset = 0x00]

Figure 81. CONFIG25

7	6	5	4	3	2	1	0
Reserved					extref_ena	Reserved	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. CONFIG25 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R/W	00000	Turns on the temperature sensor when asserted.
2	extref_ena	R/W	0	Allows the device to use an external reference or the internal reference. (0=internal, 1=external)
1	Reserved	R/W	0	Reserved for factory use.
0	Reserved	R/W	0	Reserved for factory use.

8.5.27 CONFIG26 (address = 0x1a) [reset = 0x00]

Figure 82. CONFIG26

7	6	5	4	3	2	1	0
Reserved		Reserved		Unused	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. CONFIG26 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	Reserved for factory use.
5:4	Reserved	R/W	00	Reserved for factory use.
3	Unused	R/W	0	Reserved for factory use.
2:0	Reserved	R/W	000	Reserved for factory use.

8.5.28 CONFIG27 (address =0x1b) [reset = 0x00] (CAUSES AUTOSYNC)

Figure 83. CONFIG27

7	6	5	4	3	2	1	0
qmc_gaina							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. CONFIG27 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	qmc_gaina	R/W	0x00	Lower 8 bits of the 11-bit DAC A QMC gain word. The upper 3 bits are located in the CONFIG30 register. The full 11-bit qmc_gaina(10:0) value is formatted as UNSIGNED with a range of 0 to 1.9990 and a default gain of 1. The implied decimal point for the multiplication is between bits 9 and 10. **Writing this register causes an autosync to be generated. This loads the values of all four qmc_phase/gain registers (CONFIG27-CONFIG30) into the QMC block at the same time. When updating the QMC phase and/or gain values CONFIG27 should be written last. Programming any of the other three registers will not affect the QMC settings.**

8.5.29 CONFIG28 (address = 0x1C) [reset = 0x00]

Figure 84. CONFIG28

7	6	5	4	3	2	1	0
gmc_gainb							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. CONFIG28 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	gmc_gainb	R/W	0x00	Lower 8 bits of the 11-bit DAC B QMC gain word. The upper 3 bits are located in the CONFIG30 register. Refer to CONFIG27 for formatting.

8.5.30 CONFIG29 (address = 0x1D) [reset = 0x00]

Figure 85. CONFIG29

7	6	5	4	3	2	1	0
qmc_phase							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. CONFIG29 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	qmc_phase	R/W	0x00	Lower 8-bits of the 10-bit QMC phase word. The upper 2 bits are in the CONFIG30 register. The full 10-bit qmc_phase(9:0) word is formatted as two's complement and scaled to occupy a range of –0.125 to 0.12475 (note this value does not correspond to degrees) and a default phase correction of 0. To accomplish QMC phase correction, this value is multiplied by the current 'Q' sample, then summed into the 'I' sample.

8.5.31 CONFIG30 (address = 0x1E) [reset = 0x24]

Figure 86. CONFIG30

7	6	5	4	3	2	1	0
qmc_phase(9:8)		qmc_gaina(10:8)			qmc_gainb(10:8)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. CONFIG30 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	qmc_phase(9:8)	R/W	00	Upper 2 bits of qmc_phase. Defaults to zero.
5:3	qmc_gaina(10:8)	R/W	100	Upper 3 bits of qmc_gaina. Defaults to unity gain.
2:0	qmc_gainb(10:8)	R/W	100	Upper 3 bits of qmc_gainb. Defaults to unity gain.

8.5.32 VERSION31 (address = 0x1F) [reset = 0x12] (PARTIAL READ ONLY)

Figure 87. VERSION31

7	6	5	4	3	2	1	0
clk_alarm	tx_off	version(5:0)					
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. VERSION31 Field Descriptions

Bit	Field	Type	Reset	Description
7	clk_alarm	R	0	This bit is set to '1' when DATACLK is stopped for 4 clock cycles. Once set, the bit needs to be cleared by writing a '0'.
6	tx_off	R	0	This bit is set to '1' when the clk_alarm is triggered. When set the DAC outputs are forced to mid-level. Once set, the bit needs to be cleared by writing a '0'.
5:0	version(5:0)	R	010010	A hardwired register that contains the version of the chip. (Read Only)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DAC3283 is appropriate for a variety of transmitter applications including complex I/Q direct conversion, up-conversion using an intermediate frequency (IF) and diversity applications.

9.2 Typical Application

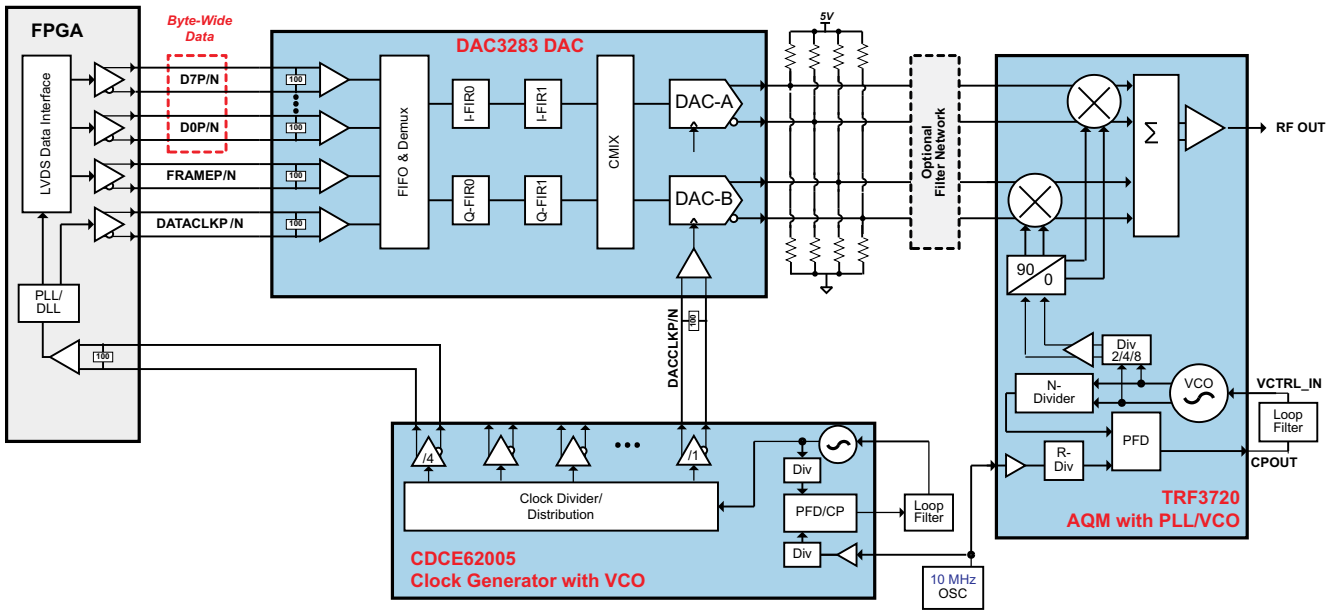


Figure 88. System Diagram of Direct Conversion Radio

9.2.1 Design Requirements

For this design example of a direct conversion transmitter, use the parameters in Table 41.

Table 41. Design Parameters

PARAMETER	VALUE
Channel Type	4x W-CDMA Carriers, each with 3.84 MHz bandwidth (20 MHz total bandwidth)
Input Data Rate	184.32 MSPS
Interpolation	4
NCO Frequency	Bypassed
Output IF	None (Complex baseband)
DAC Conversion Rate (DACCLK frequency)	737.28 MSPS

9.2.2 Detailed Design Procedure

9.2.2.1 Direct Conversion Radio

Refer to Figure 88 for an example Direct Conversion Radio. The DAC3283 receives an interleaved complex I/Q baseband input data stream and increases the sample rate through interpolation by a factor of 2 or 4. By performing digital interpolation on the input data, undesired images of the original signal can be push out of the band of interest and more easily suppressed with analog filters.

For a Zero IF (ZIF) frequency plan, complex mixing of the baseband signal is not required. Alternatively, for a Complex IF frequency plan the input data can be pre-placed at an IF within the bandwidth limitations of the interpolation filters. In addition, complex mixing is available using the coarse mixer block to up-convert the signal. The output of both DAC channels is used to produce a Hilbert transform pair and can be expressed as:

$$A_{OUT}(t) = A(t)\cos(\omega_c t) - B(t)\sin(\omega_c t) = m(t) \quad (1)$$

$$B_{OUT}(t) = A(t)\sin(\omega_c t) + B(t)\cos(\omega_c t) = m_h(t) \quad (2)$$

where m(t) and $m_h(t)$ connote a Hilbert transform pair and ω_c is the mixer frequency. The complex output is input to an analog quadrature modulator (AQM) such as the Texas Instruments TRF3720 for a single side-band (SSB) up conversion to RF. A passive (resistor only) interface to the AQM with an optional LC filter network is recommended. The TRF3720 includes a VCO/PLL to generate the LO frequency. Upper single-sideband upconversion is achieved at the output of the analog quadrature modulator, whose output is expressed as:

$$RF(t) = A(t)\cos(\omega_c + \omega_{LO})t - B(t)\sin(\omega_c + \omega_{LO})t \quad (3)$$

Flexibility is provided to the user by allowing for the selection of negative mixing frequency to produce a lower-sideband upconversion. Note that the process of complex mixing translates the signal frequency from 0Hz means that the analog quadrature modulator IQ imbalance produces a sideband that falls outside the signal of interest. DC offset error in DAC and AQM signal path may produce LO feed-through at the RF output which may fall in the band of interest. To suppress the LO feed-through, the DAC3283 provides a digital offset correction capability for both DAC-A and DAC-B paths. In addition phase and gain imbalances in the DAC and AQM result in a lower-sideband product. The DAC3283 offers gain and phase correction capabilities to minimize the sideband product.

The complex IF architecture has several advantages over the real IF architecture:

- Uncalibrated side-band suppression ~ 35dBc compared to 0dBc for real IF architecture.
- Direct DAC to AQM interface – no amplifiers required
- DAC 2nd Nyquist zone image is offset f_{DAC} compared with f_{DAC}– 2 x IF for a real IF architecture, reducing the need for filtering at the DAC output.
- Uncalibrated LO feed through for AQM is ~ 35 dBc and calibration can reduce or completely remove the LO feed through.

9.2.3 Application Performance Plots

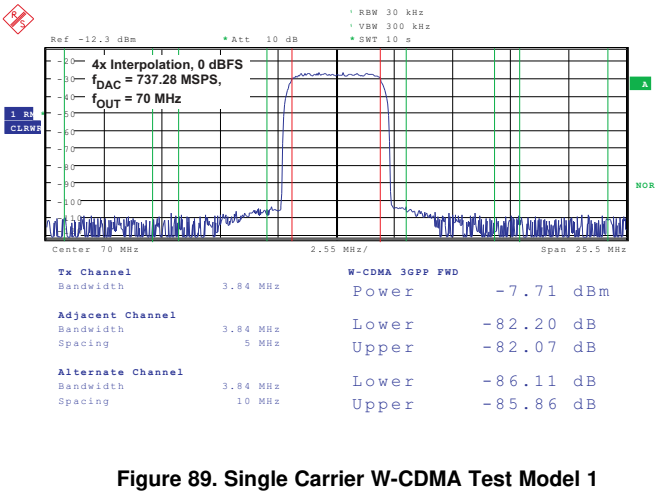


Figure 89. Single Carrier W-CDMA Test Model 1

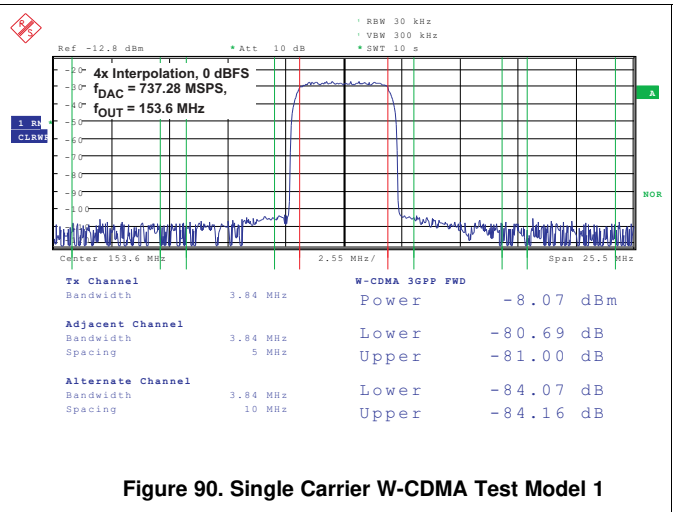


Figure 90. Single Carrier W-CDMA Test Model 1

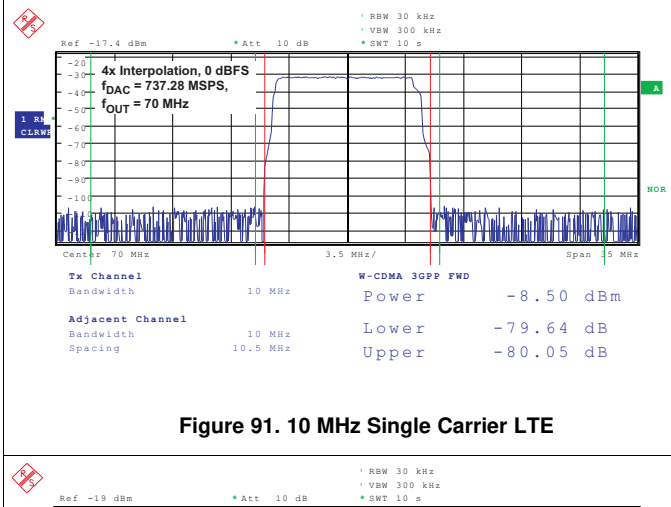


Figure 91. 10 MHz Single Carrier LTE

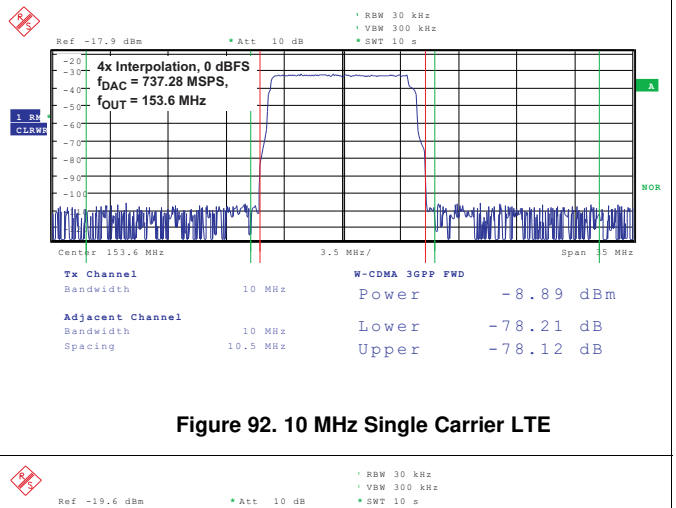


Figure 92. 10 MHz Single Carrier LTE

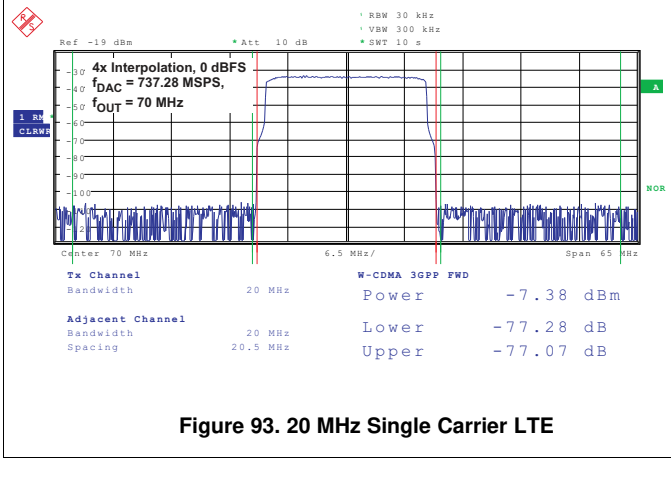


Figure 93. 20 MHz Single Carrier LTE

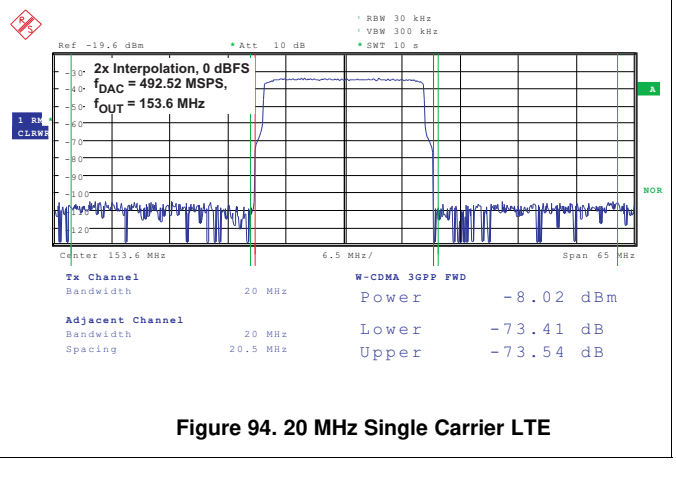


Figure 94. 20 MHz Single Carrier LTE

10 Power Supply Recommendations

10.1 Power-up Sequence

The following startup sequence is recommended to power-up the DAC3283:

1. Set TXENABLE low.
2. Supply all 1.8V voltages (DACVDD, DIGVDD, CLKVDD and VFUSE) and all 3.3V voltages (AVDD). The 1.8V and 3.3V supplies can be powered up simultaneously or in any order. There are no specific requirements on the ramp rate for the supplies.
3. Provide all LVPECL inputs: DACCLKP/N and the optional OSTRP/N. These inputs can also be provided after the SIF register programming.
4. Program all the SIF registers. Also program default value to the registers not being used.
5. FIFO configuration needed for synchronization:
   (a) Program *fifo_reset_ena* (config0, bit<5>) to enable FRAMEP/N as the FIFO input pointer sync source.
   (b) Program *multi_sync_ena* (config0, bit<4>) to enable syncing of the FIFO output pointer.
   (c) Program *multi_sync_sel* (config19, bit<1>) to select the FIFO output pointer and clock divider sync source
6. Clock divider configuration needed for synchronization:
   (a) Program *clkdiv_sync_ena*(config18, bit<1>) to "1" to enable clock divider sync.
7. Provide all LVDS inputs (D[7:0]P/N, DATACLKP/N, and FRAMEP/N) simultaneously. Synchronize the FIFO and clock divider by providing the pulse or periodic signals needed.
   (a) For Single Sync Source Mode where FRAMEP/N is used to sync the FIFO, a single rising edge for FIFO, FIFO data formatter, and clock divider sync is recommended. Periodic sync signal is not recommended due to the non-deterministic latency of the sync signal through the clock domain transfer.
   (b) For Dual Sync Sources Mode, either single pulse or periodic sync signals can be used.
8. FIFO and clock divider configurations after all the sync signals have provided the initial sync pulses needed for synchronization:
   (a) For Single Sync Source Mode where the clock divider sync source is FRAMEP/N, clock divider syncing may be disabled after DAC3283 initialization and before the data transmission by setting *clkdiv_sync_ena* (config18, bit<1>) to “0”. This is to prevent accidental syncing of the clock divider when sending FRAMEP/N pulse to other digital blocks.
   (b) For Dual Sync Sources Mode, where the clock divider sync source is from the OSTRP/N, the clock divider syncing may be enabled at all time.
   (c) Optionally, to prevent accidental syncing of the FIFO, disable FIFO syncing by setting *fifo_reset_ena* and *multi_sync_ena* to "0" after the FIFO input and output pointers are initialized. If the FIFO sync remains enabled after initialization, the FRAMEP/N pulse must occur in ways to not disturb the FIFO operation. Refer to the INPUT FIFO section for detail.
9. Enable transmit of data by asserting the TXENABLE pin.
10. At all times, if any of the clocks (i.e. DATACLK or DACCLK) is lost or FIFO collision alarm is detected, a complete resynchronization of the DAC is necessary. Set TXENABLE low and repeat step 5 through 9. Program the FIFO configuration and clock divider configuration per step 5 and 6 appropriately to accept the new sync pulse or pulses for the synchronization.

11 Layout

11.1 Layout Guidelines

The design of the PCB is critical to achieve the full performance of the DAC3283 device. Defining the PCB stackup should be the first step in the board design. Experience has shown that at least 6 layers are required to adequately route all required signals to and from the device. Each signal routing layer must have an adjacent solid ground plane to control signal return paths to have minimal loop areas and to achieve controlled impedances for microstrip and stripline routing. Power planes must also have adjacent solid ground planes to control supply return paths. Minimizing the spacing between supply and ground planes improves performance by increasing the distributed decoupling.

Although the DAC3283 device consists of both analog and digital circuitry, TI highly recommends solid ground planes that encompass the device and its input and output signal paths. TI does not recommend split ground planes that divide the analog and digital portions of the device. Split ground planes may improve performance if a nearby, noisy, digital device is corrupting the ground reference of the analog signal path. When split ground planes are employed, one must carefully control the supply return paths and keep the paths on top of their respective ground reference planes.

Quality analog output signals and input conversion clock signal path layout is required for full dynamic performance. Symmetry of the differential signal paths and discrete components in the path is mandatory and symmetrical shunt-oriented components should have a common grounding via. The high frequency requirements of the analog output and clock signal paths necessitate using differential routing with controlled impedances and minimizing signal path stubs (including vias) when possible.

Coupling onto or between the clock and output signal paths should be avoided using any isolation techniques available including distance isolation, orientation planning to prevent field coupling of components like inductors and transformers, and providing well coupled reference planes. Via stitching around the clock signal path and the input analog signal path provides a quiet ground reference for the critical signal paths and reduces noise coupling onto these paths. Sensitive signal traces must not cross other signal traces or power routing on adjacent PCB layers, rather a ground plane must separate the traces. If necessary, the traces should cross at 90 ° angles to minimize crosstalk.

The substrate (dielectric) material requirements of the PCB are largely influenced by the speed and length of the high speed serial lanes. Affordable and common FR4 varieties are adequate in most cases.

Coupling of ambient signals into the signal path is reduced by providing quiet, close reference planes and by maintaining signal path symmetry to ensure the coupled noise is common-mode. Faraday caging may be used in very noisy environments and high dynamic range applications to isolate the signal path.

11.2 Layout Example

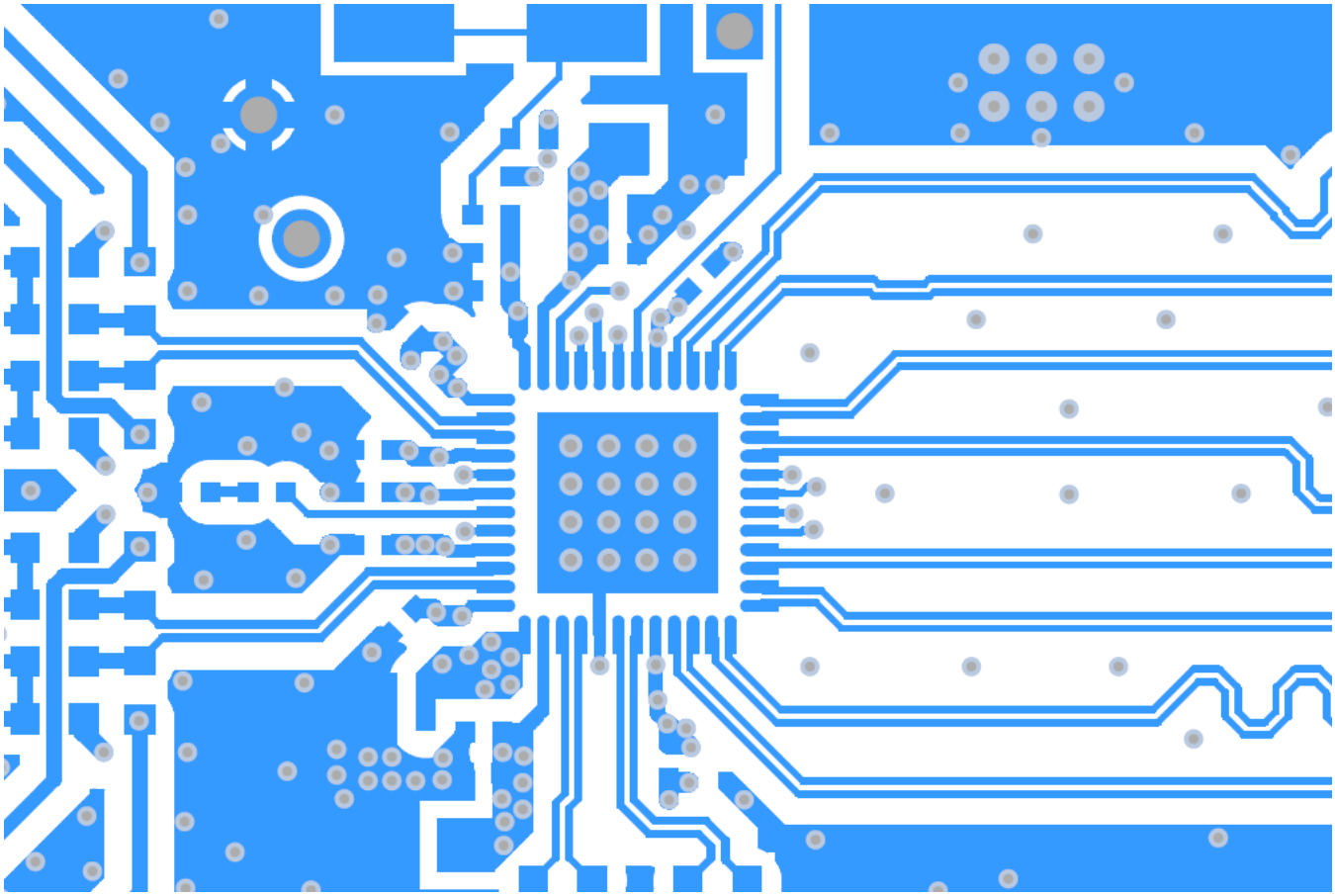


Figure 95. Layout

12 Device and Documentation Support

12.1 Documentation Support

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC3283IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	DAC3283I	Samples
DAC3283IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	DAC3283I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

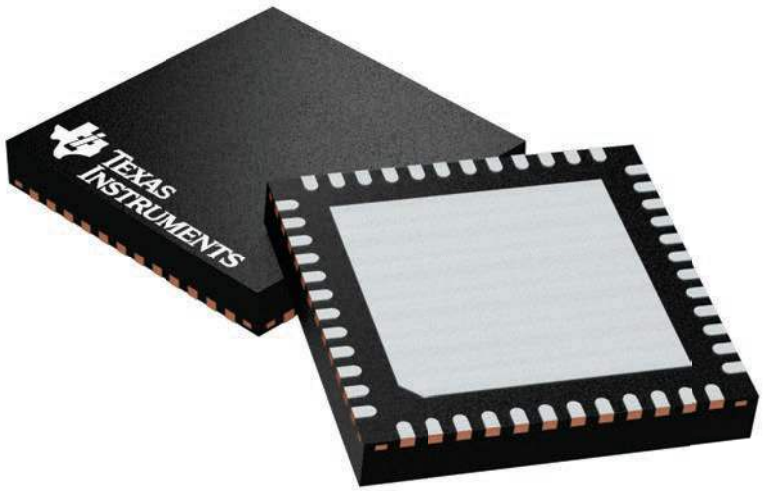
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

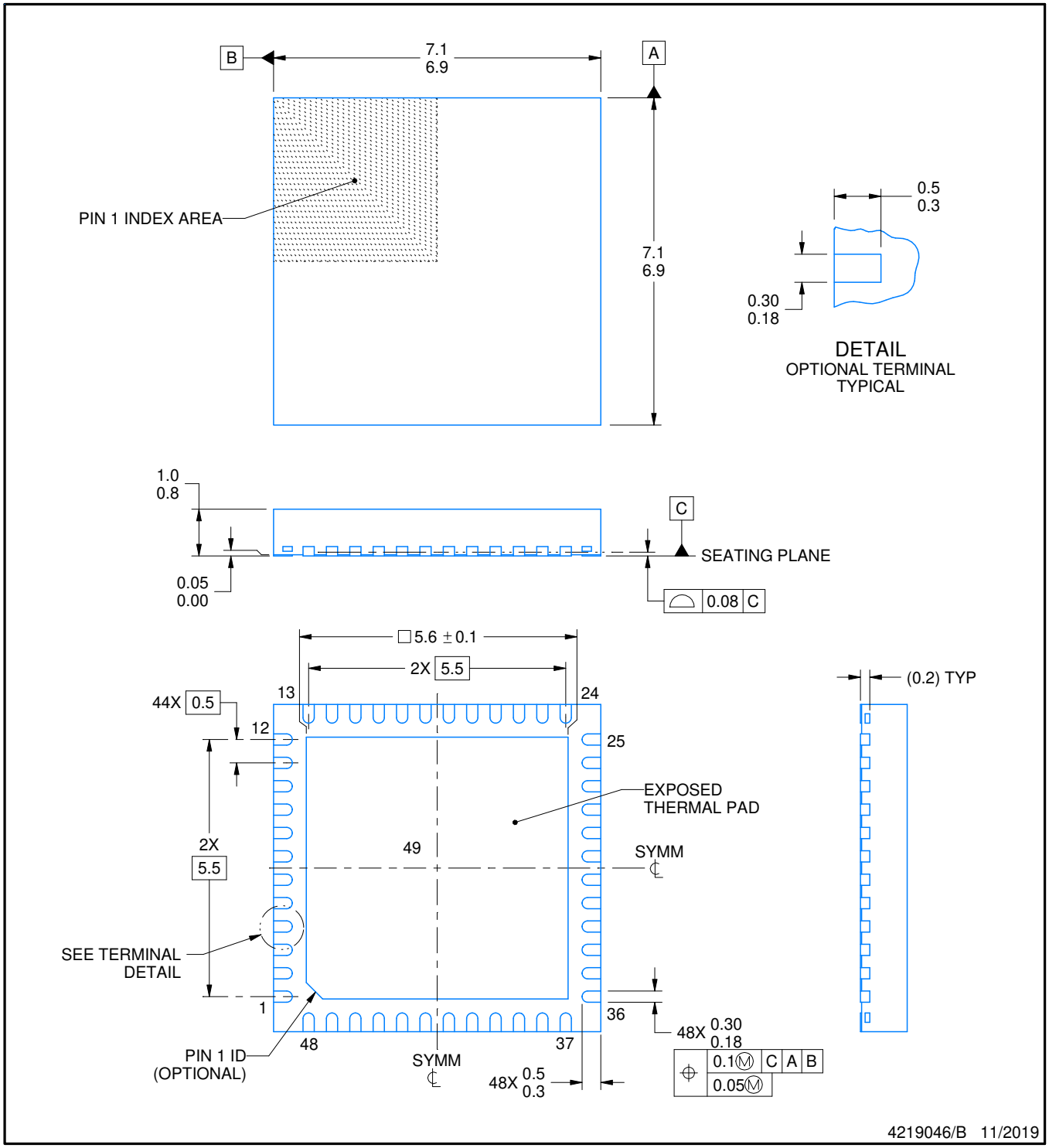
4224671/A

PACKAGE OUTLINE

RGZ0048D

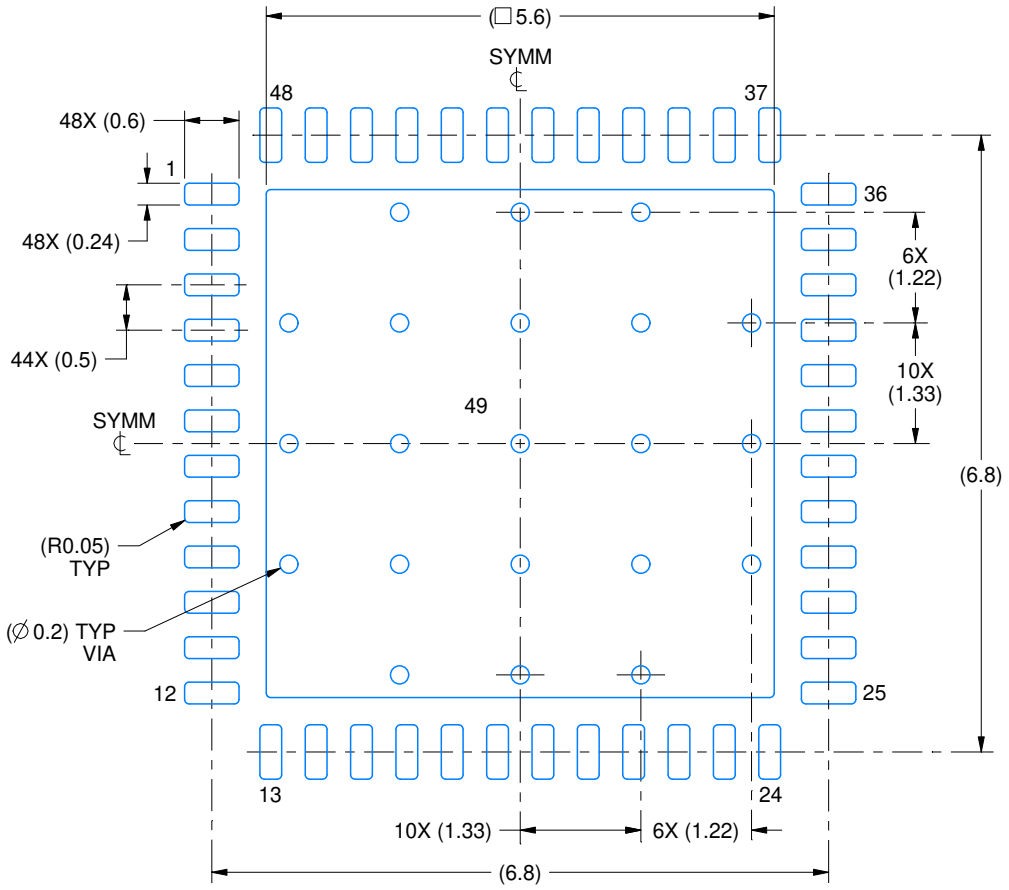
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

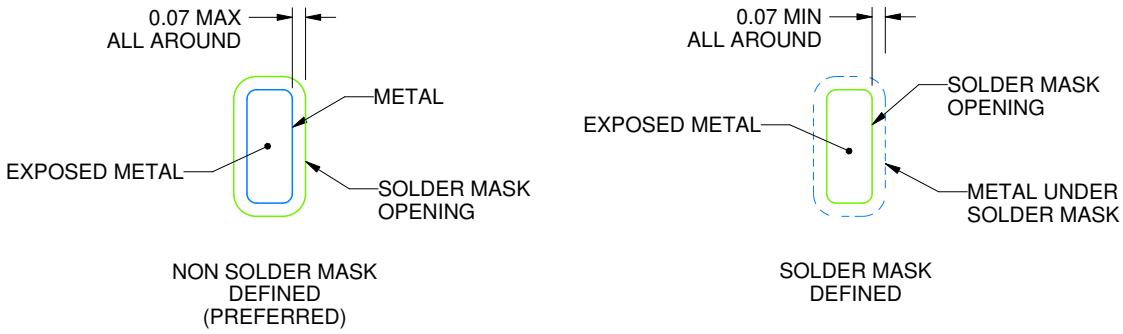


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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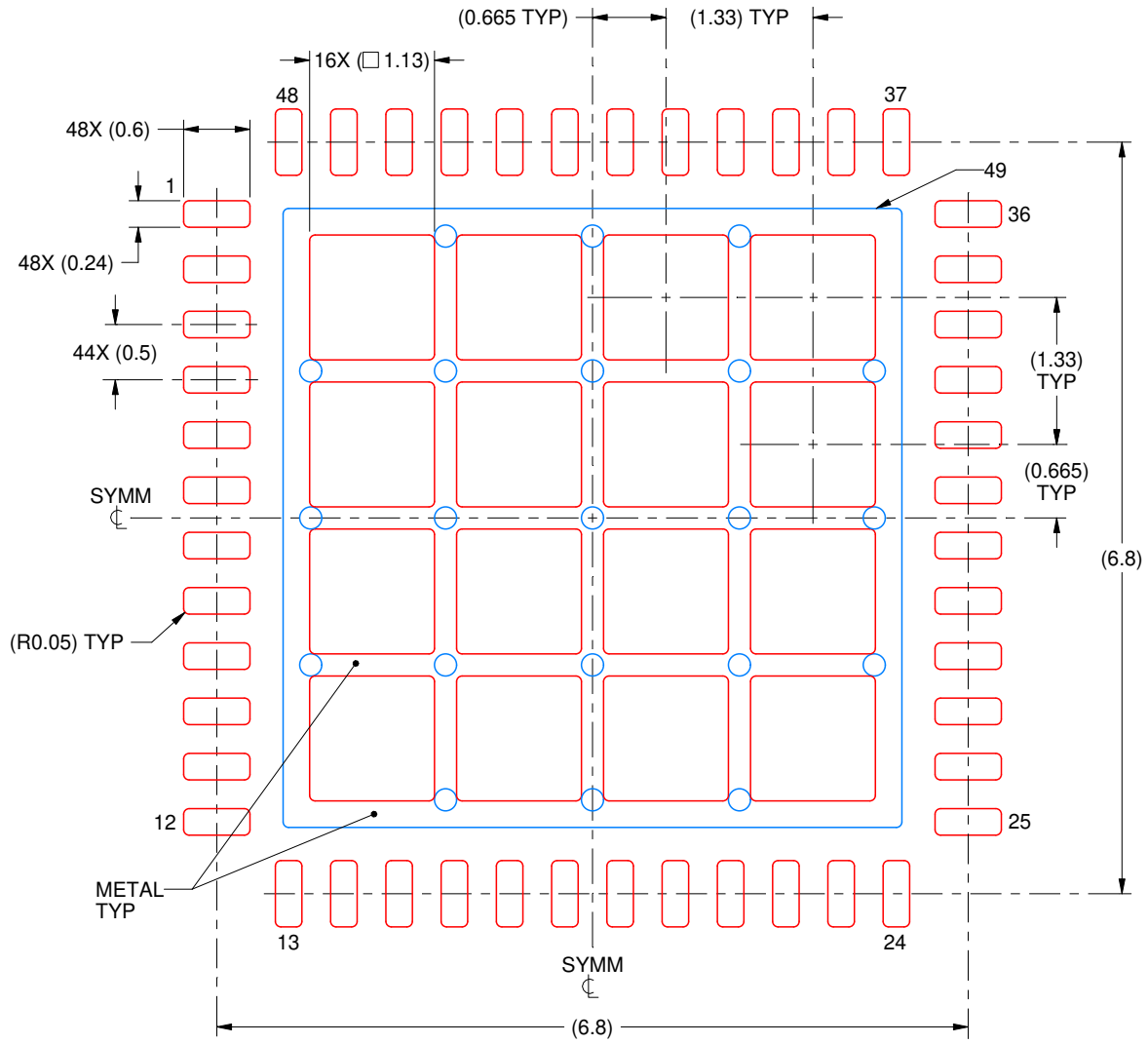
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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