

CGD1700HB3P-HM3

Dual Channel Differential Isolated Gate Driver

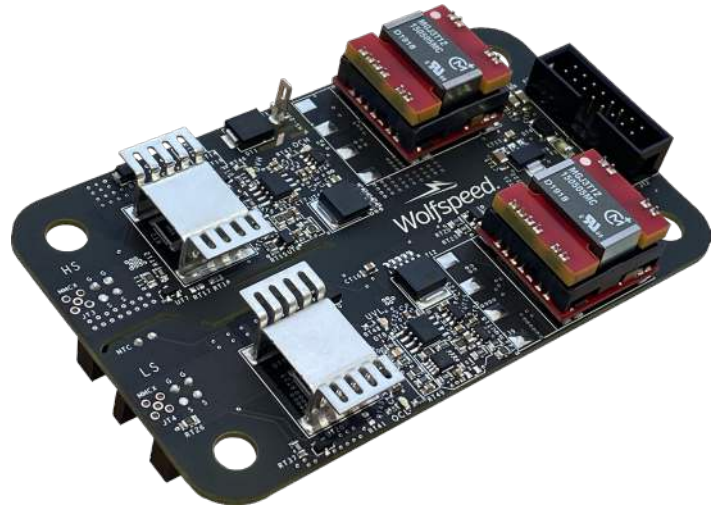
HM3 CPM3 SiC Half-Bridge Module Companion Tool

| | |
|-----------------|----------------|
| V_{Drive} | +15/-4V |
| I_G | ±14 A |
| $R_{G,EXT-ON}$ | 5 Ω |
| $R_{G,EXT-OFF}$ | 2.5 Ω |

Technical Features

- Optimized for use with Cree’s High-Performance [HM3 Half-Bridge Power Modules](#)
- High-Frequency, Ultra-Fast Switching Operation
- On-Board 3 W Isolated Power Supplies
- Configurable UVLO with Hysteresis
- On-Board Over-Current, Shoot-Through, and Reverse Polarity Protection
- Differential Inputs for Increased Noise Immunity
- Direct Mount, Low Inductance Design
- Isolated PWM-Encoded NTC resistance measurement
- Single-Ended to Differential Daughter Board Available Upon Request ([CGD12HB00D](#))

Package



Applications

- DC Bus Voltages up to 1500 V

Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-------------|---|-------------|------|
| V_{DC} | Supply Voltage | -0.5 to 18 | V |
| V_I | Logic Level Inputs | -0.5 to 5.5 | |
| I_O | Output Peak Current ($T_A = 25\text{ °C}$) | ±14 | A |
| P_{Drive} | Output Power per Channel ($T_A = 25\text{ °C}$) | 3 | W |
| f_S | Maximum Switching Frequency (Module & MOSFET Dependent, see Power Estimate Section) | 94 | kHz |
| T_{op} | Ambient Operating Temperature | -35 to 85 | |
| T_{stg} | Storage Temperature | -50 to 125 | |

Gate Driver Electrical Characterization

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------|--|------|------|------|-------------|---|
| V_{DC} | Supply Voltage | 9 | 12 | 18 | V | |
| V_{UVLO} | Secondary Under Voltage Lockout | 13.8 | 14 | 14.3 | | $V_{GATE,HIGH}$, Voltage Going High |
| | Secondary UVLO Hysteresis | | 1.2 | | | |
| V_{IH} | High Level Logic Input Voltage | 3.5 | | 5.5 | | Single-Ended Inputs |
| V_{IL} | Low Level Logic Input Voltage | 0 | | 1.5 | | |
| V_{IDCM} | Differential Input Common Mode Range | -7 | - | +12 | | Differential Inputs |
| V_{IDTH} | Differential Input Threshold Voltage | -200 | -125 | -50 | mV | $V_{ID} = V_{Pos-Line} - V_{Neg-Line}$ |
| V_{OD} | Differential Output Magnitude | 2 | 3.1 | | V | $R_L = 100 \Omega$ |
| $V_{GATE,HIGH}$ | High Level Output Voltage | | +15 | | | |
| $V_{GATE,LOW}$ | Low Level Output Voltage | | -4 | | | |
| V_{IOWM} | Working Isolation Voltage | | 1500 | | | V_{RMS} |
| C_{ISO} | Isolation Capacitance | | 17 | | pF | Per Channel |
| CMTI | Common Mode Transient Immunity | 100 | | | kV/ μ s | $V_{CM} = 1500$ V |
| R_{GIC-ON} | Output Resistance | | 0.4 | 0.8 | Ω | Gate Drive Buffer IC |
| $R_{GIC-OFF}$ | Output Resistance | | 0.3 | 0.6 | | |
| $R_{G,EXT-ON}$ | External Turn-on Resistance ¹ | | 5 | | | External SMD Resistor 2512 (6432 Metric) |
| $R_{G,EXT-OFF}$ | Equivalent External Turn-off Resistance ¹ | | 2.5 | | | |
| D_{VF-OFF} | Turn-off Diode Forward Voltage | 0.62 | 0.67 | 0.82 | V | |
| t_{ON} | Output Rise Time | | 906 | | ns | $R_{G,Ext-ON} = 5 \Omega$, $R_{G,Ext-OFF} = 2.5 \Omega$ $C_{Load} = 68$ nF From 10% to 90% |
| t_{OFF} | Output Fall Time | | 527 | | | |
| t_{PHL} | Propagation Delay (Turn Off) | | 95 | | | $R_{G,Ext-ON} = 5 \Omega$, $R_{G,Ext-OFF} = 2.5 \Omega$ $C_{Load} = 0$ nF From 50% to 50% |
| t_{PHL} | Propagation Delay (Turn On) | | 83 | | | |
| $t_{PD-FAULT}$ | Over-Current Propagation Delay to FAULT Signal Low | | 40 | | | Does Not Include Blanking |
| V_{OCTH} | Over-Current Trip Threshold Voltage | | 3.5 | | V | Measured V_{DS} of FET |
| R_{SS} | Soft-Shutdown Resistance ² | | 5 | | Ω | |

- 1 Additional output resistance is added with 5 Ω 2512 SMD resistors. A diode is provided in the turn-off path allowing for separate control of turn-on and turn-off. The equivalent turn-off resistance is the parallel combination of the two resistors.
- 2 Soft-Shutdown network will safely turn off the gate in the event an over-current is detected.

Input Connector Information

| Pin Number | Parameter | Description |
|------------|---------------------------------|---|
| 1 | V_{DC} | Power supply input pin (+12 V Nominal Input) |
| 2 | Common | Common |
| 3 | HS-P (*) | Positive line of 5 V differential high-side PWM signal pair. Terminated Into 250 Ω . |
| 4 | HS-N (*) | Negative line of 5 V differential high-side PWM signal pair. Terminated into 250 Ω . |
| 5 | LS-P (*) | Positive line of 5 V differential low-side PWM signal pair. Terminated into 250 Ω . |
| 6 | LS-N (*) | Negative line of 5 V differential low-side PWM signal pair. Terminated into 250 Ω . |
| 7 | $\overline{\text{FAULT-P}}$ (*) | Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. |
| 8 | $\overline{\text{FAULT-N}}$ (*) | Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA. |
| 9 | NTC-P (*) | Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via PWM. |
| 10 | NTC-N (*) | Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20mA. Temperature measurement is encoded via PWM. |
| 11 | $\overline{\text{PS-Dis}}$ | Pull down to disable power supply. Pull up (+5 V) or leave floating to enable. Gate and source are connected with 10 k Ω when disabled. |
| 12 | Common | Common |
| 13 | PWM-EN | Pull down to disable PWM input logic. Pull up (+5 V) or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled. |
| 14 | Common | Common |
| 15 | $\overline{\text{RESET}}$ | Pull down to clear over-current fault condition or disable over-current protection. Pull up (+5 V) or leave floating to enable. |
| 16 | Common | Common |

* Inputs 3 - 10 are differential pairs.

Signal Descriptions

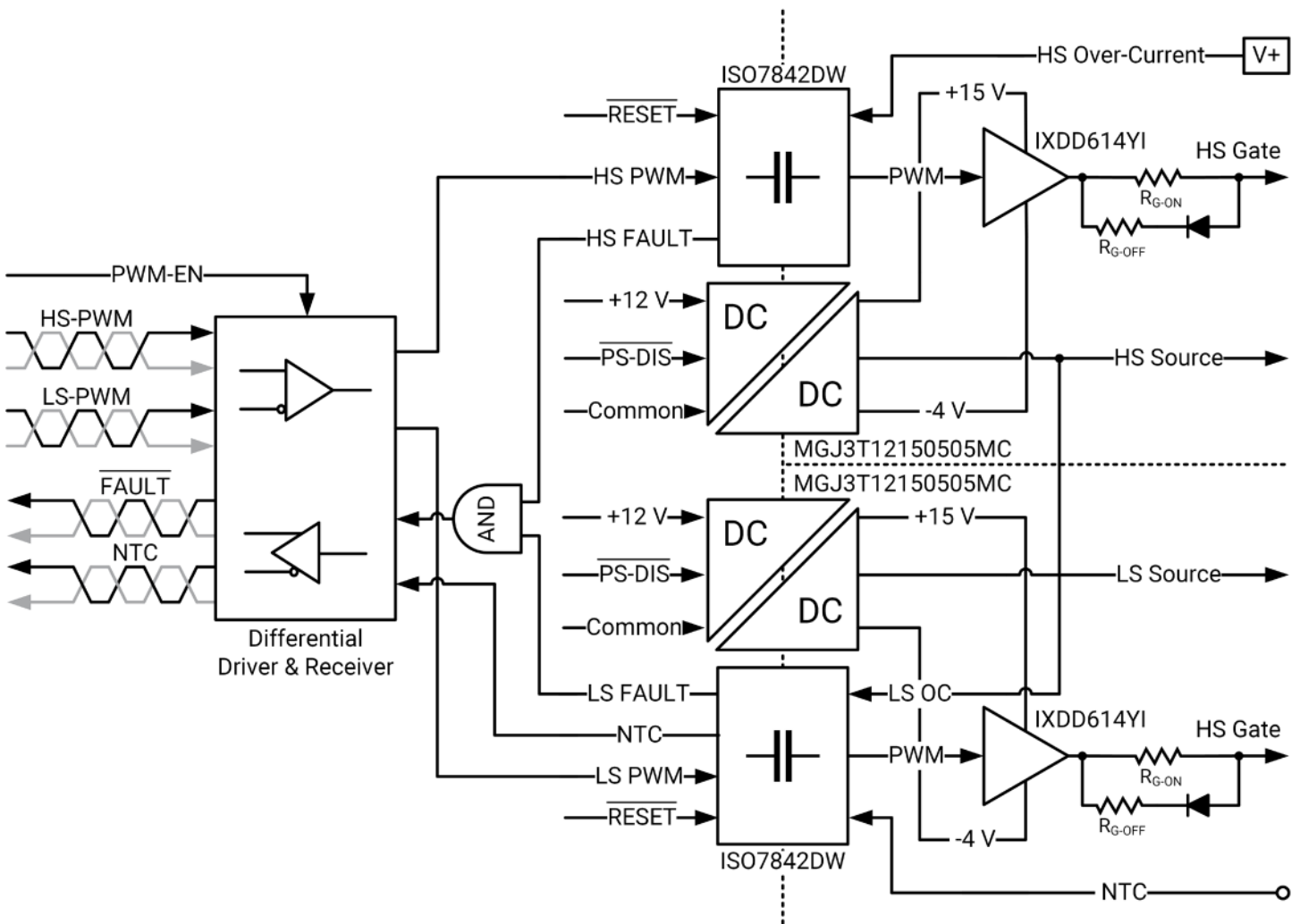
- PWM Signals:** High-side and low-side PWM are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 250 Ω . Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator. A single-ended to differential daughter board is available upon request ([CGD12HB00D](#)).
- FAULT Signal:** The fault signal is a RS-422 compatible differential output with a maximum drive strength of 20 mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an over-current fault or UVLO fault condition is detected on either channel.
- UVLO Fault:** The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through $R_{G,EXT-OFF}$ for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. When there is no UVLO fault present, a green LED indicates a power good state. The LED, UVH, indicates a high-side power good status and UVL indicates a low-side power good status.
- Over-Current Fault:** An over-current fault is an indication of an over-current event in the SiC power module. The over-current protection circuit measures the drain-source voltage, and the fault will indicate if this voltage has risen above a level corresponding to the safe current limit. When a fault has occurred the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft-shutdown resistor, R_{SS} . The drain-source limit can be configured through on-board resistors. The over-current fault is latched upon detection and must be cleared by the user with a low pulse of at least 25 ns on the **RESET** signal, which is a +5 V logic-level input signal. The over-current protection is enabled by default, but it can be disabled by pulling RESET low. A drain sense connection is provided by a quick-connect spade connector JT1 for the high-side channel. The low-side drain sense connection is provided by a direct on-board connection to the high-side source.
- NTC:** The NTC output is a differential signal that returns the resistance of the NTC temperature sensor integrated into HM3 modules. The signal is a 50 kHz PWM signal that encodes the resistance of the temperature sensor. The approximate temperature of the module can be determined from this resistance. See the section NTC Temperature Feedback for further details.
- PS-DIS:** The PS-DIS signal is a +5 V logic-level input that disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. With the power supplies disabled the gate will be tied to the source via a 10 k Ω resistor. This signal can be used for startup sequencing.
- PWM-EN:** The PWM-EN is a +5 V logic-level input that enables the PWM inputs for both channels. When this signal is pulled down the differential receivers for both channels are disabled and the gates will both be pulled low through $R_{G,EXT-OFF}$. All protection circuitry and power supplies will continue to operate including FAULT and NTC outputs.
- Over-Voltage and Reverse Polarity Protection:** Power input on pin 1 of the gate driver connector features a Zener diode to protect the gate driver from damage by connecting a power source that exceeds the voltage rating of the gate driver. There is also a diode in-line with the power input to protect against connecting a power source with positive and negative polarity reversed.

Truth Table

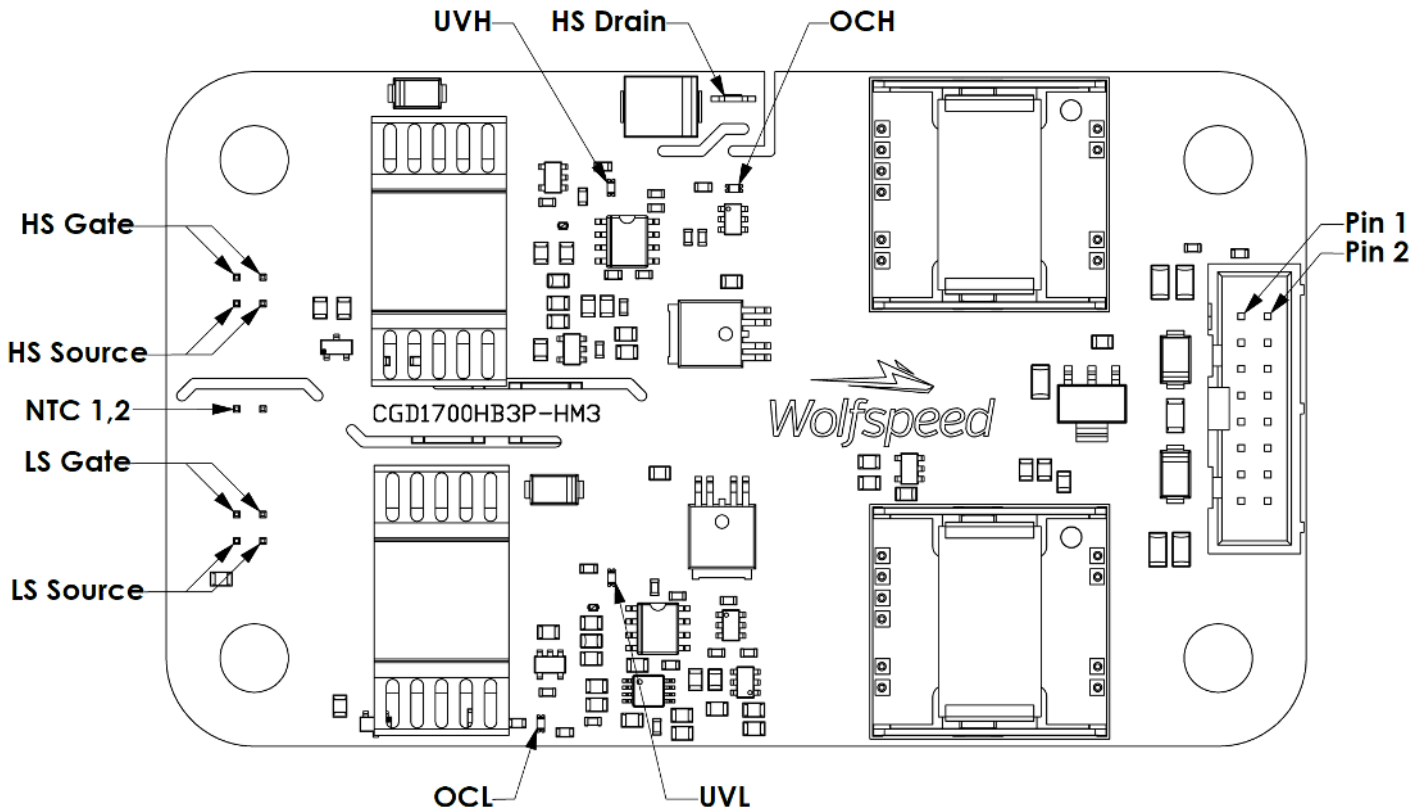
| PWM | PWM-EN | PS-DIS | RESET | Over-Current/ UVLO | FAULT | Output |
|-----|--------|--------|---------|-----------------------|-------|--------|
| H | H or Z | H or Z | H or Z | No | H | H |
| L | H or Z | H or Z | H or Z | No | H | L |
| X | L | H or Z | H or Z | No | H | L |
| X | X | L | X | UVLO | L | Z |
| X | H or Z | H or Z | Hi or Z | Yes | L | L |

H = High | L = Low | X = Irrelevant | Z = High Impedance

Function Block Diagram

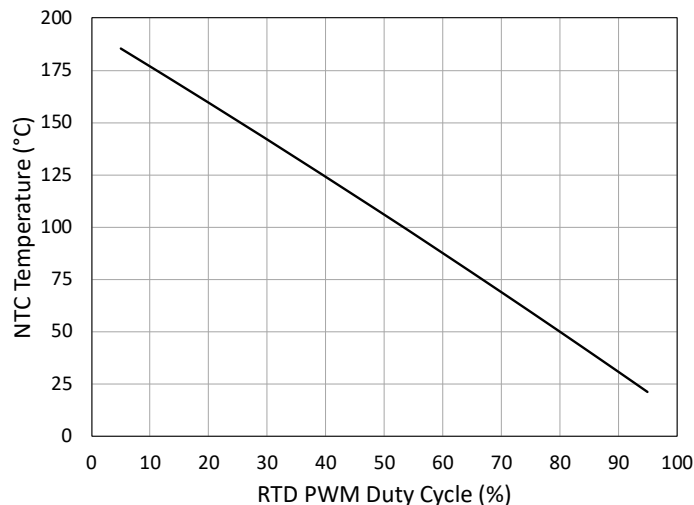


Gate Driver Interface



NTC Temperature Feedback

The resistance measurement of the HM3 power module's NTC is available on the input connector of the gate driver as a differential pair on pins 9 and 10. The NTC resistance is converted to a pulse-width modulated (PWM) 50 kHz square wave. The temperature to duty cycle relationship is displayed in the figure below. The NTC measurement circuit is referenced to low-side gate drive channel, with the low-side digital isolator used to transmit the duty cycle-encoded signal back to the primary side of the driver. For this reason, the NTC signal does not need any additional isolation, and can be included in the same ribbon cable as the rest of the gate driver's signals. The temperature reported by the NTC differs largely from the junction temperature of the SiC MOSFETs and should not be used as an accurate junction temperature measurement.



Power Estimates

The gate driver power required is calculated using the formula below. The gate charge is dependent on the module being driven. Once the required gate driver power is calculated, the required input power can be calculated from the efficiency curves on the power supplies datasheet. This calculation is for one channel of the gate driver.

$$P_{sw} = Q_G * F_{sw} * \Delta V_{PS}$$

- P_{sw} : gate driver power (per channel)
- Q_G : total gate charge (MOSFET gate charge × number of MOSFETs per switch position)
- F_{sw} : switching frequency
- ΔV_{PS} : difference in isolated power supply voltage rails ($V_{PS,HIGH} - V_{PS,LOW}$)

Example Calculation: Maximum Switching Frequency for CAS480M12HM3

- P_{sw} 3 W (rated output power of isolated power supply on gate driver)
- Q_G 1589 nC (provided in CAS480M12HM3 datasheet)
- ΔV_{PS} 20 V

$$3 W = 1589 nC * F_{sw} * 20 V$$

$F_{sw-Max} \approx 94$ kHz with margin

Input Connector Information

- 16 Positions Header, 0.100" (2.54mm) Pitch, Through Hole, Gold (SBH11-PBPC-D08-ST-BK)
- Quick-Connect Tab, 0.110" Width (735187-2)

Suggested Mating Parts

- 16 Position Rectangular Header, IDC, Gold, 28 AWG (SFH210-PPPC-D08-ID-BK)
- 16 Position Header, 0.100" (2.54mm) Pitch, Through Hole, Gold (SFH11-PBPC-D08-RA-BK)
- 16 Position Header, 0.100" (2.54mm) Pitch, Through Hole, Right Angle, Gold (SFH11-PBPC-D08-RA-BK)

Output Connector Information

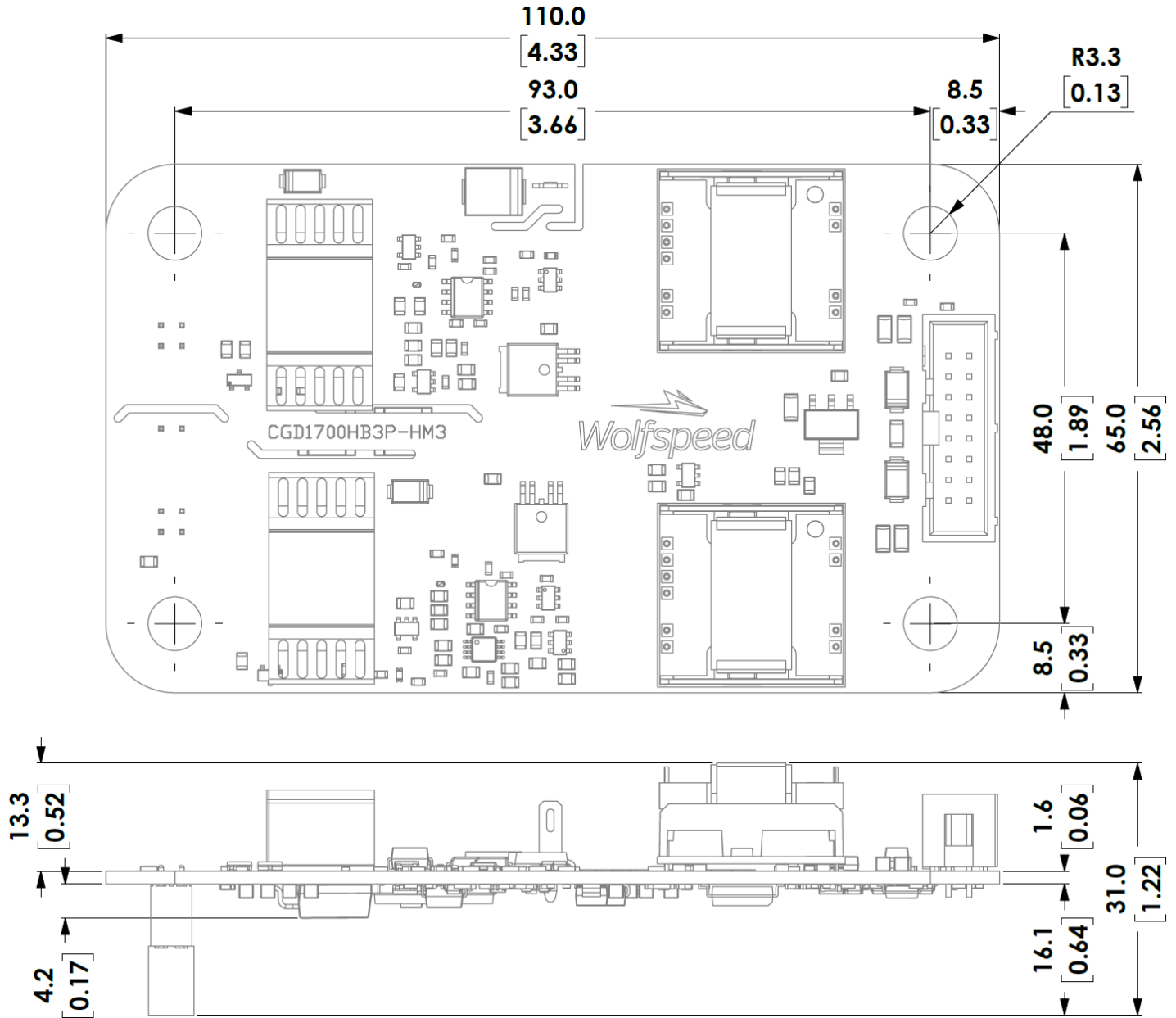
- 4 Positions Header, 0.100" (2.54mm) Pitch, Through Hole, Gold (Samtec® HW-TH-02-08-G-D-350-055)
- 2 Positions Header, 0.100" (2.54mm) Pitch, Through Hole, Gold (Samtec® HW-02-09-G-S-430-100)

Supporting Links & Tools

- [HM3 SiC Half-Bridge Module Platform](#)
- [CGD12HB00D: Single-Ended to Differential Transceiver Board](#)



Dimensions (mm [in])



Important Notes

- This Cree-designed gate driver hardware for Cree components is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. The hardware is not designed to meet any particular safety standards and the tool is not a production qualified assembly.
- Each part that is used in this gate driver and is manufactured by an entity other than Cree or one of Cree's affiliates is provided "as is" without warranty of any kind, including but not limited to any warranty of non-infringement, merchantability, or fitness for a particular purpose, whether express or implied. There is no representation that the operation of each such part will be uninterrupted or error free.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.
- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.