

74VHC126; 74VHCT126

Quad buffer/line driver; 3-state

Rev. 2 — 6 April 2020

Product data sheet

1. General description

The 74VHC126; 74VHCT126 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7-A.

The 74VHC126; 74VHCT126 provide four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW-level at pin nOE causes the outputs to assume a high-impedance OFF-state.

The 74VHC126; 74VHCT126 are identical to the 74VHC125; 74VHCT125 but have active HIGH output enable inputs.

2. Features

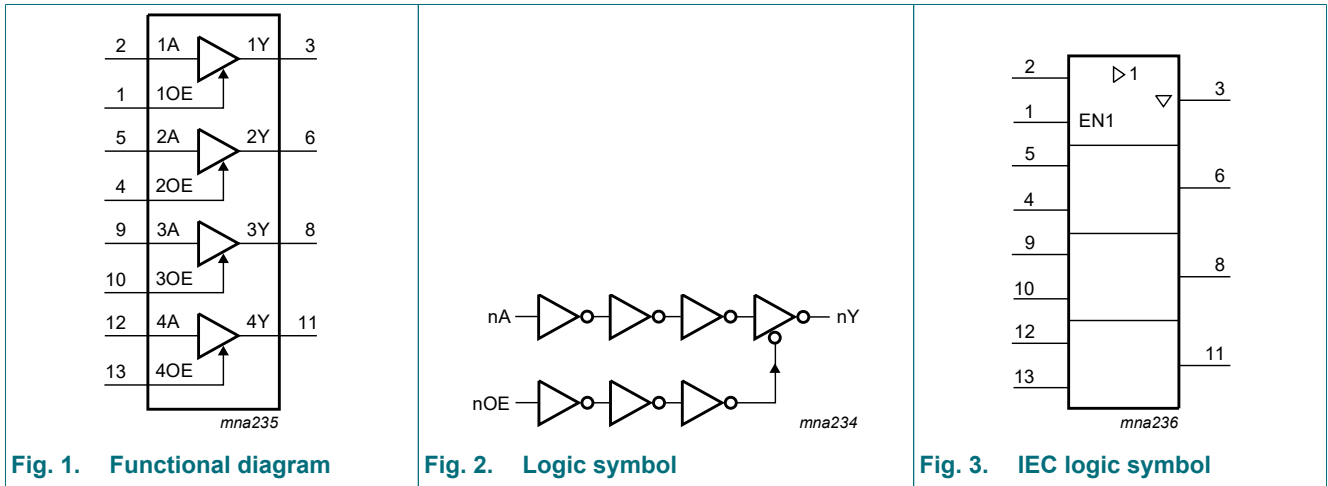
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - The 74VHC126 operates with CMOS input level
 - The 74VHCT126 operates with TTL input level
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

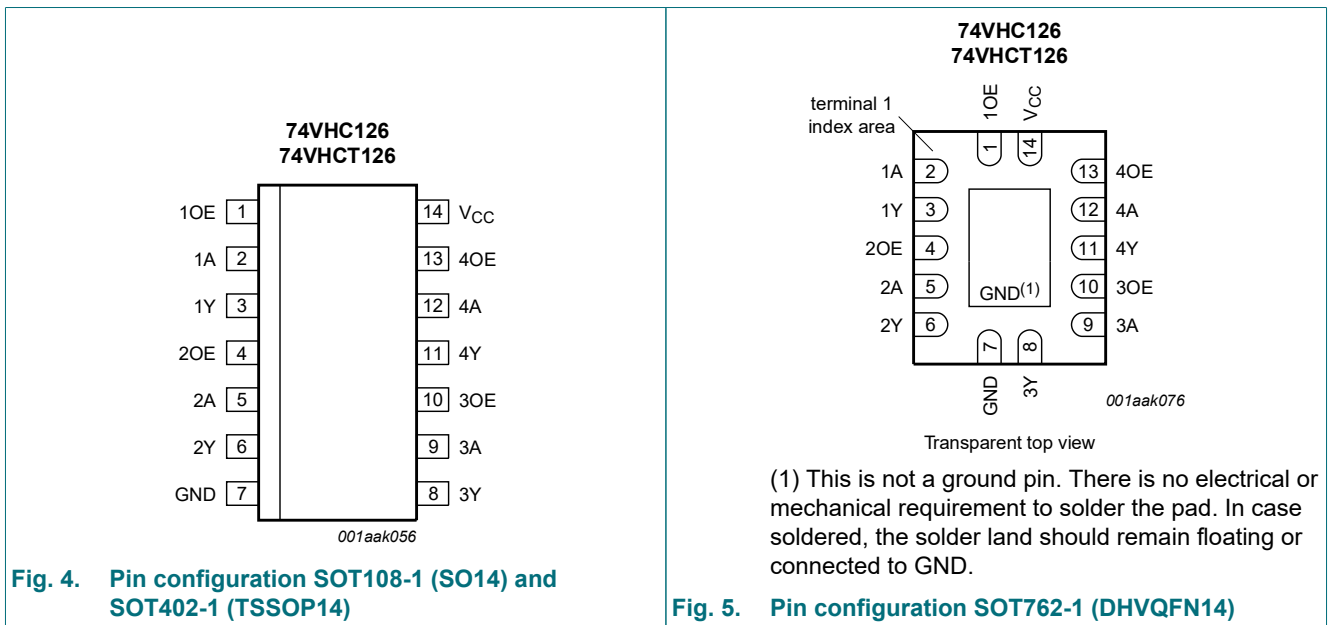
| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74VHC126D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74VHCT126D | | | | |
| 74VHC126PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74VHCT126PW | | | | |
| 74VHC126BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74VHCT126BQ | | | | |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------|--------------|-----------------------------------|
| 1OE, 2OE, 3OE, 4OE | 1, 4, 10, 13 | output enable input (active HIGH) |
| 1A, 2A, 3A, 4A | 2, 5, 9, 12 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Control | Input | Output |
|---------|-------|--------|
| nOE | nA | nY |
| H | L | L |
| H | H | H |
| L | X | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V [1] | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1] | -20 | +20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5)$ V | -25 | +25 | mA |
| I_{CC} | supply current | | - | +75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | 74VHC126 | | | 74VHCT126 | | | Unit |
|---------------------|-------------------------------------|---------------------------|----------|-----|----------|-----------|-----|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.0$ V to 3.6 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC} = 4.5$ V to 5.5 V | - | - | 20 | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---------------------------|---|-------|------|-------|------------------|------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74VHC126 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| I _O = -8.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V | | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V | | |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4 | - | - | - | - | - | pF |
| 74VHCT126 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|-----|-------|------------------|------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{OZ} | OFF-state output current | Per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|-------|---------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | Min | Max | |
| 74VHC126 | | | | | | | | | | |
| t _{pd} | propagation delay | nA to nY; see Fig. 6 [2] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 4.7 | 8.0 | 1.0 | 9.5 | 1.0 | 10.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF | - | 6.7 | 11.5 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 3.3 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| t _{en} | enable time | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 4.7 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| | | nOE to nY; see Fig. 7 [3] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 5.3 | 8.0 | 1.0 | 9.5 | 1.0 | 10.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF | - | 7.6 | 11.5 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| t _{dis} | disable time | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 3.6 | 5.3 | 1.0 | 6.1 | 1.0 | 7.0 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 5.1 | 7.6 | 1.0 | 8.7 | 1.0 | 9.5 | ns |
| | | nOE to nY; see Fig. 7 [4] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 6.6 | 9.7 | 1.0 | 11.5 | 1.0 | 12.5 | ns |
| C _{PD} | power dissipation capacitance | V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF | - | 9.4 | 13.2 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 4.7 | 6.8 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 6.7 | 8.8 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | f _i = 1 MHz; V _I = GND to V _{CC} [5] | - | 10 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|--|-------|---------|-----|------------------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | Min | Max | |
| 74VHCT126 | | | | | | | | | | |
| t _{pd} | propagation delay | nA to nY; see Fig. 6 [2] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 3.0 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 4.3 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| t _{en} | enable time | nOE to nY; see Fig. 7 [3] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 3.3 | 5.1 | 1.0 | 6.0 | 1.0 | 6.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 4.7 | 7.1 | 1.0 | 8.0 | 1.0 | 9.0 | ns |
| t _{dis} | disable time | nOE to nY; see Fig. 7 [4] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 4.8 | 6.8 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 6.9 | 8.9 | 1.0 | 10.0 | 1.0 | 11.5 | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} ; V _{CC} = 4.5 V to 5.5 V [5] | - | 12 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

10.1. Waveforms

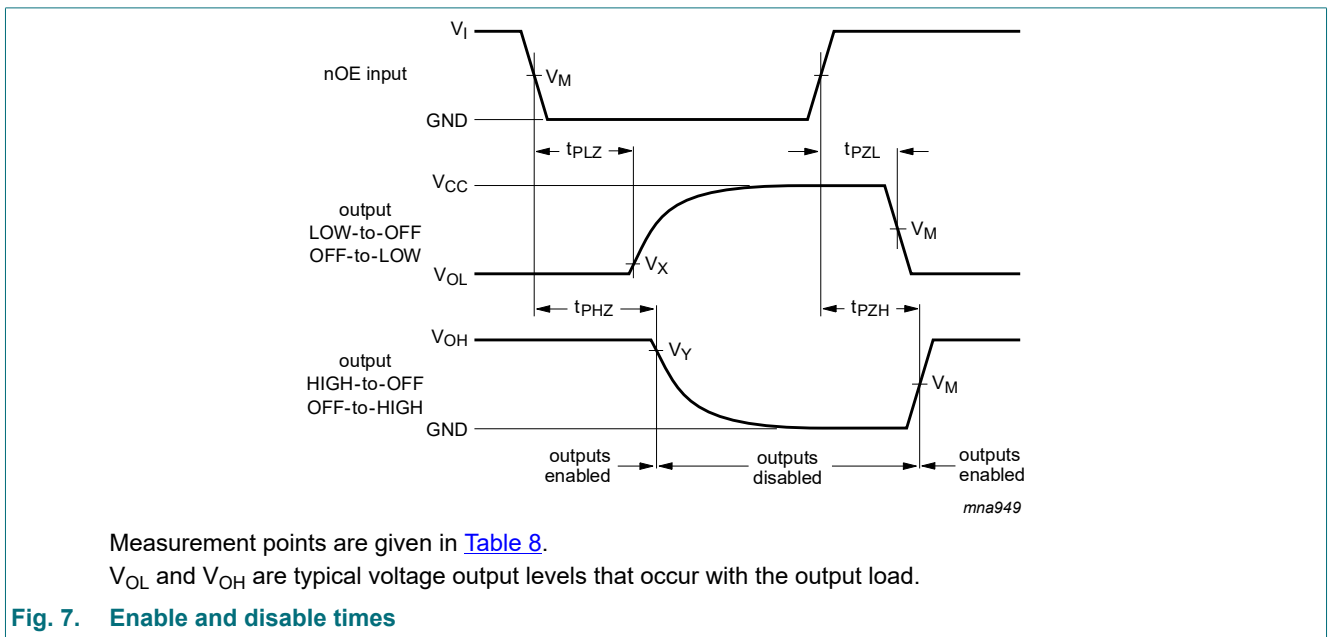
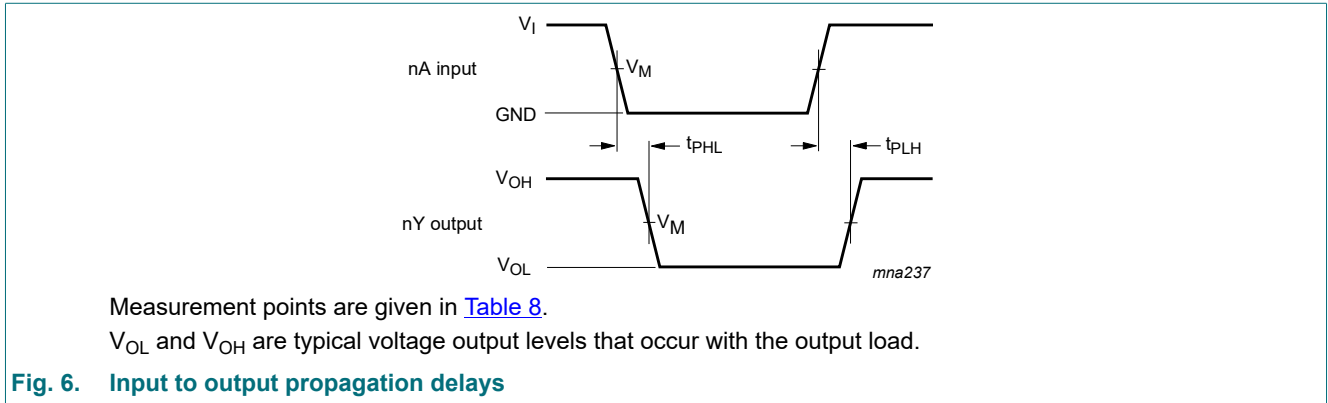


Table 8. Measurement points

| Type | Input | Output | | |
|-----------|-------------|-------------|------------------|------------------|
| | V_M | V_M | V_X | V_Y |
| 74VHC126 | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |
| 74VHCT126 | 1.5 V | $0.5V_{CC}$ | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |

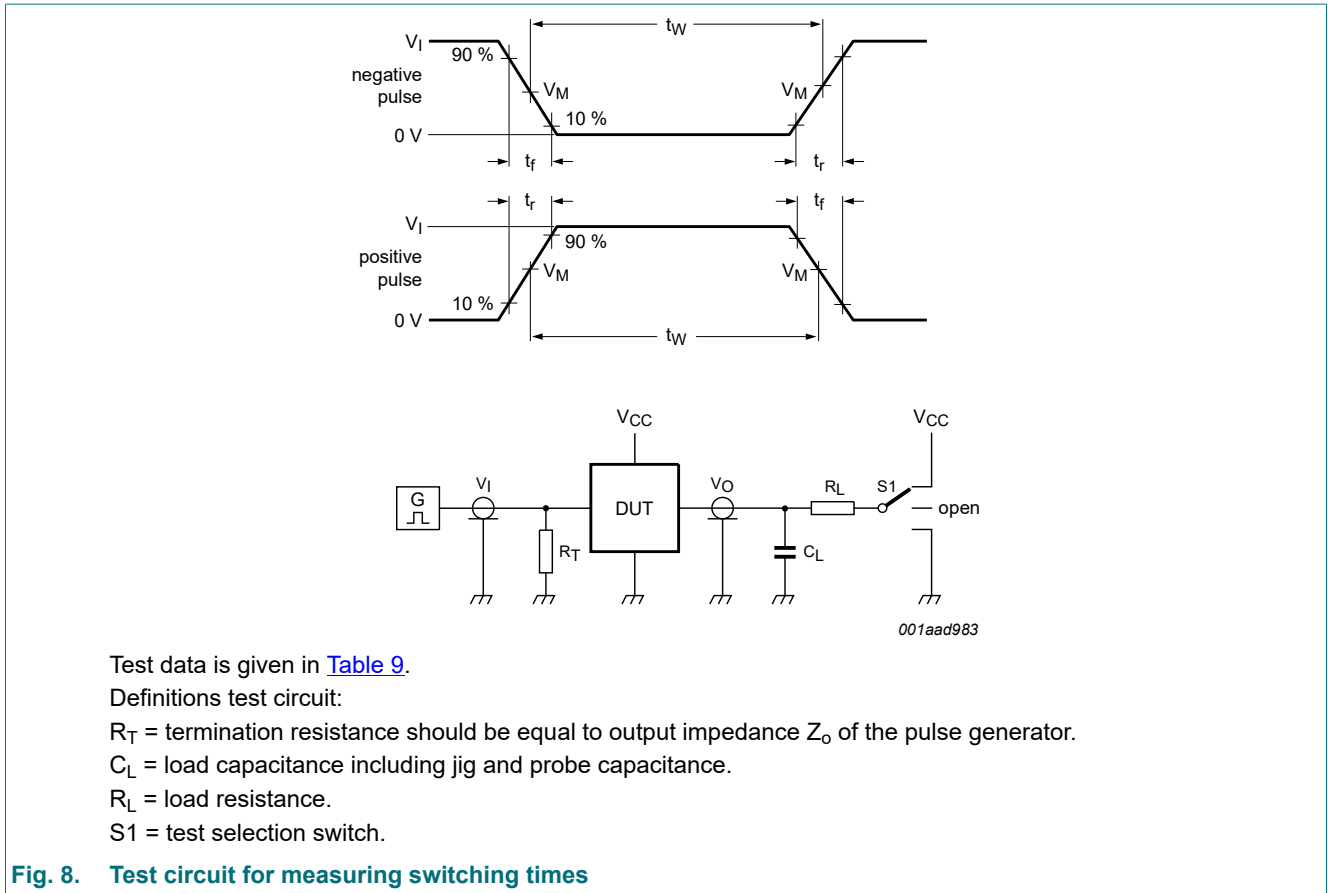


Fig. 8. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|-----------|----------|---------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74VHC126 | V_{CC} | ≤ 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74VHCT126 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

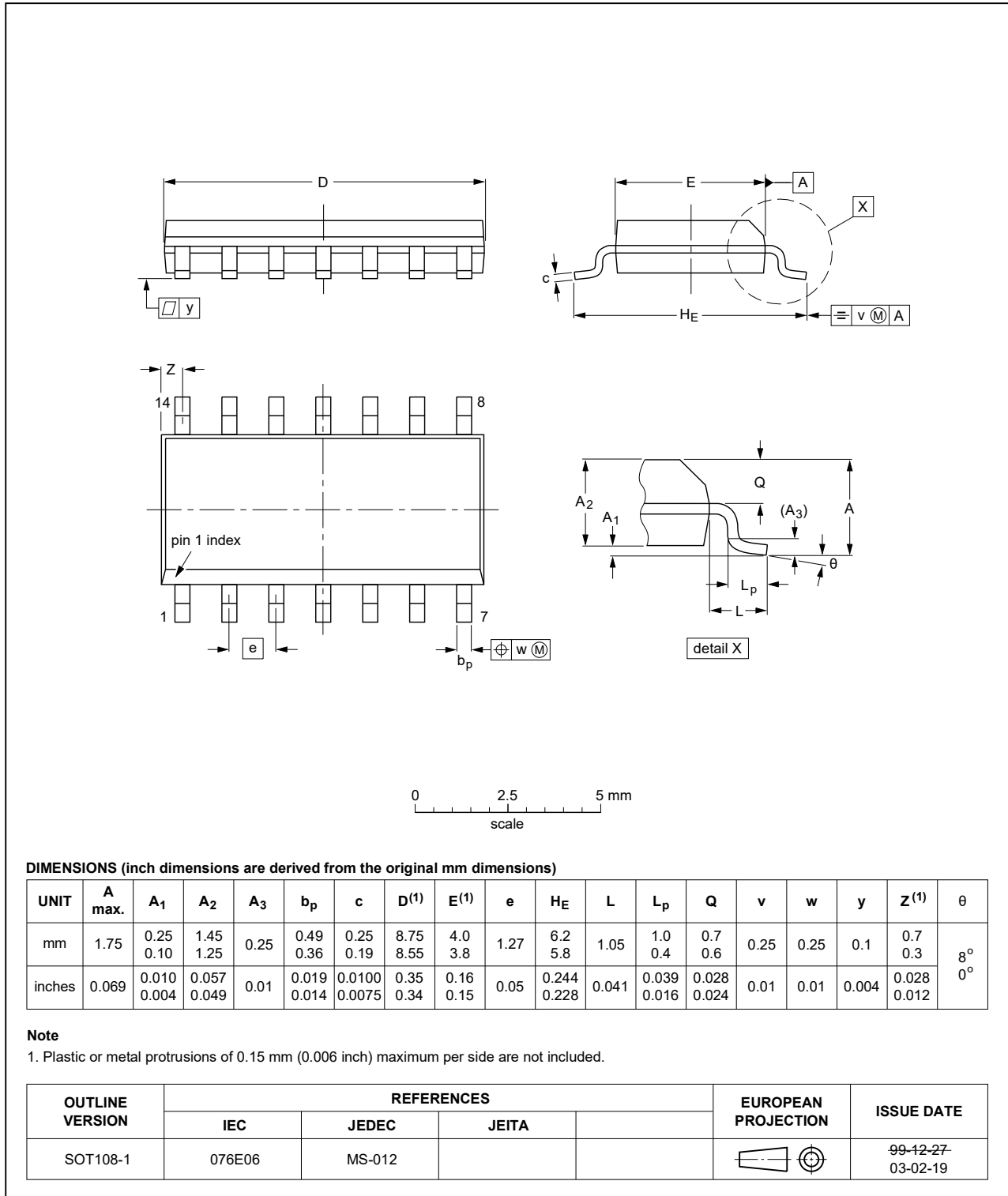


Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

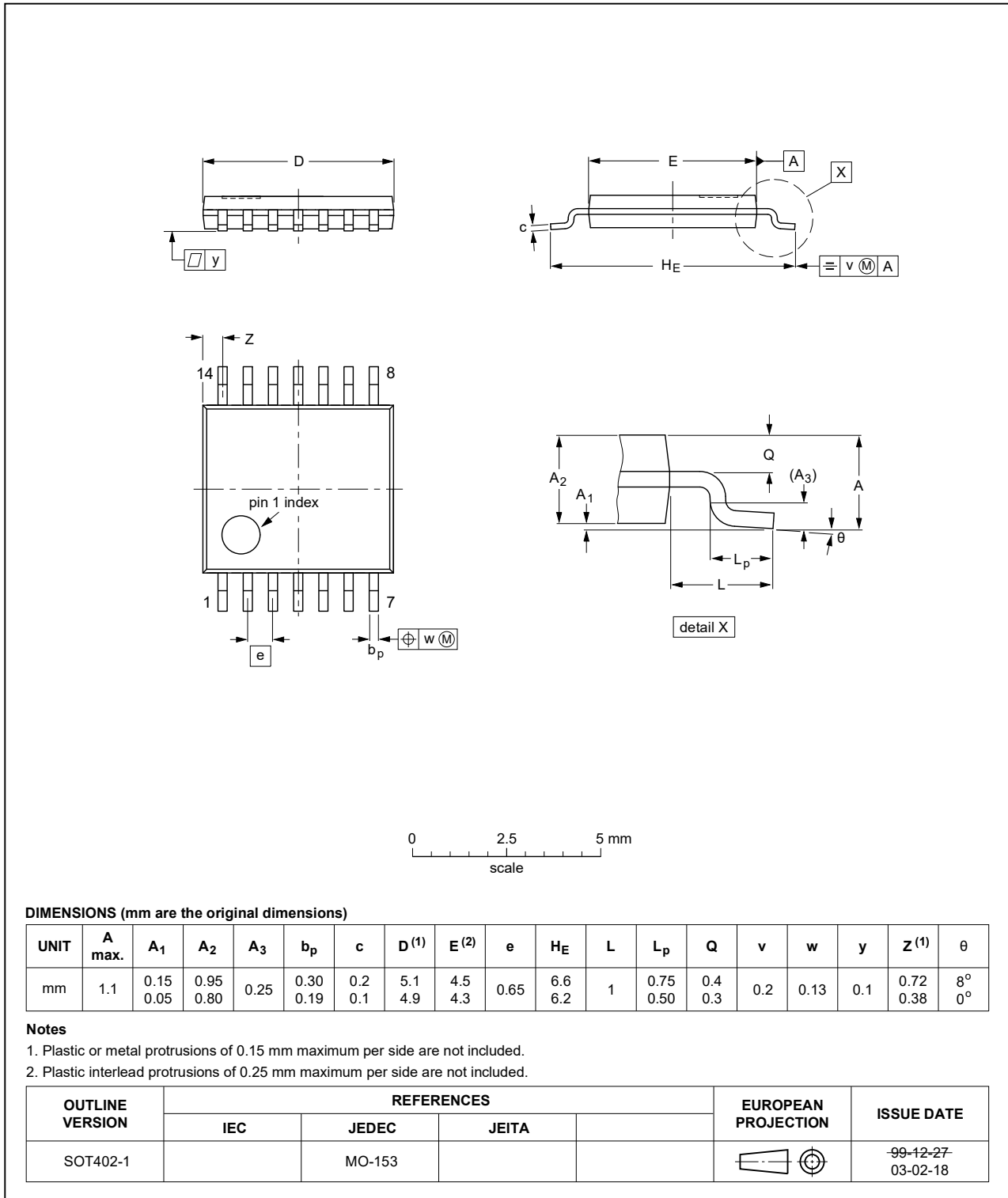


Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

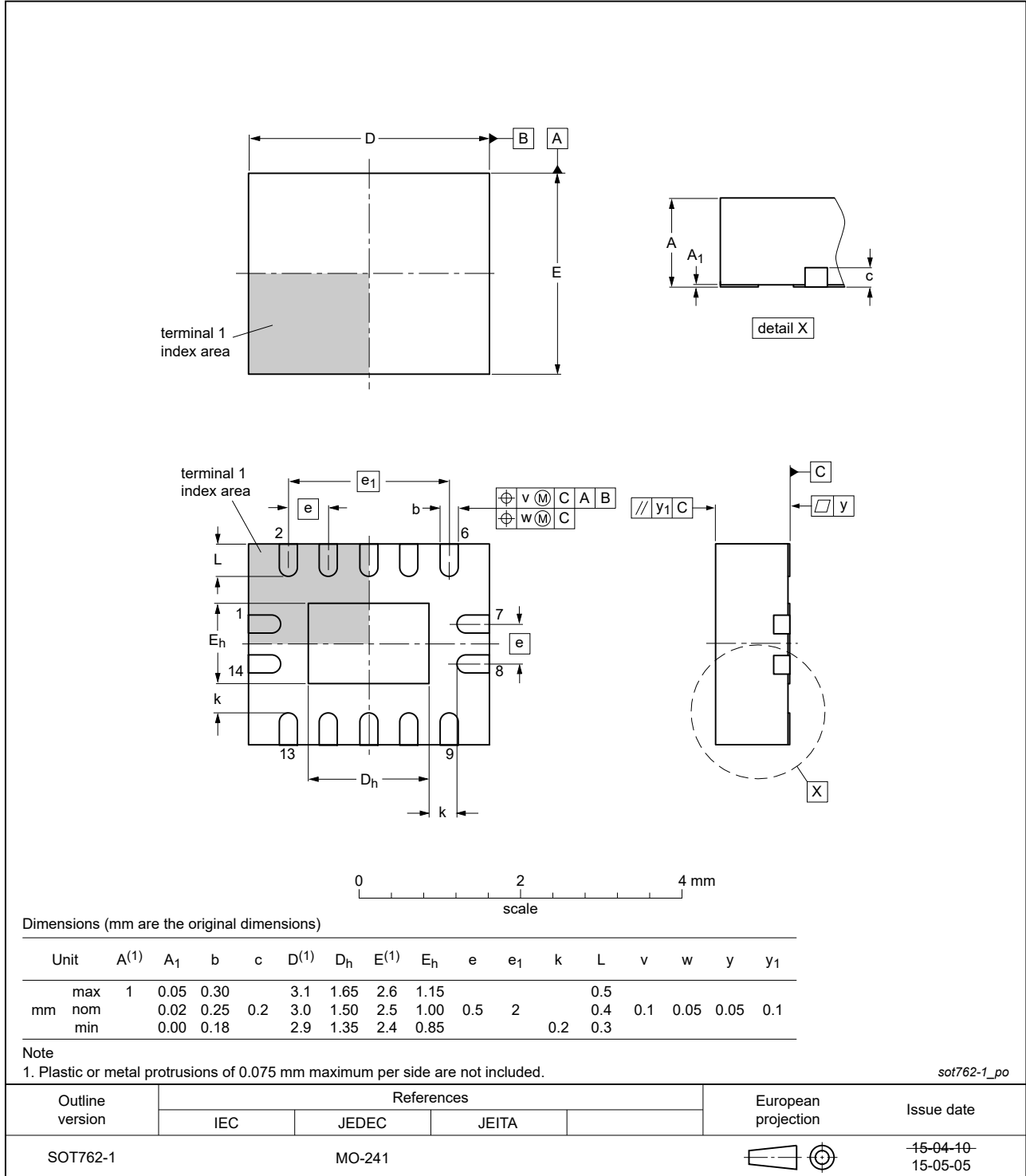


Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|--------------------|---------------|-----------------|
| 74VHC_VHCT126 v.2 | 20200406 | Product data sheet | - | 74VHC_VHCT126_1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 4: Derating values for P_{tot} total power dissipation have been updated. Package outline drawing SOT762-1 (DHVQFN14) updated. | | | |
| 74VHC_VHCT126_1 | 20090813 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

| | |
|--|-----------|
| 1. General description | 1 |
| 2. Features | 1 |
| 3. Ordering information | 1 |
| 4. Functional diagram | 2 |
| 5. Pinning information | 2 |
| 5.1. Pinning..... | 2 |
| 5.2. Pin description..... | 2 |
| 6. Functional description | 3 |
| 7. Limiting values | 3 |
| 8. Recommended operating conditions | 3 |
| 9. Static characteristics | 4 |
| 10. Dynamic characteristics | 5 |
| 10.1. Waveforms..... | 7 |
| 11. Package outline | 9 |
| 12. Abbreviations | 12 |
| 13. Revision history | 12 |
| 14. Legal information | 13 |

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